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Datasheet

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Version 1.0

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Sitronix Technology Corporation

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1 GENERAL DESCRIPTION

The ST7789VW is a single-chip controller/driver for 262K-color, graphic type TFT-LCD. It consists of 720 source line and 320 gate line driving circuits. This chip is capable of connecting directly to an external microprocessor, and accepts, 8-bits/9-bits/16-bits/18-bits parallel interface. Display data can be stored in the on-chip display data RAM of 240x320x18 bits. It can perform display data RAM read/write operation with no external operation clock to minimize power consumption. In addition, because of the integrated power supply circuit necessary to drive liquid crystal; it is possible to make a display system with the fewest components.

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2 FEATURES

- Single chip TFT-LCD Controller/Driver with On-chip Frame Memory (FM)
- Display Resolution: 240*RGB (H) *320(V)
- Frame Memory Size: 240 x 320 x 18-bit = 1,382,400 bits
- LCD Driver Output Circuits
  - Source Outputs: 240 RGB Channels
  - Gate Outputs: 320 Channels
  - Common Electrode Output
- Display Colors (Color Mode)
  - Full Color: 262K, RGB=(666) max., Idle Mode Off
  - Color Reduce: 8-color, RGB=(111), Idle Mode On
- Programmable Pixel Color Format (Color Depth) for Various Display Data input Format
  - 12-bit/pixel: RGB=(444)
  - 16-bit/pixel: RGB=(565)
  - 18-bit/pixel: RGB=(666)
- MCU Interface
  - Parallel 8080-series MCU Interface (8-bit, 9-bit, 16-bit & 18-bit)
  - 6/16/18 RGB Interface(VSYNC, HSYNC, DOTCLK, ENABLE, DB[17:0])
  - Serial Peripheral Interface(SPI Interface)
  - VSYNC Interface
- Display Features
  - Programmable Partial Display Duty
  - CABC for saving current consumption
  - Color enhancement
- On Chip Build-In Circuits
  - DC/DC Converter
  - Adjustable VCOM Generation
  - Non-Volatile (NV) Memory to Store Initial Register Setting and Factory Default Value (Module ID, Module Version, etc)
  - Timing Controller
  - 4 preset Gamma curve with separated RGB Gamma setting
- Build-In NV Memory for LCD Initial Register Setting
  - 8-bits for ID1 setting
  - 8-bits for ID2 setting
  - 8-bits for ID3 setting
  - 6-bits for VCOM Offset adjustment
- Driving Algorithm

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  - Dot Inversion
  - Column Inversion
- Wide Supply Voltage Range
  - I/O Voltage (VDDI to DGND): 1.65V ~ 3.3V (VDDI≦VDD)
  - Analog Voltage (VDD to AGND): 2.4V ~ 3.3V
- On-Chip Power System
  - Source Voltage (VAP (GVDD) to VAN (GVCL)): +6.4~-4.6V
  - VCOM level: GND
  - Gate driver HIGH level (VGH to AGND): +12.2V ~ +14.97V
  - Gate driver LOW level (VGL to AGND): -12.5V ~ -7.16V
- Optimized layout for COG Assembly
- Operate temperature range: –30℃ to +85℃
- Lower Power Consumption

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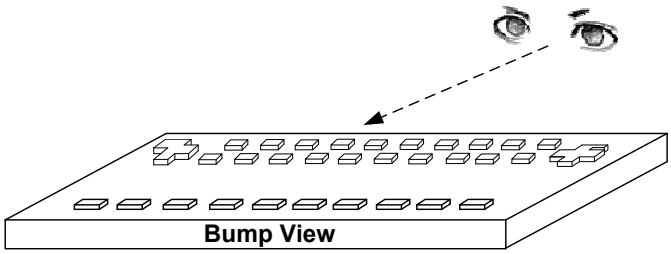
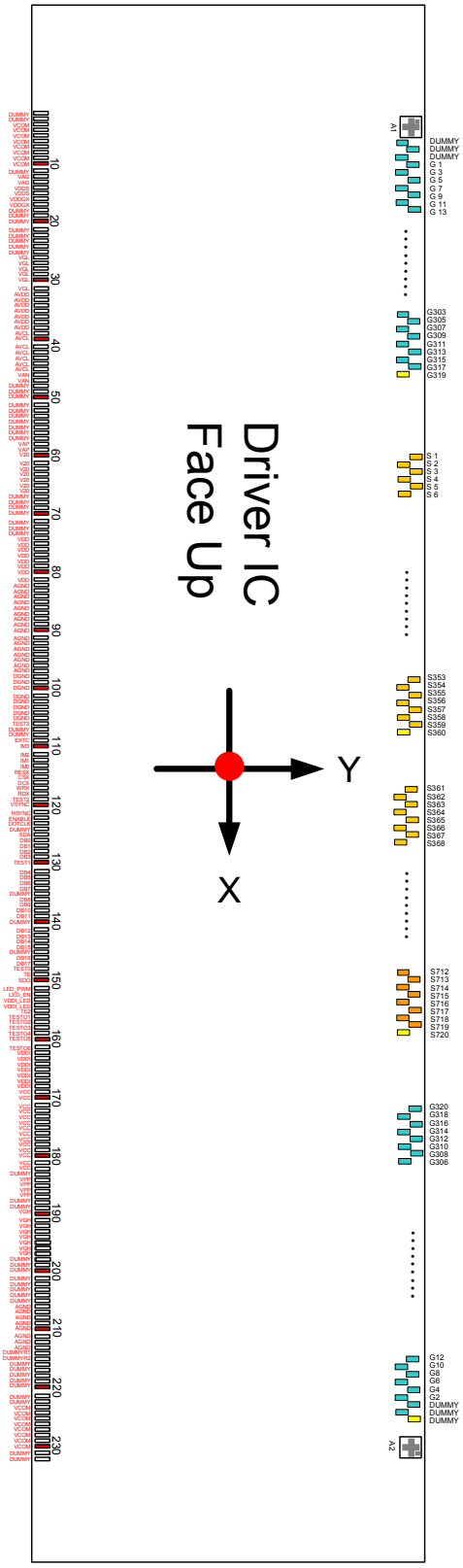
3 PAD ARRANGEMENT

3.1 Output Bump Dimension

Au bump height	9μm
Au bump size	14μmx100μm Gate : G1~G320 Source : S1~S720
	40μmx56μm Input Pads : Pad 12 to Pad 239





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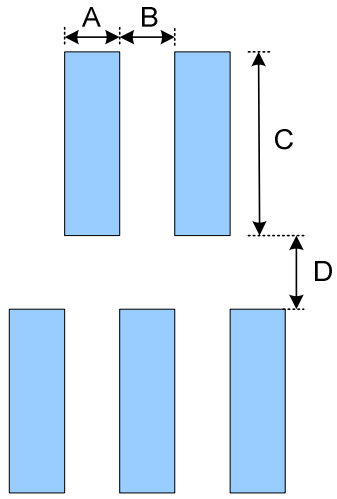
3.2 Input Bump Dimension

- **Output Pads**

S1~S720、G1~G320、DUMMY

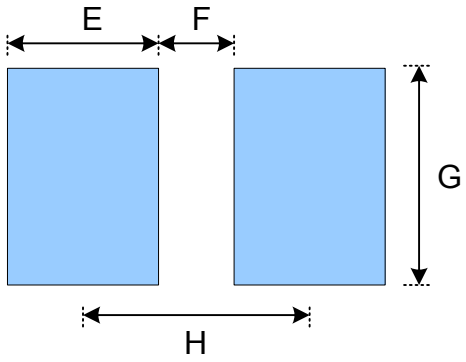
(No.233~1278)



Symbol	Item	Size
A	Bump Width	14 um
B	Bump Gap 1 (Horizontal)	14 um
C	Bump Height	100 um
D	Bump Gap 2 (Vertical)	31 um

- **Input Pads**

No.1~232



Symbol	Item	Size
E	Bump Width	40 um
F	Bump Gap	20、32.5、45 um
G	Bump Height	56 um
H	Bump Pitch	60、72.5、85 um

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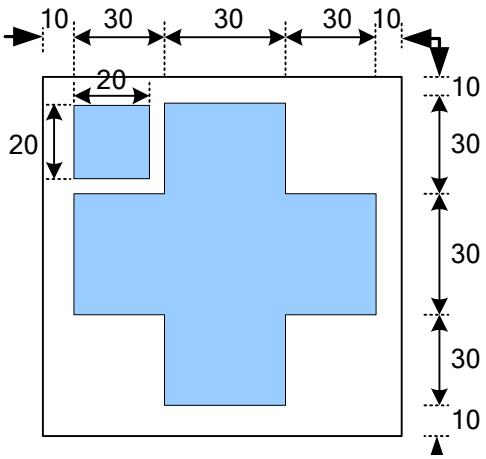
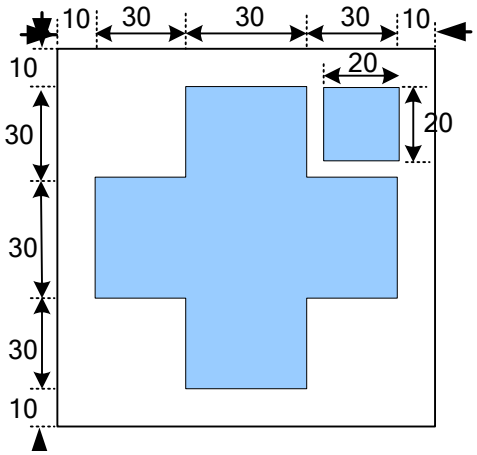
3.3 Alignment Mark Dimension

- **Alignment Mark : A1(X,Y)=(-7480,251.58)**



- **Alignment Mark : A2(X,Y)=(+7480,251.58)**



3.4 Chip Information

Chip size	15155μm x698μm
Chip thickness	300μm
Pad Location	Pad center
Coordinate Origin	Chip center

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4 PAD CENTER COORDINATES

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1	DUMMY	-7292.5	-256.62	33	AVDD	-5372.5	-256.62	65	V20	-3452.5	-256.62
2	DUMMY	-7232.5	-256.62	34	AVDD	-5312.5	-256.62	66	V20	-3392.5	-256.62
3	VCOM	-7172.5	-256.62	35	AVDD	-5252.5	-256.62	67	DUMMY	-3332.5	-256.62
4	VCOM	-7112.5	-256.62	36	AVDD	-5192.5	-256.62	68	DUMMY	-3272.5	-256.62
5	VCOM	-7052.5	-256.62	37	AVDD	-5132.5	-256.62	69	DUMMY	-3212.5	-256.62
6	VCOM	-6992.5	-256.62	38	AVDD	-5072.5	-256.62	70	DUMMY	-3152.5	-256.62
7	VCOM	-6932.5	-256.62	39	AVCL	-5012.5	-256.62	71	DUMMY	-3092.5	-256.62
8	VCOM	-6872.5	-256.62	40	AVCL	-4952.5	-256.62	72	DUMMY	-3032.5	-256.62
9	VCOM	-6812.5	-256.62	41	AVCL	-4892.5	-256.62	73	DUMMY	-2972.5	-256.62
10	VCOM	-6752.5	-256.62	42	AVCL	-4832.5	-256.62	74	VDD	-2912.5	-256.62
11	DUMMY	-6692.5	-256.62	43	AVCL	-4772.5	-256.62	75	VDD	-2852.5	-256.62
12	VAG	-6632.5	-256.62	44	AVCL	-4712.5	-256.62	76	VDD	-2792.5	-256.62
13	VAG	-6572.5	-256.62	45	AVCL	-4652.5	-256.62	77	VDD	-2732.5	-256.62
14	VDDS	-6512.5	-256.62	46	VAN	-4592.5	-256.62	78	VDD	-2672.5	-256.62
15	VDDS	-6452.5	-256.62	47	VAN	-4532.5	-256.62	79	VDD	-2612.5	-256.62
16	VDDGX	-6392.5	-256.62	48	DUMMY	-4472.5	-256.62	80	VDD	-2552.5	-256.62
17	VDDGX	-6332.5	-256.62	49	DUMMY	-4412.5	-256.62	81	VDD	-2492.5	-256.62
18	DUMMY	-6272.5	-256.62	50	DUMMY	-4352.5	-256.62	82	AGND	-2432.5	-256.62
19	DUMMY	-6212.5	-256.62	51	DUMMY	-4292.5	-256.62	83	AGND	-2372.5	-256.62
20	DUMMY	-6152.5	-256.62	52	DUMMY	-4232.5	-256.62	84	AGND	-2312.5	-256.62
21	DUMMY	-6092.5	-256.62	53	DUMMY	-4172.5	-256.62	85	AGND	-2252.5	-256.62
22	DUMMY	-6032.5	-256.62	54	DUMMY	-4112.5	-256.62	86	AGND	-2192.5	-256.62
23	DUMMY	-5972.5	-256.62	55	DUMMY	-4052.5	-256.62	87	AGND	-2132.5	-256.62
24	DUMMY	-5912.5	-256.62	56	DUMMY	-3992.5	-256.62	88	AGND	-2072.5	-256.62
25	DUMMY	-5852.5	-256.62	57	DUMMY	-3932.5	-256.62	89	AGND	-2012.5	-256.62
26	VGL	-5792.5	-256.62	58	VAP	-3872.5	-256.62	90	AGND	-1952.5	-256.62
27	VGL	-5732.5	-256.62	59	VAP	-3812.5	-256.62	91	AGND	-1892.5	-256.62
28	VGL	-5672.5	-256.62	60	V20	-3752.5	-256.62	92	AGND	-1832.5	-256.62
29	VGL	-5612.5	-256.62	61	V20	-3692.5	-256.62	93	AGND	-1772.5	-256.62
30	VGL	-5552.5	-256.62	62	V20	-3632.5	-256.62	94	AGND	-1712.5	-256.62
31	VGL	-5492.5	-256.62	63	V20	-3572.5	-256.62	95	AGND	-1652.5	-256.62
32	AVDD	-5432.5	-256.62	64	V20	-3512.5	-256.62	96	AGND	-1592.5	-256.62

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PAD No.	PIN Name	X	Y
97	AGND	-1532.5	-256.62
98	DGND	-1472.5	-256.62
99	DGND	-1412.5	-256.62
100	DGND	-1352.5	-256.62
101	DGND	-1292.5	-256.62
102	DGND	-1232.5	-256.62
103	DGND	-1172.5	-256.62
104	DGND	-1112.5	-256.62
105	DGND	-1052.5	-256.62
106	TEST3	-992.5	-256.62
107	DUMMY	-932.5	-256.62
108	DUMMY	-872.5	-256.62
109	EXTC	-812.5	-256.62
110	IM3	-752.5	-256.62
111	IM2	-692.5	-256.62
112	IM1	-632.5	-256.62
113	IM0	-572.5	-256.62
114	RESX	-512.5	-256.62
115	CSX	-452.5	-256.62
116	DCX	-392.5	-256.62
117	WRX	-332.5	-256.62
118	RDX	-272.5	-256.62
119	TEST2	-212.5	-256.62
120	VSYNC	-152.5	-256.62
121	HSYNC	-92.5	-256.62
122	ENABLE	-32.5	-256.62
123	DOTCLK	27.5	-256.62
124	DUMMY	87.5	-256.62
125	SDA	160	-256.62
126	DB0	245	-256.62
127	DB1	330	-256.62
128	DB2	415	-256.62
129	DB3	500	-256.62
130	TEST1	572.5	-256.62
131	DB4	645	-256.62
132	DB5	730	-256.62
133	DB6	815	-256.62
134	DB7	900	-256.62
135	DUMMY	972.5	-256.62
136	DB8	1045	-256.62
137	DB9	1130	-256.62
138	DB10	1215	-256.62
139	DB11	1300	-256.62
140	DUMMY	1372.5	-256.62
141	DB12	1445	-256.62
142	DB13	1530	-256.62
143	DB14	1615	-256.62
144	DB15	1700	-256.62
145	DUMMY	1772.5	-256.62
146	DB16	1845	-256.62
147	DB17	1930	-256.62
148	TEST0	2002.5	-256.62
149	TE	2075	-256.62
150	SDO	2160	-256.62
151	LED_PWM	2245	-256.62
152	LED_EN	2330	-256.62
153	VDDI_LED	2402.5	-256.62
154	VDDI_LED	2462.5	-256.62
155	TE2	2535	-256.62
156	TESTO1	2620	-256.62
157	TESTO2	2705	-256.62
158	TESTO3	2790	-256.62
159	TESTO4	2875	-256.62
160	TESTO5	2960	-256.62
161	TESTO6	3032.5	-256.62
162	VDDI	3092.5	-256.62
163	VDDI	3152.5	-256.62
164	VDDI	3212.5	-256.62
165	VDDI	3272.5	-256.62
166	VDDI	3332.5	-256.62
167	VDDI	3392.5	-256.62
168	VDDI	3452.5	-256.62
169	VCC	3512.5	-256.62
170	VCC	3572.5	-256.62
171	VCC	3632.5	-256.62
172	VCC	3692.5	-256.62
173	VCC	3752.5	-256.62
174	VCC	3812.5	-256.62
175	VCC	3872.5	-256.62
176	VCC	3932.5	-256.62
177	VCC	3992.5	-256.62
178	VCC	4052.5	-256.62
179	VCC	4112.5	-256.62
180	VCC	4172.5	-256.62
181	VCC	4232.5	-256.62
182	VCC	4292.5	-256.62
183	DUMMY	4352.5	-256.62
184	VPP	4412.5	-256.62
185	VPP	4472.5	-256.62
186	VPP	4532.5	-256.62
187	VPP	4592.5	-256.62
188	DUMMY	4652.5	-256.62
189	DUMMY	4712.5	-256.62
190	VGH	4772.5	-256.62
191	VGH	4832.5	-256.62
192	VGH	4892.5	-256.62
193	VGH	4952.5	-256.62
194	VGH	5012.5	-256.62
195	VGH	5072.5	-256.62
196	VGH	5132.5	-256.62
197	VGH	5192.5	-256.62
198	DUMMY	5252.5	-256.62

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PAD No.	PIN Name	X	Y
199	DUMMY	5312.5	-256.62
200	DUMMY	5372.5	-256.62
201	DUMMY	5432.5	-256.62
202	DUMMY	5492.5	-256.62
203	DUMMY	5552.5	-256.62
204	DUMMY	5612.5	-256.62
205	DUMMY	5672.5	-256.62
206	AGND	5732.5	-256.62
207	AGND	5792.5	-256.62
208	AGND	5852.5	-256.62
209	AGND	5912.5	-256.62
210	AGND	5972.5	-256.62
211	AGND	6032.5	-256.62
212	AGND	6092.5	-256.62
213	AGND	6152.5	-256.62
214	DUMMYR1	6212.5	-256.62
215	DUMMYR2	6272.5	-256.62
216	DUMMY	6332.5	-256.62
217	DUMMY	6392.5	-256.62
218	DUMMY	6452.5	-256.62
219	DUMMY	6512.5	-256.62
220	DUMMY	6572.5	-256.62
221	DUMMY	6632.5	-256.62
222	DUMMY	6692.5	-256.62
223	VCOM	6752.5	-256.62
224	VCOM	6812.5	-256.62
225	VCOM	6872.5	-256.62
226	VCOM	6932.5	-256.62
227	VCOM	6992.5	-256.62
228	VCOM	7052.5	-256.62
229	VCOM	7112.5	-256.62
230	VCOM	7172.5	-256.62
231	DUMMY	7232.5	-256.62
232	DUMMY	7292.5	-256.62
233	DUMMY	7399	250.58
234	DUMMY	7385	119.58
235	DUMMY	7371	250.58
236	G2	7357	119.58
237	G4	7343	250.58
238	G6	7329	119.58
239	G8	7315	250.58
240	G10	7301	119.58
241	G12	7287	250.58
242	G14	7273	119.58
243	G16	7259	250.58
244	G18	7245	119.58
245	G20	7231	250.58
246	G22	7217	119.58
247	G24	7203	250.58
248	G26	7189	119.58
249	G28	7175	250.58
250	G30	7161	119.58
251	G32	7147	250.58
252	G34	7133	119.58
253	G36	7119	250.58
254	G38	7105	119.58
255	G40	7091	250.58
250.58	G42	7077	119.58
257	G44	7063	250.58
258	G46	7049	119.58
259	G48	7035	250.58
260	G50	7021	119.58
261	G52	7007	250.58
262	G54	6993	119.58
263	G56	6979	250.58
264	G58	6965	119.58
265	G60	6951	250.58
266	G62	6937	119.58
267	G64	6923	250.58
268	G66	6909	119.58
269	G68	6895	250.58
270	G70	6881	119.58
271	G72	6867	250.58
272	G74	6853	119.58
273	G76	6839	250.58
274	G78	6825	119.58
275	G80	6811	250.58
276	G82	6797	119.58
277	G84	6783	250.58
278	G86	6769	119.58
279	G88	6755	250.58
280	G90	6741	119.58
281	G92	6727	250.58
282	G94	6713	119.58
283	G96	6699	250.58
284	G98	6685	119.58
285	G100	6671	250.58
286	G102	6657	119.58
287	G104	6643	250.58
288	G106	6629	119.58
289	G108	6615	250.58
290	G110	6601	119.58
291	G112	6587	250.58
292	G114	6573	119.58
293	G116	6559	250.58
294	G118	6545	119.58
295	G120	6531	250.58
296	G122	6517	119.58
297	G124	6503	250.58
298	G126	6489	119.58
299	G128	6475	250.58
300	G130	6461	119.58

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PAD No.	PIN Name	X	Y
301	G132	6447	250.58
302	G134	6433	119.58
303	G136	6419	250.58
304	G138	6405	119.58
305	G140	6391	250.58
306	G142	6377	119.58
307	G144	6363	250.58
308	G146	6349	119.58
309	G148	6335	250.58
310	G150	6321	119.58
311	G152	6307	250.58
312	G154	6293	119.58
313	G156	6279	250.58
314	G158	6265	119.58
315	G160	6251	250.58
316	G162	6237	119.58
317	G164	6223	250.58
318	G166	6209	119.58
319	G168	6195	250.58
320	G170	6181	119.58
321	G172	6167	250.58
322	G174	6153	119.58
323	G176	6139	250.58
324	G178	6125	119.58
325	G180	6111	250.58
326	G182	6097	119.58
327	G184	6083	250.58
328	G186	6069	119.58
329	G188	6055	250.58
330	G190	6041	119.58
331	G192	6027	250.58
332	G194	6013	119.58
333	G196	5999	250.58
334	G198	5985	119.58
335	G200	5971	250.58
336	G202	5957	119.58
337	G204	5943	250.58
338	G206	5929	119.58
339	G208	5915	250.58
340	G210	5901	119.58
341	G212	5887	250.58
342	G214	5873	119.58
343	G216	5859	250.58
344	G218	5845	119.58
345	G220	5831	250.58
346	G222	5817	119.58
347	G224	5803	250.58
348	G226	5789	119.58
349	G228	5775	250.58
350	G230	5761	119.58
351	G232	5747	250.58
352	G234	5733	119.58
353	G236	5719	250.58
354	G238	5705	119.58
355	G240	5691	250.58
356	G242	5677	119.58
357	G244	5663	250.58
358	G246	5649	119.58
359	G248	5635	250.58
360	G250	5621	119.58
361	G252	5607	250.58
362	G254	5593	119.58
363	G256	5579	250.58
364	G258	5565	119.58
365	G260	5551	250.58
366	G262	5537	119.58
367	G264	5523	250.58
368	G266	5509	119.58
369	G268	5495	250.58
370	G270	5481	119.58
371	G272	5467	250.58
372	G274	5453	119.58
373	G276	5439	250.58
374	G278	5425	119.58
375	G280	5411	250.58
376	G282	5397	119.58
377	G284	5383	250.58
378	G286	5369	119.58
379	G288	5355	250.58
380	G290	5341	119.58
381	G292	5327	250.58
382	G294	5313	119.58
383	G296	5299	250.58
384	G298	5285	119.58
385	G300	5271	250.58
386	G302	5257	119.58
387	G304	5243	250.58
388	G306	5229	119.58
389	G308	5215	250.58
390	G310	5201	119.58
391	G312	5187	250.58
392	G314	5173	119.58
393	G316	5159	250.58
394	G318	5145	119.58
395	G320	5131	250.58
396	S720	5075	119.58
397	S719	5061	250.58
398	S718	5047	119.58
399	S717	5033	250.58
400	S716	5019	119.58
401	S715	5005	250.58
402	S714	4991	119.58

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PAD No.	PIN Name	X	Y
403	S713	4977	250.58
404	S712	4963	119.58
405	S711	4949	250.58
406	S710	4935	119.58
407	S709	4921	250.58
408	S708	4907	119.58
409	S707	4893	250.58
410	S706	4879	119.58
411	S705	4865	250.58
412	S704	4851	119.58
413	S703	4837	250.58
414	S702	4823	119.58
415	S701	4809	250.58
416	S700	4795	119.58
417	S699	4781	250.58
418	S698	4767	119.58
419	S697	4753	250.58
420	S696	4739	119.58
421	S695	4725	250.58
422	S694	4711	119.58
423	S693	4697	250.58
424	S692	4683	119.58
425	S691	4669	250.58
426	S690	4655	119.58
427	S689	4641	250.58
428	S688	4627	119.58
429	S687	4613	250.58
430	S686	4599	119.58
431	S685	4585	250.58
432	S684	4571	119.58
433	S683	4557	250.58
434	S682	4543	119.58
435	S681	4529	250.58
436	S680	4515	119.58
437	S679	4501	250.58
438	S678	4487	119.58
439	S677	4473	250.58
440	S676	4459	119.58
441	S675	4445	250.58
442	S674	4431	119.58
443	S673	4417	250.58
444	S672	4403	119.58
445	S671	4389	250.58
446	S670	4375	119.58
447	S669	4361	250.58
448	S668	4347	119.58
449	S667	4333	250.58
450	S666	4319	119.58
451	S665	4305	250.58
452	S664	4291	119.58
453	S663	4277	250.58
454	S662	4263	119.58
455	S661	4249	250.58
456	S660	4235	119.58
457	S659	4221	250.58
458	S658	4207	119.58
459	S657	4193	250.58
460	S656	4179	119.58
461	S655	4165	250.58
462	S654	4151	119.58
463	S653	4137	250.58
464	S652	4123	119.58
465	S651	4109	250.58
466	S650	4095	119.58
467	S649	4081	250.58
468	S648	4067	119.58
469	S647	4053	250.58
470	S646	4039	119.58
471	S645	4025	250.58
472	S644	4011	119.58
473	S643	3997	250.58
474	S642	3983	119.58
475	S641	3969	250.58
476	S640	3955	119.58
477	S639	3941	250.58
478	S638	3927	119.58
479	S637	3913	250.58
480	S636	3899	119.58
481	S635	3885	250.58
482	S634	3871	119.58
483	S633	3857	250.58
484	S632	3843	119.58
485	S631	3829	250.58
486	S630	3815	119.58
487	S629	3801	250.58
488	S628	3787	119.58
489	S627	3773	250.58
490	S626	3759	119.58
491	S625	3745	250.58
492	S624	3731	119.58
493	S623	3717	250.58
494	S622	3703	119.58
495	S621	3689	250.58
496	S620	3675	119.58
497	S619	3661	250.58
498	S618	3647	119.58
499	S617	3633	250.58
500	S616	3619	119.58
501	S615	3605	250.58
502	S614	3591	119.58
503	S613	3577	250.58
504	S612	3563	119.58

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PAD No.	PIN Name	X	Y
505	S611	3549	250.58
506	S610	3535	119.58
507	S609	3521	250.58
508	S608	3507	119.58
509	S607	3493	250.58
510	S606	3479	119.58
511	S605	3465	250.58
512	S604	3451	119.58
513	S603	3437	250.58
514	S602	3423	119.58
515	S601	3409	250.58
516	S600	3395	119.58
517	S599	3381	250.58
518	S598	3367	119.58
519	S597	3353	250.58
520	S596	3339	119.58
521	S595	3325	250.58
522	S594	3311	119.58
523	S593	3297	250.58
524	S592	3283	119.58
525	S591	3269	250.58
526	S590	3255	119.58
527	S589	3241	250.58
528	S588	3227	119.58
529	S587	3213	250.58
530	S586	3199	119.58
531	S585	3185	250.58
532	S584	3171	119.58
533	S583	3157	250.58
534	S582	3143	119.58
535	S581	3129	250.58
536	S580	3115	119.58
537	S579	3101	250.58
538	S578	3087	119.58
539	S577	3073	250.58
540	S576	3059	119.58
541	S575	3045	250.58
542	S574	3031	119.58
543	S573	3017	250.58
544	S572	3003	119.58
545	S571	2989	250.58
546	S570	2975	119.58
547	S569	2961	250.58
548	S568	2947	119.58
549	S567	2933	250.58
550	S566	2919	119.58
551	S565	2905	250.58
552	S564	2891	119.58
553	S563	2877	250.58
554	S562	2863	119.58
555	S561	2849	250.58
556	S560	2835	119.58
557	S559	2821	250.58
558	S558	2807	119.58
559	S557	2793	250.58
560	S556	2779	119.58
561	S555	2765	250.58
562	S554	2751	119.58
563	S553	2737	250.58
564	S552	2723	119.58
565	S551	2709	250.58
566	S550	2695	119.58
567	S549	2681	250.58
568	S548	2667	119.58
569	S547	2653	250.58
570	S546	2639	119.58
571	S545	2625	250.58
572	S544	2611	119.58
573	S543	2597	250.58
574	S542	2583	119.58
575	S541	2569	250.58
576	S540	2555	119.58
577	S539	2541	250.58
578	S538	2527	119.58
579	S537	2513	250.58
580	S536	2499	119.58
581	S535	2485	250.58
582	S534	2471	119.58
583	S533	2457	250.58
584	S532	2443	119.58
585	S531	2429	250.58
586	S530	2415	119.58
587	S529	2401	250.58
588	S528	2387	119.58
589	S527	2373	250.58
590	S526	2359	119.58
591	S525	2345	250.58
592	S524	2331	119.58
593	S523	2317	250.58
594	S522	2303	119.58
595	S521	2289	250.58
596	S520	2275	119.58
597	S519	2261	250.58
598	S518	2247	119.58
599	S517	2233	250.58
600	S516	2219	119.58
601	S515	2205	250.58
602	S514	2191	119.58
603	S513	2177	250.58
604	S512	2163	119.58
605	S511	2149	250.58
606	S510	2135	119.58

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
607	S509	2121	250.58	641	S475	1645	250.58	675	S441	1169	250.58
608	S508	2107	119.58	642	S474	1631	119.58	676	S440	1155	119.58
609	S507	2093	250.58	643	S473	1617	250.58	677	S439	1141	250.58
610	S506	2079	119.58	644	S472	1603	119.58	678	S438	1127	119.58
611	S505	2065	250.58	645	S471	1589	250.58	679	S437	1113	250.58
612	S504	2051	119.58	646	S470	1575	119.58	680	S436	1099	119.58
613	S503	2037	250.58	647	S469	1561	250.58	681	S435	1085	250.58
614	S502	2023	119.58	648	S468	1547	119.58	682	S434	1071	119.58
615	S501	2009	250.58	649	S467	1533	250.58	683	S433	1057	250.58
616	S500	1995	119.58	650	S466	1519	119.58	684	S432	1043	119.58
617	S499	1981	250.58	651	S465	1505	250.58	685	S431	1029	250.58
618	S498	1967	119.58	652	S464	1491	119.58	686	S430	1015	119.58
619	S497	1953	250.58	653	S463	1477	250.58	687	S429	1001	250.58
620	S496	1939	119.58	654	S462	1463	119.58	688	S428	987	119.58
621	S495	1925	250.58	655	S461	1449	250.58	689	S427	973	250.58
622	S494	1911	119.58	656	S460	1435	119.58	690	S426	959	119.58
623	S493	1897	250.58	657	S459	1421	250.58	691	S425	945	250.58
624	S492	1883	119.58	658	S458	1407	119.58	692	S424	931	119.58
625	S491	1869	250.58	659	S457	1393	250.58	693	S423	917	250.58
626	S490	1855	119.58	660	S456	1379	119.58	694	S422	903	119.58
627	S489	1841	250.58	661	S455	1365	250.58	695	S421	889	250.58
628	S488	1827	119.58	662	S454	1351	119.58	696	S420	875	119.58
629	S487	1813	250.58	663	S453	1337	250.58	697	S419	861	250.58
630	S486	1799	119.58	664	S452	1323	119.58	698	S418	847	119.58
631	S485	1785	250.58	665	S451	1309	250.58	699	S417	833	250.58
632	S484	1771	119.58	666	S450	1295	119.58	700	S416	819	119.58
633	S483	1757	250.58	667	S449	1281	250.58	701	S415	805	250.58
634	S482	1743	119.58	668	S448	1267	119.58	702	S414	791	119.58
635	S481	1729	250.58	669	S447	1253	250.58	703	S413	777	250.58
636	S480	1715	119.58	670	S446	1239	119.58	704	S412	763	119.58
637	S479	1701	250.58	671	S445	1225	250.58	705	S411	749	250.58
638	S478	1687	119.58	672	S444	1211	119.58	706	S410	735	119.58
639	S477	1673	250.58	673	S443	1197	250.58	707	S409	721	250.58
640	S476	1659	119.58	674	S442	1183	119.58	708	S408	707	119.58

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PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
709	S407	693	250.58	743	S373	217	250.58	777	S339	-343	250.58
710	S406	679	119.58	744	S372	203	119.58	778	S338	-357	119.58
711	S405	665	250.58	745	S371	189	250.58	779	S337	-371	250.58
712	S404	651	119.58	746	S370	175	119.58	780	S336	-385	119.58
713	S403	637	250.58	747	S369	161	250.58	781	S335	-399	250.58
714	S402	623	119.58	748	S368	147	119.58	782	S334	-413	119.58
715	S401	609	250.58	749	S367	133	250.58	783	S333	-427	250.58
716	S400	595	119.58	750	S366	119	119.58	784	S332	-441	119.58
717	S399	581	250.58	751	S365	105	250.58	785	S331	-455	250.58
718	S398	567	119.58	752	S364	91	119.58	786	S330	-469	119.58
719	S397	553	250.58	753	S363	77	250.58	787	S329	-483	250.58
720	S396	539	119.58	754	S362	63	119.58	788	S328	-497	119.58
721	S395	525	250.58	755	S361	49	250.58	789	S327	-511	250.58
722	S394	511	119.58	756	S360	-49	119.58	790	S326	-525	119.58
723	S393	497	250.58	757	S359	-63	250.58	791	S325	-539	250.58
724	S392	483	119.58	758	S358	-77	119.58	792	S324	-553	119.58
725	S391	469	250.58	759	S357	-91	250.58	793	S323	-567	250.58
726	S390	455	119.58	760	S356	-105	119.58	794	S322	-581	119.58
727	S389	441	250.58	761	S355	-119	250.58	795	S321	-595	250.58
728	S388	427	119.58	762	S354	-133	119.58	796	S320	-609	119.58
729	S387	413	250.58	763	S353	-147	250.58	797	S319	-623	250.58
730	S386	399	119.58	764	S352	-161	119.58	798	S318	-637	119.58
731	S385	385	250.58	765	S351	-175	250.58	799	S317	-651	250.58
732	S384	371	119.58	766	S350	-189	119.58	800	S316	-665	119.58
733	S383	357	250.58	767	S349	-203	250.58	801	S315	-679	250.58
734	S382	343	119.58	768	S348	-217	119.58	802	S314	-693	119.58
735	S381	329	250.58	769	S347	-231	250.58	803	S313	-707	250.58
736	S380	315	119.58	770	S346	-245	119.58	804	S312	-721	119.58
737	S379	301	250.58	771	S345	-259	250.58	805	S311	-735	250.58
738	S378	287	119.58	772	S344	-273	119.58	806	S310	-749	119.58
739	S377	273	250.58	773	S343	-287	250.58	807	S309	-763	250.58
740	S376	259	119.58	774	S342	-301	119.58	808	S308	-777	119.58
741	S375	245	250.58	775	S341	-315	250.58	809	S307	-791	250.58
742	S374	231	119.58	776	S340	-329	119.58	810	S306	-805	119.58

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PAD No.	PIN Name	X	Y
811	S305	-819	250.58
812	S304	-833	119.58
813	S303	-847	250.58
814	S302	-861	119.58
815	S301	-875	250.58
816	S300	-889	119.58
817	S299	-903	250.58
818	S298	-917	119.58
819	S297	-931	250.58
820	S296	-945	119.58
821	S295	-959	250.58
822	S294	-973	119.58
823	S293	-987	250.58
824	S292	-1001	119.58
825	S291	-1015	250.58
826	S290	-1029	119.58
827	S289	-1043	250.58
828	S288	-1057	119.58
829	S287	-1071	250.58
830	S286	-1085	119.58
831	S285	-1099	250.58
832	S284	-1113	119.58
833	S283	-1127	250.58
834	S282	-1141	119.58
835	S281	-1155	250.58
836	S280	-1169	119.58
837	S279	-1183	250.58
838	S278	-1197	119.58
839	S277	-1211	250.58
840	S276	-1225	119.58
841	S275	-1239	250.58
842	S274	-1253	119.58
843	S273	-1267	250.58
844	S272	-1281	119.58
845	S271	-1295	250.58
846	S270	-1309	119.58
847	S269	-1323	250.58
848	S268	-1337	119.58
849	S267	-1351	250.58
850	S266	-1365	119.58
851	S265	-1379	250.58
852	S264	-1393	119.58
853	S263	-1407	250.58
854	S262	-1421	119.58
855	S261	-1435	250.58
856	S260	-1449	119.58
857	S259	-1463	250.58
858	S258	-1477	119.58
859	S257	-1491	250.58
860	S256	-1505	119.58
861	S255	-1519	250.58
862	S254	-1533	119.58
863	S253	-1547	250.58
864	S252	-1561	119.58
865	S251	-1575	250.58
866	S250	-1589	119.58
867	S249	-1603	250.58
868	S248	-1617	119.58
869	S247	-1631	250.58
870	S246	-1645	119.58
871	S245	-1659	250.58
872	S244	-1673	119.58
873	S243	-1687	250.58
874	S242	-1701	119.58
875	S241	-1715	250.58
876	S240	-1729	119.58
877	S239	-1743	250.58
878	S238	-1757	119.58
879	S237	-1771	250.58
880	S236	-1785	119.58
881	S235	-1799	250.58
882	S234	-1813	119.58
883	S233	-1827	250.58
884	S232	-1841	119.58
885	S231	-1855	250.58
886	S230	-1869	119.58
887	S229	-1883	250.58
888	S228	-1897	119.58
889	S227	-1911	250.58
890	S226	-1925	119.58
891	S225	-1939	250.58
892	S224	-1953	119.58
893	S223	-1967	250.58
894	S222	-1981	119.58
895	S221	-1995	250.58
896	S220	-2009	119.58
897	S219	-2023	250.58
898	S218	-2037	119.58
899	S217	-2051	250.58
900	S216	-2065	119.58
901	S215	-2079	250.58
902	S214	-2093	119.58
903	S213	-2107	250.58
904	S212	-2121	119.58
905	S211	-2135	250.58
906	S210	-2149	119.58
907	S209	-2163	250.58
908	S208	-2177	119.58
909	S207	-2191	250.58
910	S206	-2205	119.58
911	S205	-2219	250.58
912	S204	-2233	119.58

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PAD No.	PIN Name	X	Y
913	S203	-2247	250.58
914	S202	-2261	119.58
915	S201	-2275	250.58
916	S200	-2289	119.58
917	S199	-2303	250.58
918	S198	-2317	119.58
919	S197	-2331	250.58
920	S196	-2345	119.58
921	S195	-2359	250.58
922	S194	-2373	119.58
923	S193	-2387	250.58
924	S192	-2401	119.58
925	S191	-2415	250.58
926	S190	-2429	119.58
927	S189	-2443	250.58
928	S188	-2457	119.58
929	S187	-2471	250.58
930	S186	-2485	119.58
931	S185	-2499	250.58
932	S184	-2513	119.58
933	S183	-2527	250.58
934	S182	-2541	119.58
935	S181	-2555	250.58
936	S180	-2569	119.58
937	S179	-2583	250.58
938	S178	-2597	119.58
939	S177	-2611	250.58
940	S176	-2625	119.58
941	S175	-2639	250.58
942	S174	-2653	119.58
943	S173	-2667	250.58
944	S172	-2681	119.58
945	S171	-2695	250.58
946	S170	-2709	119.58
947	S169	-2723	250.58
948	S168	-2737	119.58
949	S167	-2751	250.58
950	S166	-2765	119.58
951	S165	-2779	250.58
952	S164	-2793	119.58
953	S163	-2807	250.58
954	S162	-2821	119.58
955	S161	-2835	250.58
956	S160	-2849	119.58
957	S159	-2863	250.58
958	S158	-2877	119.58
959	S157	-2891	250.58
960	S156	-2905	119.58
961	S155	-2919	250.58
962	S154	-2933	119.58
963	S153	-2947	250.58
964	S152	-2961	119.58
965	S151	-2975	250.58
966	S150	-2989	119.58
967	S149	-3003	250.58
968	S148	-3017	119.58
969	S147	-3031	250.58
970	S146	-3045	119.58
971	S145	-3059	250.58
972	S144	-3073	119.58
973	S143	-3087	250.58
974	S142	-3101	119.58
975	S141	-3115	250.58
976	S140	-3129	119.58
977	S139	-3143	250.58
978	S138	-3157	119.58
979	S137	-3171	250.58
980	S136	-3185	119.58
981	S135	-3199	250.58
982	S134	-3213	119.58
983	S133	-3227	250.58
984	S132	-3241	119.58
985	S131	-3255	250.58
986	S130	-3269	119.58
987	S129	-3283	250.58
988	S128	-3297	119.58
989	S127	-3311	250.58
990	S126	-3325	119.58
991	S125	-3339	250.58
992	S124	-3353	119.58
993	S123	-3367	250.58
994	S122	-3381	119.58
995	S121	-3395	250.58
996	S120	-3409	119.58
997	S119	-3423	250.58
998	S118	-3437	119.58
999	S117	-3451	250.58
1000	S116	-3465	119.58
1001	S115	-3479	250.58
1002	S114	-3493	119.58
1003	S113	-3507	250.58
1004	S112	-3521	119.58
1005	S111	-3535	250.58
1006	S110	-3549	119.58
1007	S109	-3563	250.58
1008	S108	-3577	119.58
1009	S107	-3591	250.58
1010	S106	-3605	119.58
1011	S105	-3619	250.58
1012	S104	-3633	119.58
1013	S103	-3647	250.58
1014	S102	-3661	119.58

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PAD No.	PIN Name	X	Y
1015	S101	-3675	250.58
1016	S100	-3689	119.58
1017	S99	-3703	250.58
1018	S98	-3717	119.58
1019	S97	-3731	250.58
1020	S96	-3745	119.58
1021	S95	-3759	250.58
1022	S94	-3773	119.58
1023	S93	-3787	250.58
1024	S92	-3801	119.58
1025	S91	-3815	250.58
1026	S90	-3829	119.58
1027	S89	-3843	250.58
1028	S88	-3857	119.58
1029	S87	-3871	250.58
1030	S86	-3885	119.58
1031	S85	-3899	250.58
1032	S84	-3913	119.58
1033	S83	-3927	250.58
1034	S82	-3941	119.58
1035	S81	-3955	250.58
1036	S80	-3969	119.58
1037	S79	-3983	250.58
1038	S78	-3997	119.58
1039	S77	-4011	250.58
1040	S76	-4025	119.58
1041	S75	-4039	250.58
1042	S74	-4053	119.58
1043	S73	-4067	250.58
1044	S72	-4081	119.58
1045	S71	-4095	250.58
1046	S70	-4109	119.58
1047	S69	-4123	250.58
1048	S68	-4137	119.58
1049	S67	-4151	250.58
1050	S66	-4165	119.58
1051	S65	-4179	250.58
1052	S64	-4193	119.58
1053	S63	-4207	250.58
1054	S62	-4221	119.58
1055	S61	-4235	250.58
1056	S60	-4249	119.58
1057	S59	-4263	250.58
1058	S58	-4277	119.58
1059	S57	-4291	250.58
1060	S56	-4305	119.58
1061	S55	-4319	250.58
1062	S54	-4333	119.58
1063	S53	-4347	250.58
1064	S52	-4361	119.58
1065	S51	-4375	250.58
1066	S50	-4389	119.58
1067	S49	-4403	250.58
1068	S48	-4417	119.58
1069	S47	-4431	250.58
1070	S46	-4445	119.58
1071	S45	-4459	250.58
1072	S44	-4473	119.58
1073	S43	-4487	250.58
1074	S42	-4501	119.58
1075	S41	-4515	250.58
1076	S40	-4529	119.58
1077	S39	-4543	250.58
1078	S38	-4557	119.58
1079	S37	-4571	250.58
1080	S36	-4585	119.58
1081	S35	-4599	250.58
1082	S34	-4613	119.58
1083	S33	-4627	250.58
1084	S32	-4641	119.58
1085	S31	-4655	250.58
1086	S30	-4669	119.58
1087	S29	-4683	250.58
1088	S28	-4697	119.58
1089	S27	-4711	250.58
1090	S26	-4725	119.58
1091	S25	-4739	250.58
1092	S24	-4753	119.58
1093	S23	-4767	250.58
1094	S22	-4781	119.58
1095	S21	-4795	250.58
1096	S20	-4809	119.58
1097	S19	-4823	250.58
1098	S18	-4837	119.58
1099	S17	-4851	250.58
1100	S16	-4865	119.58
1101	S15	-4879	250.58
1102	S14	-4893	119.58
1103	S13	-4907	250.58
1104	S12	-4921	119.58
1105	S11	-4935	250.58
1106	S10	-4949	119.58
1107	S9	-4963	250.58
1108	S8	-4977	119.58
1109	S7	-4991	250.58
1110	S6	-5005	119.58
1111	S5	-5019	250.58
1112	S4	-5033	119.58
1113	S3	-5047	250.58
1114	S2	-5061	119.58
1115	S1	-5075	250.58
1116	G319	-5131	119.58

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PAD No.	PIN Name	X	Y
1117	G317	-5145	250.58
1118	G315	-5159	119.58
1119	G313	-5173	250.58
1120	G311	-5187	119.58
1121	G309	-5201	250.58
1122	G307	-5215	119.58
1123	G305	-5229	250.58
1124	G303	-5243	119.58
1125	G301	-5257	250.58
1126	G299	-5271	119.58
1127	G297	-5285	250.58
1128	G295	-5299	119.58
1129	G293	-5313	250.58
1130	G291	-5327	119.58
1131	G289	-5341	250.58
1132	G287	-5355	119.58
1133	G285	-5369	250.58
1134	G283	-5383	119.58
1135	G281	-5397	250.58
1136	G279	-5411	119.58
1137	G277	-5425	250.58
1138	G275	-5439	119.58
1139	G273	-5453	250.58
1140	G271	-5467	119.58
1141	G269	-5481	250.58
1142	G267	-5495	119.58
1143	G265	-5509	250.58
1144	G263	-5523	119.58
1145	G261	-5537	250.58
1146	G259	-5551	119.58
1147	G257	-5565	250.58
1148	G255	-5579	119.58
1149	G253	-5593	250.58
1150	G251	-5607	119.58
1151	G249	-5621	250.58
1152	G247	-5635	119.58
1153	G245	-5649	250.58
1154	G243	-5663	119.58
1155	G241	-5677	250.58
1156	G239	-5691	119.58
1157	G237	-5705	250.58
1158	G235	-5719	119.58
1159	G233	-5733	250.58
1160	G231	-5747	119.58
1161	G229	-5761	250.58
1162	G227	-5775	119.58
1163	G225	-5789	250.58
1164	G223	-5803	119.58
1165	G221	-5817	250.58
1166	G219	-5831	119.58
1167	G217	-5845	250.58
1168	G215	-5859	119.58
1169	G213	-5873	250.58
1170	G211	-5887	119.58
1171	G209	-5901	250.58
1172	G207	-5915	119.58
1173	G205	-5929	250.58
1174	G203	-5943	119.58
1175	G201	-5957	250.58
1176	G199	-5971	119.58
1177	G197	-5985	250.58
1178	G195	-5999	119.58
1179	G193	-6013	250.58
1180	G191	-6027	119.58
1181	G189	-6041	250.58
1182	G187	-6055	119.58
1183	G185	-6069	250.58
1184	G183	-6083	119.58
1185	G181	-6097	250.58
1186	G179	-6111	119.58
1187	G177	-6125	250.58
1188	G175	-6139	119.58
1189	G173	-6153	250.58
1190	G171	-6167	119.58
1191	G169	-6181	250.58
1192	G167	-6195	119.58
1193	G165	-6209	250.58
1194	G163	-6223	119.58
1195	G161	-6237	250.58
1196	G159	-6251	119.58
1197	G157	-6265	250.58
1198	G155	-6279	119.58
1199	G153	-6293	250.58
1200	G151	-6307	119.58
1201	G149	-6321	250.58
1202	G147	-6335	119.58
1203	G145	-6349	250.58
1204	G143	-6363	119.58
1205	G141	-6377	250.58
1206	G139	-6391	119.58
1207	G137	-6405	250.58
1208	G135	-6419	119.58
1209	G133	-6433	250.58
1210	G131	-6447	119.58
1211	G129	-6461	250.58
1212	G127	-6475	119.58
1213	G125	-6489	250.58
1214	G123	-6503	119.58
1215	G121	-6517	250.58
1216	G119	-6531	119.58
1217	G117	-6545	250.58
1218	G115	-6559	119.58

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PAD No.	PIN Name	X	Y
1219	G113	-6573	250.58
1220	G111	-6587	119.58
1221	G109	-6601	250.58
1222	G107	-6615	119.58
1223	G105	-6629	250.58
1224	G103	-6643	119.58
1225	G101	-6657	250.58
1226	G99	-6671	119.58
1227	G97	-6685	250.58
1228	G95	-6699	119.58
1229	G93	-6713	250.58
1230	G91	-6727	119.58
1231	G89	-6741	250.58
1232	G87	-6755	119.58
1233	G85	-6769	250.58
1234	G83	-6783	119.58
1235	G81	-6797	250.58
1236	G79	-6811	119.58
1237	G77	-6825	250.58
1238	G75	-6839	119.58
1239	G73	-6853	250.58
1240	G71	-6867	119.58
1241	G69	-6881	250.58
1242	G67	-6895	119.58
1243	G65	-6909	250.58
1244	G63	-6923	119.58
1245	G61	-6937	250.58
1246	G59	-6951	119.58
1247	G57	-6965	250.58
1248	G55	-6979	119.58
1249	G53	-6993	250.58
1250	G51	-7007	119.58
1251	G49	-7021	250.58
1252	G47	-7035	119.58
1253	G45	-7049	250.58
1254	G43	-7063	119.58
1255	G41	-7077	250.58
1256	G39	-7091	119.58
1257	G37	-7105	250.58
1258	G35	-7119	119.58
1259	G33	-7133	250.58
1260	G31	-7147	119.58
1261	G29	-7161	250.58
1262	G27	-7175	119.58
1263	G25	-7189	250.58
1264	G23	-7203	119.58
1265	G21	-7217	250.58
1266	G19	-7231	119.58
1267	G17	-7245	250.58
1268	G15	-7259	119.58
1269	G13	-7273	250.58
1270	G11	-7287	119.58
1271	G9	-7301	250.58
1272	G7	-7315	119.58
1273	G5	-7329	250.58
1274	G3	-7343	119.58
1275	G1	-7357	250.58
1276	DUMMY	-7371	119.58
1277	DUMMY	-7385	250.58
1278	DUMMY	-7399	119.58
	A1	-7480	251.58
	A2	7480	255.58

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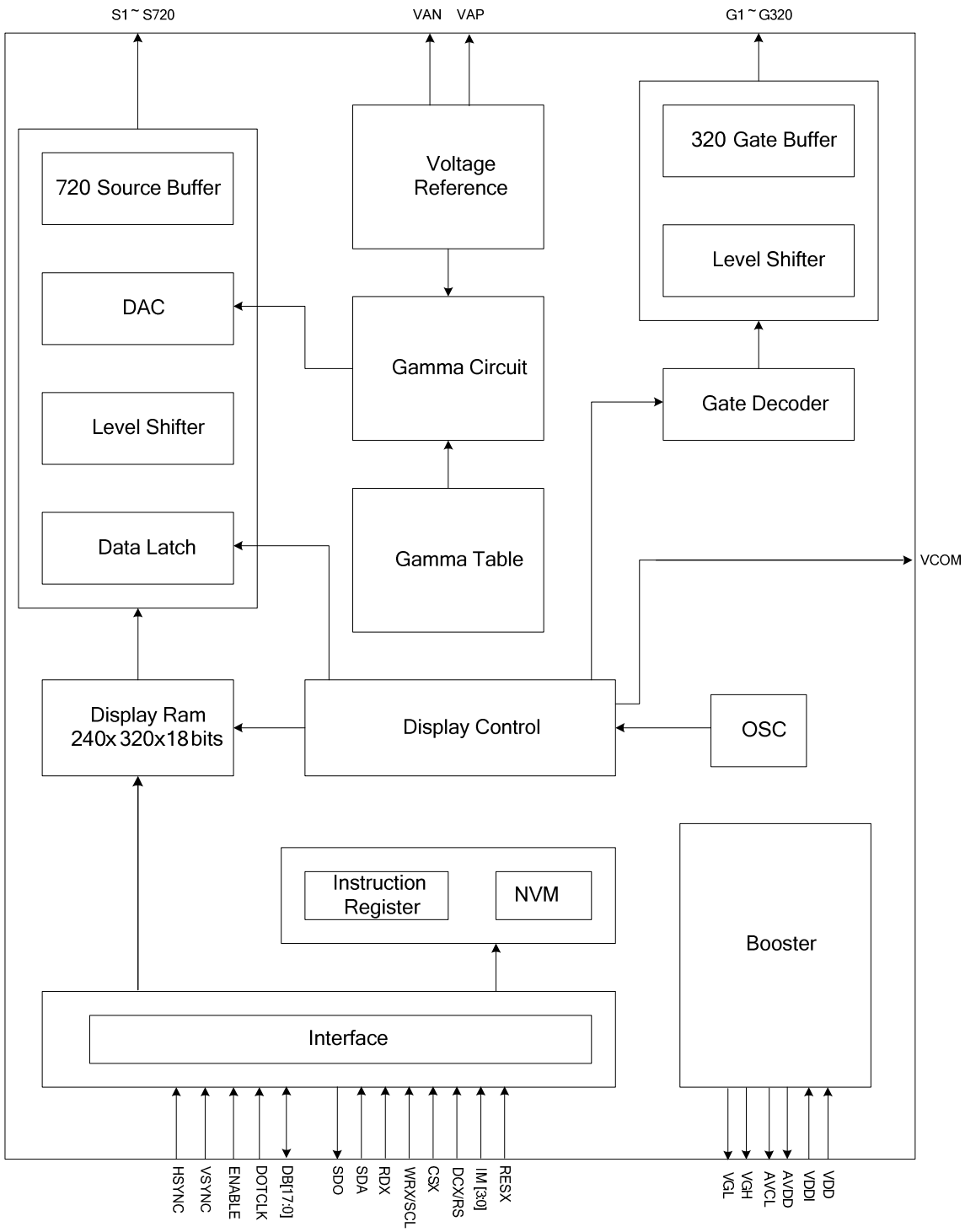
5 BLOCK DIAGRAM



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6 PIN DESCRIPTION

6.1 Power Supply Pins

Name	I/O	Description	Connect Pin
VDD	I	Power Supply for Analog, Digital System and Booster Circuit.	VDD
VDDI	I	Power Supply for I/O System.	VDDI
VDDI_LED	I	Power Supply for LED driver. If not used, please fix this pad to GND level.	-
AGND	I	System Ground for Analog System and Booster Circuit.	GND
DGND	I	System Ground for I/O System and Digital System.	GND

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6.2 Interface Logic Pins

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Connect Pin</th></tr>
<tr><td>IM3, IM2,
IM1, IM0</td><td>I</td><td>-The MCU interface mode select.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU Interface Mode</th><th>Data pin</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>80-8bit parallel I/F</td><td>DB[7:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>80-16bit parallel I/F</td><td>DB[15:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80-9bit parallel I/F</td><td>DB[8:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80-18bit parallel I/F</td><td>DB[17:0],</td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">1</td><td rowspan="2">0</td><td rowspan="2">1</td><td>3-line 9bit serial I/F</td><td>SDA: in/out</td></tr>
<tr><td>2 data lane serial I/F</td><td>SDA: in/out
WRX: in</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-line 8bit serial I/F</td><td>SDA: in/out</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>80-16bit parallel I/F Ⅱ</td><td>DB[17:10],
DB[8:1]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>80-8bit parallel I/F Ⅱ</td><td>DB[17:10]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80-18bit parallel I/F Ⅱ</td><td>DB[17:0],</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80-9bit parallel I/F Ⅱ</td><td>DB[17:9]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-line 9bit serial I/F Ⅱ</td><td>SDA: in/
SDO: out</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>4-line 8bit serial I/F Ⅱ</td><td>SDA:in/
SDO: out</td></tr>
</table></td><td>DGND/VDDI</td></tr>
<tr><td>EXTC</td><td>I</td><td>-Select to access extension command (“Low”: system command 1, “High”: system command 1 and 2).
-When programming NVM, this pin should connect to high level.</td><td>DGND/VDDI</td></tr>
<tr><td>VPP</td><td>I</td><td>-When programming NVM, it needs external power supply voltage (7.5V); the current of Ivpp must be more than 10mA.
-If not used, let this pin open.</td><td>-</td></tr>
<tr><td>RESX</td><td>I</td><td>-This signal will reset the device and it must be applied to properly initialize the chip.
-Signal is active low.</td><td>MCU</td></tr>
<tr><td>CSX</td><td>I</td><td>-Chip selection pin
Low enable.
High disable.</td><td>MCU</td></tr>
<tr><td>DCX</td><td>I</td><td>-Display data/command selection pin in parallel interface.
-This pin is used to be serial interface clock.</td><td>MCU</td></tr>
</table>

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Name	I/O	Description	Connect Pin
		DCX='1': display data or parameter. DCX='0': command data. -If not used, please fix this pin at VDDI or DGND.	
RDX	I	-Read enable in 8080 MCU parallel interface. -If not used, please fix this pin at VDDI or DGND.	MCU
WRX	I	-Write enable in MCU parallel interface. - Display data/command selection pin in 4-line serial interface. - Second Data lane in 2 data lane serial interface. -If not used, please fix this pin at VDDI or DGND.	MCU
VSYNC	I	-Vertical (Frame) synchronizing input signal for RGB interface operation. -If not used, please fix to the VDDI or DGND.	MCU
HSYNC	I	-Horizontal (Line) synchronizing input signal for RGB interface operation. - If not used, please fix to VDDI or DGND.	MCU
ENABLE	I	-Data enable signal for RGB interface operation. -If not used, please fix this pin at VDDI or DGND.	MCU
DOTCLK	I	-Dot clock signal for RGB interface operation. -If not used, please fix this pin at VDDI or DGND.	MCU
SDA	I/O	-When IM3: Low, SPI interface input/output pin. -When IM3: High, SPI interface input pin. -The data is latched on the rising edge of the SCL signal. -If not used, please fix this pin at VDDI or DGND level.	MCU
SDO	O	-SPI interface output pin. -The data is output on the falling edge of the SCL signal. -If not used, let this pin open.	MCU
DB[17:0]	I/O	-DB[17:0] are used as MCU parallel interface data bus. 8-bit I/F: when IM3:0, DB[7:0] are used; when IM3:1, DB[17:10] are used. 9-bit I/F: when IM3:0, DB[8:0] are used; when IM3:1, DB[17:9] are used. 16-bit I/F: when IM3:0, DB[15:0] are used; when IM3:1, DB[17:10] and DB[8:1] are used. 18-bit I/F: DB[17:0] are used. -DB[17:0] are used as RGB interface data bus. 6-bit RGB I/F: DB[5:0] are used. 16-bit RGB I/F: DB[17:13], DB[11:1] are used. 18-bit RGB I/F: DB[17:0] are used. -If not used, please fix this pin at VDDI or DGND.	MCU
TE	O	-Tearing effect signal is used to synchronize MCU to frame memory	MCU

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Name	I/O	Description	Connect Pin
		writing. -If not used, please let this pin open	

Note1. "1" = VDDI level, "0" = DGND level.

Note2. When in parallel mode, unused data pins must be connected to "1" or "0".

Note3. When CSX="1", there is no influence to the parallel and serial interface.

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6.3 Driver Output Pins

Name	I/O	Description	Connect pin
S1 to S720	O	-Source driver output pad.	LCD
G1 to G320	O	-Gate driver output pad. VGH: Selecting Gate Lines Level. VGL: Non-selecting Gate Lines Level.	LCD
AVDD	O	-Power pad for analog circuit.	OPEN
VAP(GVDD)	O	- A power output of grayscale voltage generator.	OPEN
AVCL	O	- A power supply pin for generating VAN.	OPEN
VAN(GVCL)	O	- A power output (Negative) of grayscale voltage generator.	OPEN
VGH	O	- Power output pin for gate driver	OPEN
VGL	O	- Power output (Negative) pin for gate driver	OPEN
VCC	O	- Monitoring pin of internal digital reference voltage.	OPEN
VCOM	O	- A power supply for the TFT-LCD common electrode.	GND
LED_PWM	O	-Output pad for PWM output signal to driving LED. -If not used, keep it open.	-
LED_EN	O	-Output pad for enabling LED. -If not used, keep it open.	-

6.4 Test and other pins

TEST3~TEST0	I	Input pins for testing. Please open these pins.	OPEN
TE2	O	Output pin for testing. Please keep this pin floating.	OPEN
TESTO6~TESTO1	O	Output pins for testing. Please keep these pins floating.	OPEN
DUMMY	-	These pins are dummy (no electrical characteristic) Can pass signal through these pads on TFT panel. Please open these pins.	OPEN
DUMMYR1 DUMMYR2	-	These pins are dummy (no electrical characteristic). DUMMYR1 and DUMMYR2 are connected each other internally.	OPEN
VAG VDDS VDDGX V20	O	Used for monitoring Please keep these pins floating.	OPEN

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7 DRIVER ELECTRICAL CHARACTERISTICS

7.1 Absolute Operation Range

Item	Symbol	Rating	Unit
Supply Voltage	VDD	- 0.3 ~ +4.6	V
Supply Voltage (Logic)	VDDI	- 0.3 ~ +4.6	V
Driver Supply Voltage	VGH-VGL	-0.3 ~ +30.0	V
Logic Input Voltage Range	VIN	-0.3 ~ VDDI + 0.5	V
Logic Output Voltage Range	VO	-0.3 ~ VDDI + 0.5	V
Operating Temperature Range	TOPR	-30 ~ +85	℃
Storage Temperature Range	TSTG	-40 ~ +125	℃

Table 1 Absolute Operation Range

Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

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7.2 DC Characteristics

Parameter	Symbol	Condition	Specification			Unit	Related Pins
			MIN.	TYP.	MAX.		
Power & Operation Voltage							
System Voltage	VDD	Operating voltage	2.4	2.75	3.3	V	
Interface Operation Voltage	VDDI	I/O Supply Voltage	1.65	1.8	3.3	V	
Gate Driver High Voltage	VGH		12.2		14.97	V	Note 4
Gate Driver Low Voltage	VGL		-12.5		-7.16	V	
Gate Driver Supply Voltage		| VGH-VGL |	19.36		27.47	V	Note 5
Input / Output							
Logic-High Input Voltage	VIH		0.7VDDI		VDDI	V	Note 1
Logic-Low Input Voltage	VIL		VSS		0.3VDDI	V	Note 1
Logic-High Output Voltage	VOH	IOH = -1.0mA	0.8VDDI		VDDI	V	Note 1
Logic-Low Output Voltage	VOL	IOL = +1.0mA	VSS		0.2VDDI	V	Note 1
Logic-High Input Current	IIH	VIN = VDDI			1	uA	Note 1
Logic-Low Input Current	IIL	VIN = VSS	-1			uA	Note 1
Input Leakage Current	IIL	IOH = -1.0mA	-0.1		+0.1	uA	Note 1
VCOM Voltage							
VCOM amplitude	VCOM			VSS		V	
Source Driver							
Source Output Range	Vsout		VAN		VAP	V	
Gamma Reference Voltage(Positive)	VAP		4.45		6.4	V	Note 6
Gamma Reference Voltage(Negative)	VAN		-4.6		-2.65	V	
Source Output Settling Time	Tr	Below with 99% precision			20	us	Note 2
Output Offset Voltage	VOFFSET				35	mV	Note 3

Table 2 Basic DC Characteristics

Notes:

1. TA= -30 to 70℃ (to +85℃ no damage).

2. Source channel loading= 2KΩ+12pF/channel, Gate channel loading=5KΩ+40pF/channel.

3. The Max. value is between measured point of source output and gamma setting value.

4. When evaluating the maximum and minimum of VGH, VDD=2.8V.

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5. The maximum value of |VGH-VGL| can no over 30V.

6. Default register setting of Vcom and Vcomoffset is 20h

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7.3 Power Consumption

Ta=25℃, Frame rate = 60Hz, Registers setting are IC default setting.

Operation Mode	Image	Current Consumption			
		Typical		Maximum	
		IDDI (mA)	IDD (mA)	IDDI (mA)	IDD (mA)
Normal Mode	Black	0.005	6.0	0.01	7.5
Partial + Idle Mode (48 lines)	Black	0.005	5.0	0.01	6.0
Sleep-in Mode	N/A	0.005	0.015	0.01	0.03

Table 3 Power Consumption

Notes:

1. The Current Consumption is DC characteristics of ST7789VW.

2. Typical: VDDI=1.8V, VDD=2.75V; Maximum: VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V

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7.4 AC Characteristics

7.4.1 8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus

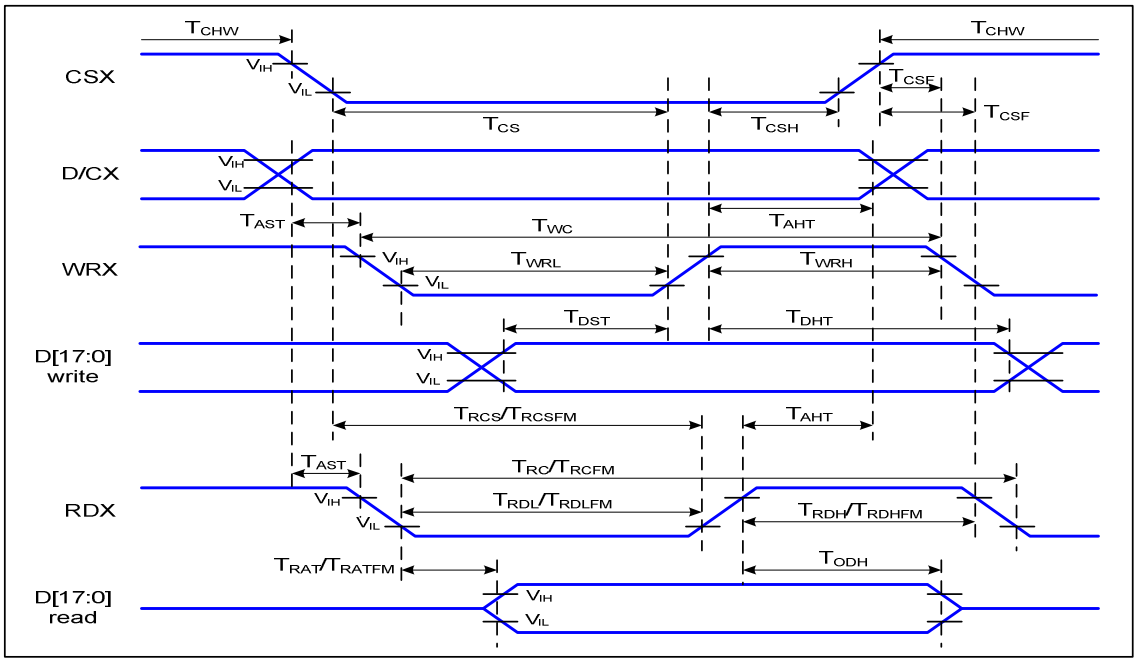

Figure 1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select “H” pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse “H” duration	15		ns	
	T_{WRL}	Control pulse “L” duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse “H” duration (ID)	90		ns	
	T_{RDL}	Control pulse “L” duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse “H” duration (FM)	90		ns	
	T_{RDLFM}	Control pulse “L” duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For CL=30pF

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	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)		40	ns	
	T_{RATFM}	Read access time (FM)		340	ns	
	T_{ODH}	Output disable time	20	80	ns	

Table 4 8080 Parallel Interface Characteristics

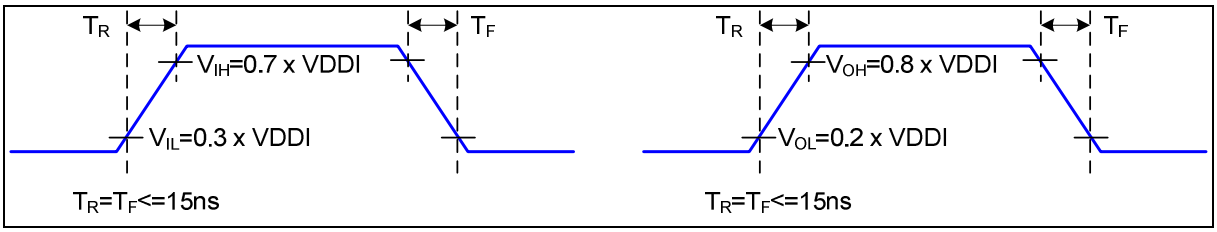

Figure 2 Rising and Falling Timing for I/O Signal

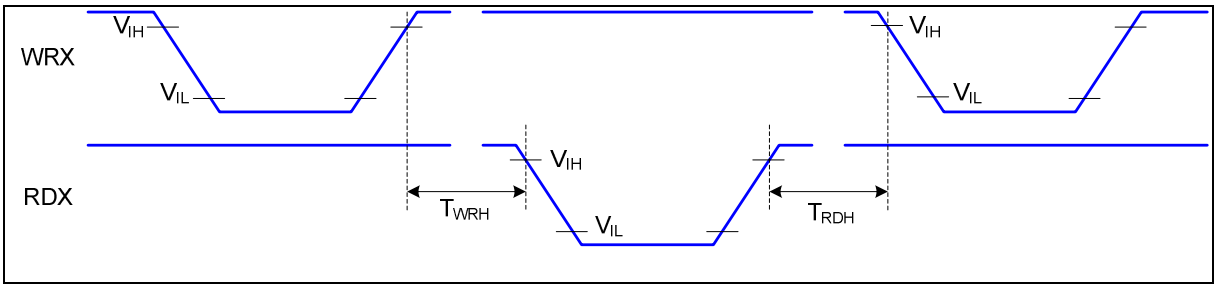

Figure 3 Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

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7.4.2 Serial Interface Characteristics (3-line serial):

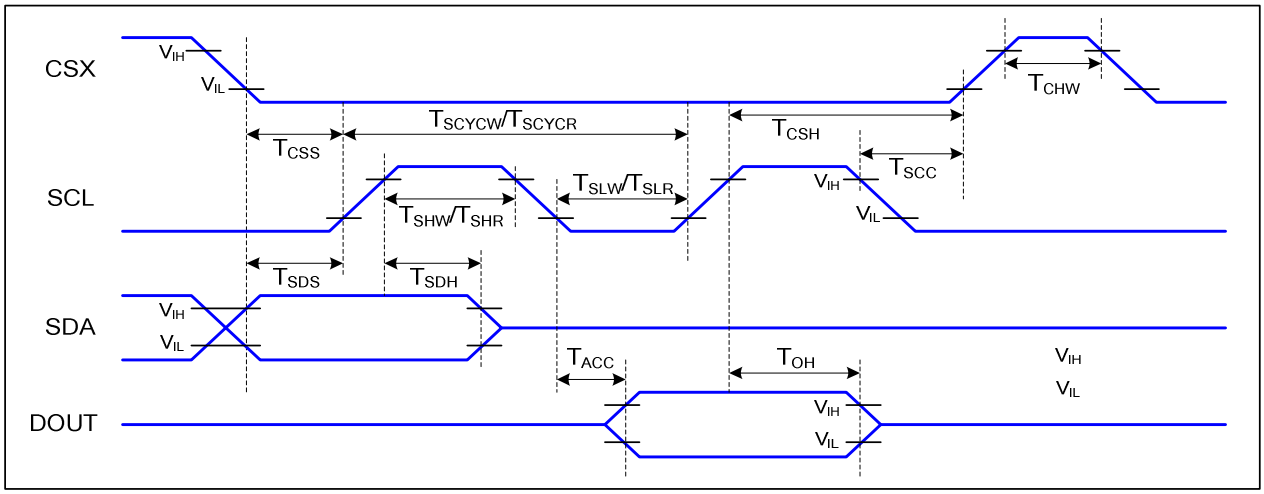

Figure 4 3-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	16		ns	
	T_{SHW}	SCL “H” pulse width (Write)	7		ns	
	T_{SLW}	SCL “L” pulse width (Write)	7		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	7		ns	
	T_{SDH}	Data hold time	7		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Table 5 3-line serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

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7.4.3 Serial Interface Characteristics (4-line serial):

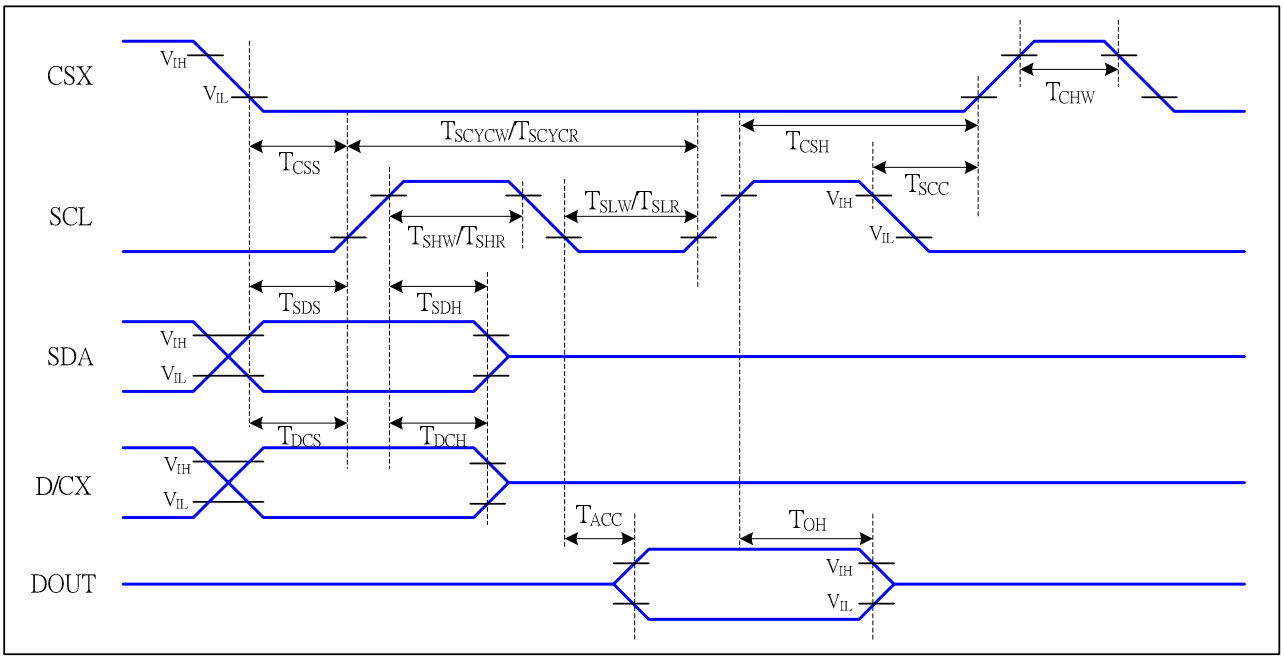

Figure 5 4-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	16		ns	-write command & data ram
	T_{SHW}	SCL “H” pulse width (Write)	7		ns	
	T_{SLW}	SCL “L” pulse width (Write)	7		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	7		ns	
	T_{SDH}	Data hold time	7		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF For minimum CL=8pF
	T_{OH}	Output disable time	15	50	ns	

Table 6 4-line serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as

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30% and 70% of VDDI for Input signals.

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7.4.4 RGB Interface Characteristics:

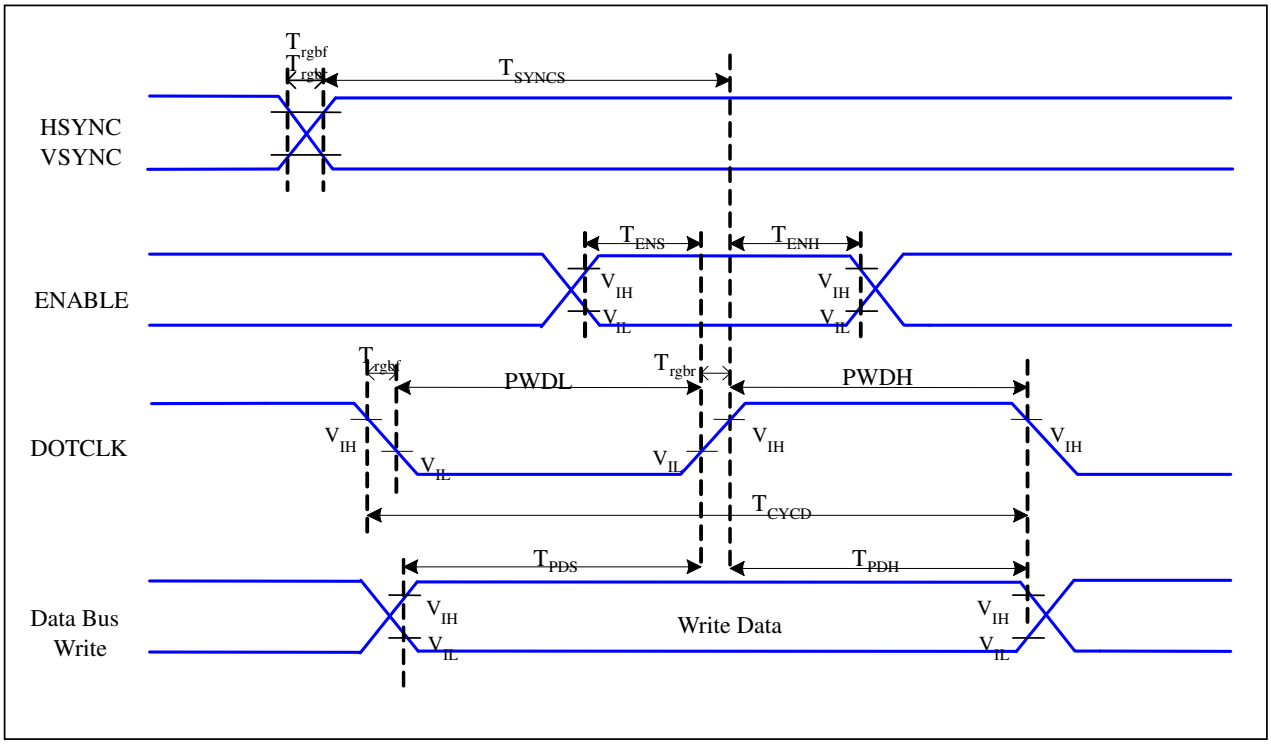

Figure 6 RGB Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	30	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	25	-	ns	
	T_{ENH}	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	60	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	60	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	120	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	20	ns	
DB	T_{PDS}	PD Data Setup Time	50	-	ns	
	T_{PDH}	PD Data Hold Time	50	-	ns	

Table 7 18/16 Bits RGB Interface Timing Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	35	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	35	-	ns	

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	T_{ENH}	Enable Hold Time	35	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	35	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	35	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	80	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	10	ns	
DB	T_{PDS}	PD Data Setup Time	35	-	ns	
	T_{PDH}	PD Data Hold Time	35	-	ns	

Table 8 6 Bits RGB Interface Timing Characteristics

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7.4.5 Reset Timing:

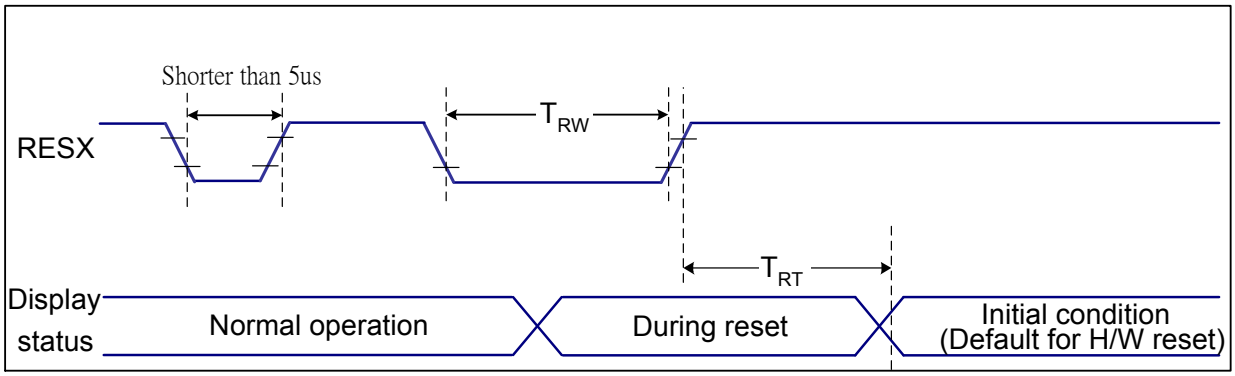

Figure 7 Reset Timing

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 9 Reset Timing

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:

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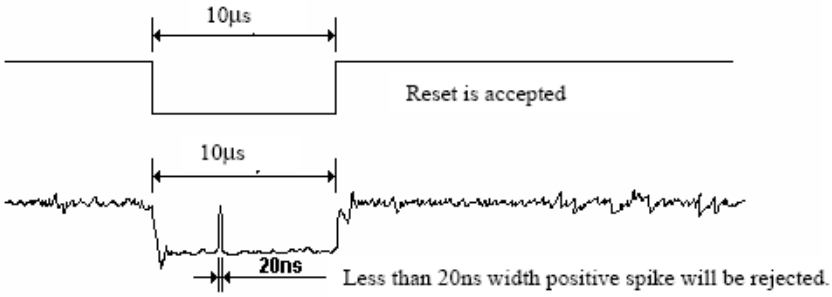

5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

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8 FUNCTION DESCRIPTION

8.1 MPU Interface Type Selection

ST7789VW supports 8/16/9/18 bit parallel data bus for 8080 series CPU, RGB serial interfaces. Selection of these interfaces are set by IM[3:0] pins as shown below.

IM3	IM2	IM1	IM0	Interface	Read Back Data Bus Selection
0	0	0	0	80-8bit parallel I/F	DB[7:0]
0	0	0	1	80-16bit parallel I/F	DB[15:0]
0	0	1	0	80-9bit parallel I/F	DB[8:0]
0	0	1	1	80-18bit parallel I/F	DB[17:0],
0	1	0	1	3-line 9bit serial I/F	SDA: in/out
				2 data lane serial I/F	SDA: in/out, WRX: in
0	1	1	0	4-line 8bit serial I/F	SDA: in/out
1	0	0	0	80-16bit parallel I/F Ⅱ	DB[17:10], DB[8:1]
1	0	0	1	80-8bit parallel I/F Ⅱ	DB[17:10]
1	0	1	0	80-18bit parallel I/F Ⅱ	DB[17:0],
1	0	1	1	80-9bit parallel I/F Ⅱ	DB[17:9]
1	1	0	1	3-line 9bit serial I/F Ⅱ	SDA: in/ SDO: out
1	1	1	0	4-line 8bit serial I/F Ⅱ	SDA: in/ SDO: out

Table 10 Interface Type Selection

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8.2 8080-Ⅰ Series MCU Parallel Interface

The MCU can use one of following interfaces: 11-lines with 8-data parallel interface, 12-lines with 9-data parallel interface, 19-line with 16-data parallel interface or 21-lines with 18-data parallel interface. The chip-select CSX (active low) enables/disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write enable, RDX is the parallel data read enable and D[17:0] is parallel data bus.

The LCD driver reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits is either display data or command parameter. When D/C='0', D[17:0] bits is command. The interface functions of 8080-series parallel interface are given in following table.

IM3	IM2	IM1	IM0	Interface	D/CX	RDX	WRX	Read back selection
0	0	0	0	8-bit parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 8-bit display data or 8-bit parameter (D7 to D0)
					1	↑	1	Read 8-bit display data (D7 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)
0	0	0	1	16-bit parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 16-bit display data or 8-bit parameter (D15 to D0)
					1	↑	1	Read 16-bit display data (D15 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)
0	0	1	0	9-bit parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 9-bit display data or 8-bit parameter (D8 to D0)
					1	↑	1	Read 9-bit display data (D8 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)
0	0	1	1	18-bit parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 18-bit display data or 8-bit parameter (D17 to D0)
					1	↑	1	Read 18-bit display data (D17 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)

Table 11 the function of 8080-series parallel interface

8.2.1 Write cycle sequence

The write cycle means that the host writes information (command / data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control signals (DCX, RDX, WRX) and data signals (DB[17:0]). DCX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data ('1').

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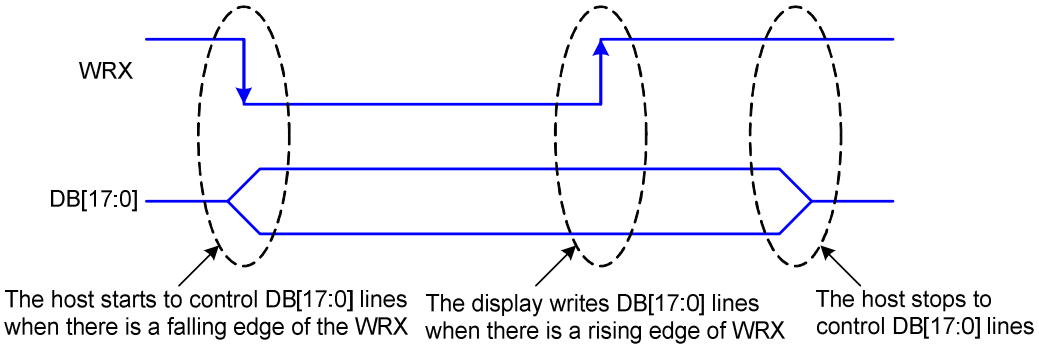

Figure 8 8080-Series WRX Protocol

Note: WRX is an unsynchronized signal (It can be stopped).

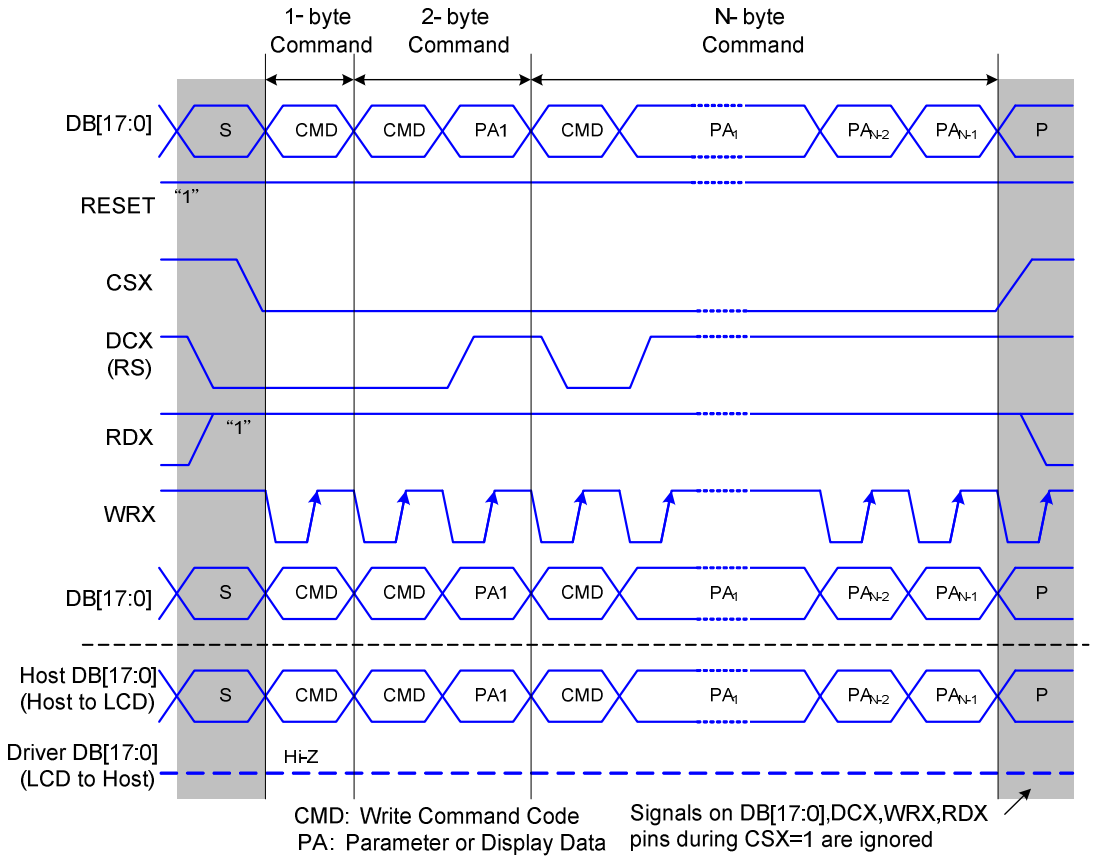

Figure 9 8080-Series Parallel Bus Protocol, Write to Register or Display RAM

8.2.2 Read cycle sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from LCD driver via interface. The driver sends data (D[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

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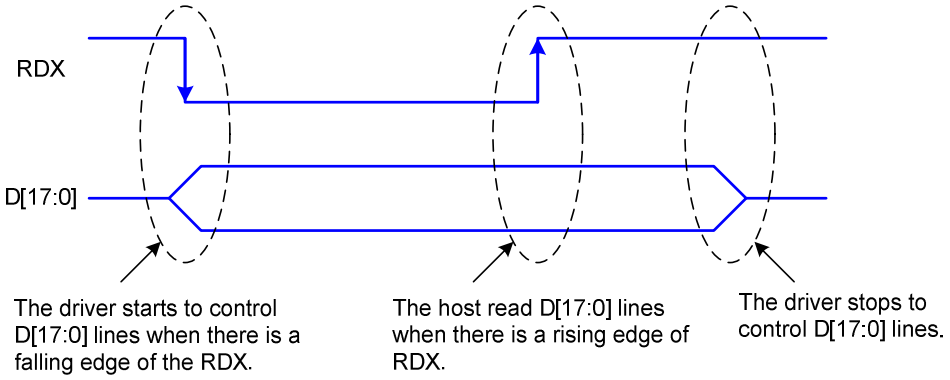

Figure 10 8080-series RDX protocol

Note: RDX is an unsynchronized signal (It can be stopped).

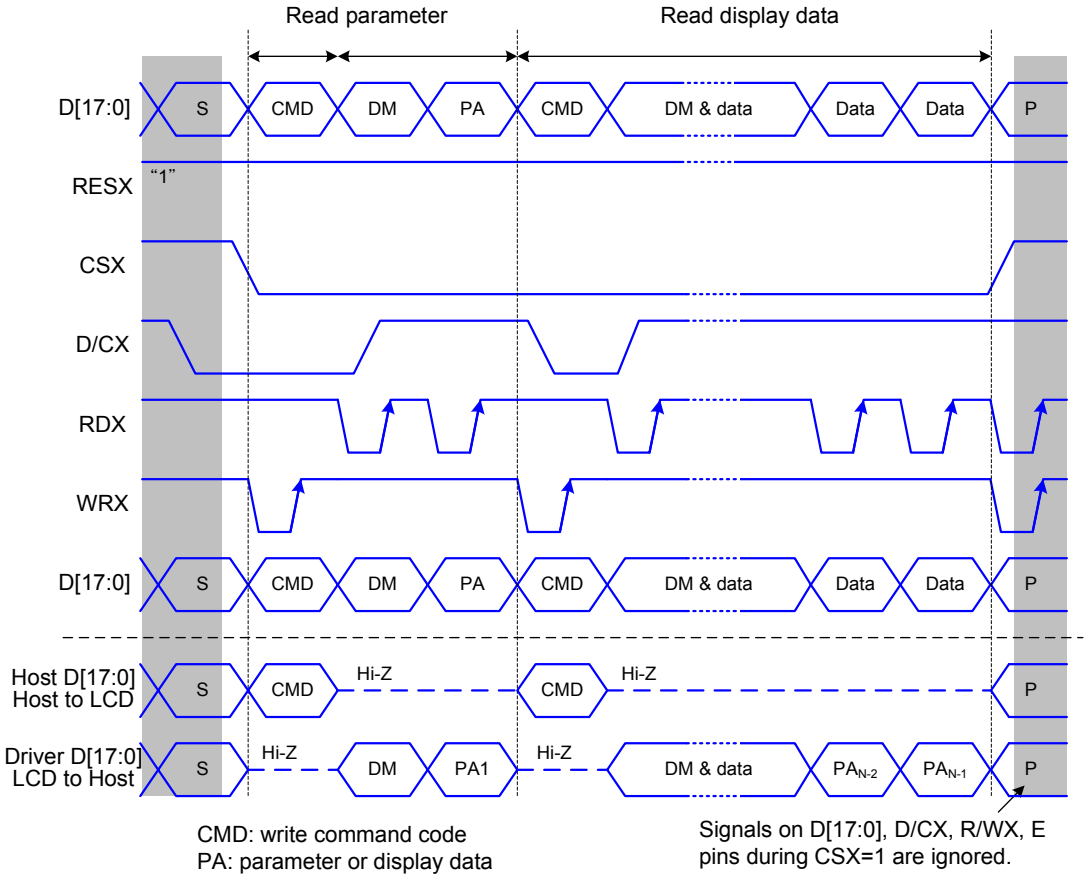

Figure 11 8080-series parallel bus protocol, read data from register or display RAM

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8.3 8080-Ⅱ series MCU Parallel Interface

The MCU uses one of following interface: 11-lines with 8-data parallel interface, 12-lines with 9-data parallel interface, 19-lines with 16-data parallel interface, or 21-lines with 18-data parallel interface. The chip-select CSX(active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. The R/WX is the Read/Write flag and D[17:0] is parallel data bus.

The LCD driver reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits is either display data or command parameter. When D/C='0', D[17:0] bits is command.

The 8080-Ⅱ series bi-directional interface can be used for communication between the micro controller and LCD driver. Interface bus width can be selected with IM3, IM2, IM1 and IM0.The interface functions of 8080-Ⅱ series parallel interface are given in Table 12 The function of 8080-Ⅱ series parallel interface.

IM3	IM2	IM1	IM0	Interface	D/CX	RDX	WRX	Function
1	0	0	0	16-bit Parallel	0	1	↑	Write 8-bit command (D[8:1])
					1	1	↑	Write 16-bit display data or 8-bit parameter (D[17:10], D[8:1])
					1	↑	1	Read 16-bit Display data (D[17:10], D[8:1])
					1	↑	1	Read 8-bit parameter or status (D[8:1])
1	0	0	1	8-bit Parallel	0	1	↑	Write 8-bit command (D[17:10])
					1	1	↑	Write 8-bit display data or 8-bit parameter (D[17:10])
					1	↑	1	Read 8-bit Display data (D[17:10])
					1	↑	1	Read 8-bit parameter or status (D[17:10])
1	0	1	0	18-bit Parallel	0	1	↑	Write 8-bit command (D[8:1])
					1	1	↑	Write 18-bit display data or 8-bit parameter (D[17:0], D[8:1])
					1	↑	1	Read 18-bit Display data (D[17:0])
					1	↑	1	Read 8-bit parameter or status (D[8:1])
1	0	1	1	9-bit Parallel	0	1	↑	Write 8-bit command (D[17:10])
					1	1	↑	Write 9-bit display data or 8-bit parameter (D[17:9])
					1	↑	1	Read 9-bit Display data (D[17:9])
					1	↑	1	Read 8-bit parameter or status (D[17:10])

Table 12 The function of 8080-Ⅱ series parallel interface

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8.4 Serial Interface

IM3	IM2	IM1	IM0	Interface	Read back selection
0	1	0	1	3-line serial interface Ⅰ	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)
0	1	1	0	4-line serial interface Ⅰ	
1	1	0	1	3-line serial interface Ⅱ	
1	1	1	0	4-line serial interface Ⅱ	

Table 13 Selection of serial interface

The serial interface is either 3-lines/9-bits or 4-lines/8-bits bi-directional interface for communication between the micro controller and the LCD driver. The 3-lines serial interface use: CSX (chip enable), SCL (serial clock) and SDA (serial data input/output), and the 4-lines serial interface use: CSX (chip enable), D/CX (data/ command flag), SCL (serial clock) and SDA (serial data input/output). Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

8.4.1 Pin description

3-line serial interface Ⅰ

Pin Name	Description
CSX	Chip selection signal
DCX	Clock signal
SDA	Serial input/output data

4-line serial interface Ⅰ

Pin Name	Description
CSX	Chip selection signal
WRX	Data is regarded as a command when WRX is low Data is regarded as a parameter or data when WRX is high
DCX	Clock signal
SDA	Serial input/output data

3-line serial interface Ⅱ

Pin Name	Description
CSX	Chip selection signal
DCX	Clock signal
SDA	Serial input data
SDO	Serial output data

4-line serial interface Ⅱ

Pin Name	Description
CSX	Chip selection signal
WRX	Data is regarded as a command when WRX is low Data is regarded as a parameter or data when WRX is high

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DCX	Clock signal
SDA	Serial input data
SDO	Serial output data

Table 14 pin description of serial interface

8.4.2 Command write mode

The write mode of the interface means the micro controller writes commands and data to the LCD driver. 3-lines serial data packet contains a control bit D/CX and a transmission byte. In 4-lines serial interface, data packet contains just transmission byte and control bit D/CX is transferred by the D/CX pin. If D/CX is “low”, the transmission byte is interpreted as a command byte. If D/CX is “high”, the transmission byte is stored in the display data RAM (memory write command), or command register as parameter.

Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

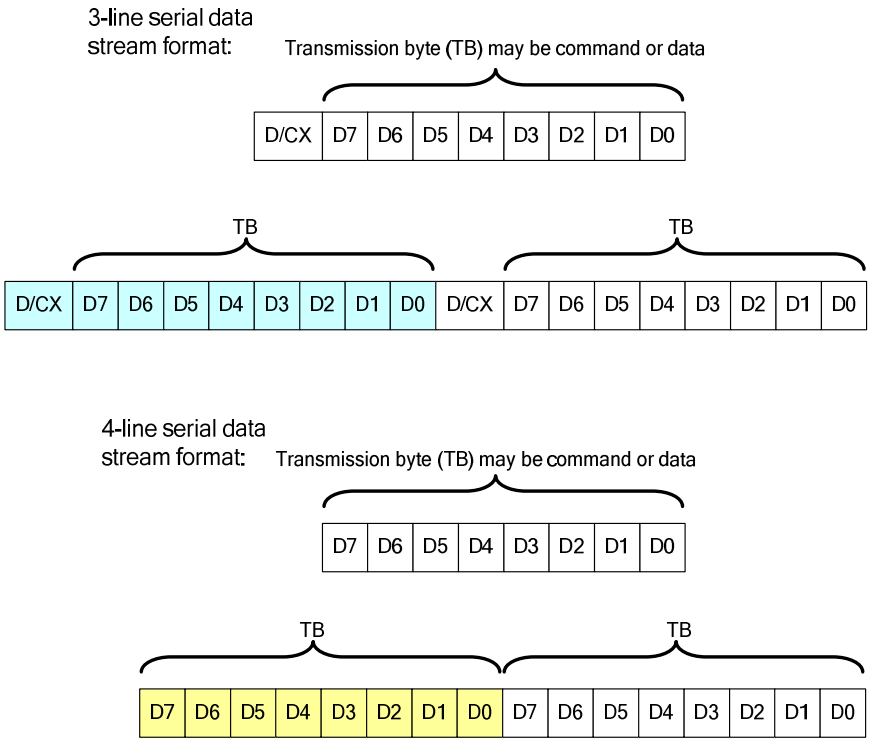

Figure 12 Serial interface data stream format

When CSX is “high”, SCL clock is ignored. During the high period of CSX the serial interface is initialized. At the falling edge of CSX, SCL can be high or low. SDA is sampled at the rising edge of SCL. D/CX indicates whether the byte is command (D/CX=’0’) or parameter/RAM data (D/CX=’1’). D/CX is sampled when first rising edge of SCL (3-line serial interface) or 8th rising edge of SCL (4-line serial interface). If CSX stays low after the last bit of command/data byte, the serial interface expects the D/CX bit (3-line serial interface) or D7

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(4-line serial interface) of the next byte at the next rising edge of SCL..

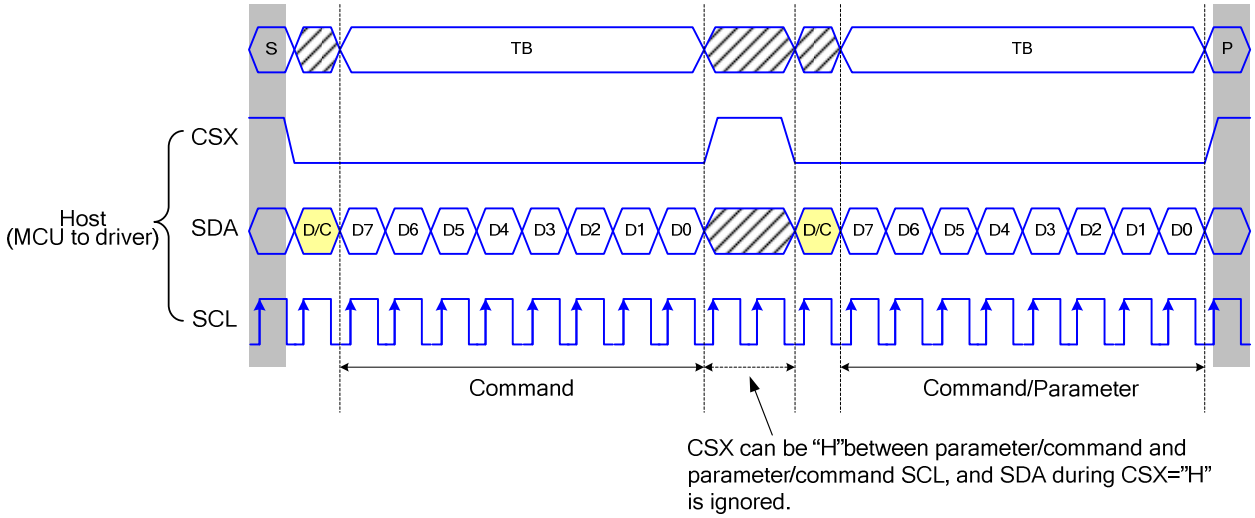

Figure 13 3-line serial interface write protocol (write to register with control bit in transmission)

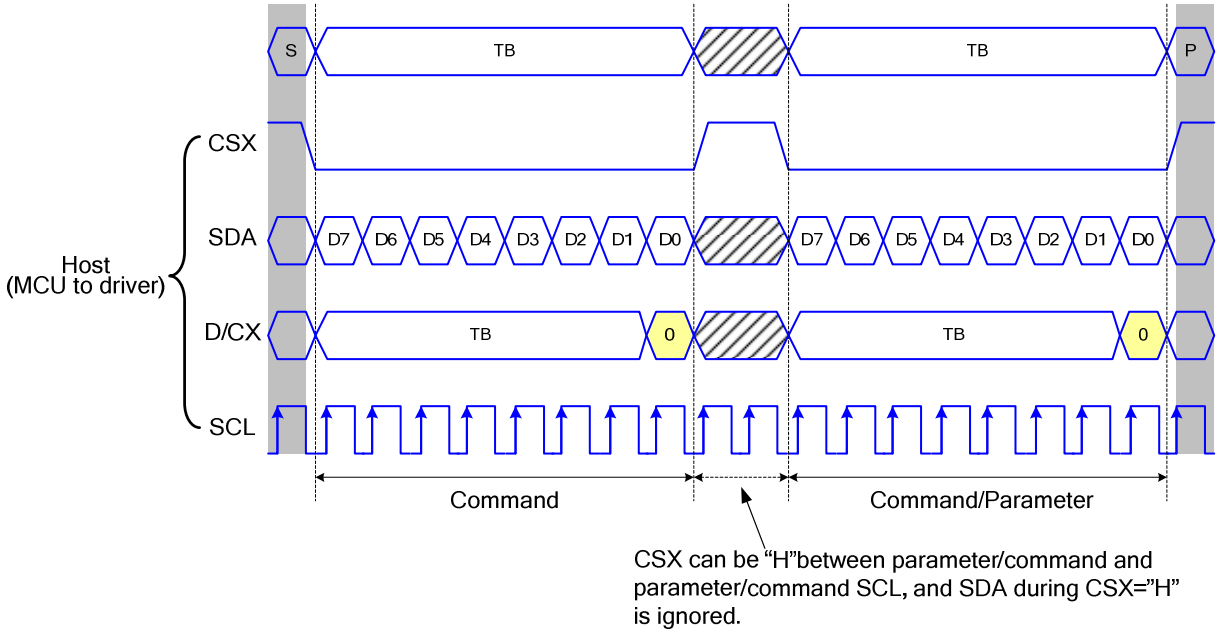

Figure 14 4-line serial interface write protocol (write to register with control bit in transmission)

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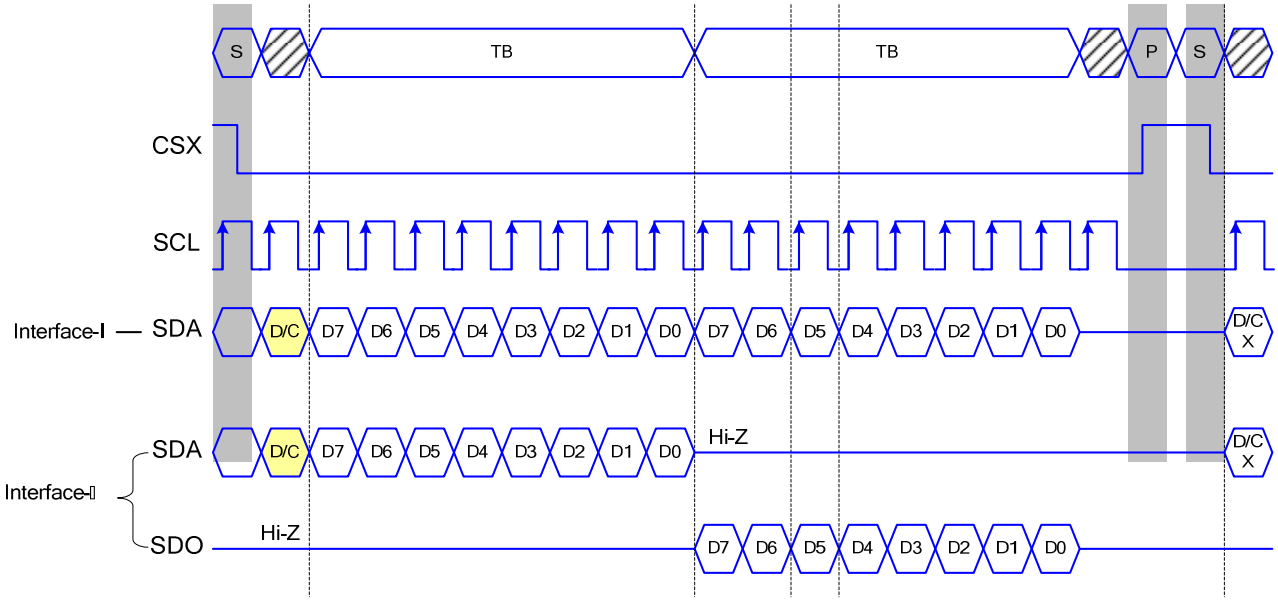
8.4.3 Read function

The read mode of the interface means that the micro controller reads register value from the driver. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

8.4.4 3-line serial interface Ⅰ/Ⅱ protocol

3-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



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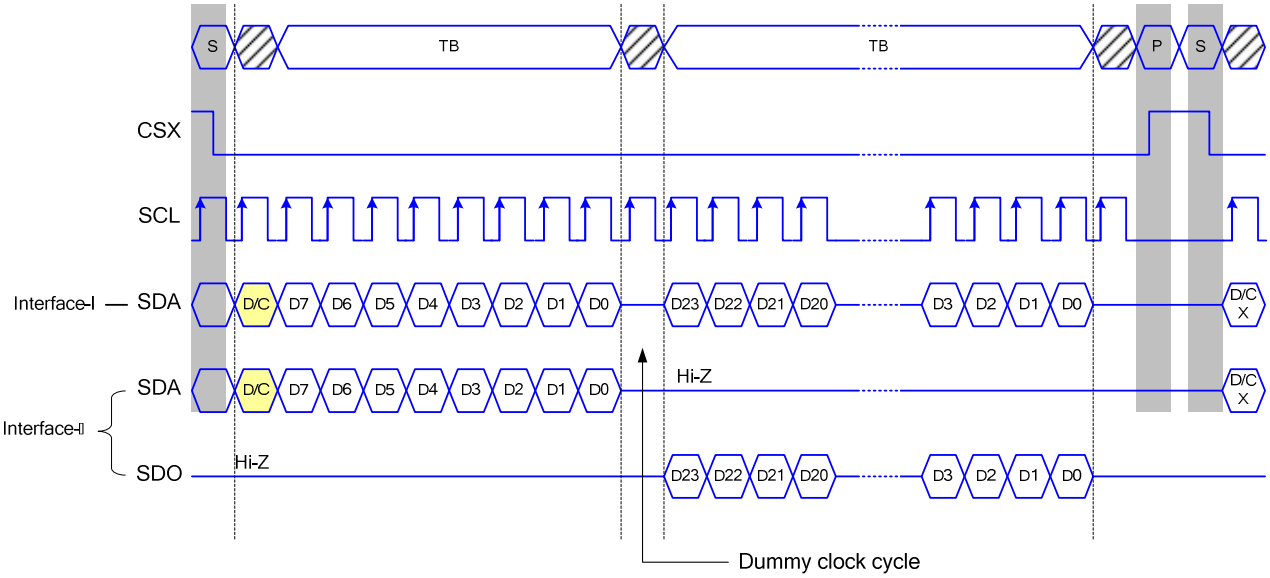
3-line serial protocol (for RDDID command: 24-bit read)



3-line Serial Protocol (for RDDST command: 32-bit read)

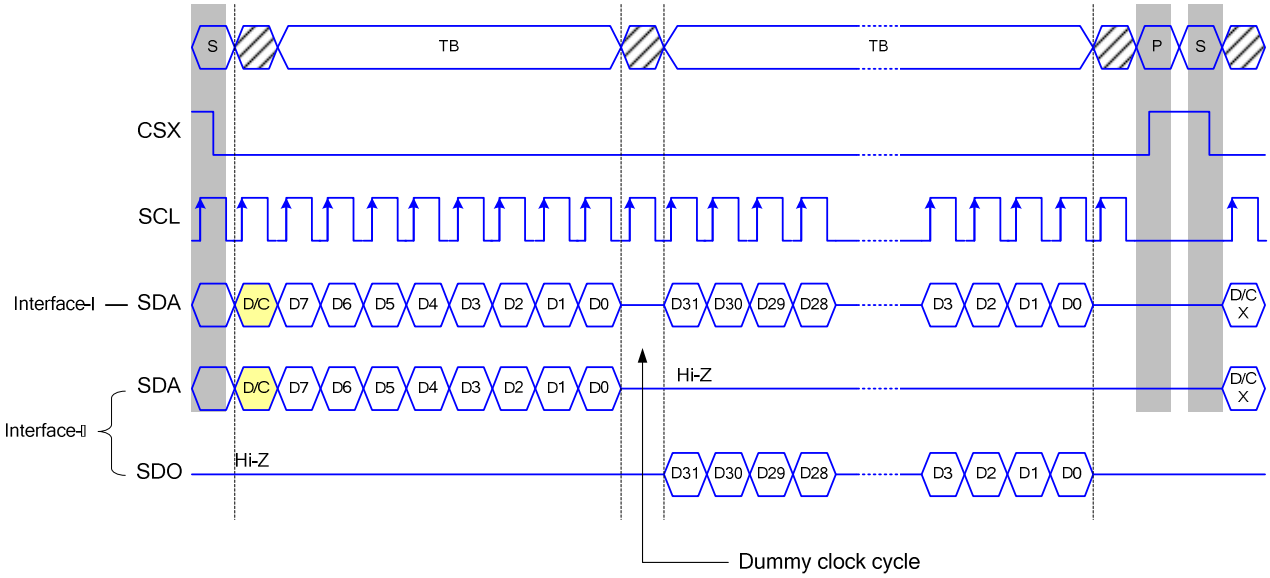


Figure 15 3-line serial interface read protocol

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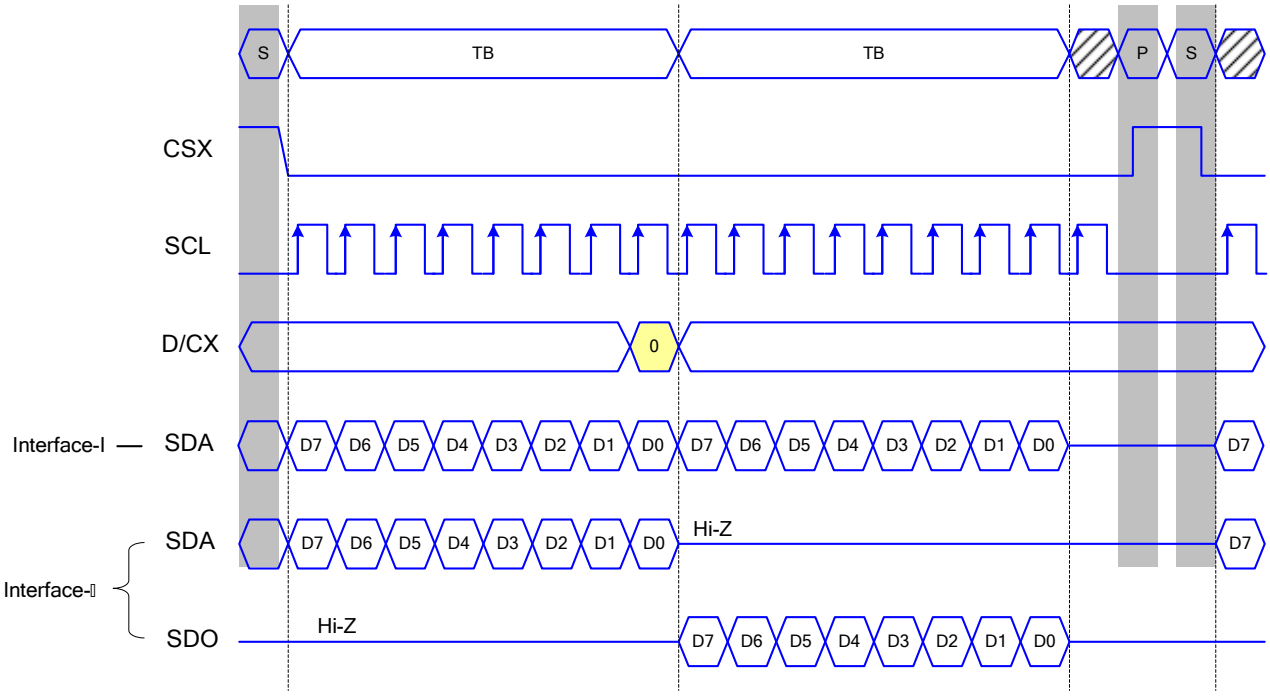
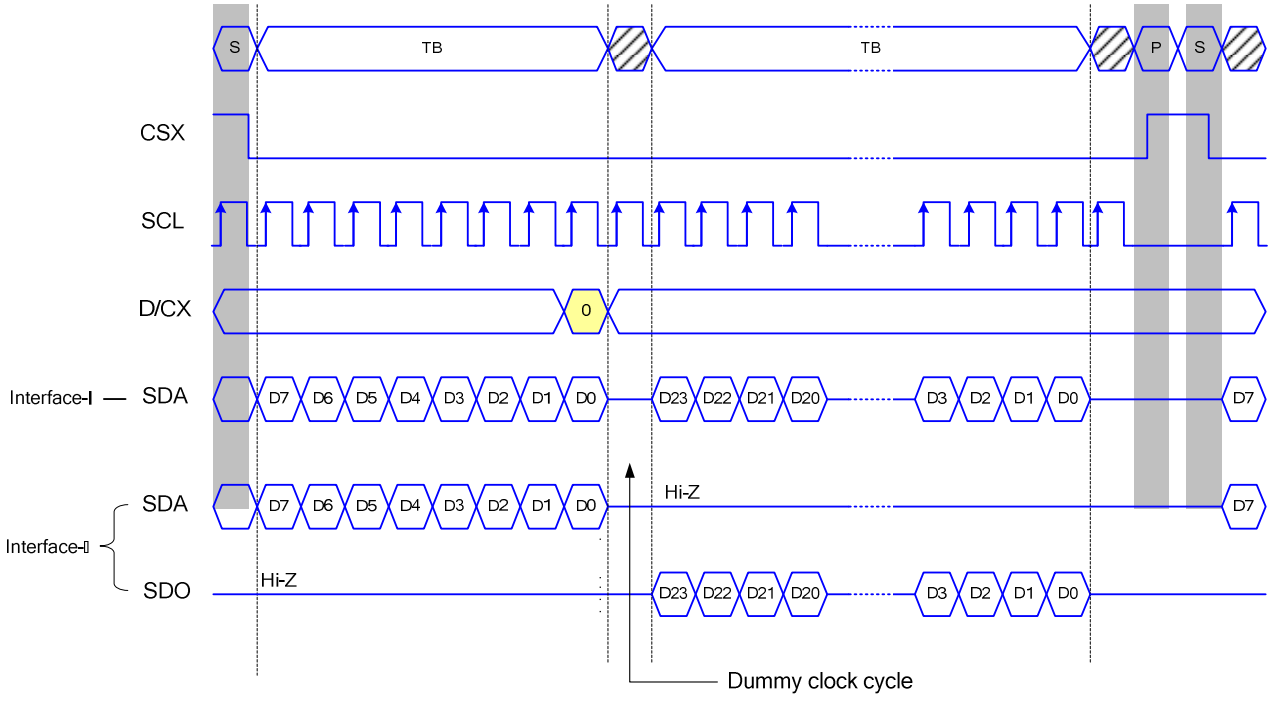
8.4.5 4-line serial protocol

4-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



4-line serial protocol (for RDDID command: 24-bit read)



4-line Serial Protocol (for RDDST command: 32-bit read)

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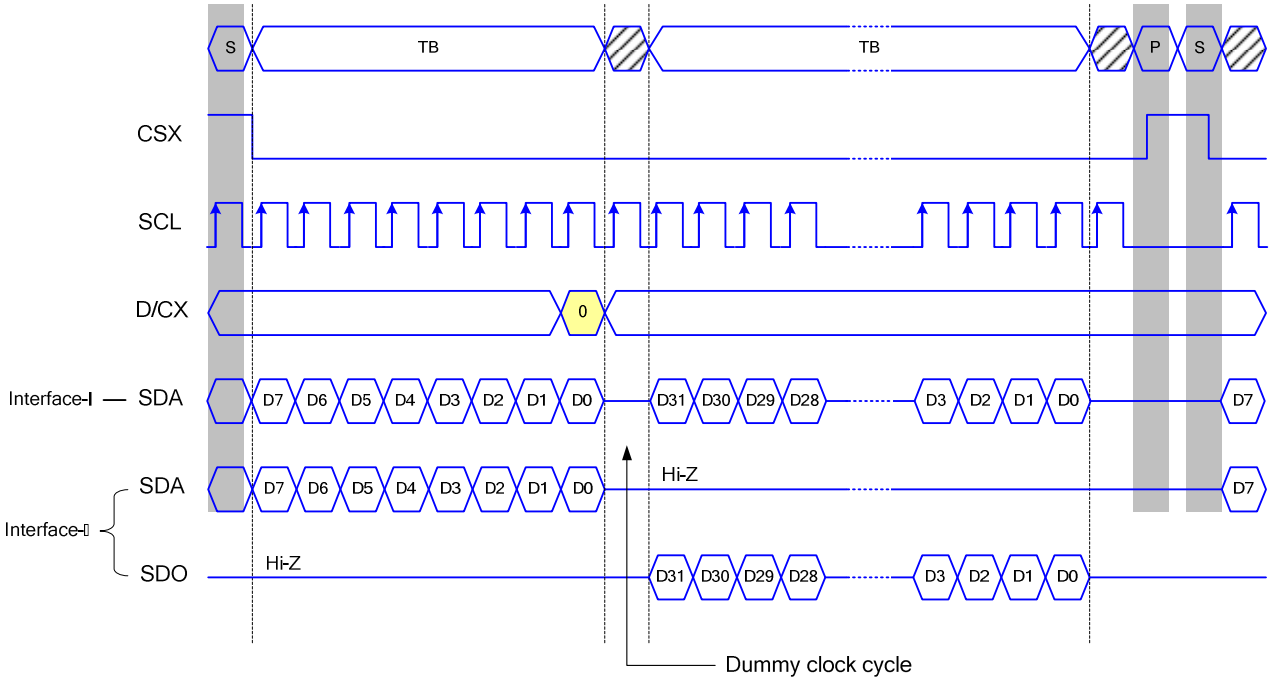

Figure 16 4-line serial interface read protocol

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8.4.6 2 data lane serial Interface

Interface selection:

IM3	IM2	IM1	IM0	Interface	Read back selection
0	1	0	1	2 data lane serial interface	Via the read instruction (8-bit, 24-bit and 32-bit read)

Table 15 IM pin selection

2-wire data lane serial interface use: CSX (chip enable), DCX (serial clock) and SDA (serial data input/output 1), and WRX (serial data input 2). To enter this interface, command E7h need set 10h.

2 data lane hardware suggestion and Pin description:

2 data lane serial interface, IM[3:0]=0101

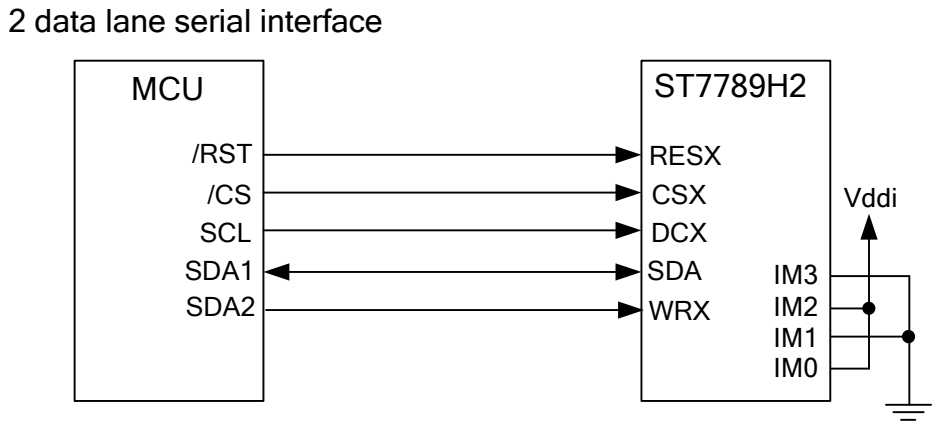

Figure 17 Hardware suggestion of 2 data lane serial interface

Pin Name	Description
CSX	Chip selection signal
DCX	Clock signal
SDA	Serial data input/output1
WRX	Serial data input2

Table 16 Pin description of 2 data lane serial interface

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Command write mode:

The command write protocol of 2-wire data lane serial interface is the same with the 3-line serial interface, so users can ignore the input data of WRX.

Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

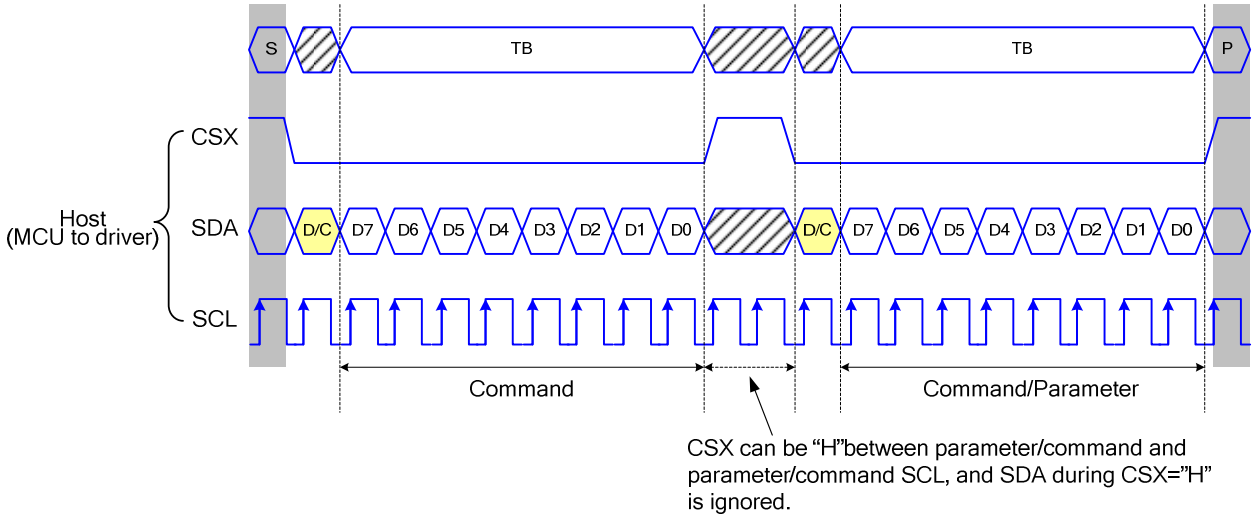

Figure 18 3-line serial interface write protocol (write to register with control bit in transmission)

SRAM write mode:

The SRAM write mode of 2-wire data line serial interface need use SDA pin and WRX pin to be data input pins.

Read function:

The read mode of 2-wire data lane serial interface is the same with the 3-line serial interface and WRX pin can be ignored. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

3-line serial interface Ⅰ/Ⅱ protocol:

3-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):

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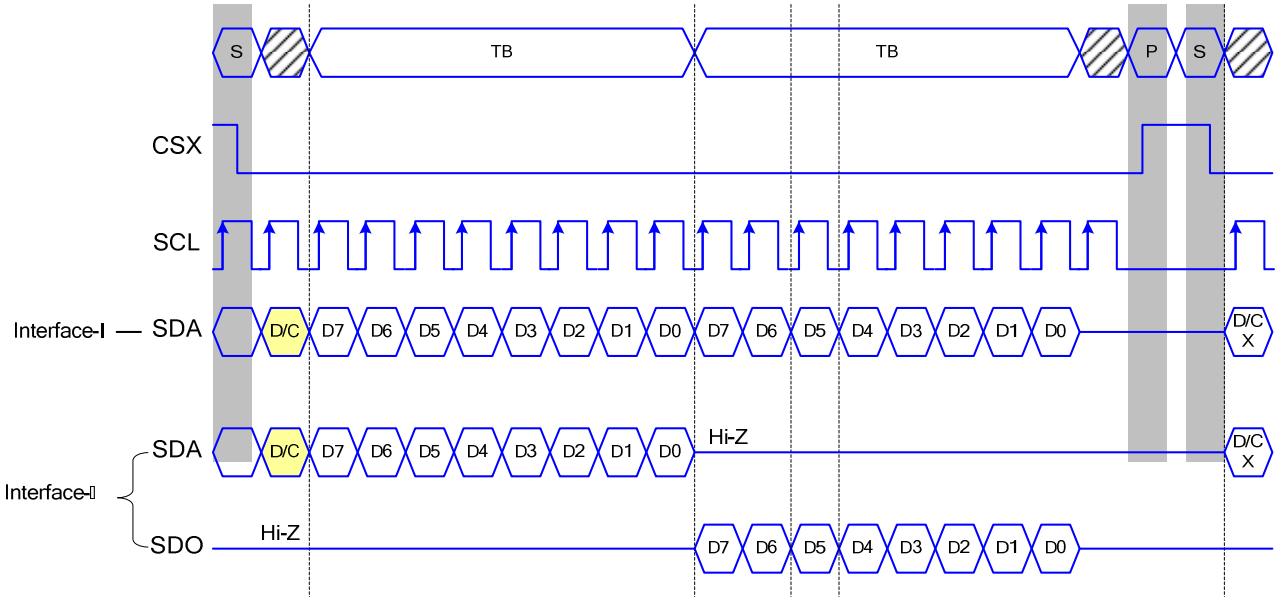
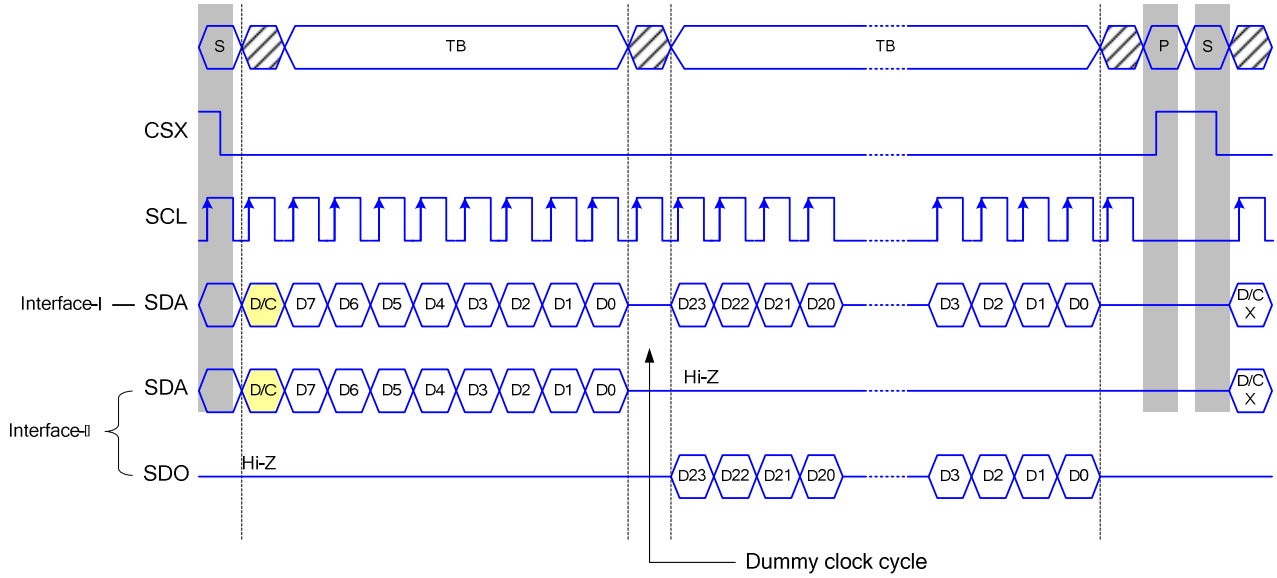


3-line serial protocol (for RDDID command: 24-bit read)



3-line Serial Protocol (for RDDST command: 32-bit read)

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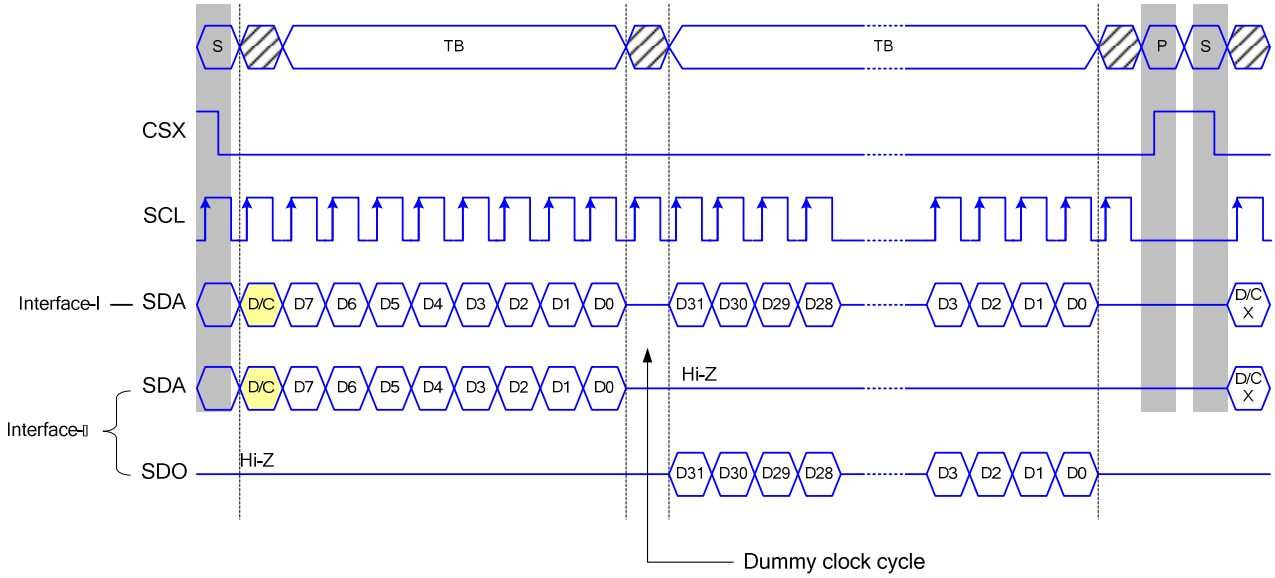

Figure 19 3-line serial interface read protocol

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8.5 Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been HIGH state.

If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated.

If 1, 2 or more parameter commands are being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

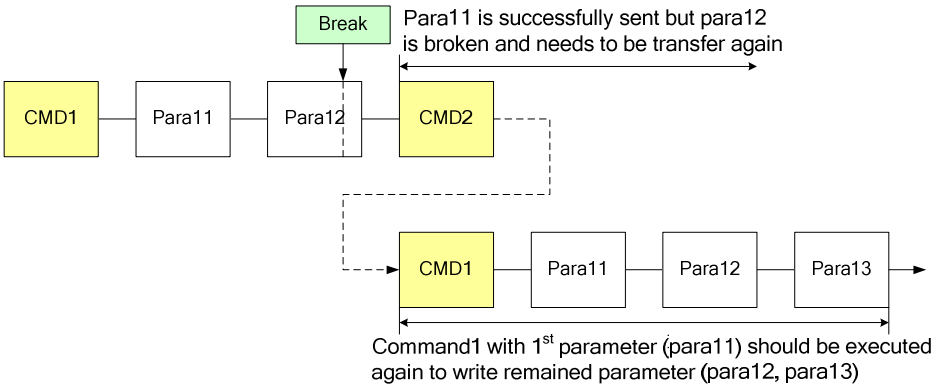

Figure 20 Write interrupts recovery (serial interface)

If a 2 or more parameter commands are being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.

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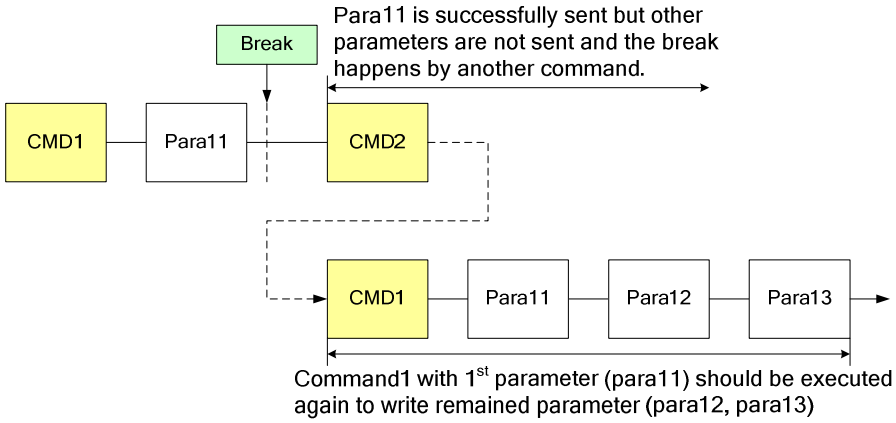

Figure 21 Write interrupts recovery (both serial and parallel Interface)

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8.6 Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select line is released after a whole byte of a frame memory data or multiple parameter data has been completed, then driver will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select Line is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select line is next enabled as shown below.

This applies to the following 4 conditions:

1) Command-Pause-Command

2) Command-Pause-Parameter

3) Parameter-Pause-Command

4) Parameter-Pause-Parameter

8.6.1 Parallel interface pause

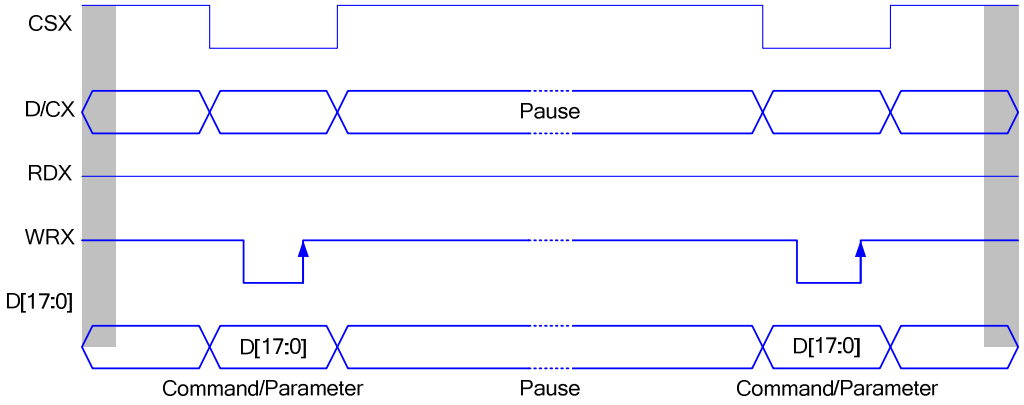


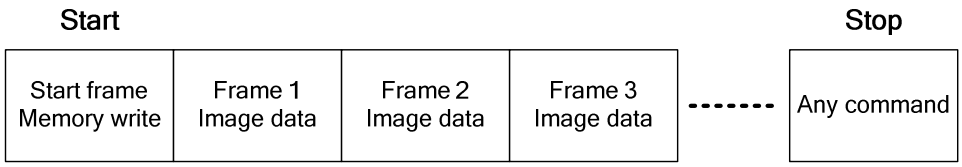
Figure 22 Parallel bus pause protocol (paused by CSX)

8.7 Data Transfer Mode

The module has three kinds color modes for transferring data to the display RAM. These are 12-bit color per pixel, 16-bit color per pixel and 18-bit color per pixel. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

8.7.1 Method 1

The image data is sent to the frame memory in successive frame writes, each time the frame memory is filled, the frame memory pointer is reset to the start point and the next frame is written.



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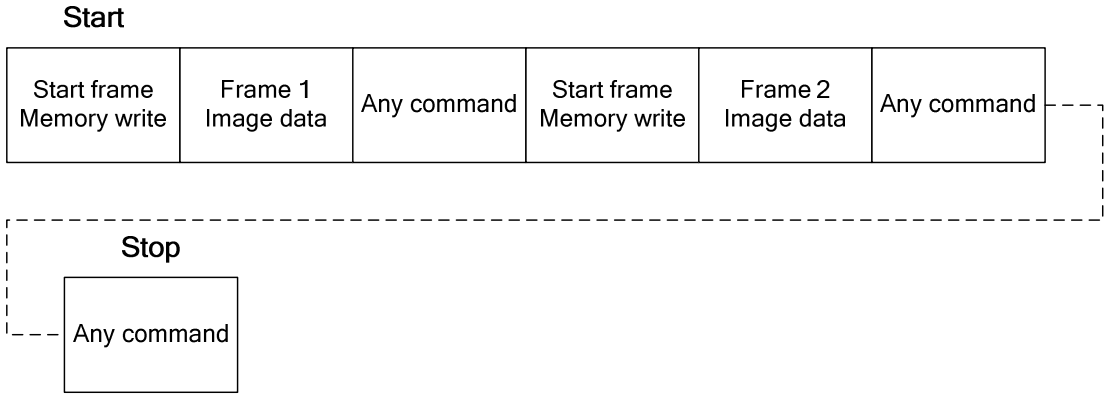
8.7.2 Method 2

The image data is sent and at the end of each frame memory download, a command is sent to stop frame memory write. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These apply to all data transfer Color modes on both serial and parallel interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

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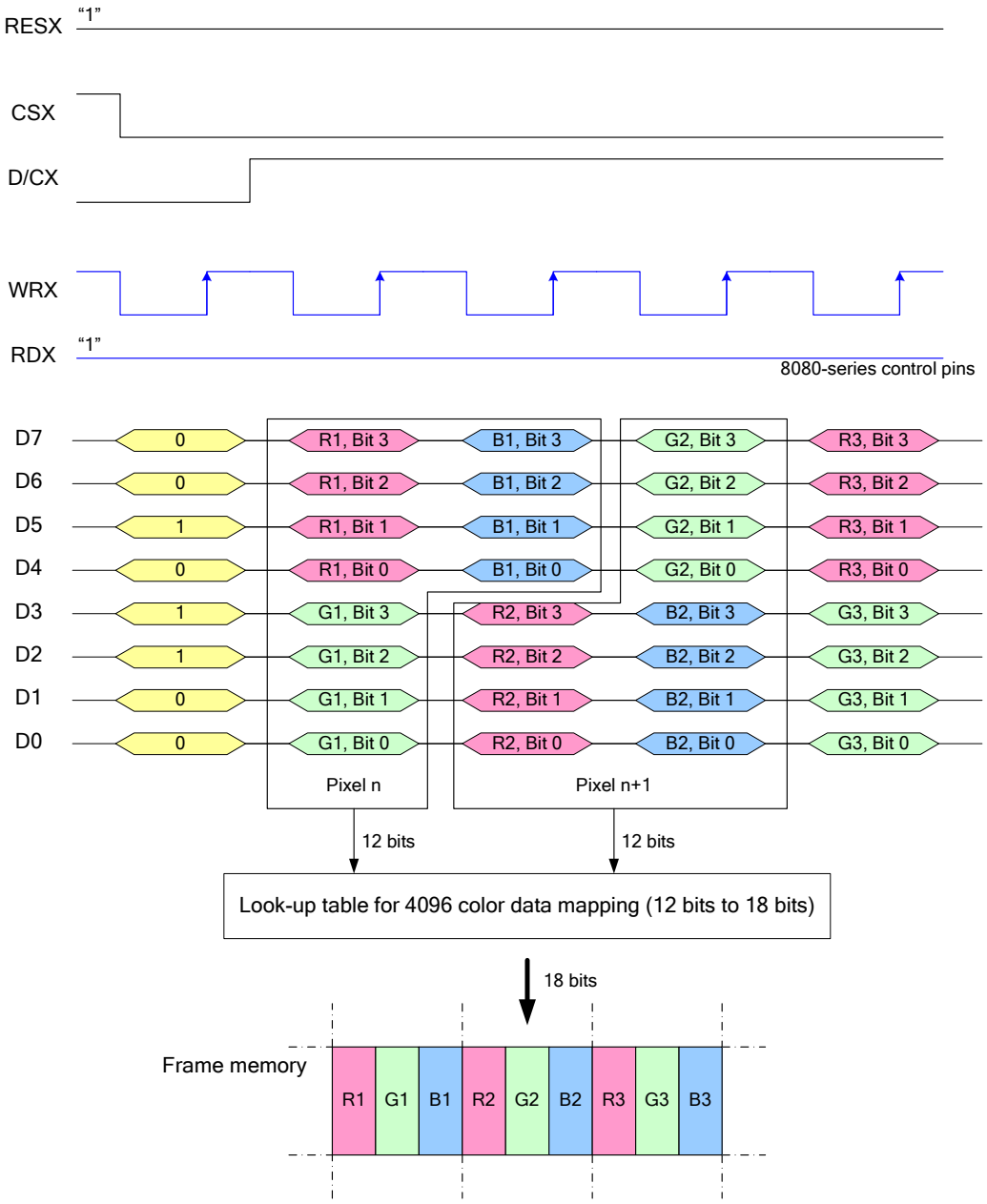
8.8 Data Color Coding

8.8.1 8080- Ⅰ series 8-bit Parallel Interface

The 8080- Ⅰ series 8-bit parallel interface of ST7789VW can be used by setting IM[3:0]="0000b". Different display data formats are available for three Colors depth supported by listed below.

- 4k colors, RGB 4,4,4-bit input.
- 65k colors, RGB 5,6,5-bit input.
- 262k colors, RGB 6,6,6-bit input.

8.8.2 8-bit data bus for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3Ah="03h"



Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.
Note 2: 3-time transfer is used to transmit 2 pixel data with the 12-bit color depth information.
Note 3: '-' = Don't care – Can be set to '0' or '1'

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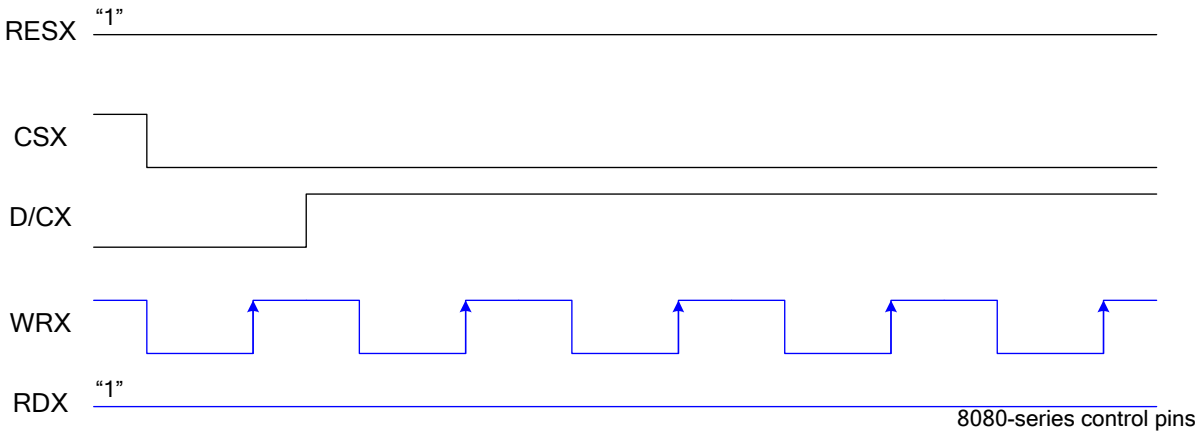
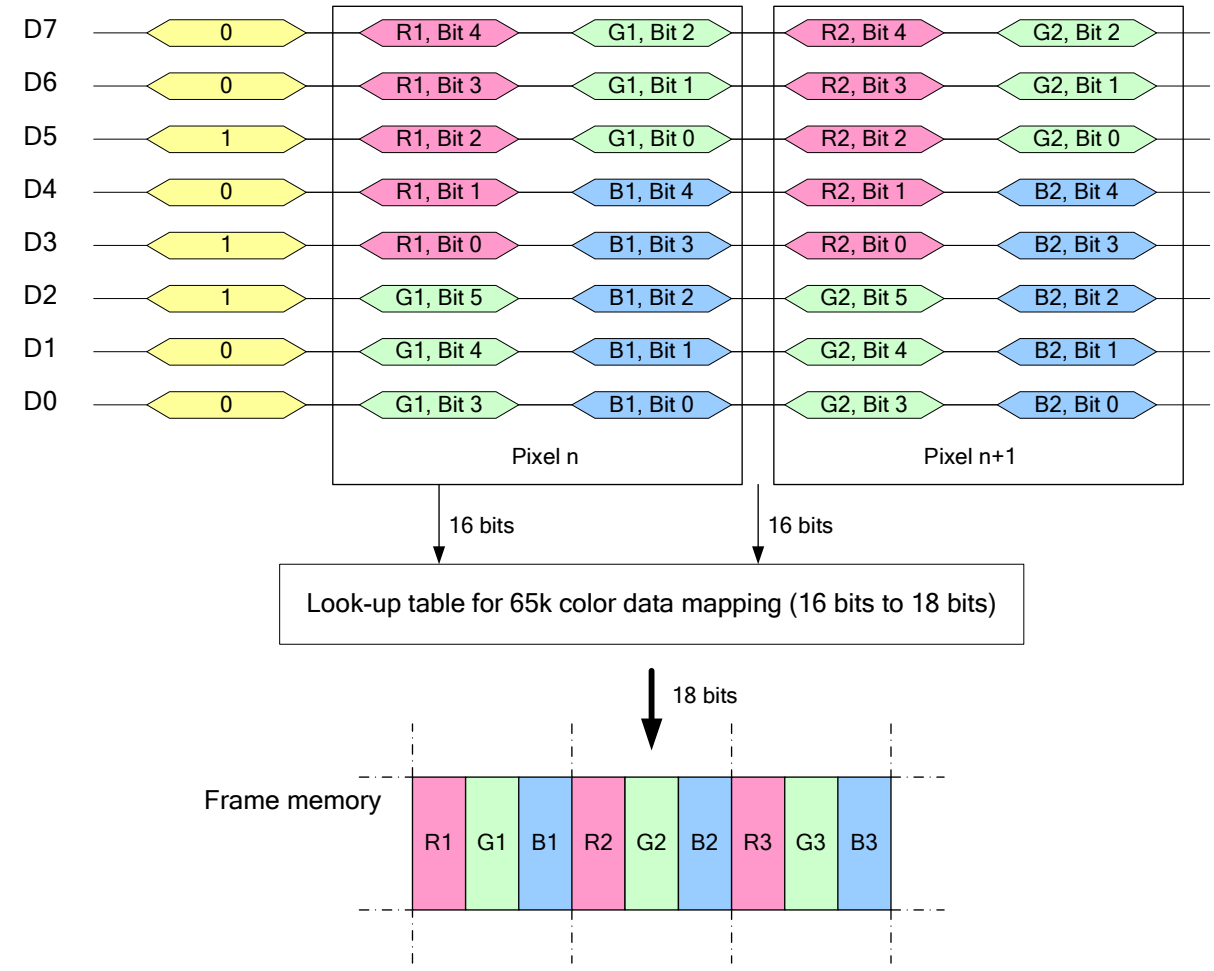
8.8.3 8-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3Ah="05h"

There is 1pixel (3 sub-pixels) per 2-byte





Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

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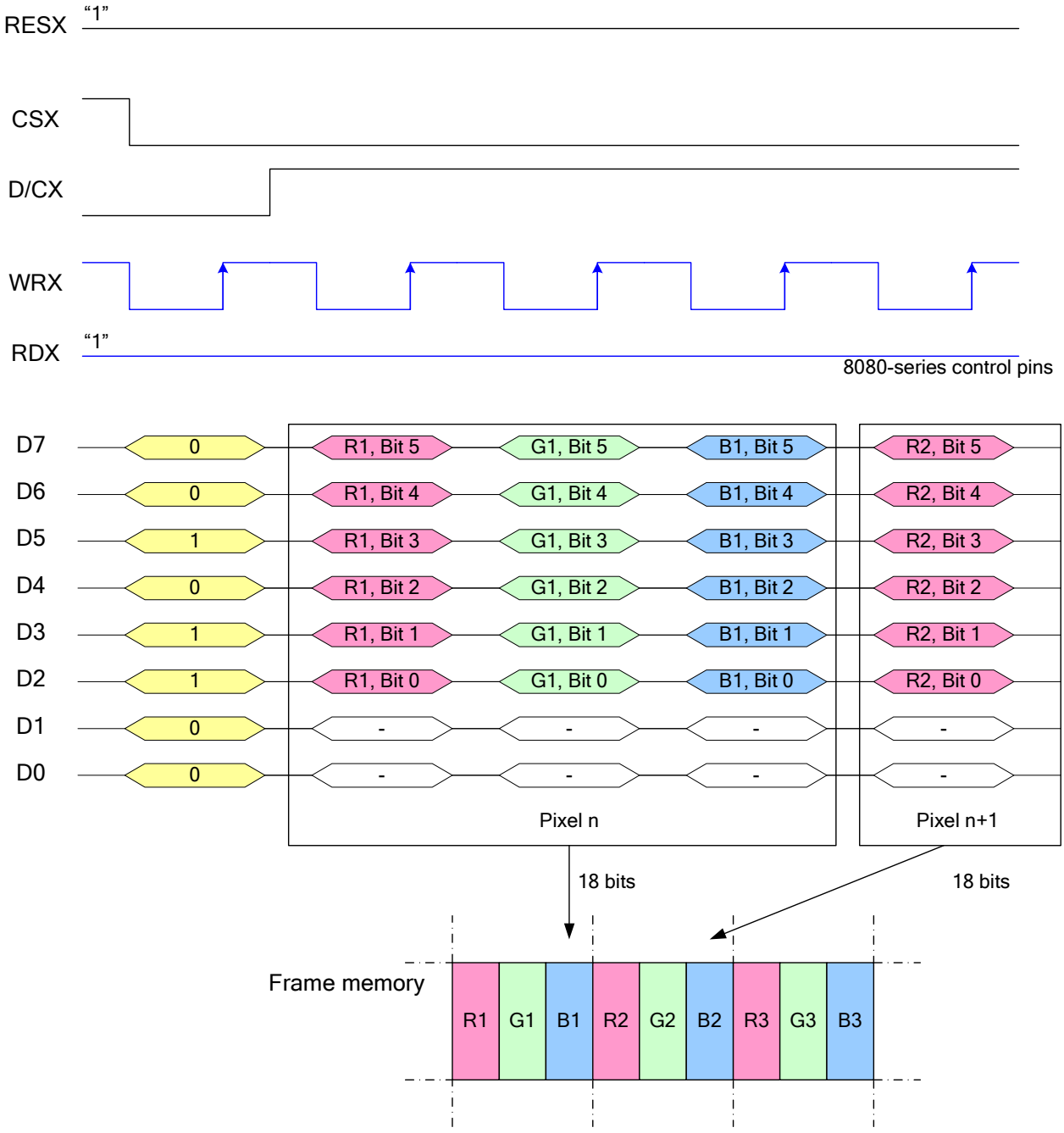
8.8.4 8-bit data bus for 18-bit/pixel (RGB-6-6-6-bit input), 262K-Colors, 3Ah="06h"

There is 1pixel (3 sub-pixels) per 3-bytes.



Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

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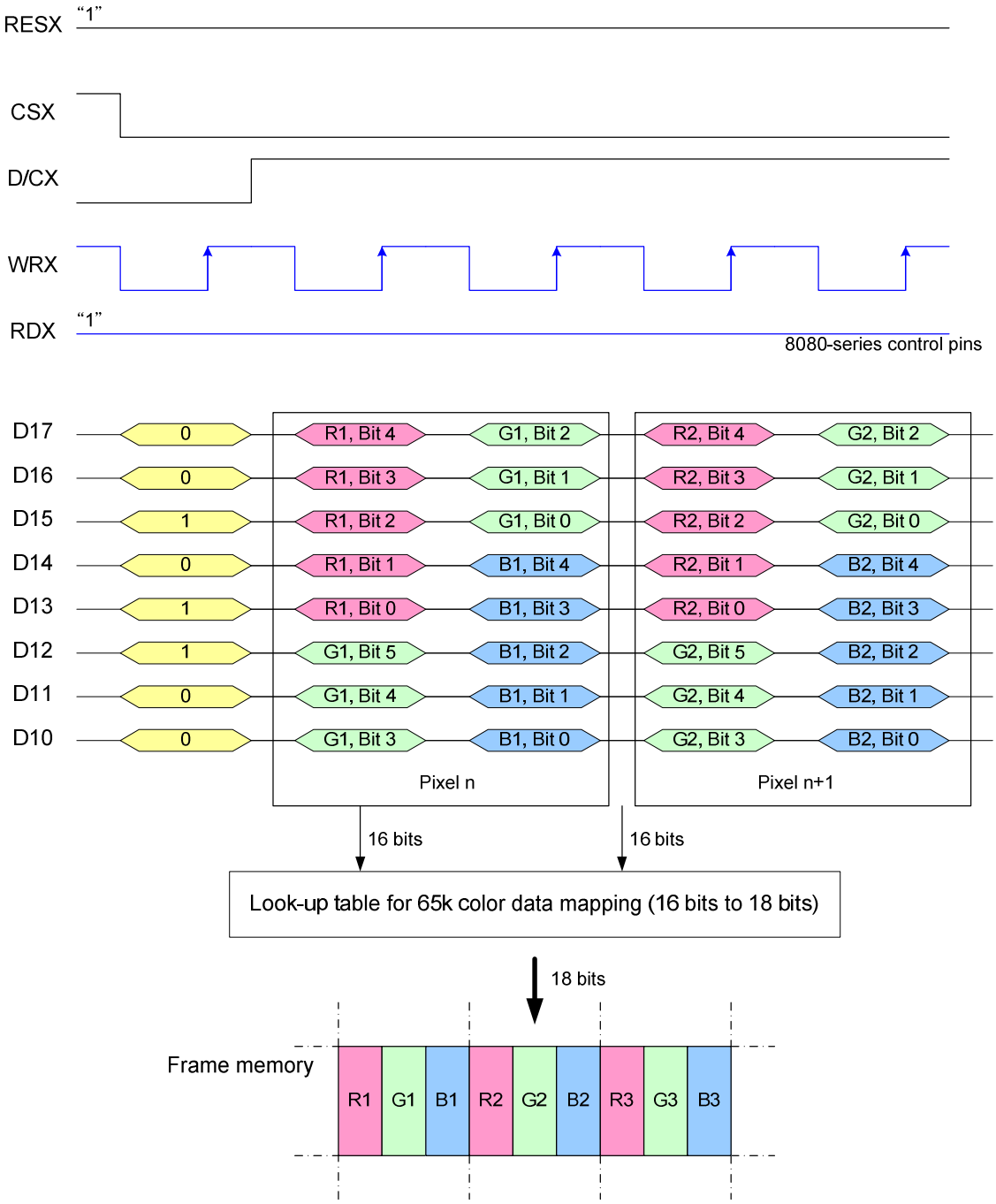
8.8.5 8080-Ⅱ series 8-bit Parallel Interface

The 8080-Ⅱ series 8-bit parallel interface of ST7789VW can be used by setting IM[3:0]="1001b". Different display data formats are available for three Colors depth supported by listed below.

- 65k colors, RGB 5,6,5-bit input.
- 262k colors, RGB 6,6,6-bit input.

8.8.6 8-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3Ah="05h"



Note 1: The data order is as follows, MSB=D17, LSB=D10 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 2-times transfer transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

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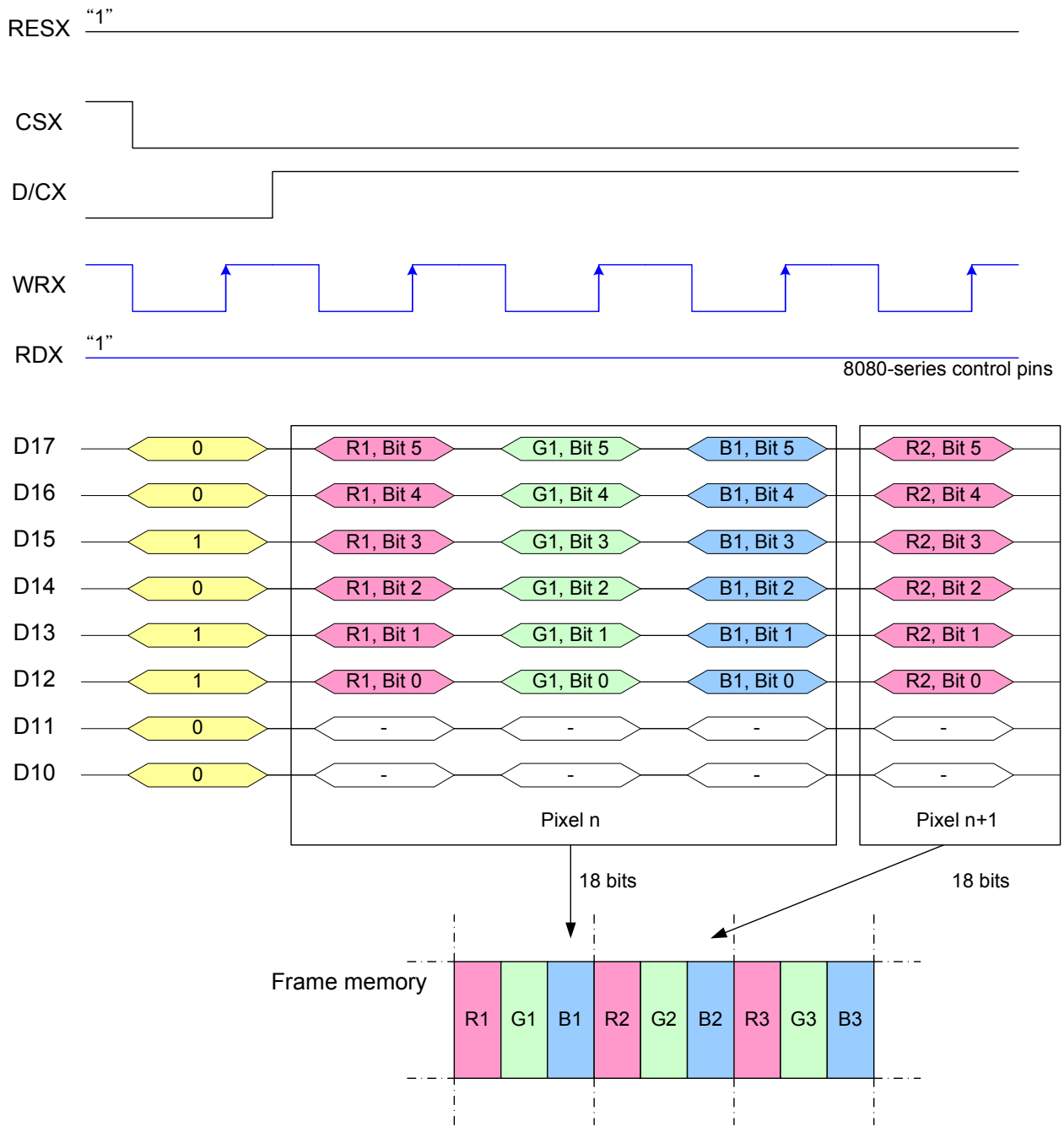
8.8.7 8-bit data bus for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3Ah="06h"



Note 1: The data order is as follows, MSB=D17, LSB=D10 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.
Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.
Note 3: '-' = Don't care – Can be set to '0' or '1'

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8.8.8 8080-Ⅰ series 16-Bit Parallel Interface

The 8080-Ⅰ series 16-bit parallel interface of ST7789VW can be used by setting IM[3:0]=”0001b”. Different display data formats are available for three colors depth supported by listed below.

- 4k colors, RGB 4,4,4-bit input
- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input

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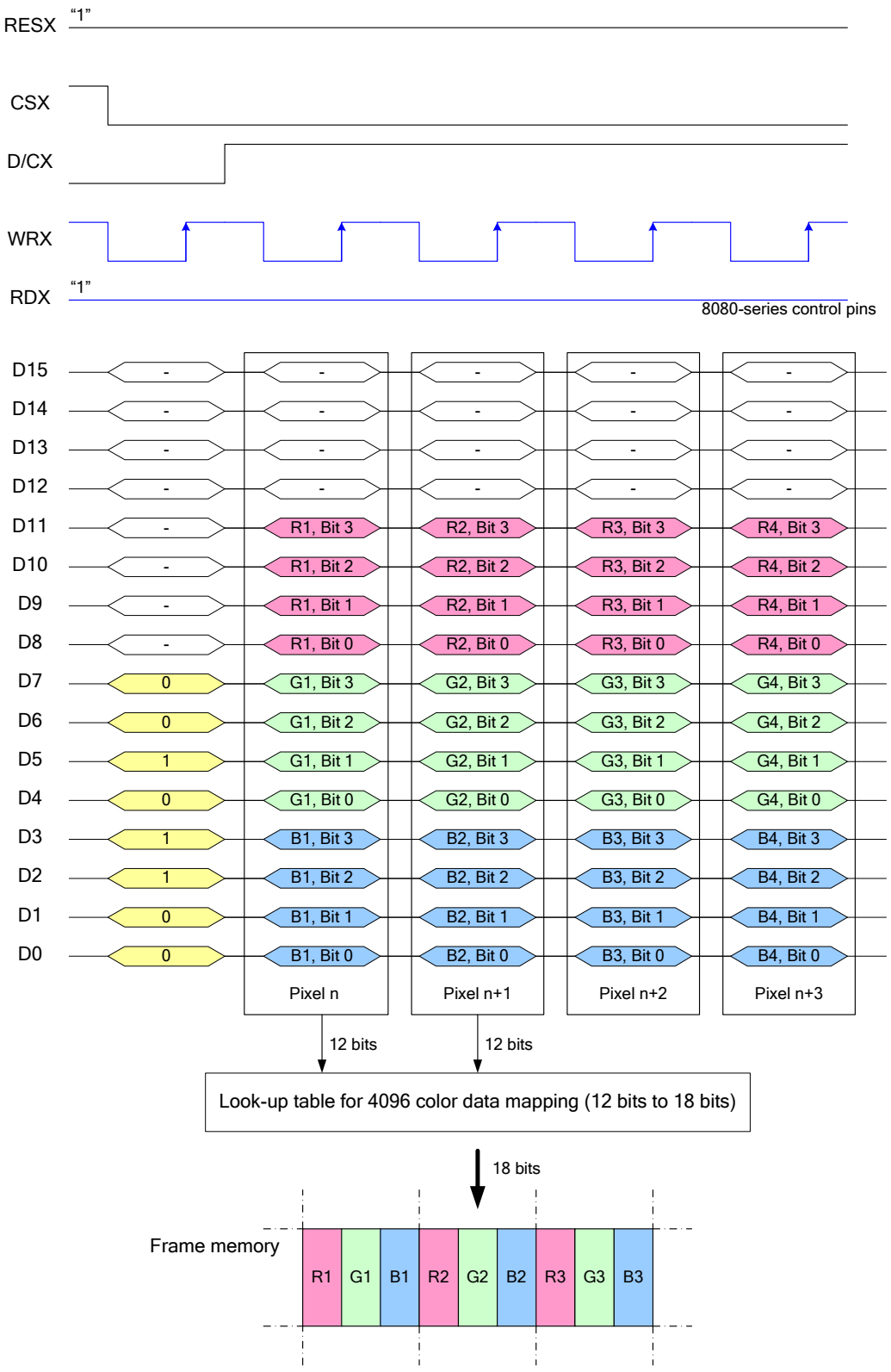
8.8.9 16-bit data bus for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3Ah="03h"

There is 1pixel (3 sub-pixels) per 1byte



Note 1: The data order is as follows, MSB=D11, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 1-times transfer (D11 to D0) is used to transmit 1 pixel data with the 12-bit color depth information.

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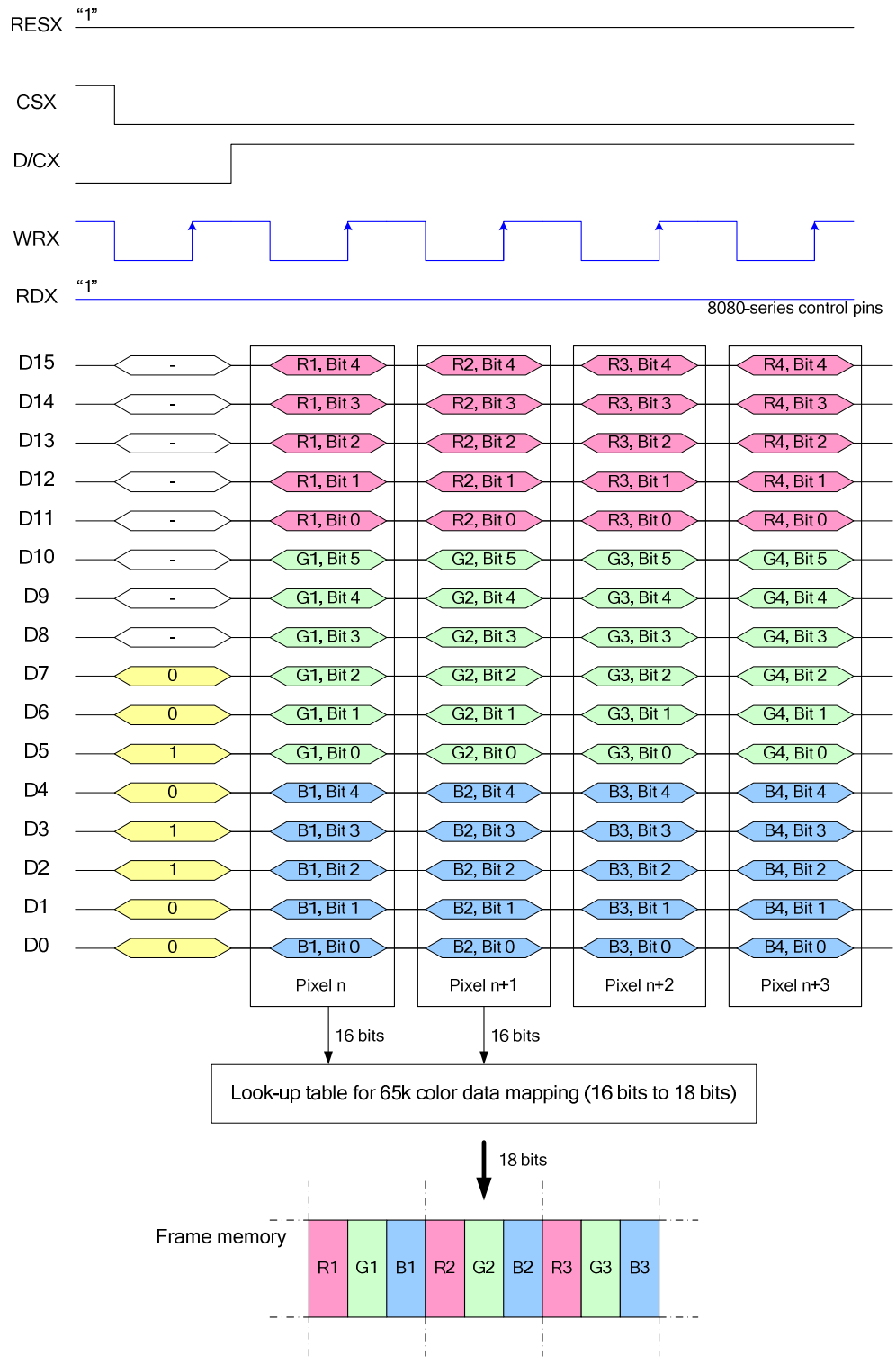
8.8.10 16-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input) 65K-Color, 3Ah="05h"

There is 1 pixel (3 sub-pixels) per 1 byte



Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-times transfer (D15 to D0) is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

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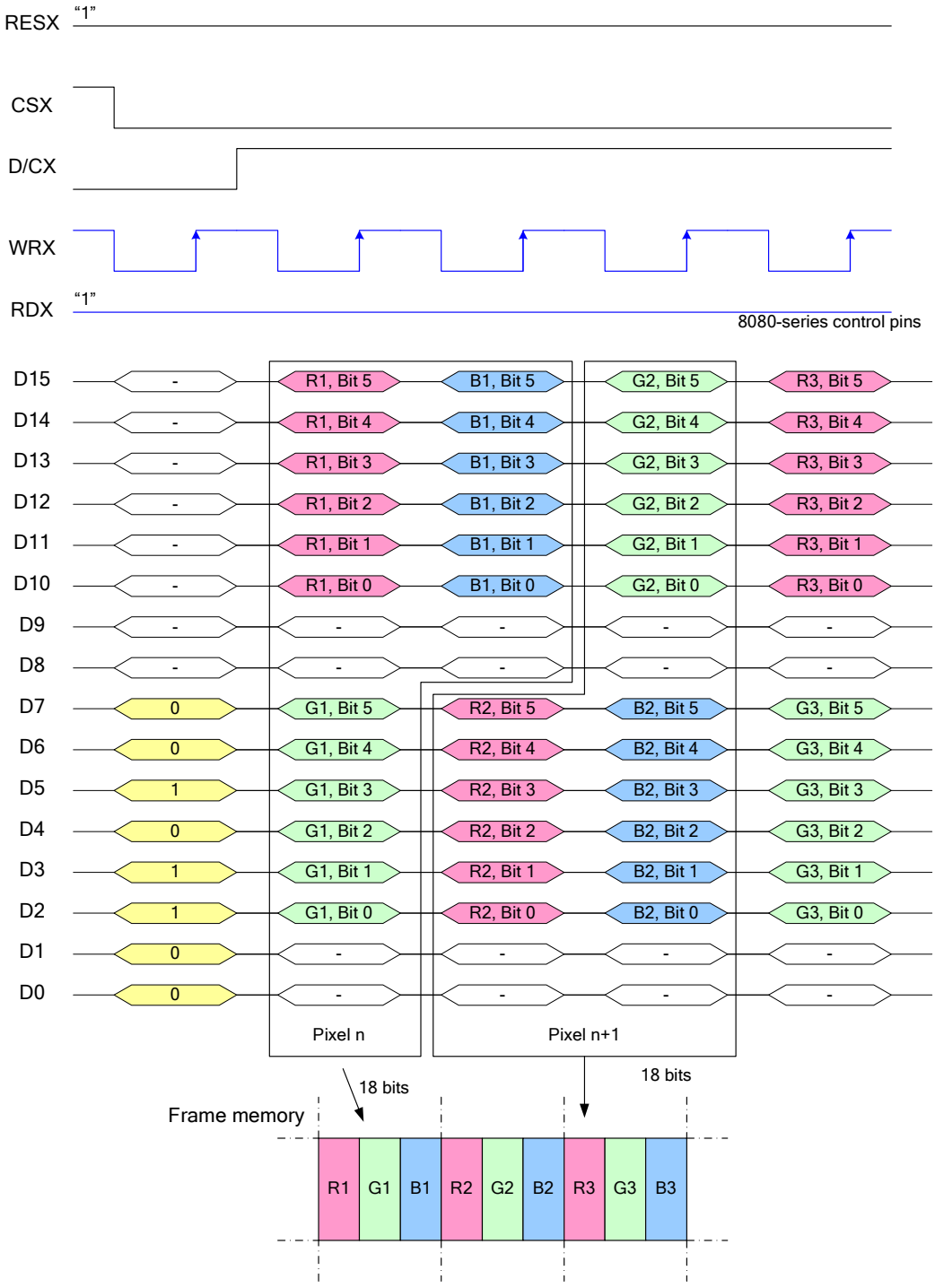
8.8.11 16-bit data bus for 18-bit/pixel (RGB-6-6-6-bit input), 262K-Colors, 3Ah="06h", MDT[1:0]="00b"

There are 2 pixels (6 sub-pixels) per 3 bytes



Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

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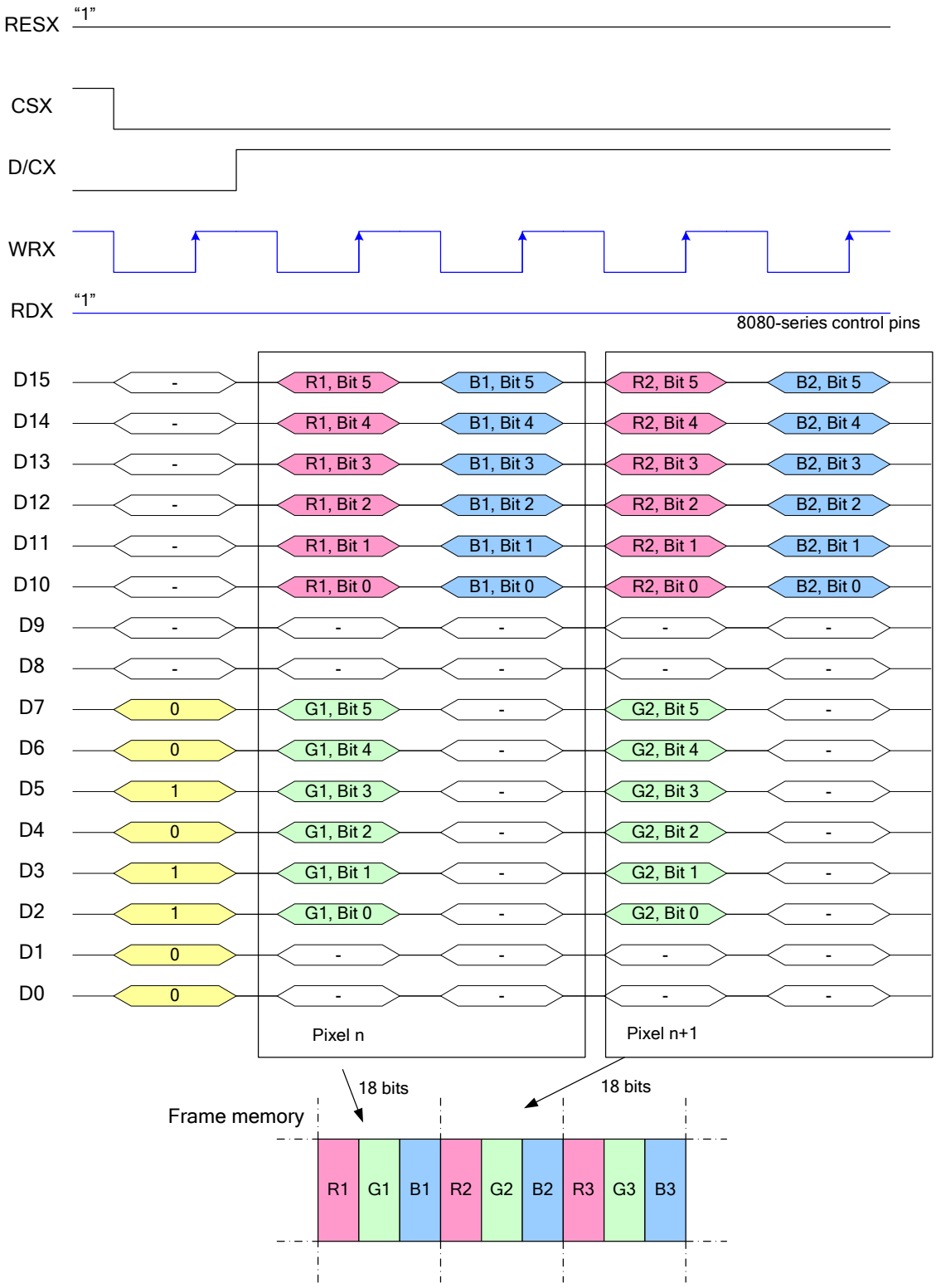
8.8.12 16-bit data bus for 18-bit/pixel (RGB-6-6-6-bit input), 262K-Colors, 3Ah="06h", MDT[1:0]="01b"



Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.
Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.
Note 3: '-' = Don't care – Can be set to '0' or '1'

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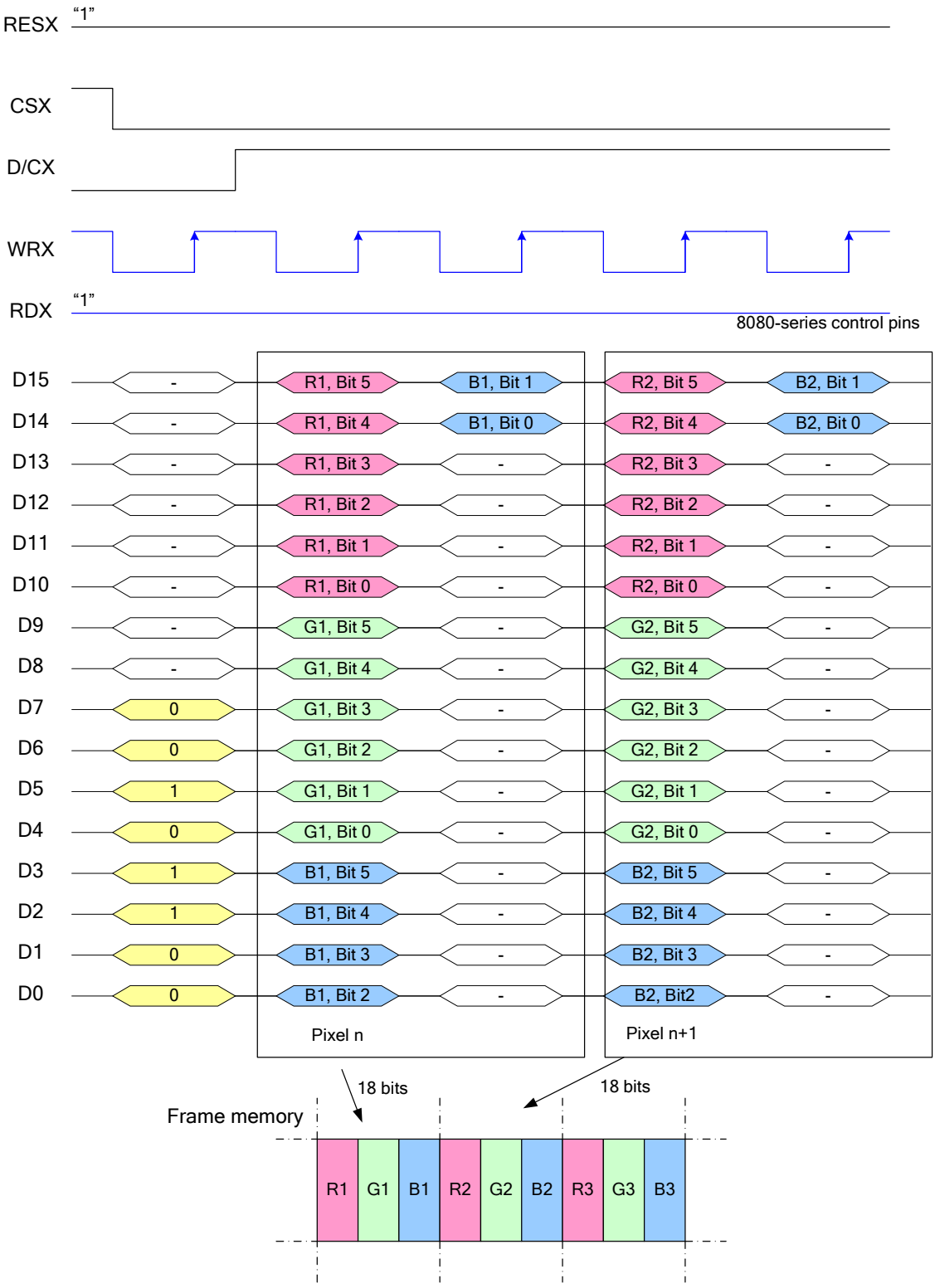
8.8.13 16-bit data bus for 18-bit/pixel (RGB-6-6-6-bit input), 262K-Colors, 3Ah="06h", MDT[1:0]="10b"



Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

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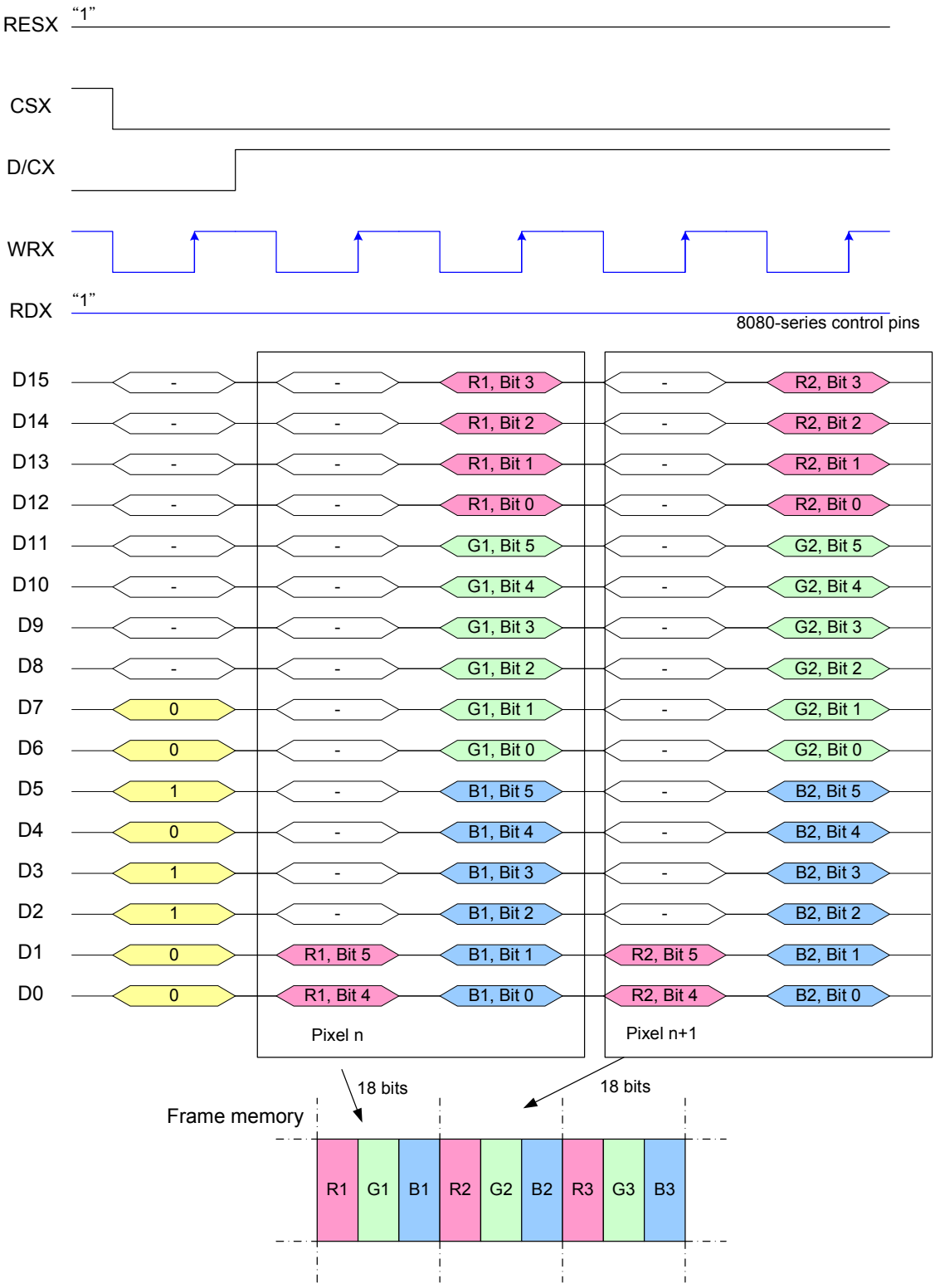
8.8.14 16-bit data bus for 18-bit/pixel (RGB-6-6-6-bit input), 262K-Colors, 3Ah="06h", MDT[1:0]="11b"



Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.
Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.
Note 3: '-' = Don't care – Can be set to '0' or '1'

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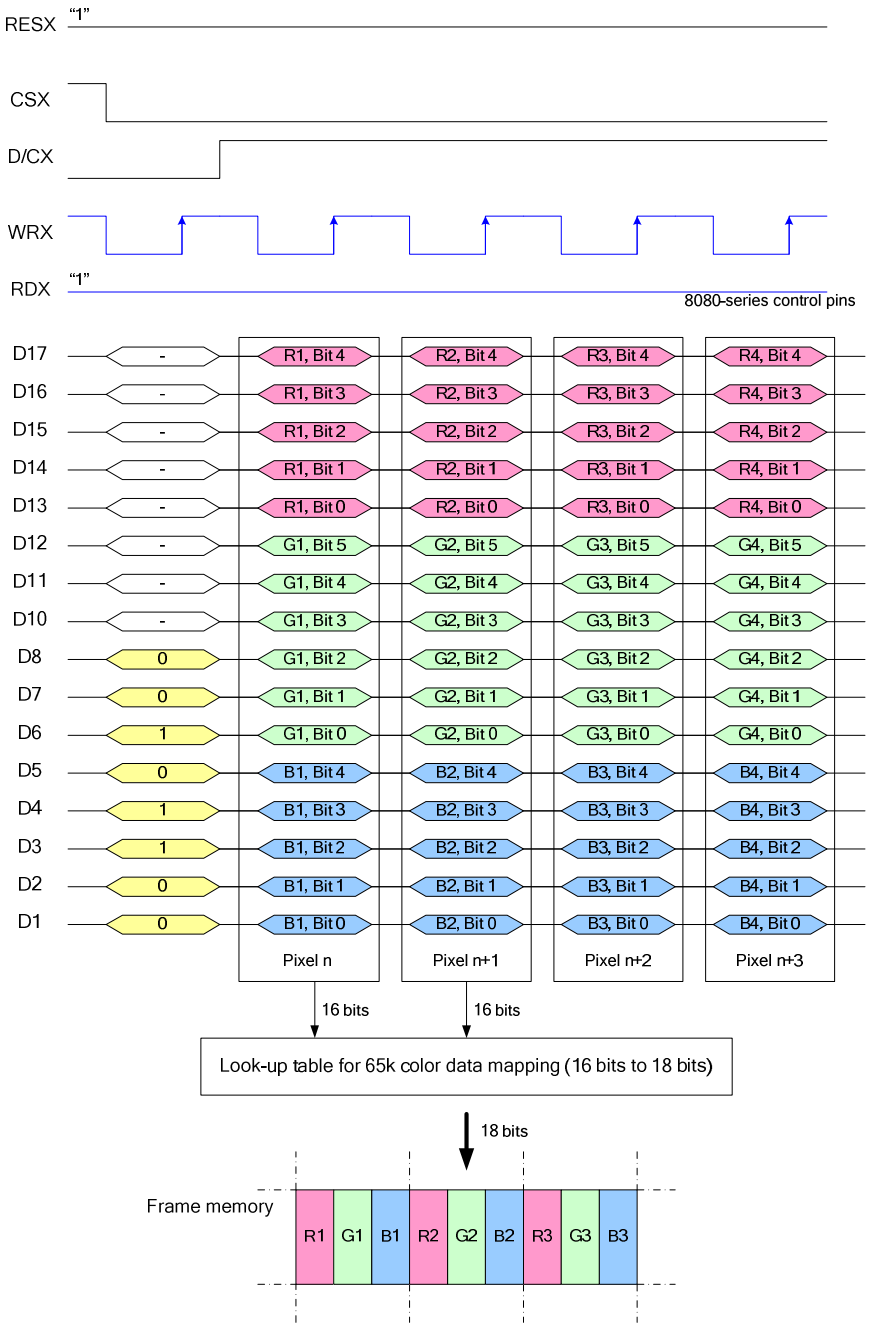
8.8.15 8080-Ⅱ series 16-Bit Parallel Interface

The 8080-Ⅱ series 16-bit parallel interface of ST7789VW can be used by setting IM[3:0]="1000b". Different display data formats are available for two colors depth supported by listed below.

- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input

8.8.16 16-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input) 65K-Color, 3Ah="05h"

There is 1 pixel (3 sub-pixels) per 1 byte



Note 1: The data order is as follows, MSB=D17, LSB=D1 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-times transfer (D17~D10, D8~D1) is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

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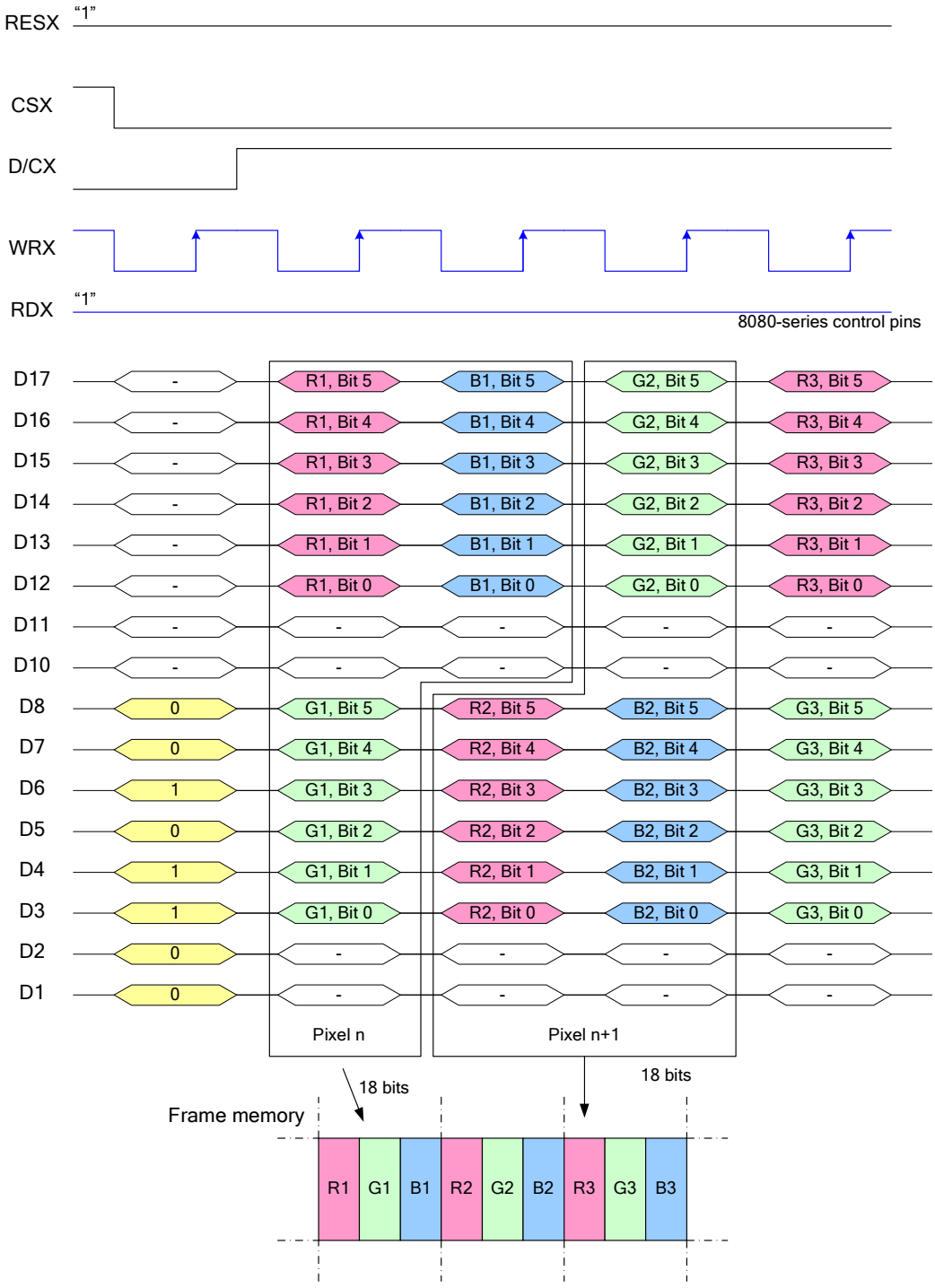
8.8.17 16-bit data bus for 18-bit/pixel (RGB-6-6-6-bit input), 262K-Colors, 3Ah="06h", MDT[1:0]="00b"

There are 2 pixels (6 sub-pixels) per 3 bytes



Note 1: The data order is as follows, MSB=D17, LSB=D1 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.
Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.
Note 3: '-' = Don't care – Can be set to '0' or '1'

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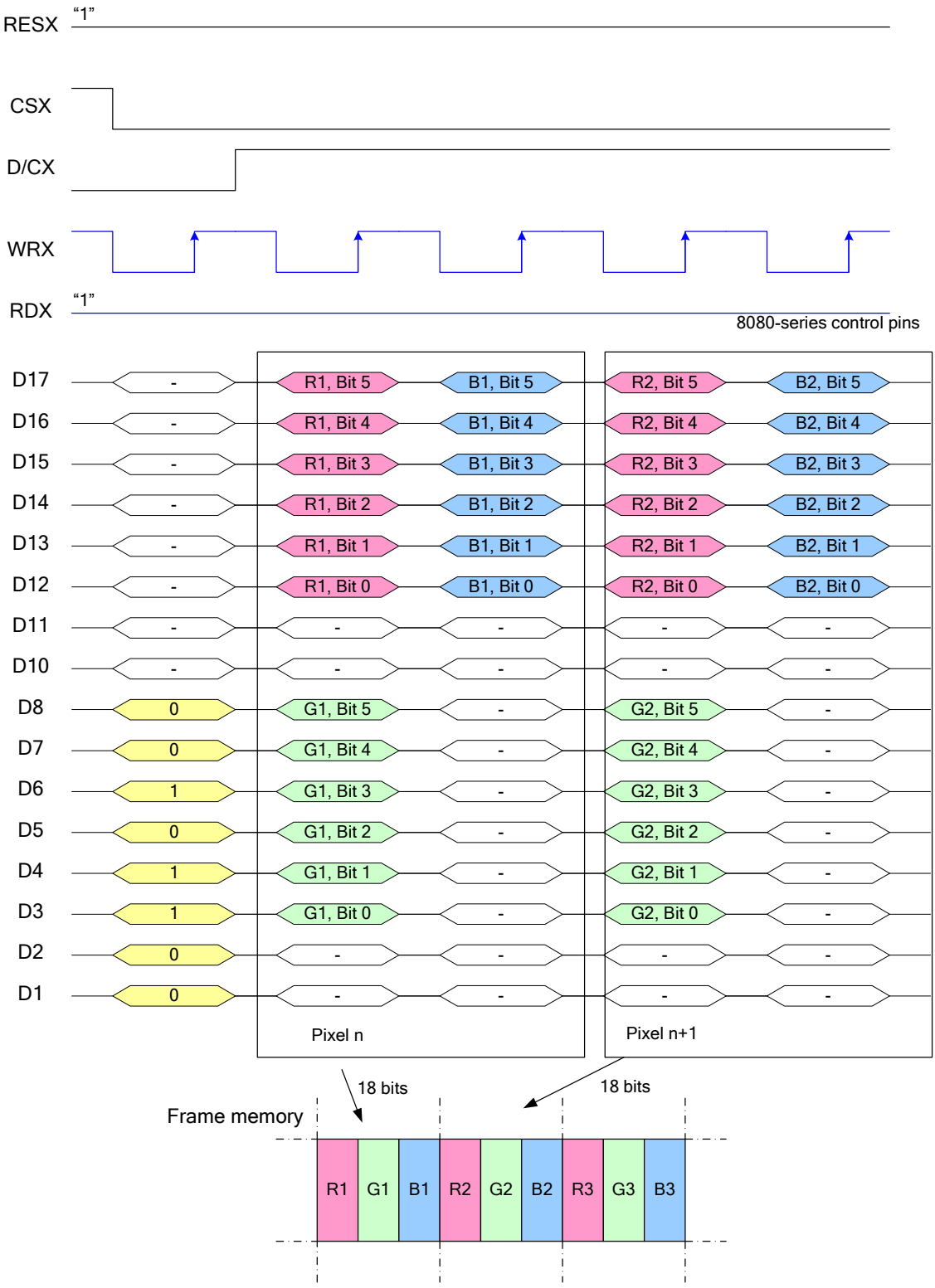
8.8.18 16-bit data bus for 18-bit/pixel (RGB-6-6-6-bit input), 262K-Colors, 3Ah="06h", MDT[1:0]="01b"



Note 1: The data order is as follows, MSB=D17, LSB=D1 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

8.8.19 16-bit data bus for 18-bit/pixel (RGB-6-6-6-bit input), 262K-Colors, 3Ah="06h",

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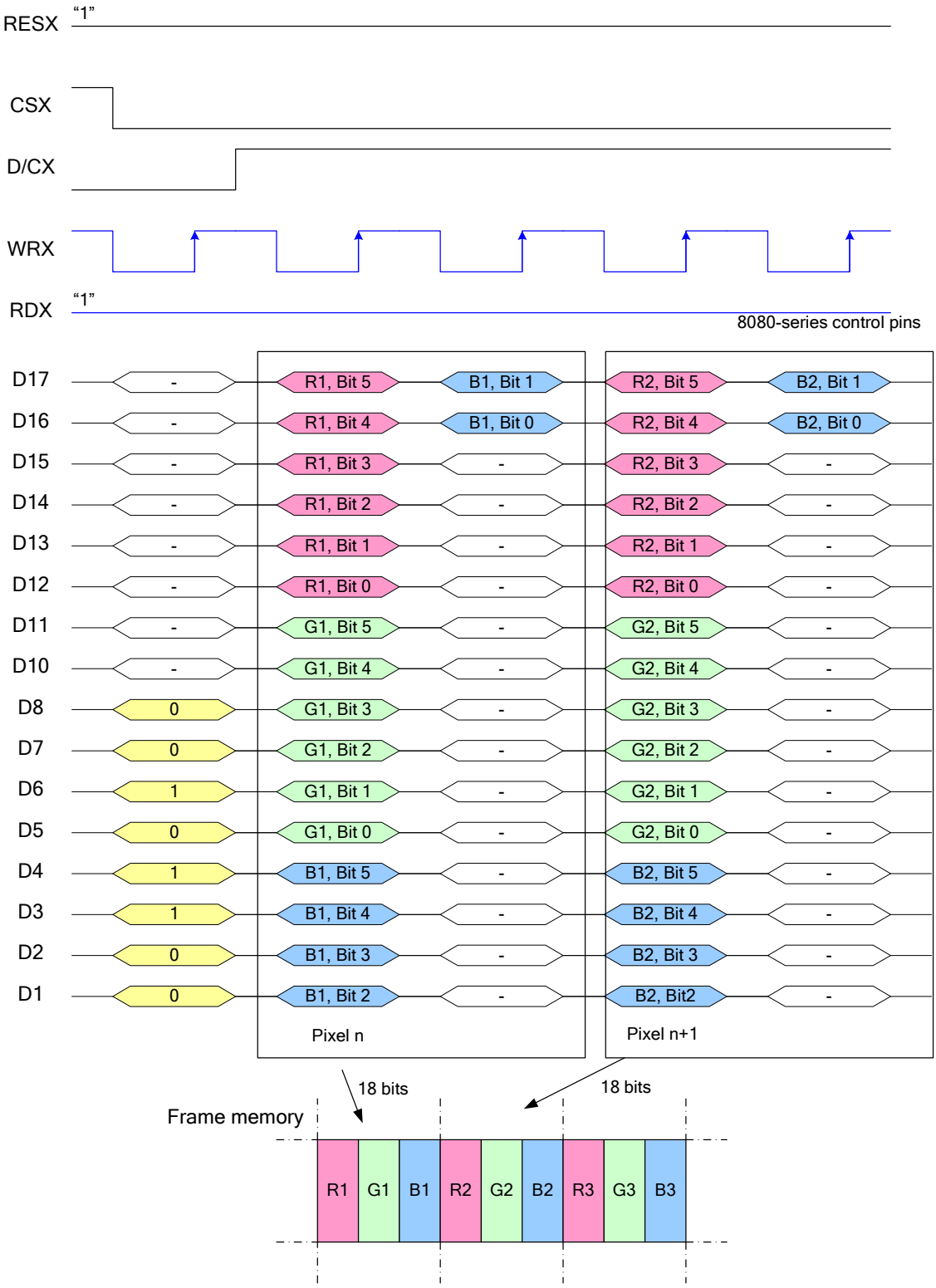
MDT[1:0]="10b"



Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

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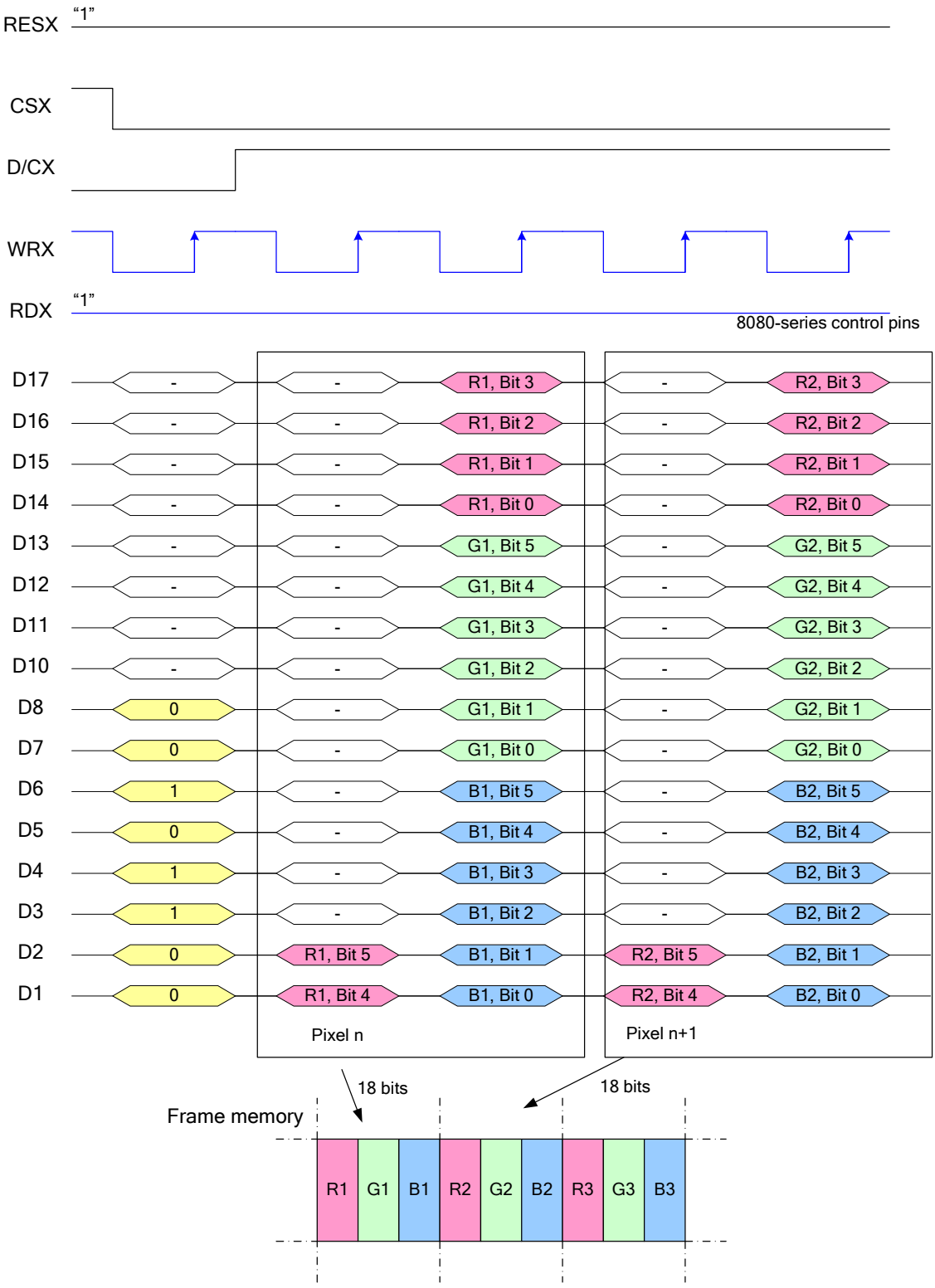
8.8.20 16-bit data bus for 18-bit/pixel (RGB-6-6-6-bit input), 262K-Colors, 3Ah="06h", MDT[1:0]="11b"



Note 1: The data order is as follows, MSB=D17, LSB=D1 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.
Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.
Note 3: '-' = Don't care – Can be set to '0' or '1'

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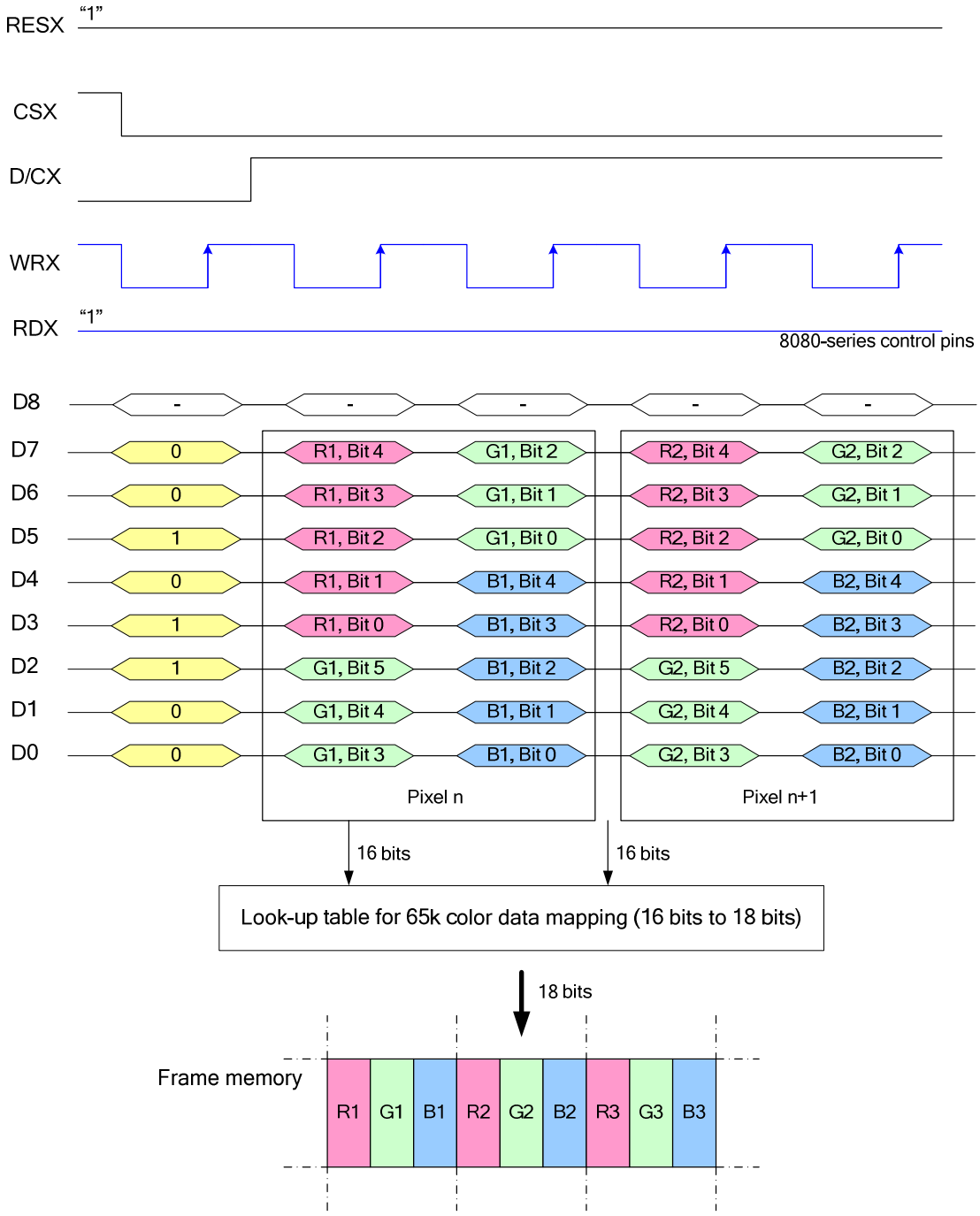
8.8.21 8080- Ⅰ series 9-Bit Parallel Interface

The 8080- Ⅰ series 9-bit parallel interface of ST7789VW can be used by setting IM[3:0]=”0010b”Different display data formats are available for two colors depth supported by listed below.

-65k colors, RGB 5,6,5-bit input

-262k colors, RGB 6,6,6-bit input

8.8.22 Write 9-bit data for RGB 5-6-5-bit input (65K-Color), 3Ah=”05h”



Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 4, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

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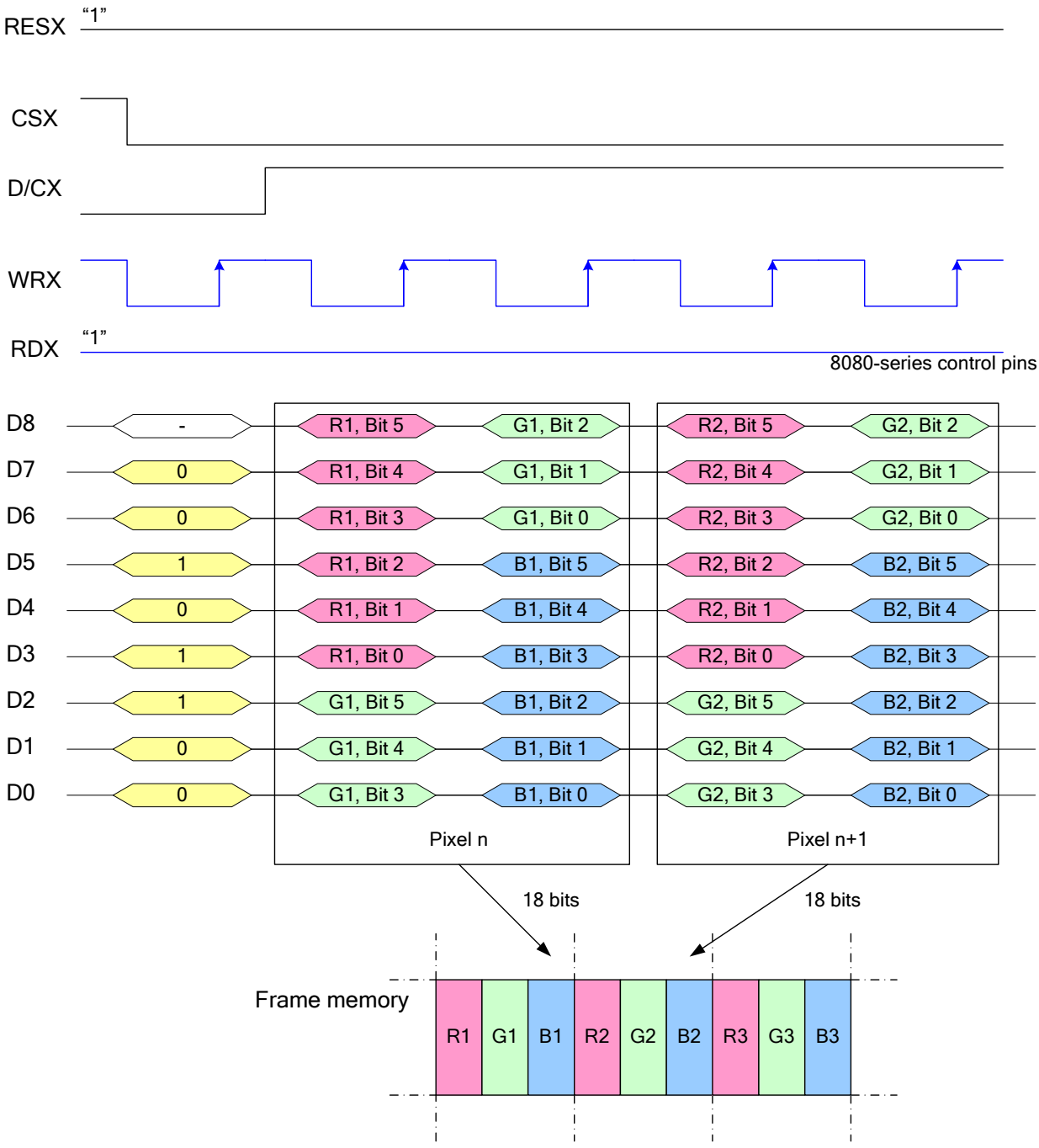
8.8.23 Write 9-bit data for RGB 6-6-6-bit input (262K-Color), 3Ah="06h", MDT[1:0]="00b"

There is 1 pixel (3 sub-pixels) per 2bytes



Note 1: The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-time transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

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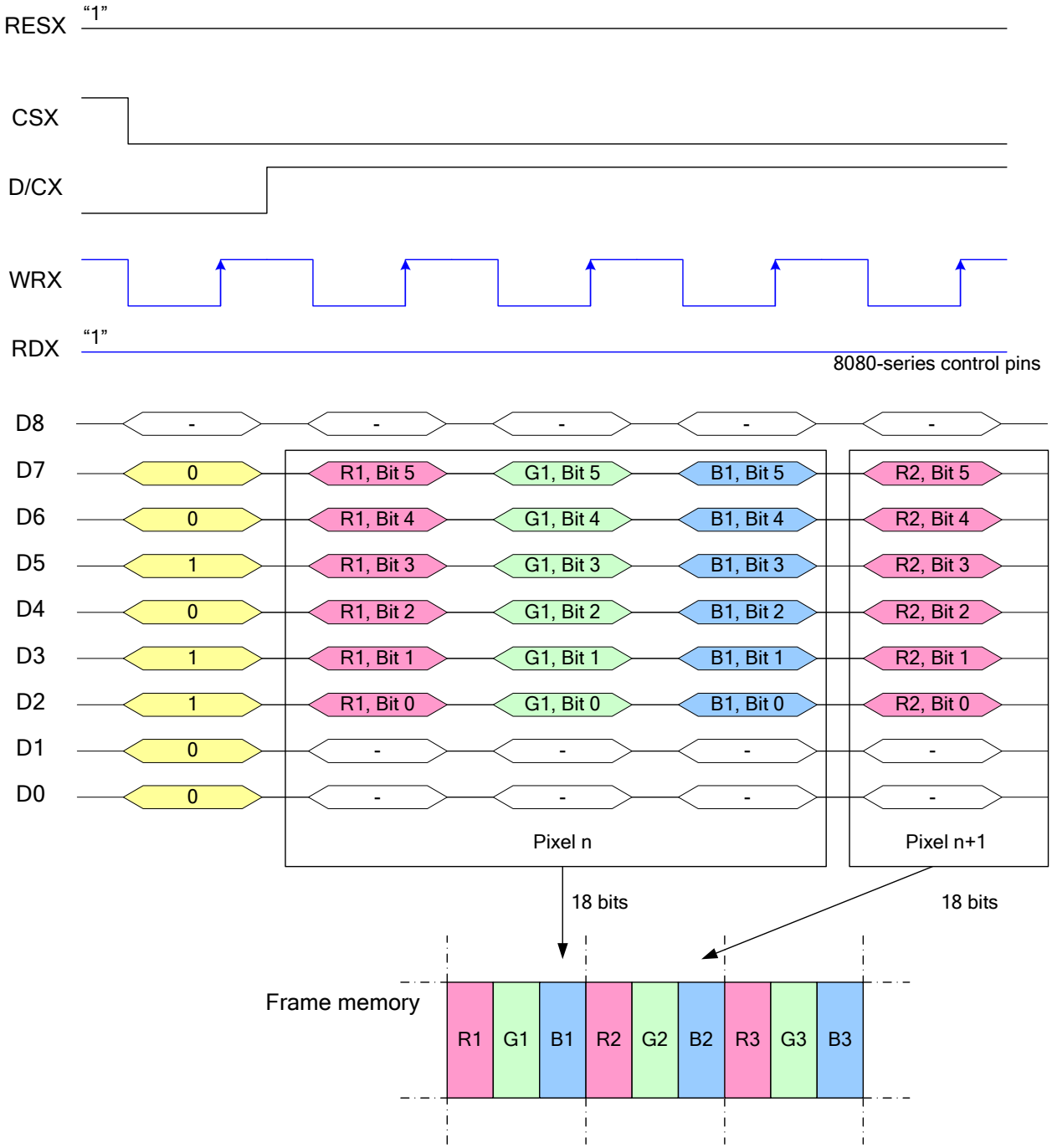
8.8.24 Write 9-bit data for RGB 6-6-6-bit input (262K-Color), 3Ah="06h", MDT[1:0]="01b"



Note 1: The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-time transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

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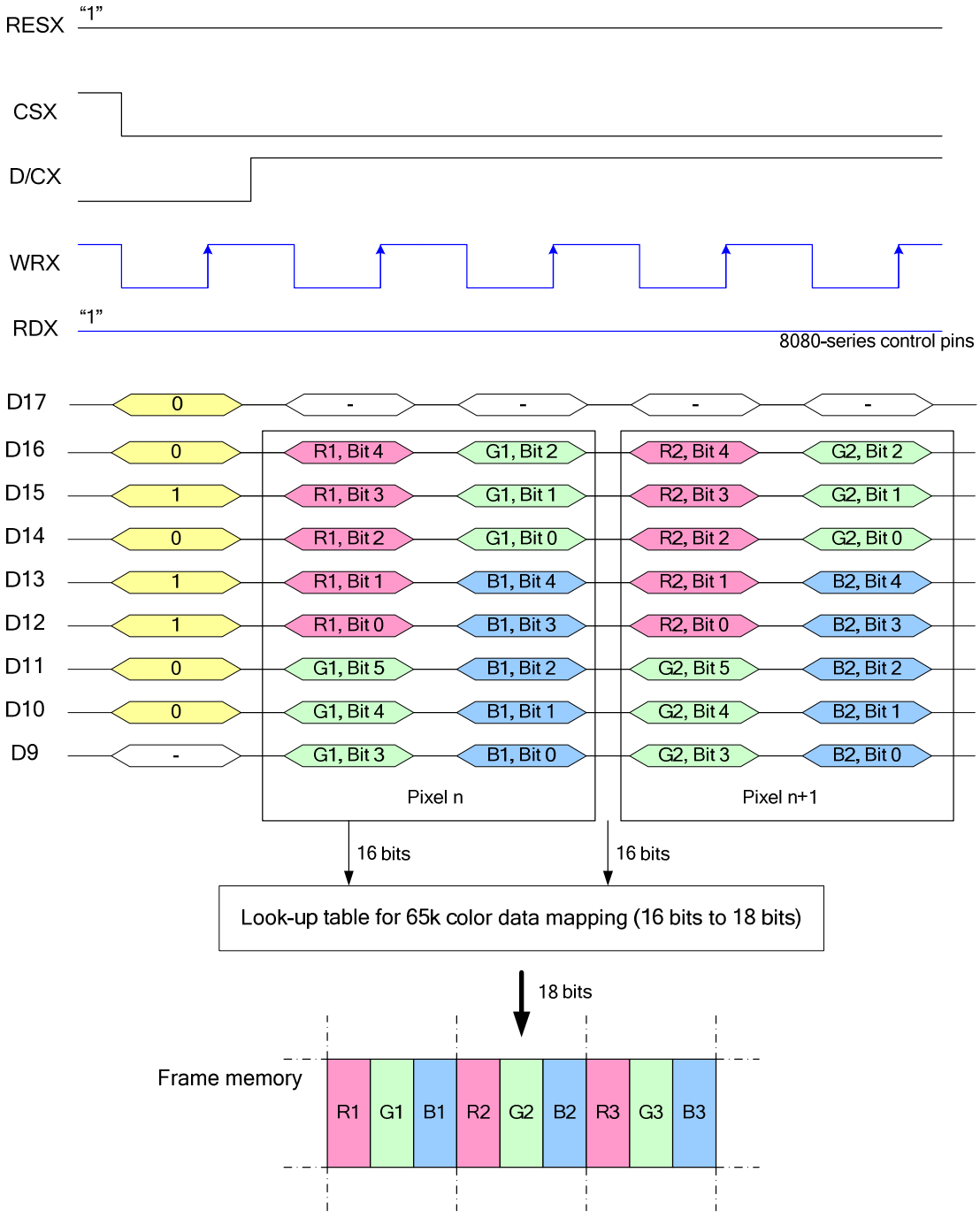
8.8.25 8080-Ⅱ series 9-bit Parallel Interface

The 8080-Ⅱ series 9-bit parallel interface of ST7789VW can be used by setting IM[3:0]=”1011b”Different display data formats are available for two colors depth supported by listed below.

-65k colors, RGB 5,6,5-bit input

-262k colors, RGB 6,6,6-bit input

8.8.26 Write 9-bit data for RGB 5-6-5-bit input (65K-Color), 3Ah=”05h”



Note 1: The data order is as follows, MSB=D16, LSB=D9 and picture data is MSB=Bit 4, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

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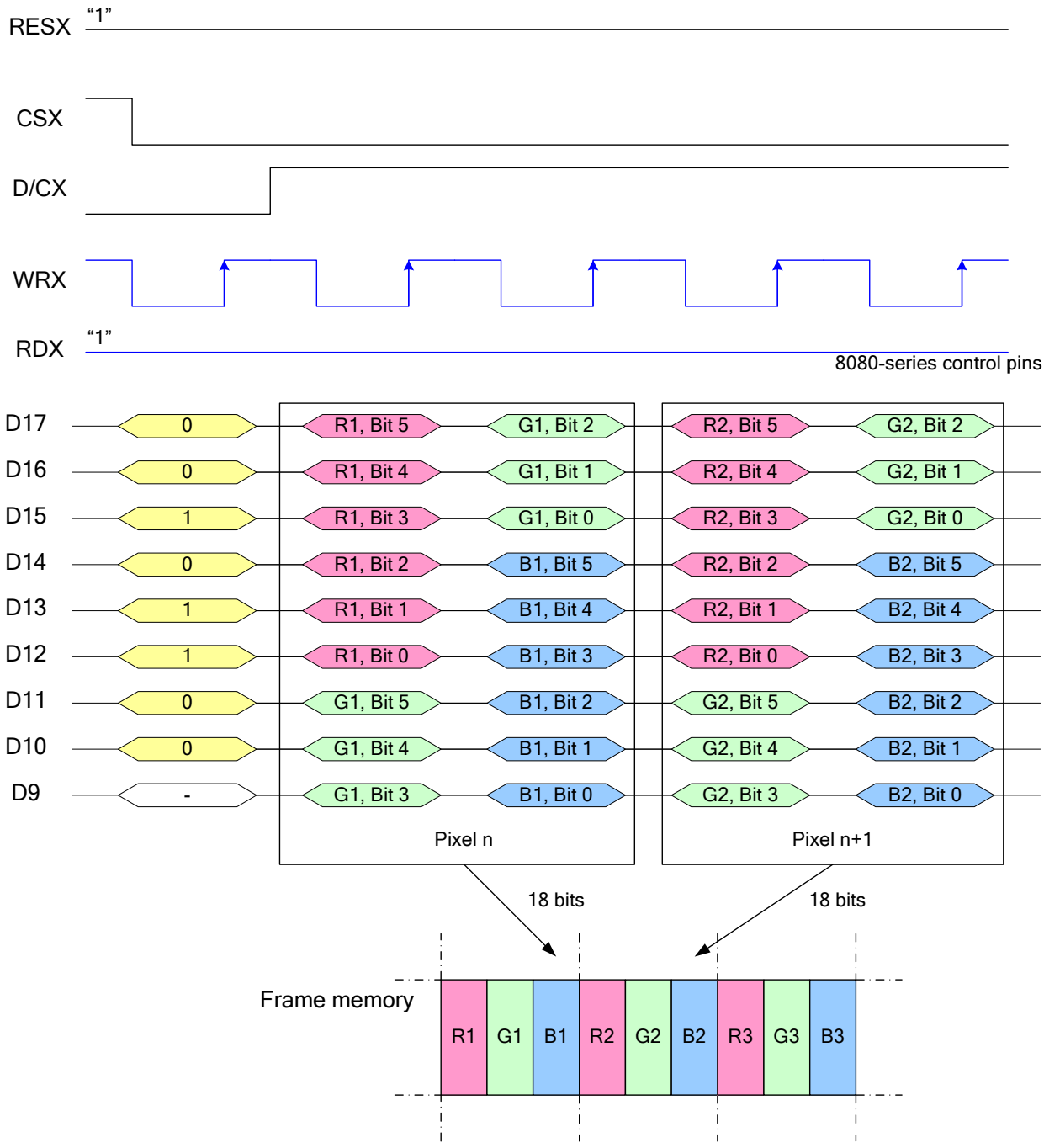
8.8.27 Write 9-bit data for RGB 6-6-6-bit input (262K-Color), 3Ah="06h", MDT[1:0]="00b"

There is 1 pixel (3 sub-pixels) per 2bytes



Note 1: The data order is as follows, MSB=D17, LSB=D9 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-time transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

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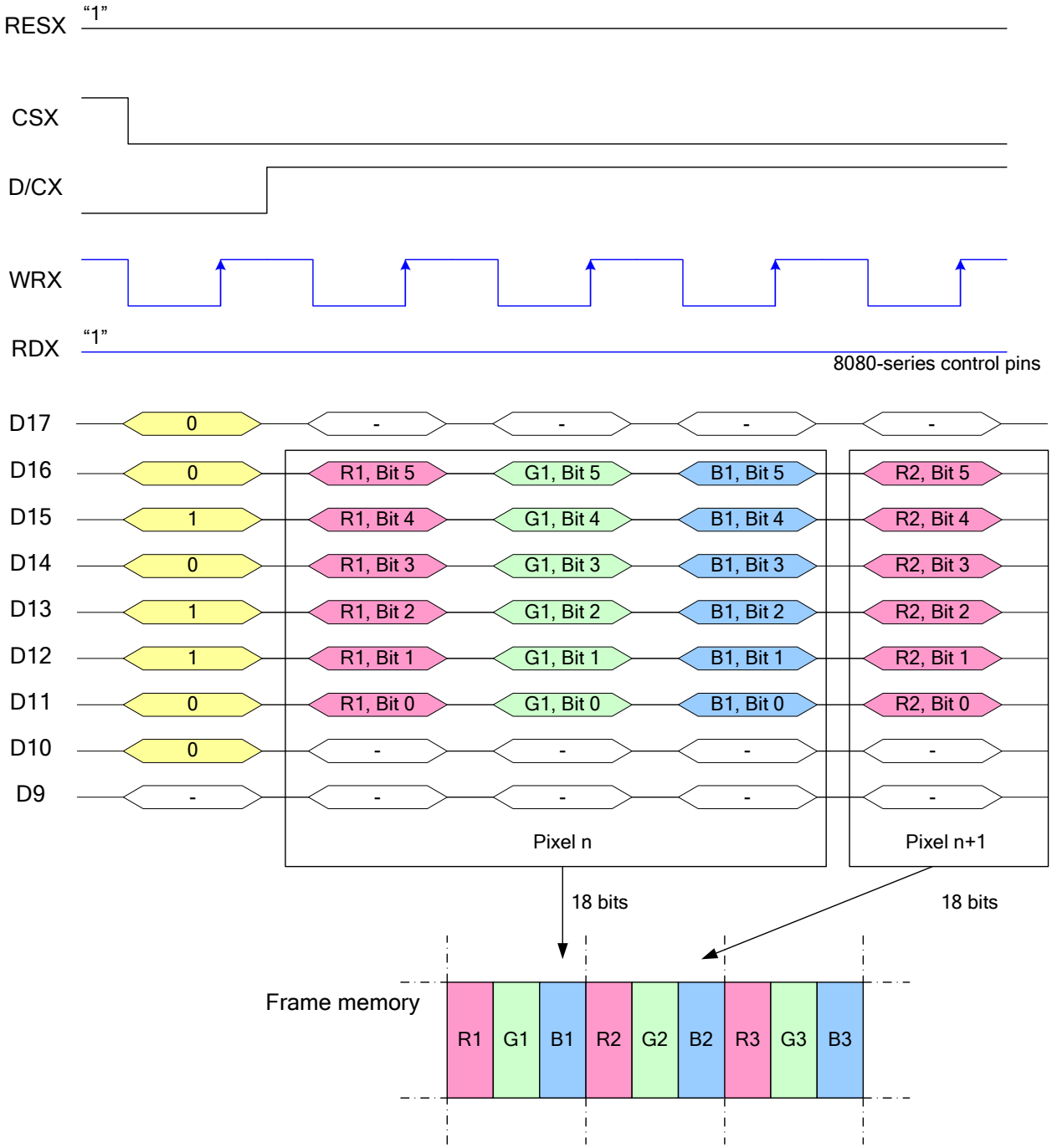
8.8.28 Write 9-bit data for RGB 6-6-6-bit input (262K-Color), 3Ah="06h", MDT[1:0]="01b"



Note 1: The data order is as follows, MSB=D16, LSB=D11 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-time transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

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8.8.29 8080- Ⅰ series 18-Bit Parallel Interface

The 8080- Ⅰ series 18-bit parallel interface of ST7789VW can be used by setting IM[3:0]="0011b". Different display data formats are available for three colors depth supported by listed below.

- 4k colors, RGB 4,4,4-bit input
- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input.

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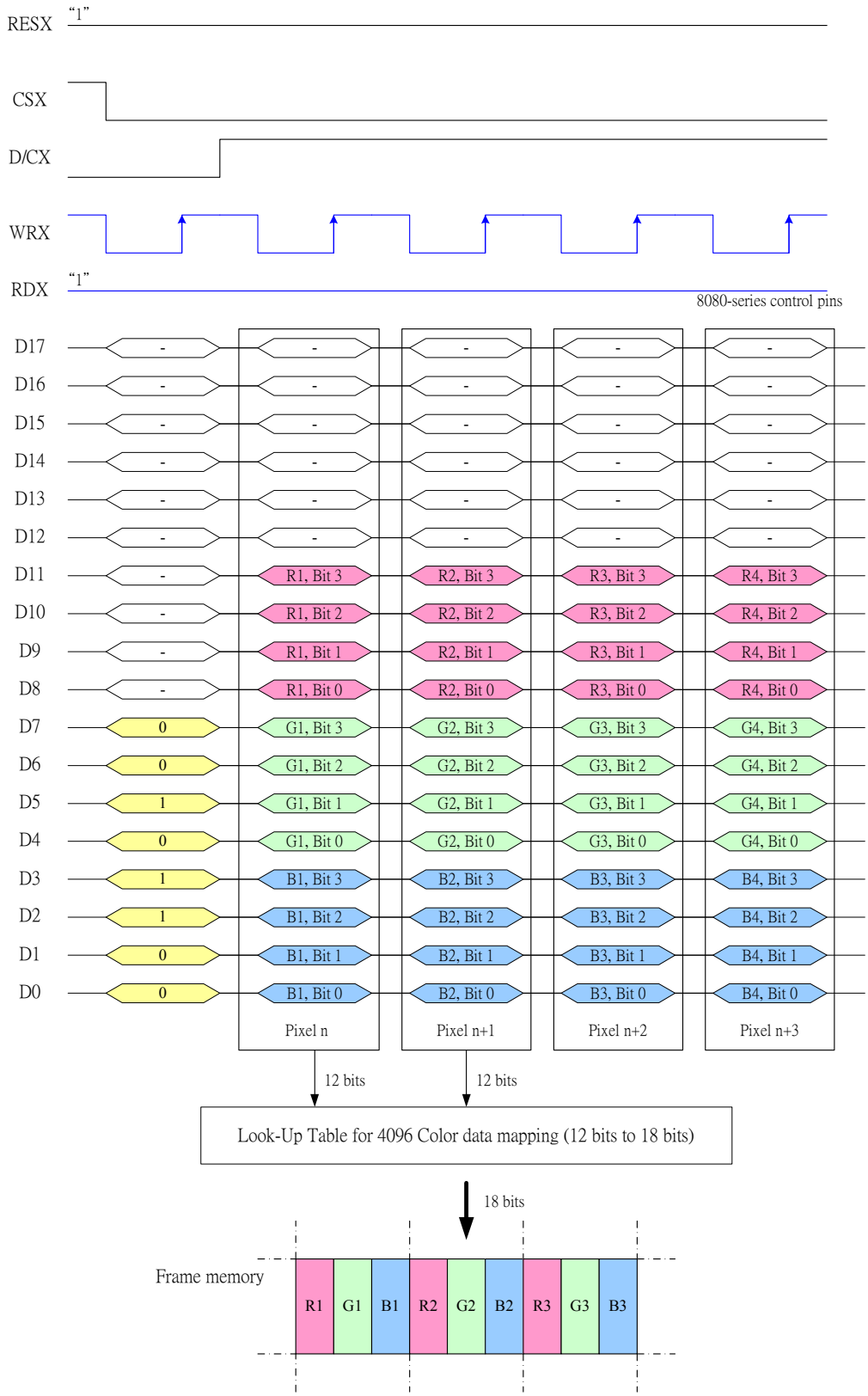
8.8.30 18-bit data bus for 12-bit/pixel (RGB-4-4-4-bit input), 4K-colors, 3Ah="03h"

There is 1 pixel (3 sub-pixels) per byte



Note 1: The data order is as follows, MSB=D11, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 1-times transfer is used to transmit 1 pixel data with the 12-bit color depth information.

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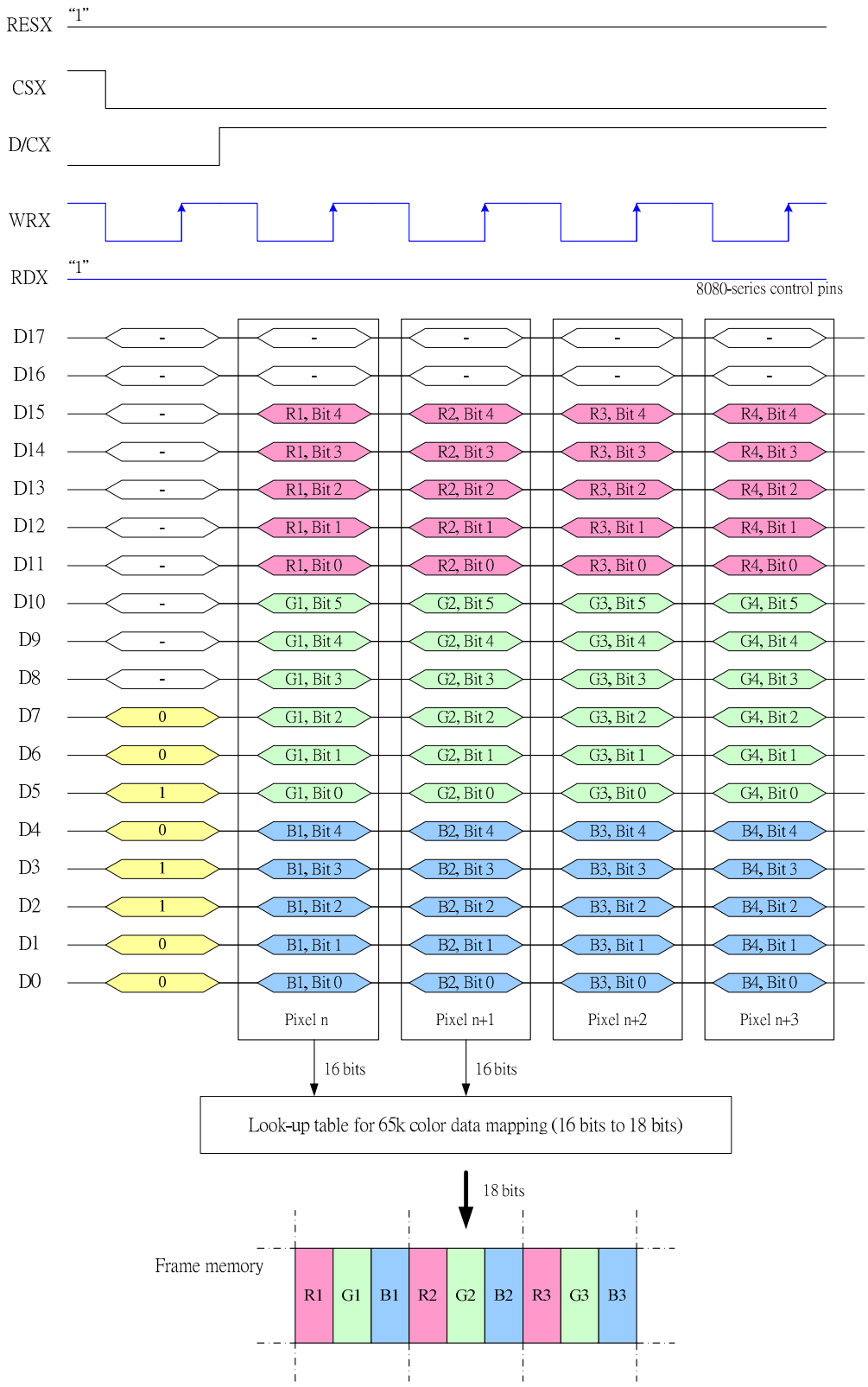
8.8.31 18-bit data bus for 16-bit/pixel (RGB-5-6-5-bit input), 65K-colors, 3Ah="05h"

There is one pixel (3 sub-pixels) per byte



Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

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Note 2: 1-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

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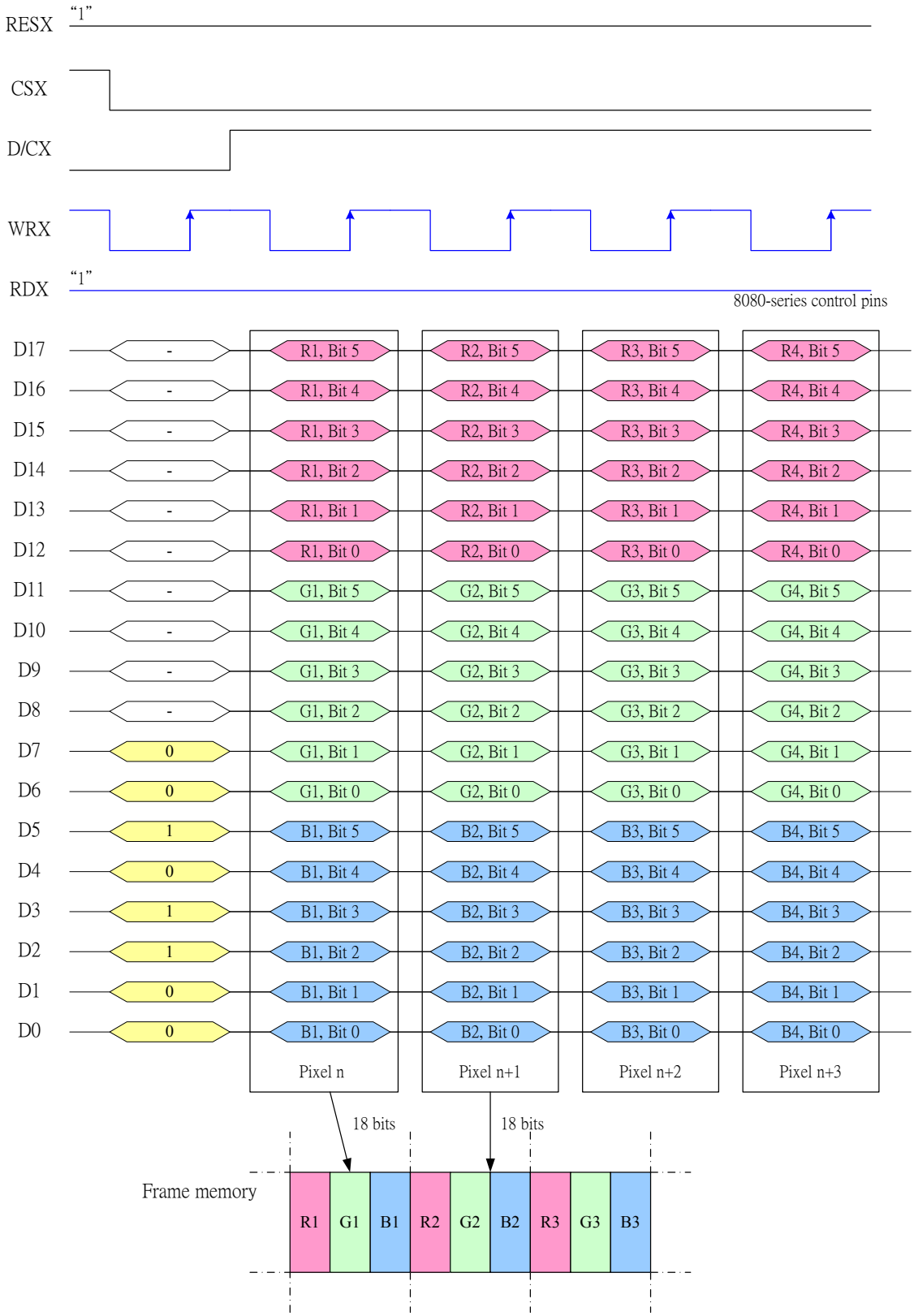
8.8.32 18-bit data bus for 18-bit/pixel (RGB-6-6-6-bit input), 262K-colors, 3Ah="06h"

There is 1 pixel (3 sub-pixels) per byte



Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Read, Green and Blue data.

Note 2: 1-times transfer (D17o D0) is used to transmit 1 pixel data with the 18-bit color depth information.

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8.8.33 8080-Ⅱ series 18-Bit Parallel Interface

The 8080-Ⅱ series 18-bit parallel interface of ST7789VW can be used by setting IM[3:0]=”1010b”. Different display data formats are available for two colors depth supported by listed below.

- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input.

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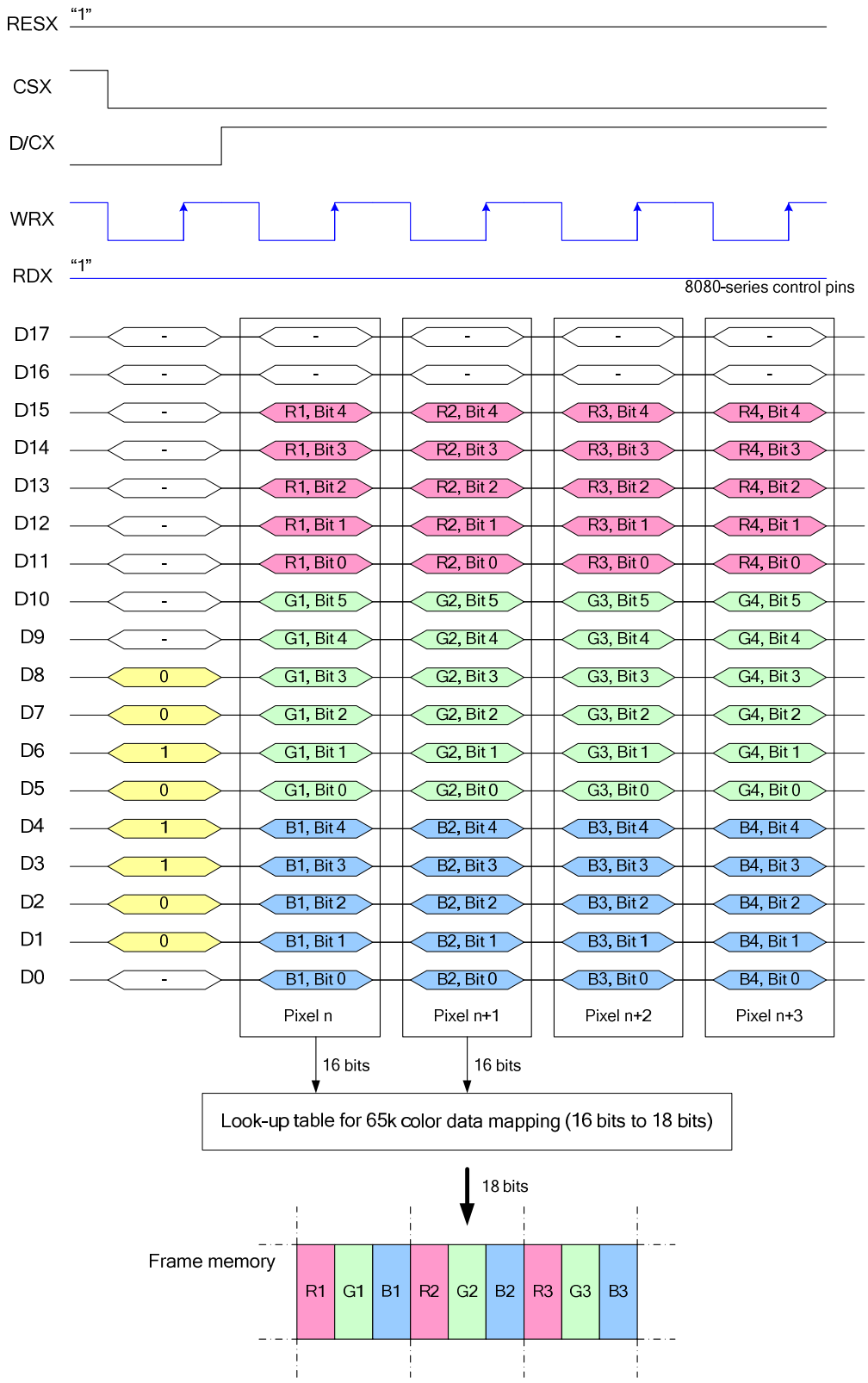
8.8.34 18-bit data bus for 16-bit/pixel (RGB-5-6-5-bit input), 65K-colors, 3Ah="05h"

There is one pixel (3 sub-pixels) per byte



Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

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Note 2: 1-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

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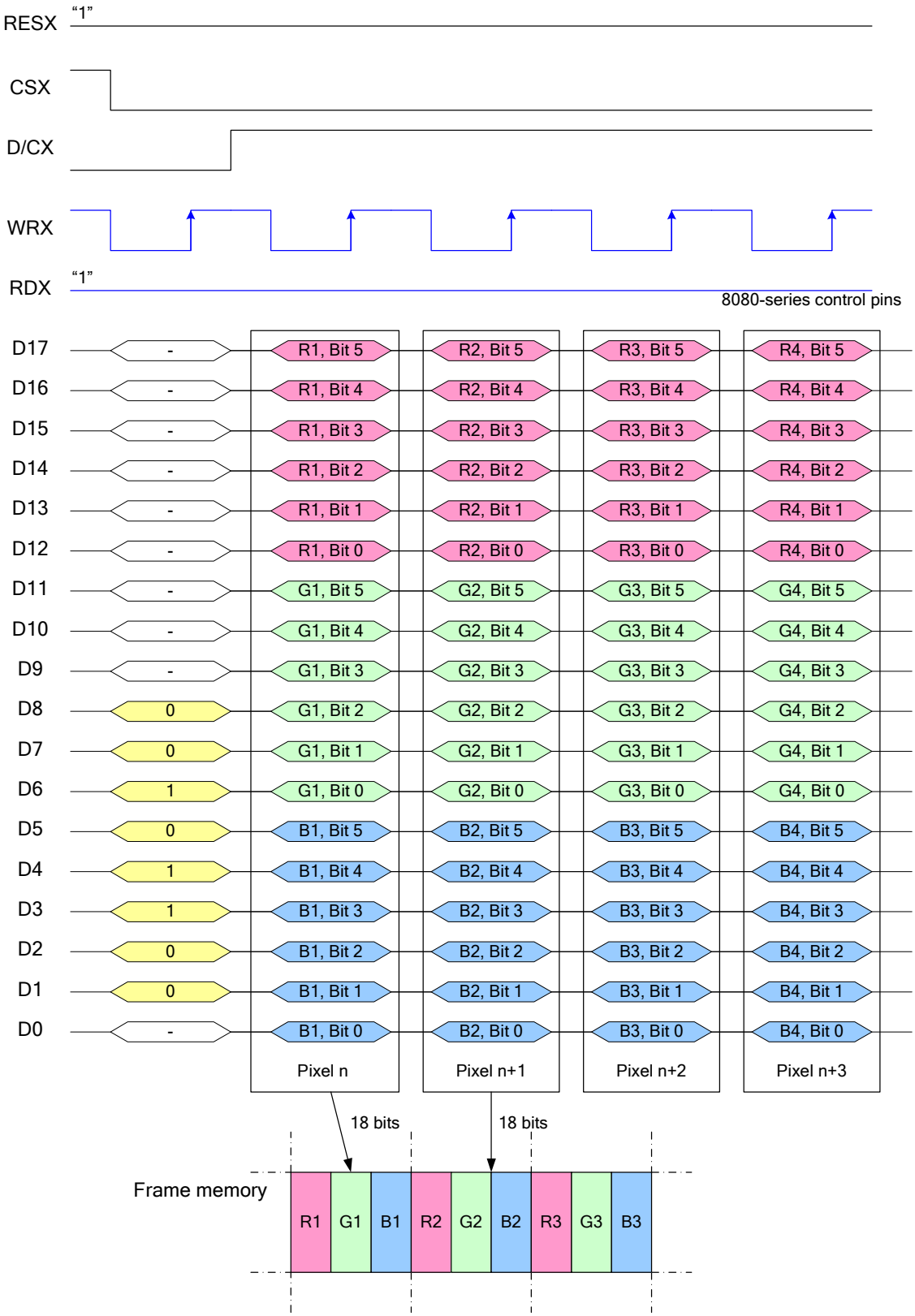
8.8.35 18-bit data bus for 18-bit/pixel (RGB-6-6-6-bit input), 262K-colors, 3Ah="06h"

There is 1 pixel (3 sub-pixels) per byte



Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Read, Green and Blue data.

Note 2: 1-times transfer (D17o D0) is used to transmit 1 pixel data with the 18-bit color depth information.

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8.8.36 3-Line Serial Interface

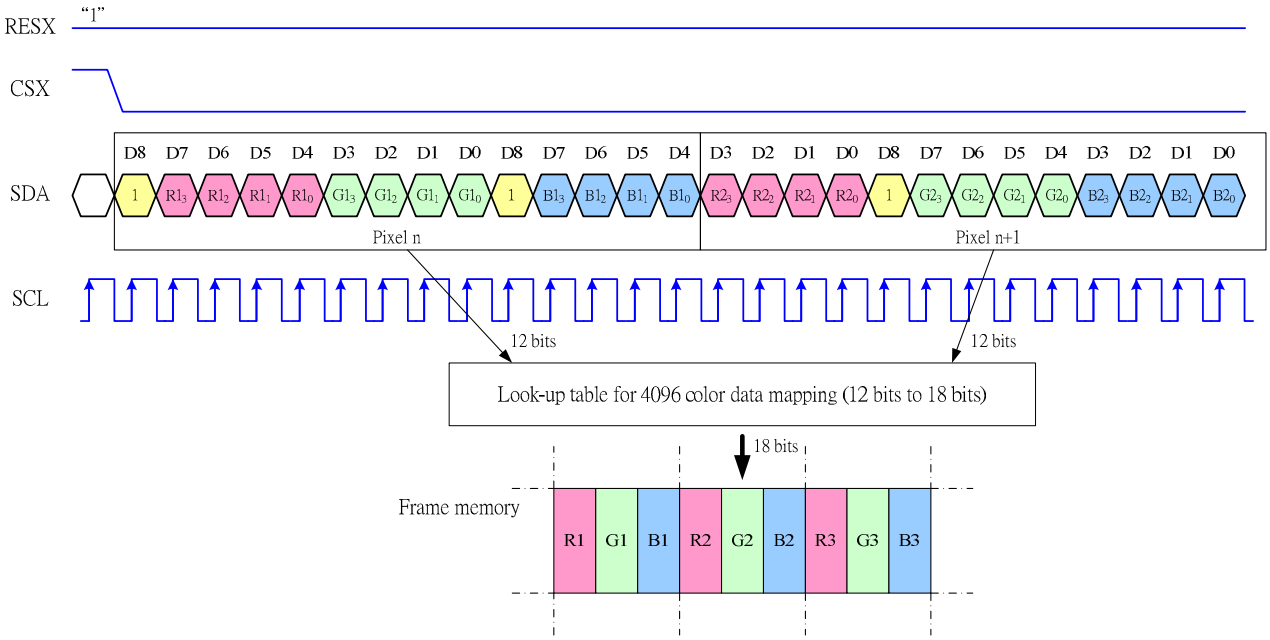
Different display data formats are available for three colors depth supported by the LCM listed below.

4k colors, RGB 4-4-4-bit input

65k colors, RGB 5-6-5-bit input

262k colors, RGB 6-6-6-bit input

8.8.37 Write data for 12-bit/pixel (RGB-4-4-4 bit input), 4K-Colors, 3Ah="03h"



Note 1: Pixel data with the 12-bit color depth information
Note 2: The most significant bits are: Rx3, Gx3 and Bx3
Note 3: The least significant bits are: Rx0, Gx0 and Bx0

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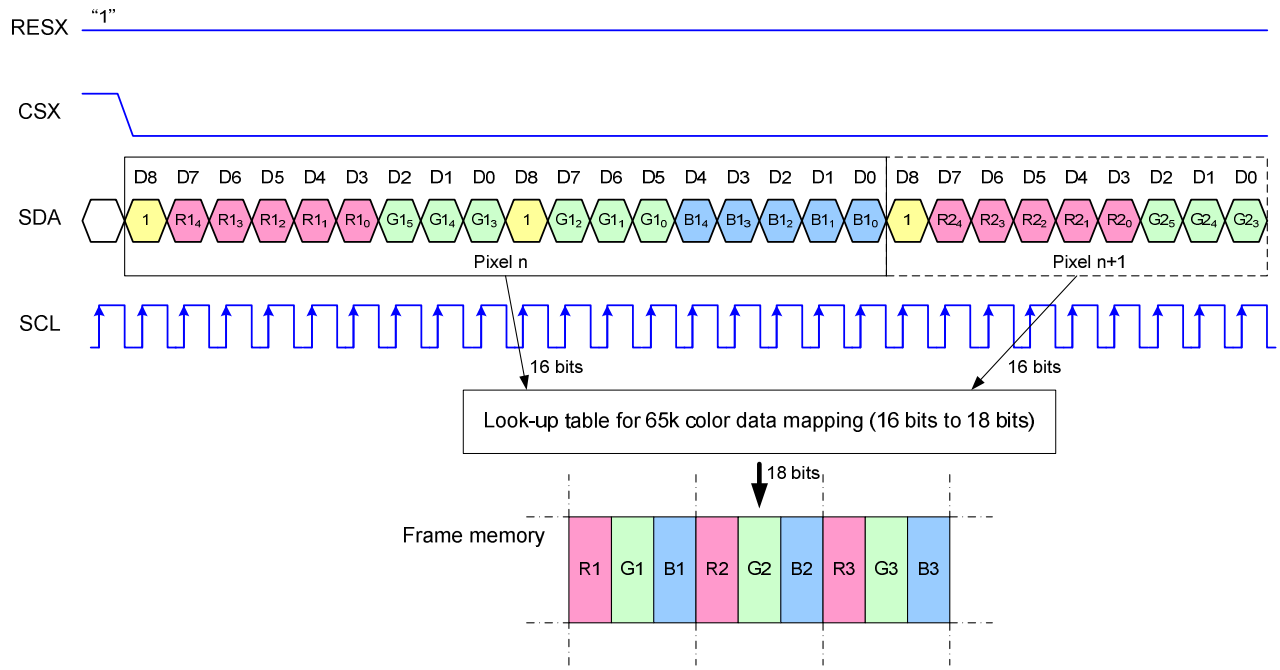
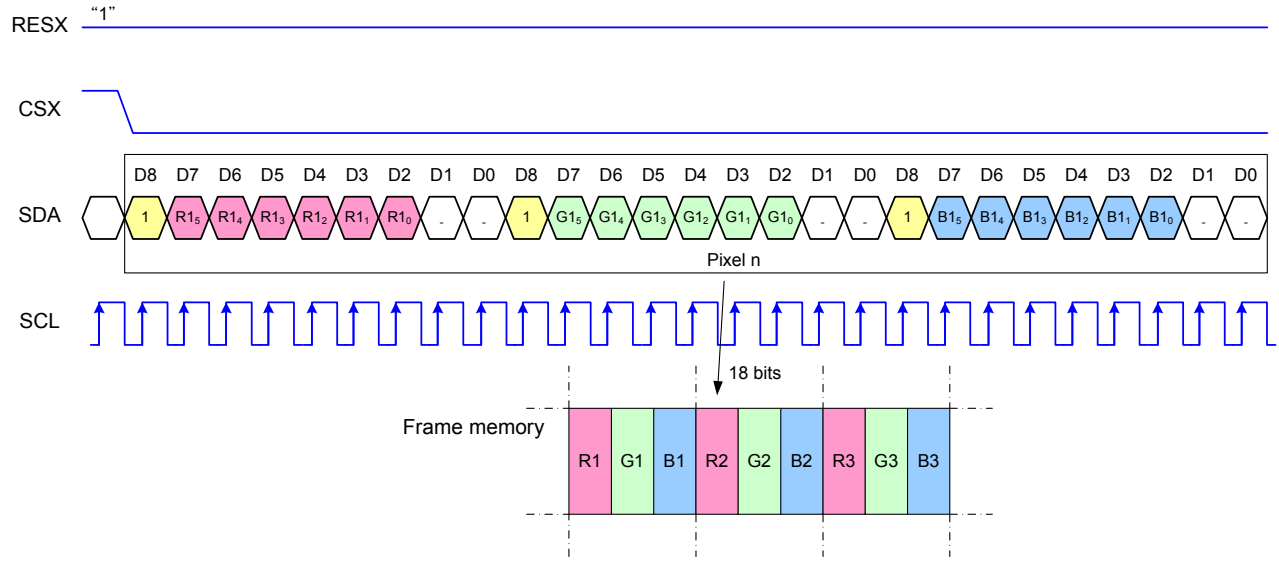
8.8.38 Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3Ah="05h"



Note 1: Pixel data with the 16-bit color depth information
Note 2: The most significant bits are: Rx4, Gx5 and Bx4
Note 3: The least significant bits are: Rx0, Gx0 and Bx0

8.8.39 Write data for 18-bit/pixel (RGB-6-6-6-bit input), 262K-Colors, 3Ah="06h"



Note 1: Pixel data with the 18-bit color depth information
Note 2: The most significant bits are: Rx5, Gx5 and Bx5
Note 3: The least significant bits are: Rx0, Gx0 and Bx0

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8.8.40 4-Line Serial Interface

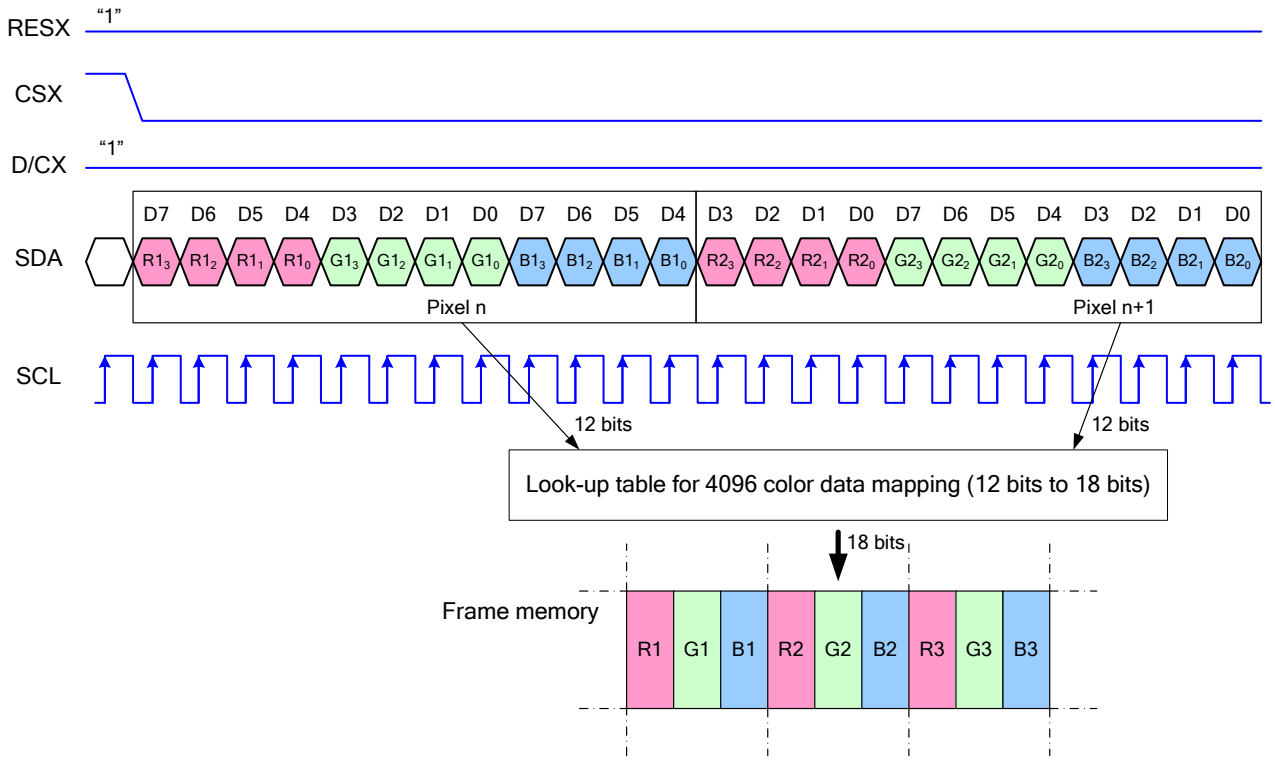
Different display data formats are available for three colors depth supported by the LCM listed below.

4k colors, RGB 4-4-4-bit input

65k colors, RGB 5-6-5-bit input

262k colors, RGB 6-6-6-bit input

8.8.41 Write data for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3Ah="03h"



Note 1. pixel data with the 12-bit color depth information
Note 2. The most significant bits are: Rx3, Gx3 and Bx3
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

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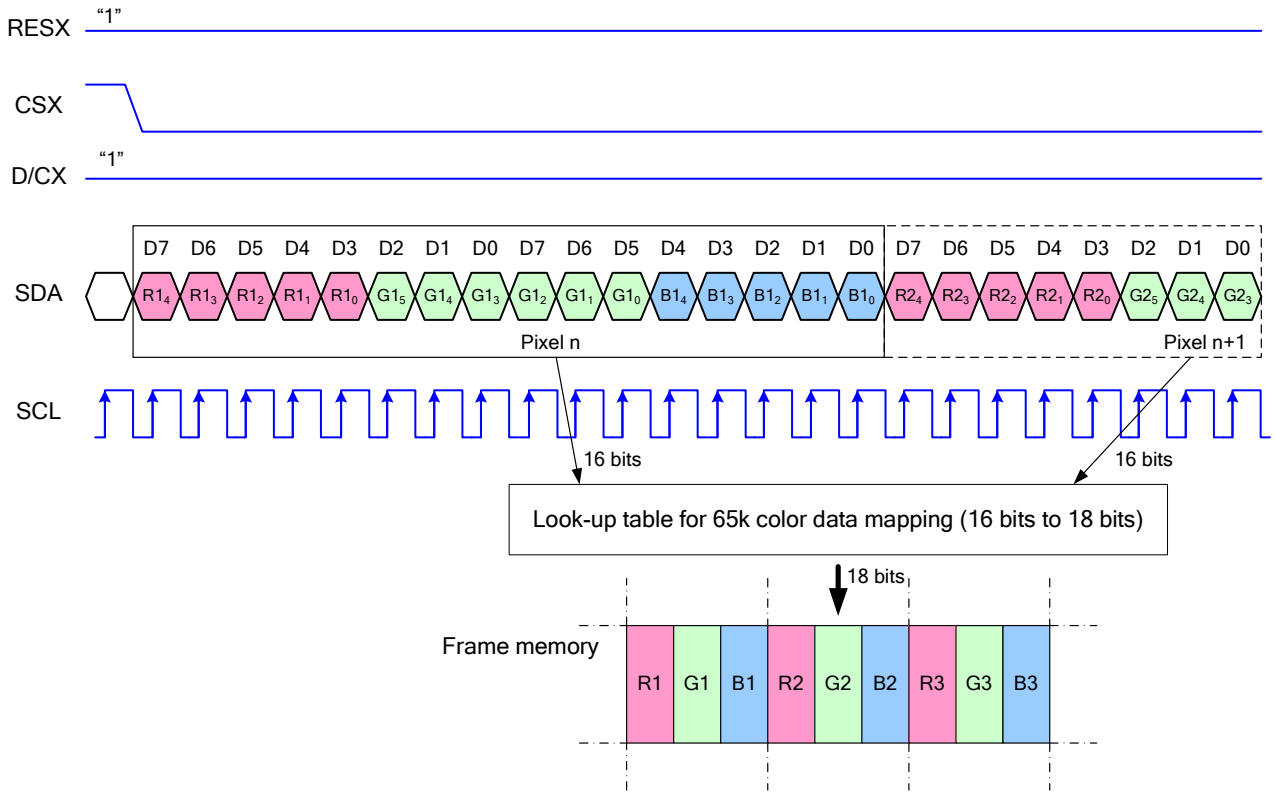
8.8.42 Write data for 16-bit/pixel (RGB-5-6-5-bit input), 65K-Colors, 3Ah="05h"



Note 1. pixel data with the 16-bit color depth information
Note 2. The most significant bits are: Rx4, Gx5 and Bx4
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

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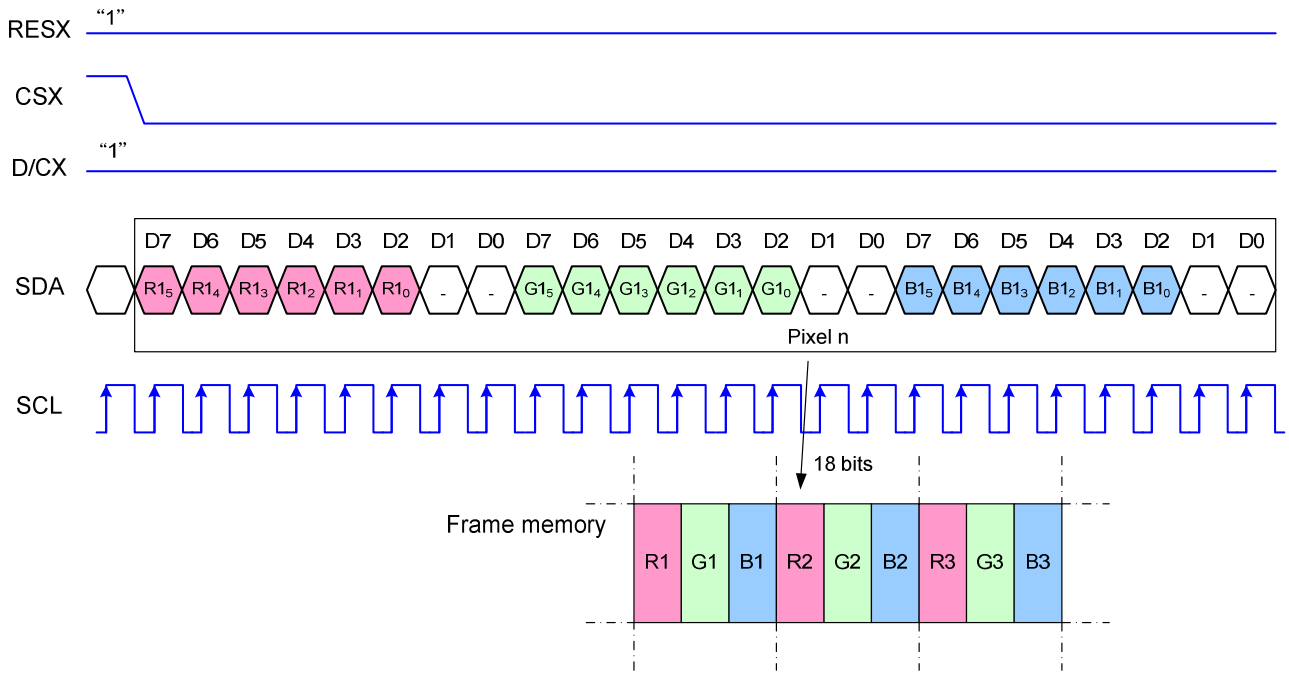
8.8.43 Write data for 18-bit/pixel (RGB-6-6-6-bit input), 262K-Colors, 3Ah="06h"



Note 1. pixel data with the 18-bit color depth information
Note 2. The most significant bits are: Rx5, Gx5 and Bx5
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

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8.9 RGB Interface

8.9.1 RGB interface Selection

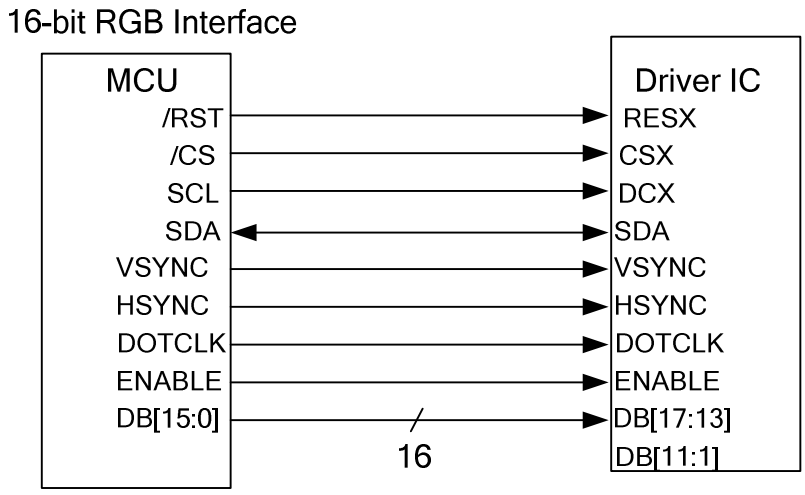
The color format selection of RGB Interface for ST7789VW is selected by setting the RIM and command 3Ah, DB[6:4].

RIM	3Ah, DB[6:4]	RGB Interface Mode	Data pins
0	110	18-bit 262K RGB Interface	DB[17:0]
0	101	16-bit 65K RGB Interface	DB[17:13], DB[11:1]
1	110	6-bit 262K RGB Interface	DB[5:0]
1	101	6-bit 65K RGB Interface	DB[5:0]

8.9.2 RGB Color Format

ST7789VW supports two kinds of RGB interface, DE mode and HV mode, and 6bit/18bit data format. When DE mode is selected and the VSYNC, HSYNC, DOTCLK, DE, D[17:0] pins can be used; when HV mode is selected and the VSYNC, HSYNC, DOTCLK, D[17:0] pins can be used. When using RGB interface, only serial interface can be selected.

16-bit RGB interface Hardware suggestion, IM[3:0]=0101.



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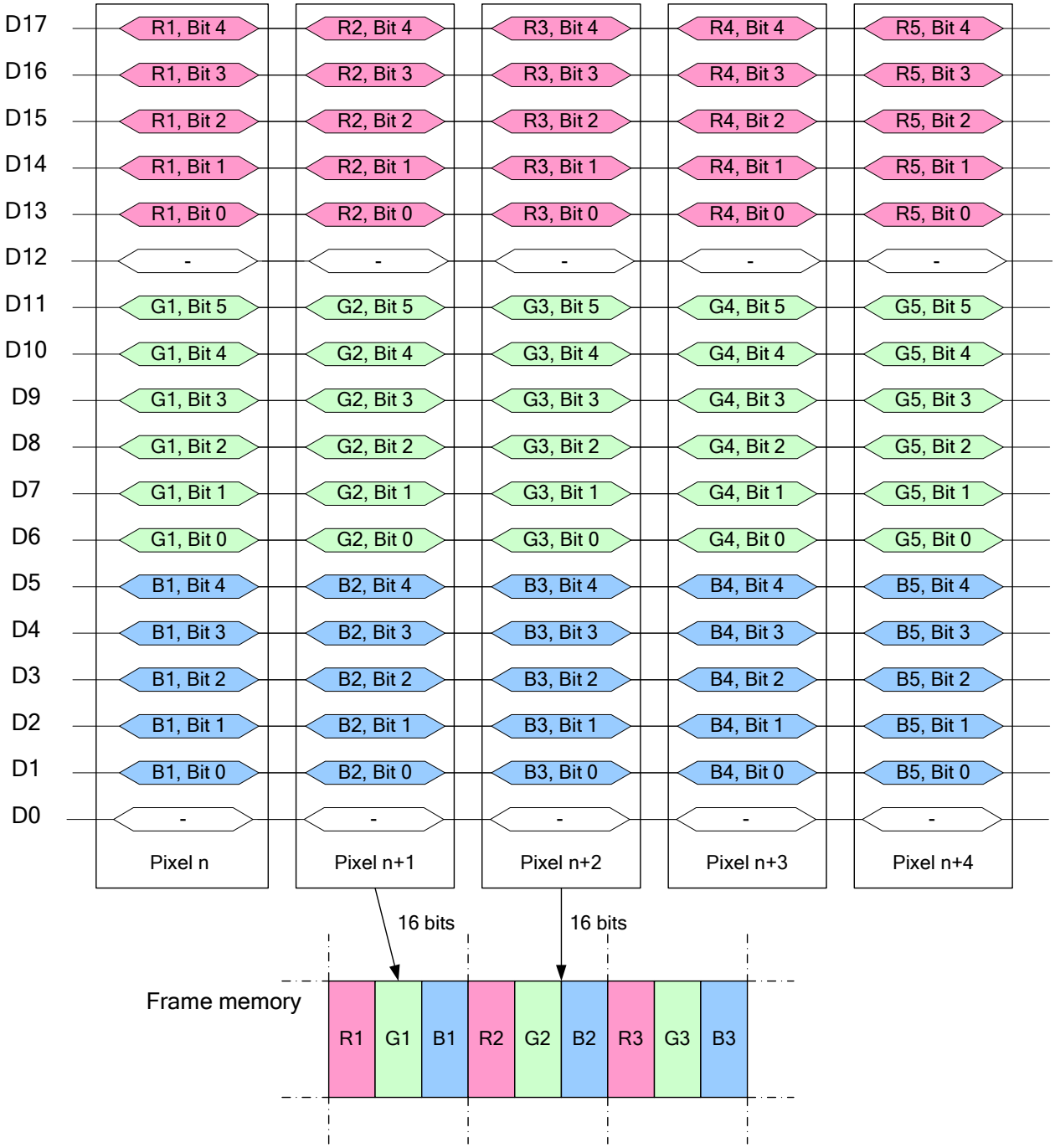
Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors



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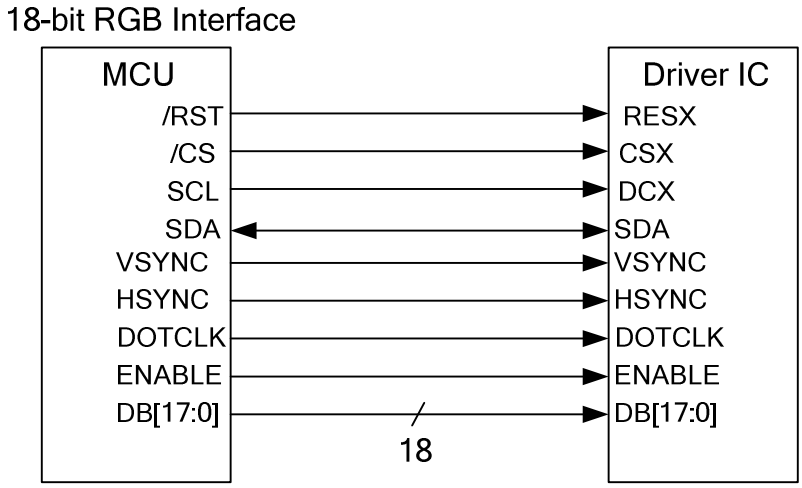
18-bit RGB interface hardware suggestion, IM[3:0]=0101.



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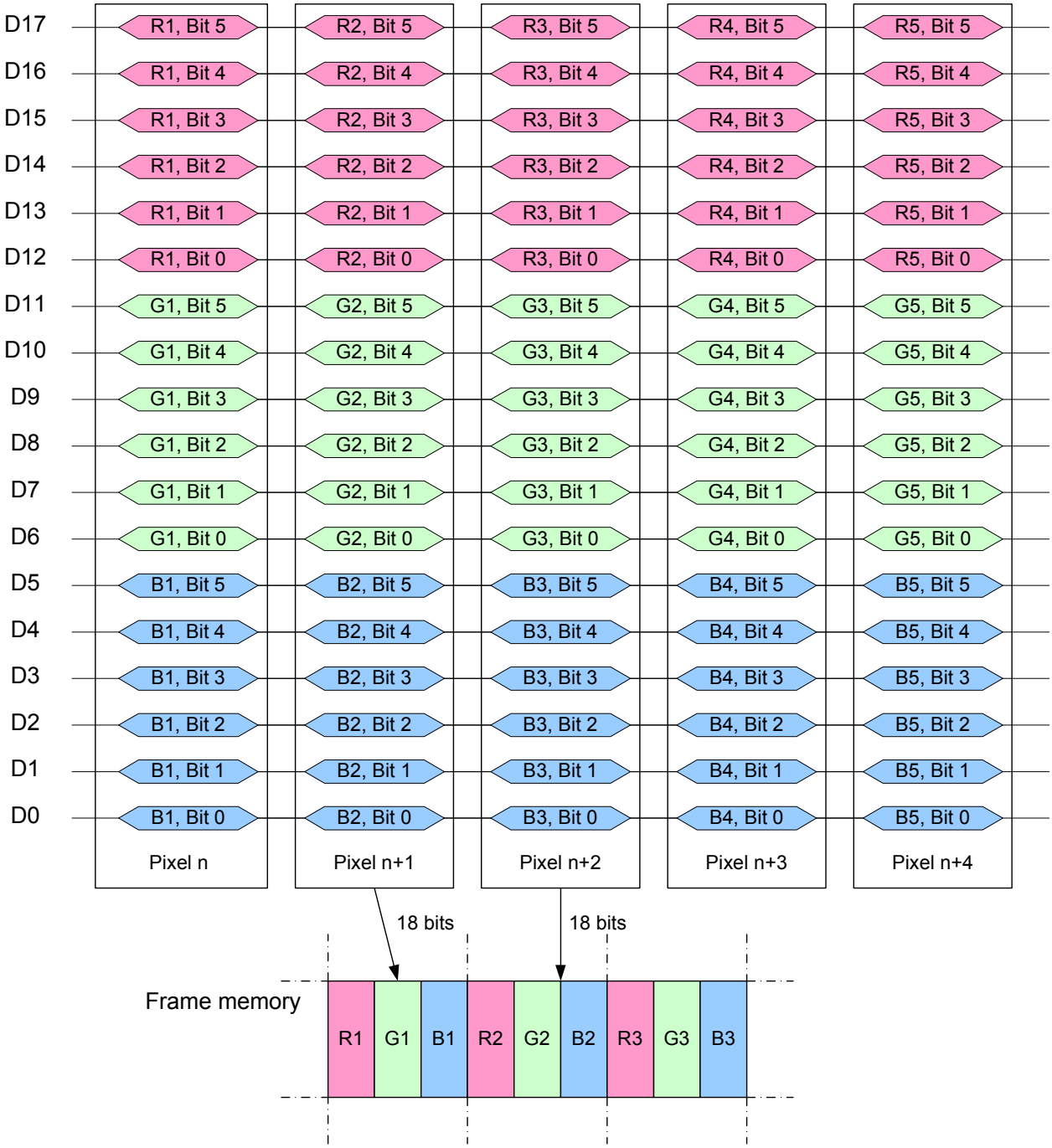
Write data for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors



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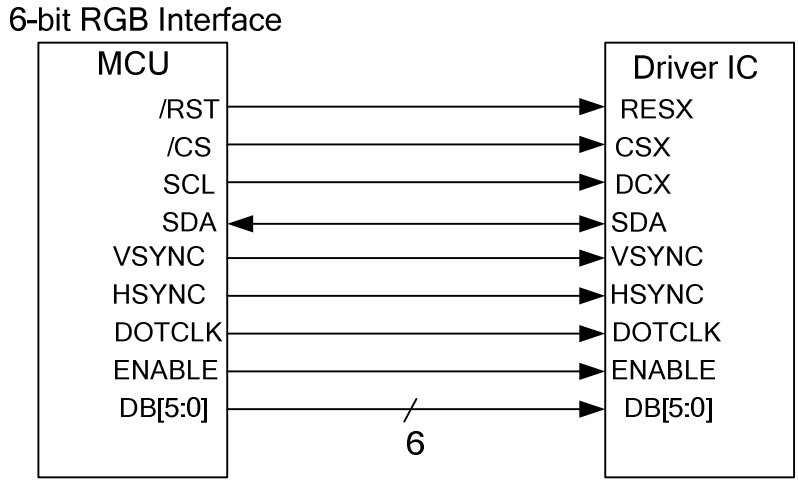
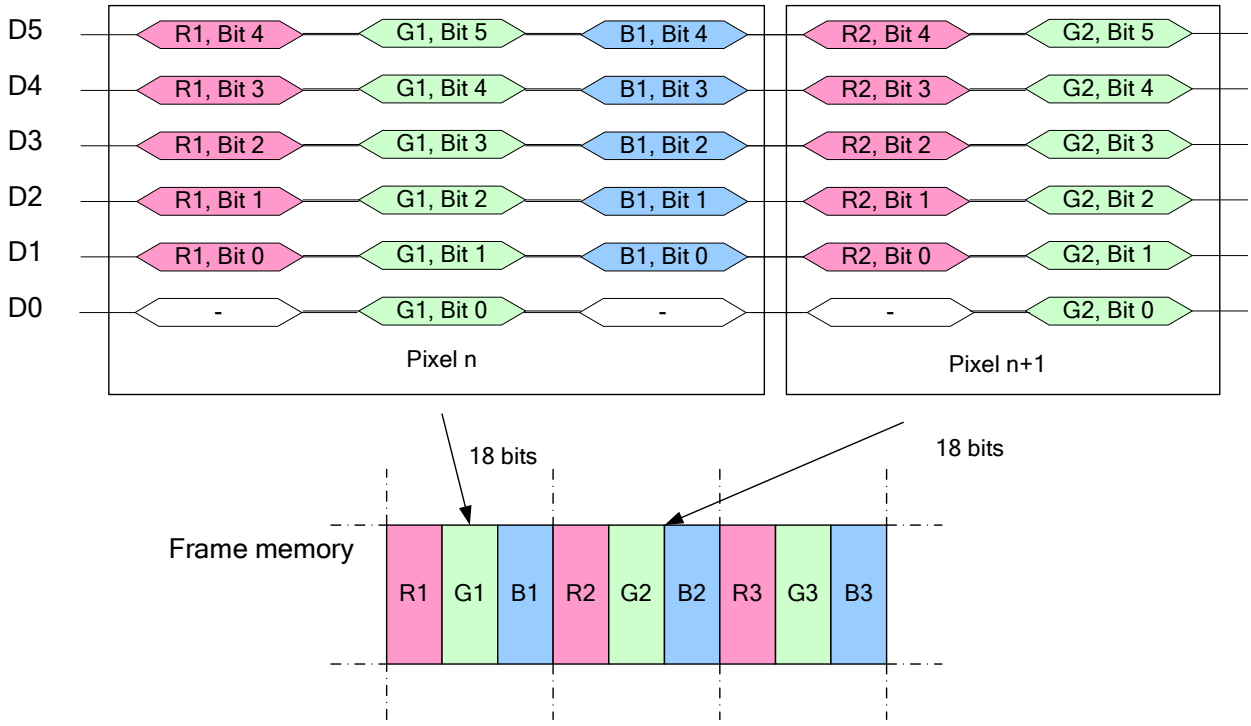
6-bit RGB interface hardware suggestion, IM[3:0]=0101.



Write data for 6-bit/pixel (RGB 5-6-5-bit input), 65K-Colors



Write data for 6-bit/pixel (RGB 6-6-6-bit input), 262K-Colors

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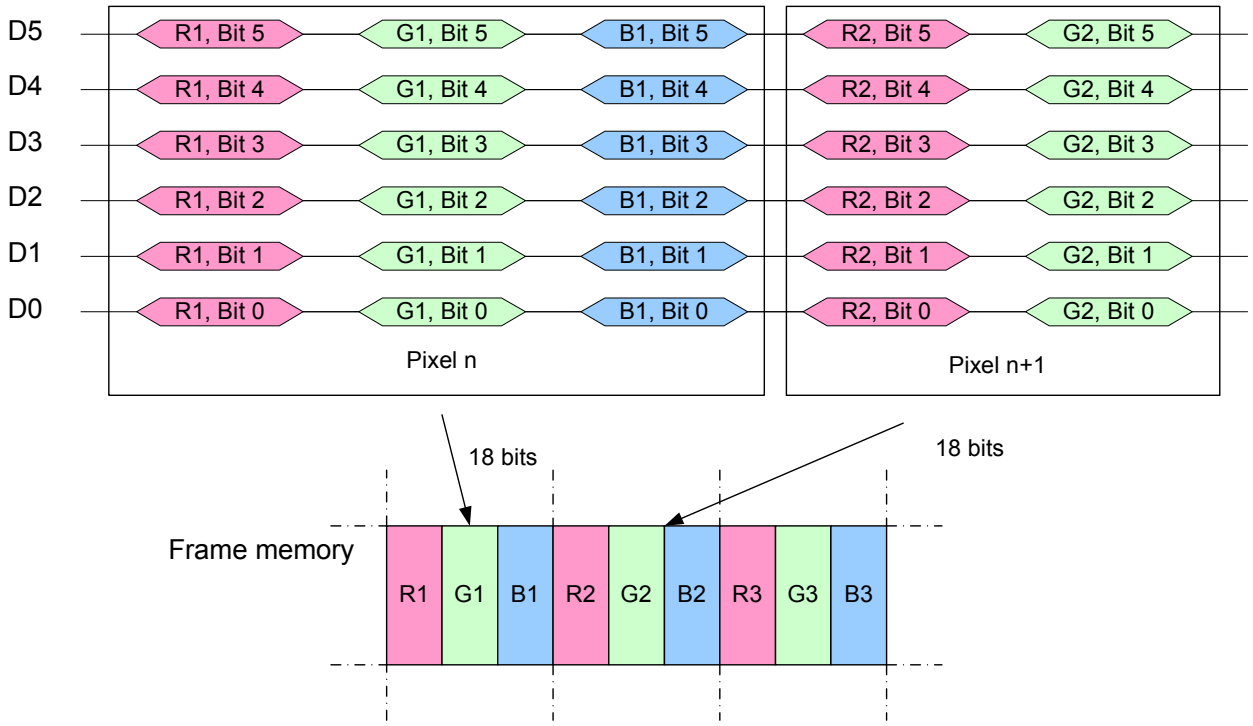

Figure 23 RGB Interface Data Format

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8.9.3 RGB Interface Definition

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The data can be written only within the specified area with low power consumption by using window address function. The back porch and front porch are used to set the RGB interface timing.

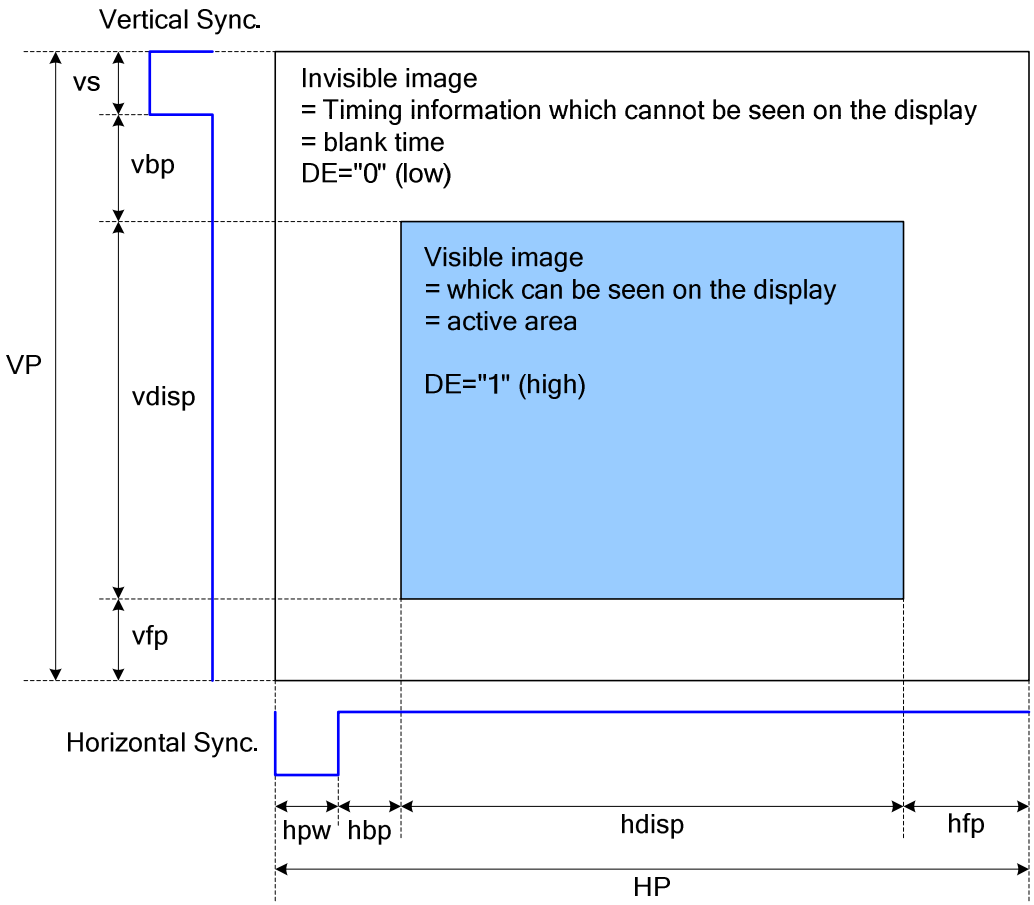

Figure 24 DRAM Access Area by RGB Interface

Please refer to the following table for the setting limitation of RGB interface signals.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Horizontal Sync. Width	hpw	2	10	hpw+hbp=31	Clock
Horizontal Sync. Back Porch	hbp	4	10		Clock
Horizontal Sync. Front Porch	hfp	2	38	-	Clock
Vertical Sync. Width	vs	2	4	vs+vbp=127	Line
Vertical Sync. Back Porch	vbp	2	4		Line
Vertical Sync. Front Porch	vfp	2	8	-	Line

Note:

Typical value are related to the setting of dot clock is 7MHz and frame rate is 70Hz..

If the setting of hpw is 10 dot clocks and hbp is 10 dot clocks, the setting of HBP in command B1h is 20 dot clocks

In with ram mode, hpw+hbp+hfp≧22

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In without ram mode, hpw+hbp≧20

6bit RGB interface:

Parameter	Symbol	Min.	Typ.	Max.	Unit
Horizontal Sync. Width	hpw	6	30	hpw+hbp=93	Clock
Horizontal Sync. Back Porch	hbp	12	30		Clock
Horizontal Sync. Front Porch	hfp	6	60	-	Clock
Vertical Sync. Width	vs	2	4	vs+vbp=127	Line
Vertical Sync. Back Porch	vbp	2	4		Line
Vertical Sync. Front Porch	vfp	2	8	-	Line

Note:

Typical value are related to the setting of dot clock is 17MHz and frame rate is 60Hz, VDD=VDDI=2.8V..

In with ram mode, hpw+hbp+hfp≧66

In without ram mode, hpw+hbp≧60

8.9.4 RGB Interface Mode Selection

ST7789VW supports two kinds of RGB interface, DE mode and HV mode. Each mode also can select with ram and without ram. The table shown below uses command B1h to select RGB interface mode.

RCM[1:0]	WO	RGB Mode	Data Path
10	0	DE mode	Ram
	1		Shift register (without Ram)
11	0	HV mode	Ram
	1		Shift register (without Ram)

8.9.5 RGB Interface Timing

The timing chart of RGB interface DE mode is shown as follows.

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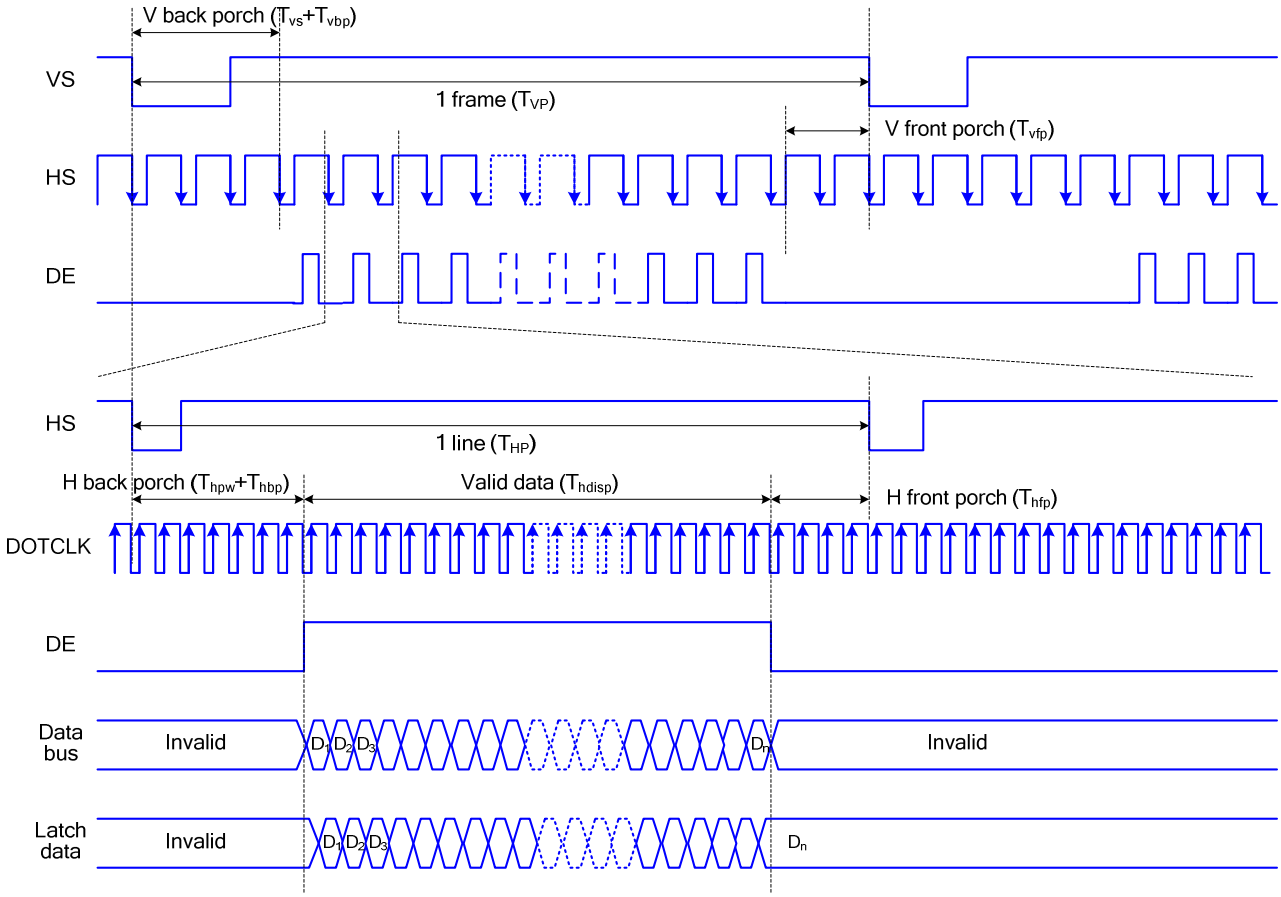

Note: The setting of front porch and back porch in host must match that in IC as this mode.

Figure 25 Timing Chart of Signals in RGB Interface DE Mode

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The timing chart of RGB interface HV mode is shown as follows.

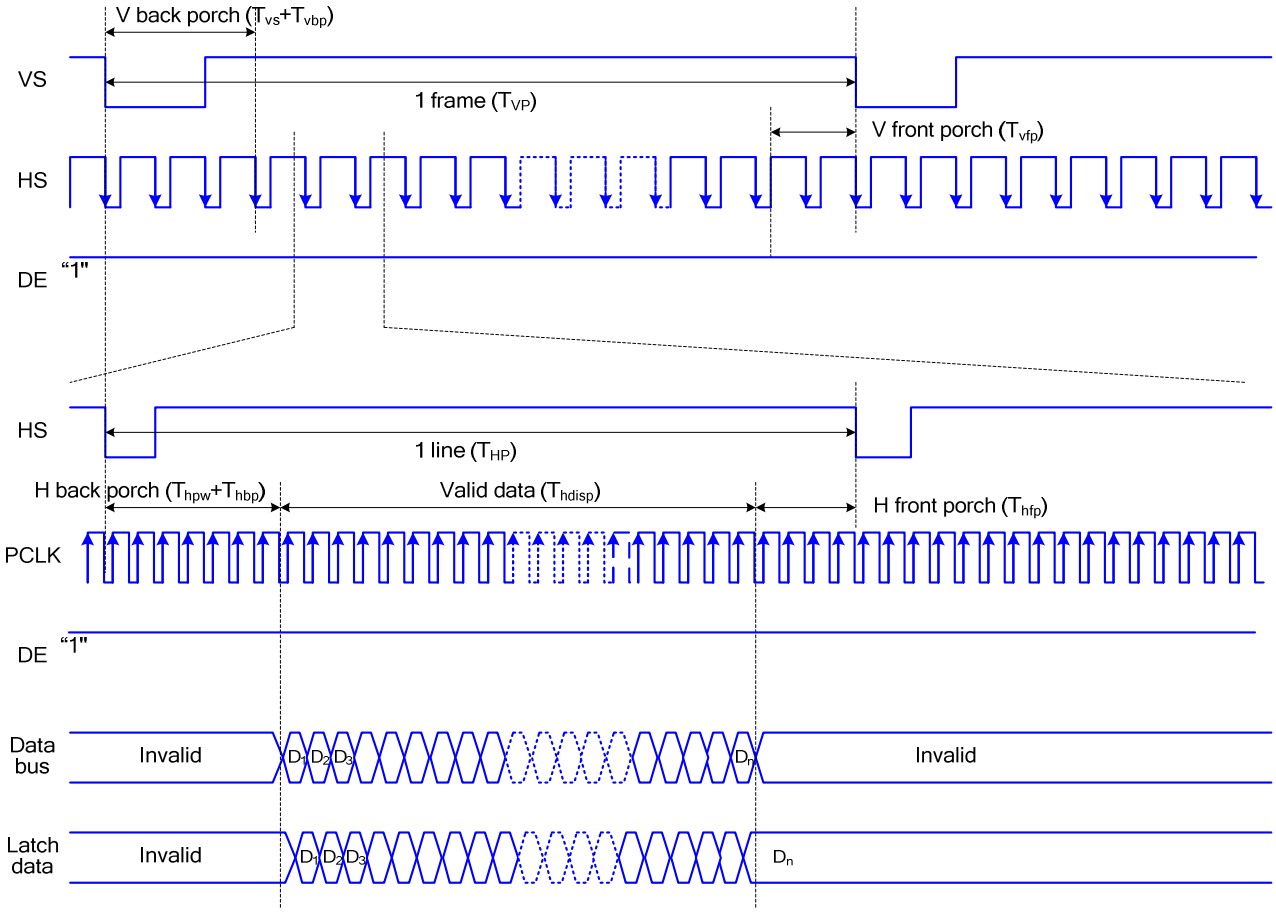

Figure 26 Timing chart of RGB interface HV mod

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The following are the functions not available in RGB Input Interface mode.

Function	RGB Interface	I80 System Interface
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced scan	Not available	Available
Graphics operation function	Not available	Available

VSYNC, HSYNC, and DOTCLK signals must be supplied during a display operation period.

In RGB interface mode, the panel controlling signals are generated from DOTCLK, not the internal clock generated from the internal oscillator.

In 6-bit RGB interface mode, each of RGB dots are transferred in synchronization with DOTCLK signals. In other words, one pixel data needs to take three DOTCLKs to transfer.

In 6-bit RGB interface mode, the cycles of VSYNC, HSYNC, ENABLE, DOTCLK signals must be set correctly so that the data transfer is completed in units of pixels.

When switching between the internal operation mode and the external display interface operation mode, follow the sequences below in setting instruction.

In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.

In RGB interface mode, a RAM address is set in the address counter every frame on the falling edge of VSYNC.

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8.10 VSYNC Interface

8.10.1 18-bit RGB Interface

The ST7789VW incorporates VSYNC interface, which enables motion pictures to be displayed with only the conventional system interface and the frame synchronization signal (VSYNC). This interface requires minimal changes from the conventional system to display motion pictures.In this interface the internal display operation is synchronized with VSYNC. Data for display is written to RAM via the system interface with higher speed than for internal display operation. This method enables tearing-free display of motion pictures with the conventional interface.

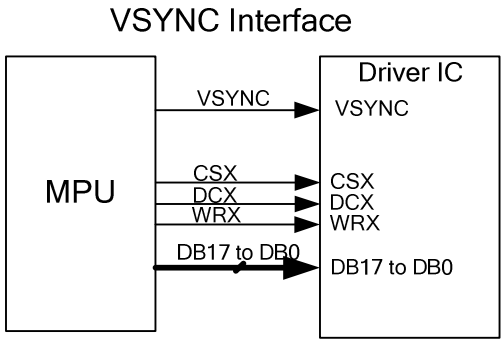

Figure 27 Data transmission through VSYNC interface

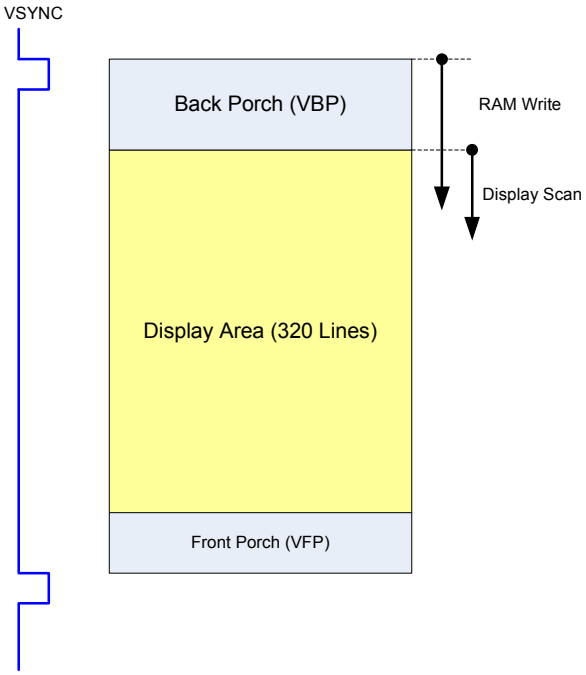

Figure 28 Operation through VSYNC Interface

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Display operation can be achieved by using the internal clock generated by the internal oscillator and the VSYNC input. Because all the data for display is written to RAM, only the data to be rewritten is transferred. This method reduces the amount of data transferred during motion picture display operation.

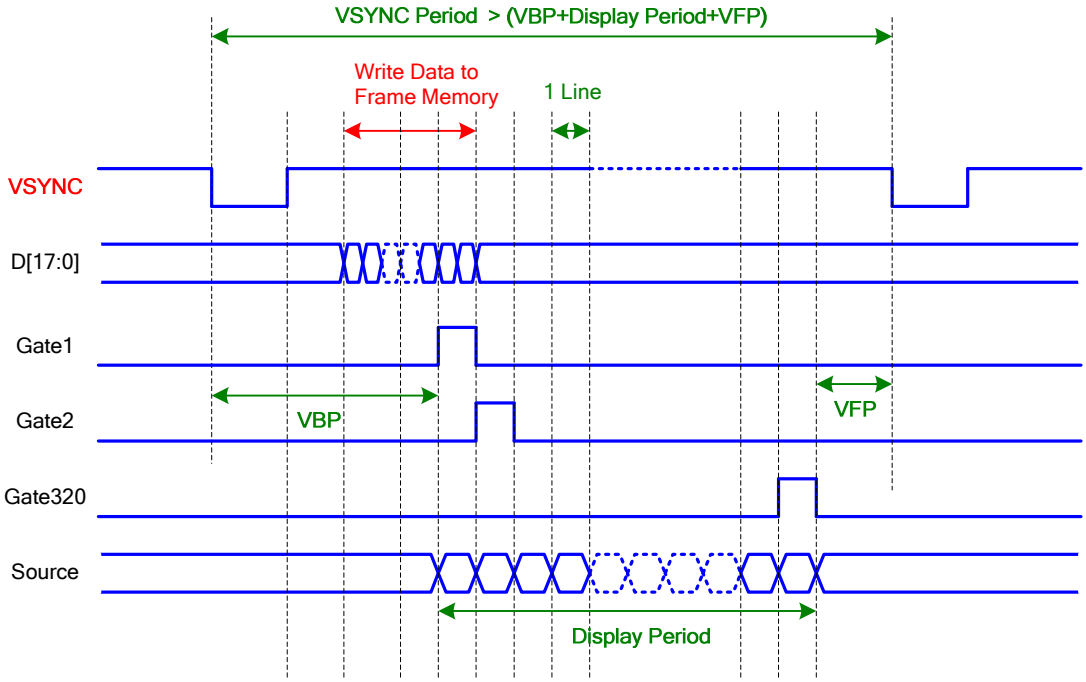

Figure 29 Timing Diagram of VSYNC Interface

VSYNC interface requires taking the minimum speed for RAM writing via the system interface and the frequency of the internal clock into consideration. RAM writing should be performed with higher speed than the result obtained from the calculation shown below. The internal memory writing address counter is reset by VSYNC. So, insure interval time between VSYNC falling and DRAM data writing.

Note:

1. VSYNC period should always be constant. If not, some degradation of display such as flicker may occur in LCD system.

2. Display data don't need to be written for every VSYNC period. For example, any system is working under 60Hz frame rate and 30-fps motion picture condition. So being written display data for every other frame would be enough.

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8.10.2 VSYNC Interface Mode

Leading Mode

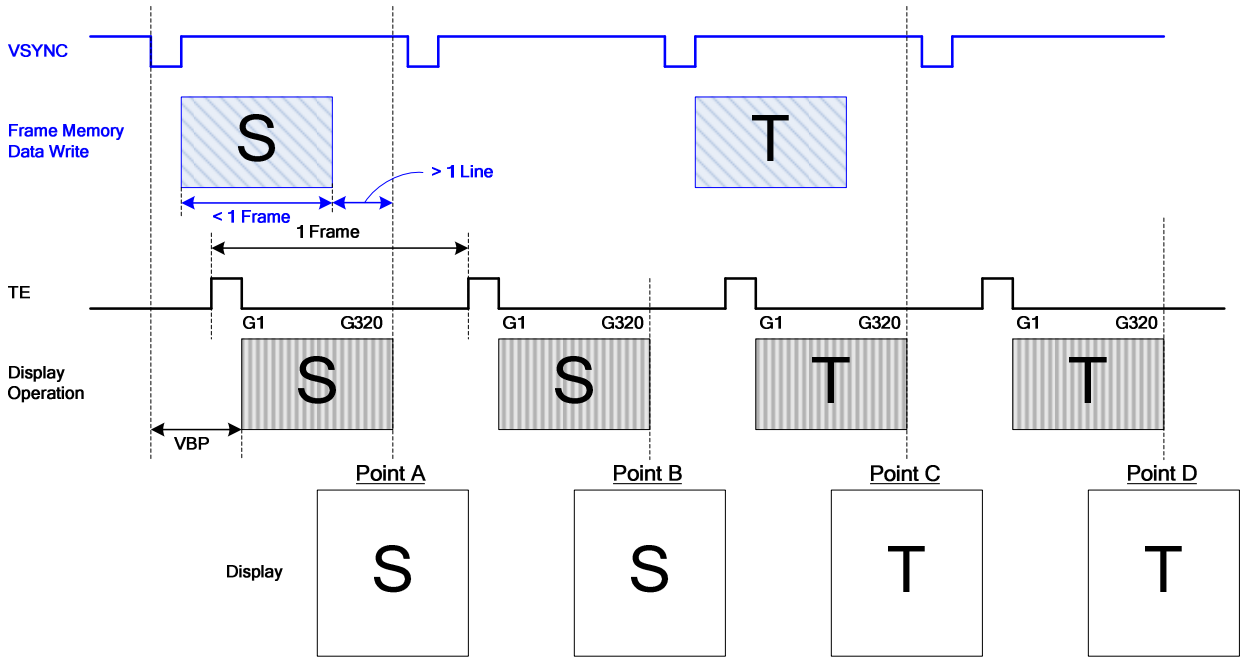

Figure 30 Operation for Leading Mode of VSYNC Interface

Lagging Mode

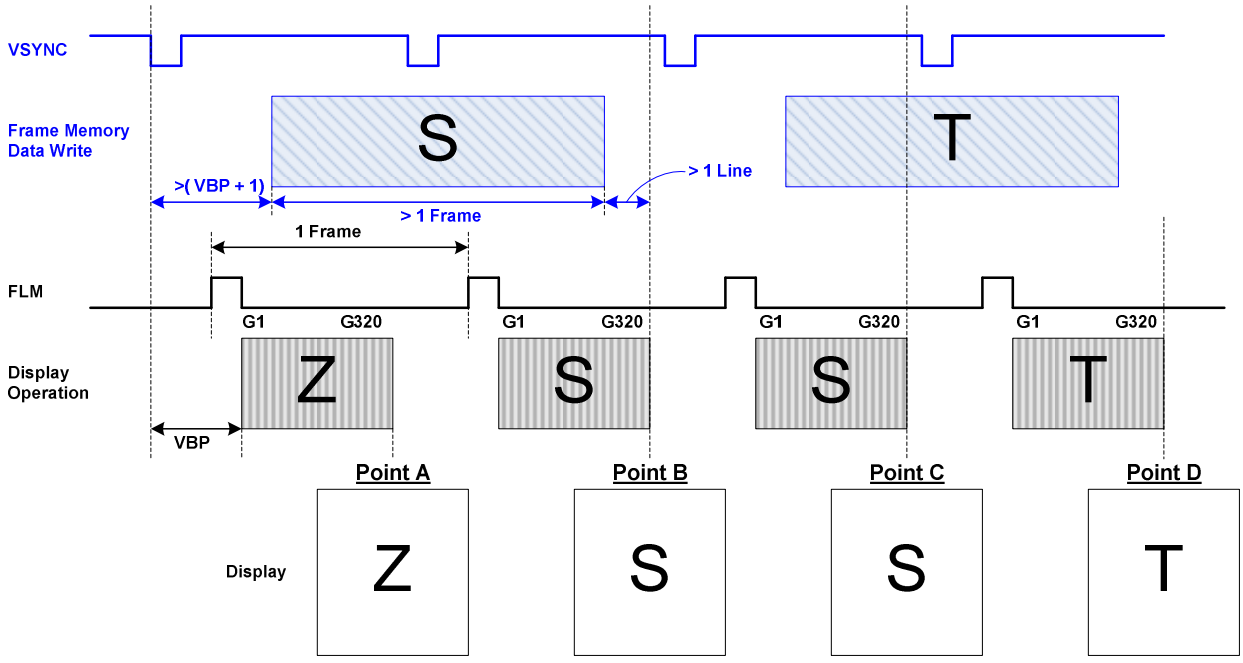

Figure 31 Operation for Lagging Mode of VSYNC Interface

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Notes:

1. When RAM writing does not start immediately after the falling edge of VSYNC, the time between the falling edge of VSYNC and the RAM writing start timing must also be considered.

1. The minimum DRAM write speed must be satisfied and the frequency variation must be taken into consideration.

2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.

3. When switching from the internal clock operation mode to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.

4. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode and set the AM bit to "0" to transfer display data.

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8.11 Display Data RAM

8.11.1 Configuration

The display module has an integrated 240x320x18-bit graphic type static RAM. This 1382400-bit memory allows storing on-chip a 240xRGBx320 image with an 18-bpp resolution (262K-color). There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

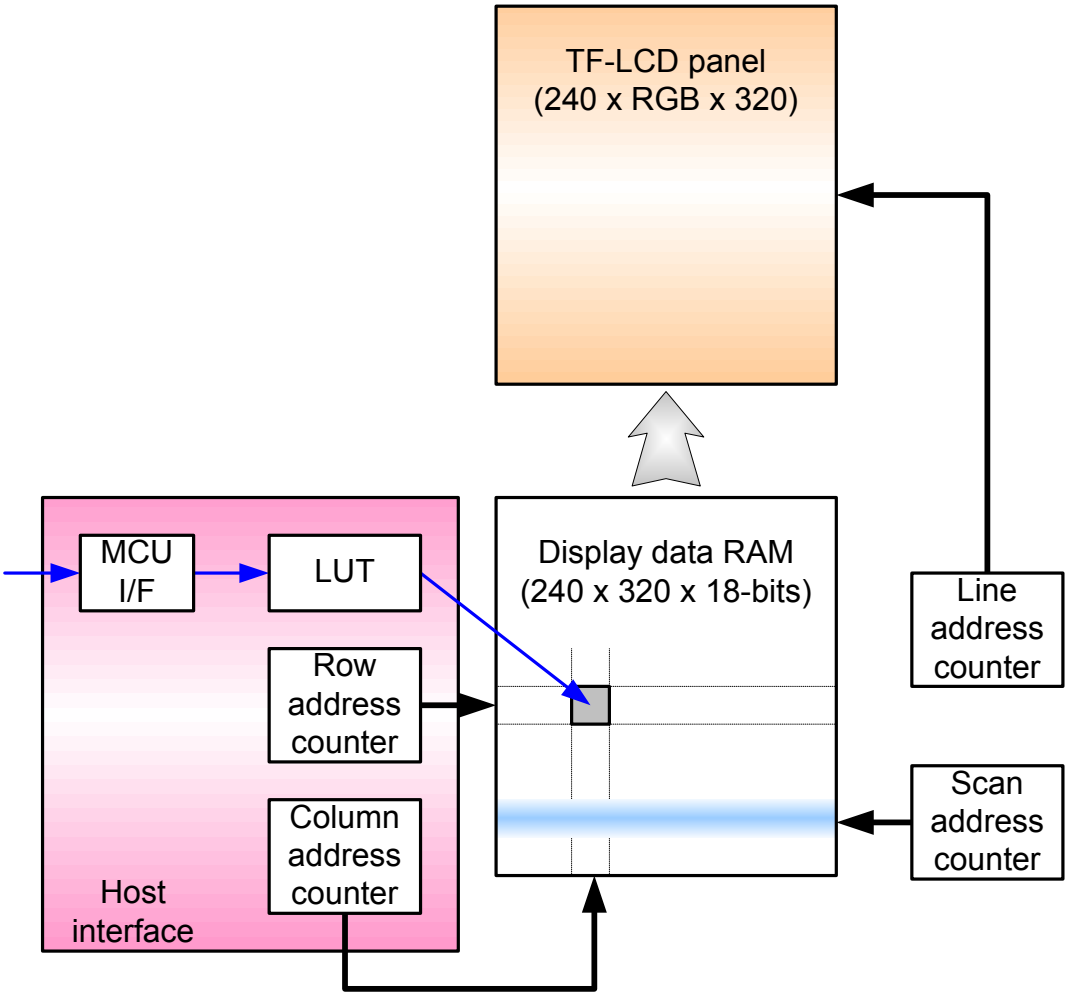

Figure 32 Display data RAM organization

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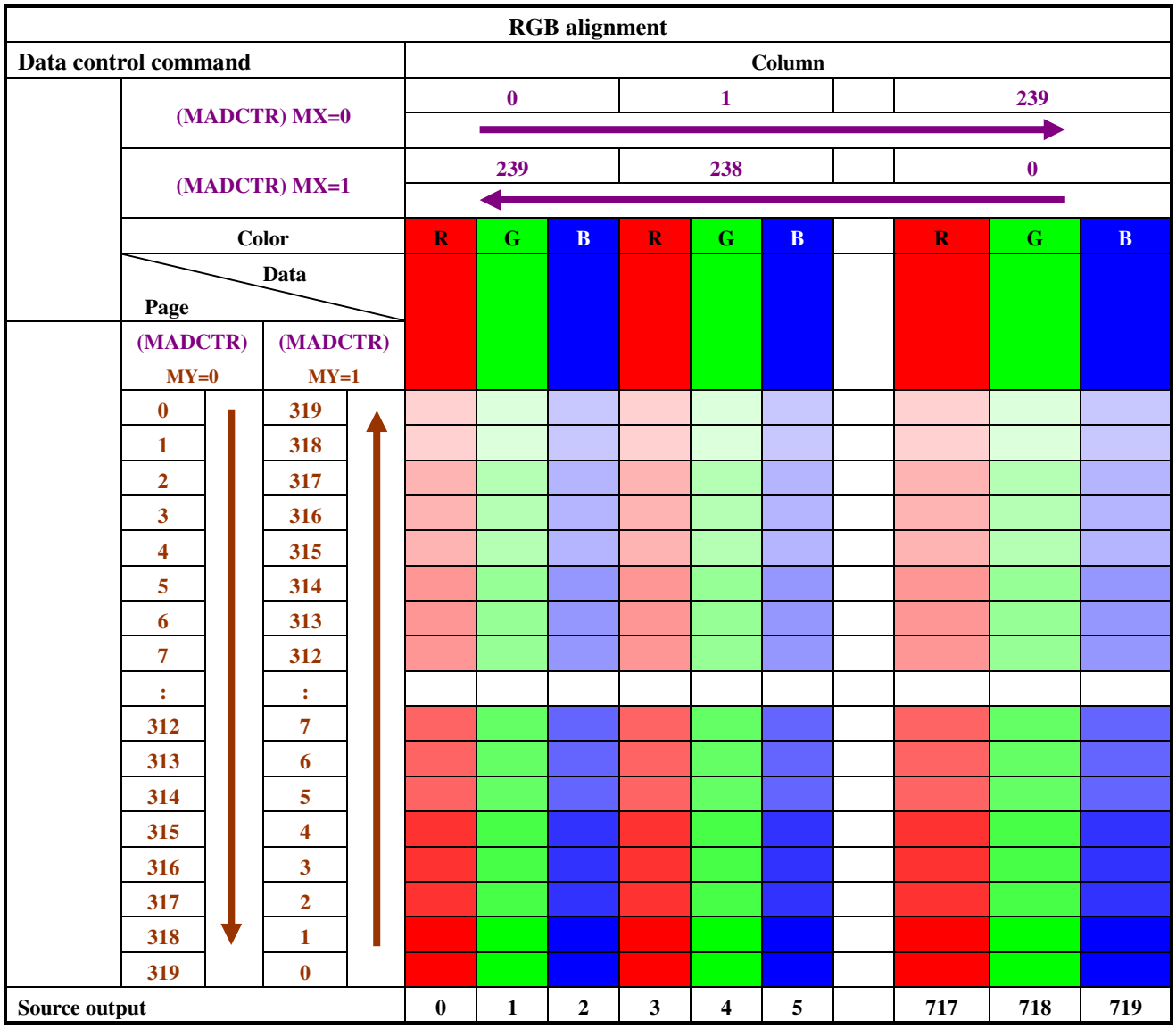
8.11.2 Memory to display address mapping



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8.12 Address Control

The address counter sets the addresses of the display data RAM for writing and reading.

Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 6-6-6-bit), according to the data formats. As soon as this pixel-data information is complete the “Write access” is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=239 (Efh) and Y=0 to Y=319 (13Fh). Addresses outside these ranges are not allowed. Before writing to the RAM, a window must be defined that will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=239 (Efh), YE=319 (13Fh).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands “CASET, RASET and MADCTL”, define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Section 8.12 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data bust be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as below

Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to “Start Column (XS)”	Return to “Start Row (YS)”
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than “End Column (XE)”	Return to “Start Column (XS)”	Increment by 1
The Column counter value is larger than “End Column (XE)” and the Row counter value is larger than “End Row (YE)”	Return to “Start Column (XS)”	Return to “Start Row (YS)”

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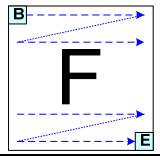
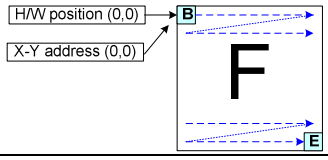
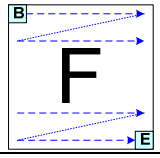
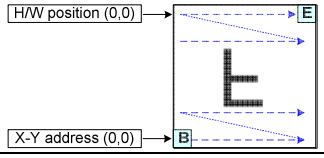
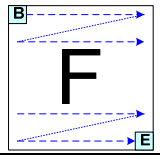
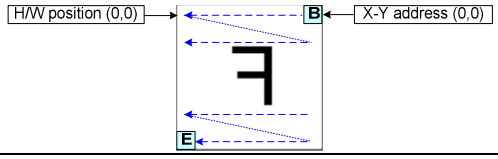
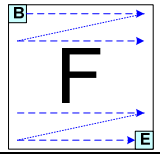
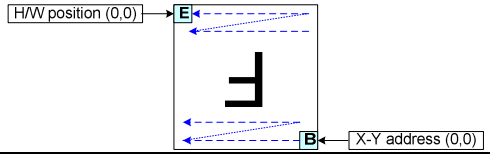
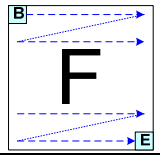
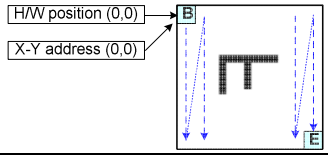
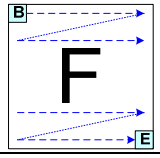
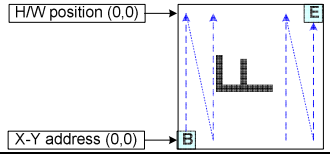
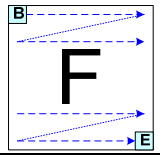
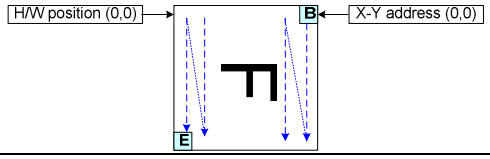
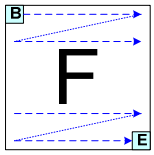
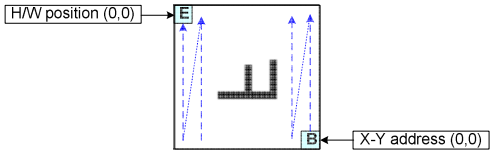
Display Data Direction	MADCTR Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

Figure 33 Display data RAM organization

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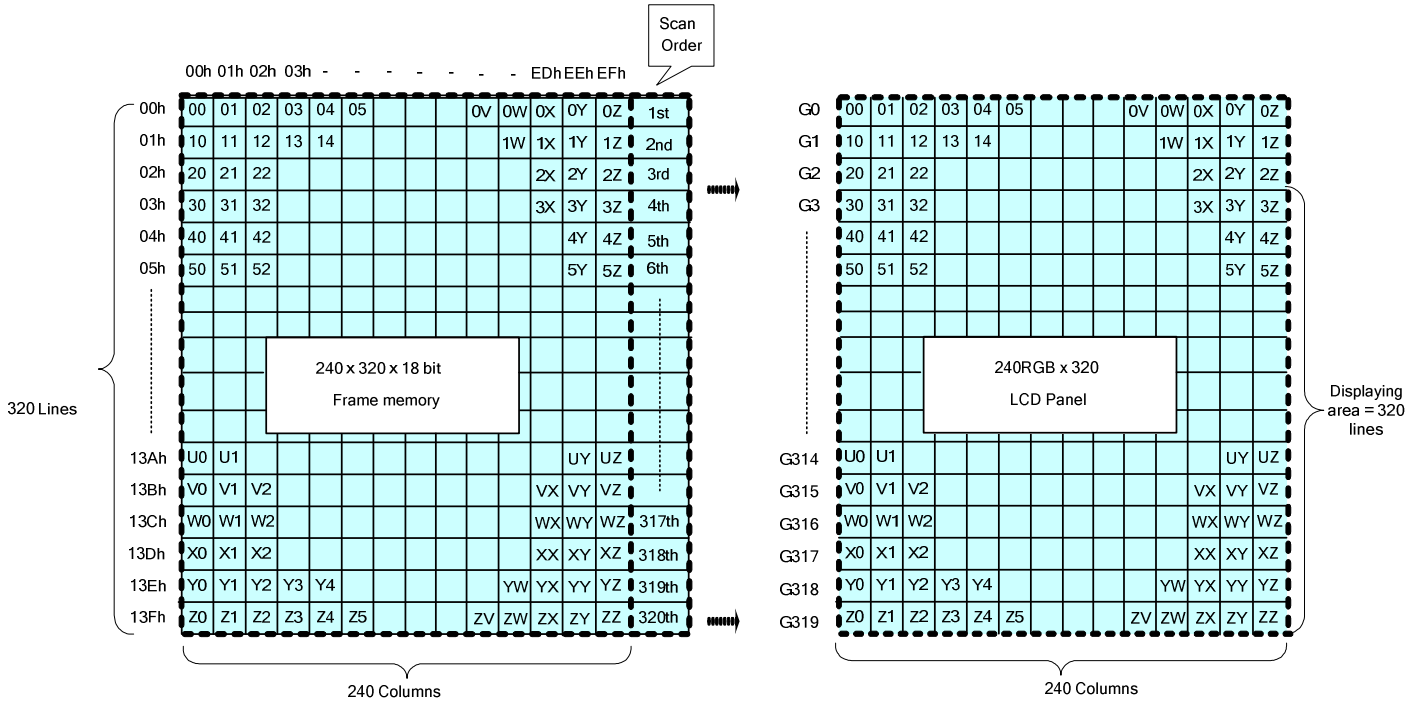
8.13 Normal Display On or Partial Mode On, Vertical Scroll Off

In this mode, contents of the frame memory within an area where column address is 00h to 83h and row address is 00h to

83h is displayed.

To display a dot on leftmost top corner, store the dot data at (column address, row address) = (0,0).

Example1) Normal Display On



Example2) Partial Display On: PSL[15:0] = 0004h, PEL[15:0] = 013Ch, MADCTR (ML)=0

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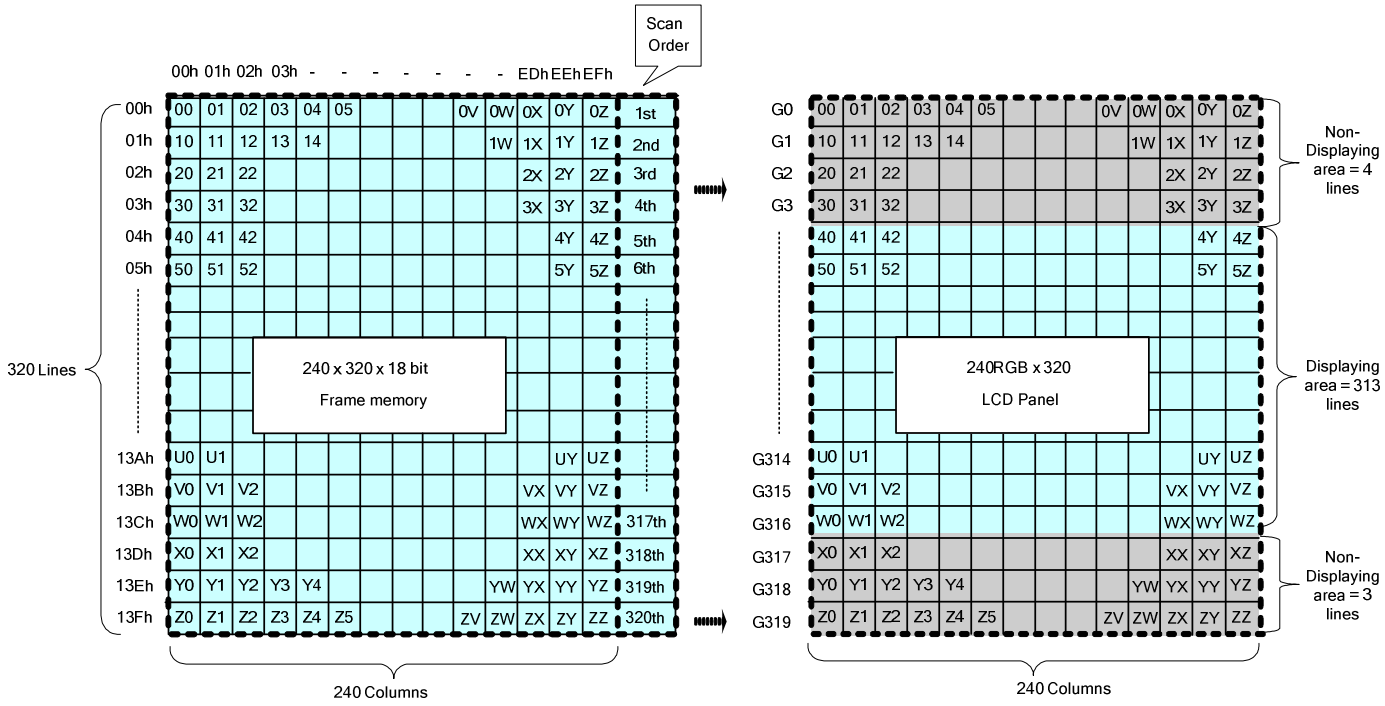

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8.14 Vertical Scroll Mode

8.14.1 Rolling scroll

There is just one types of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

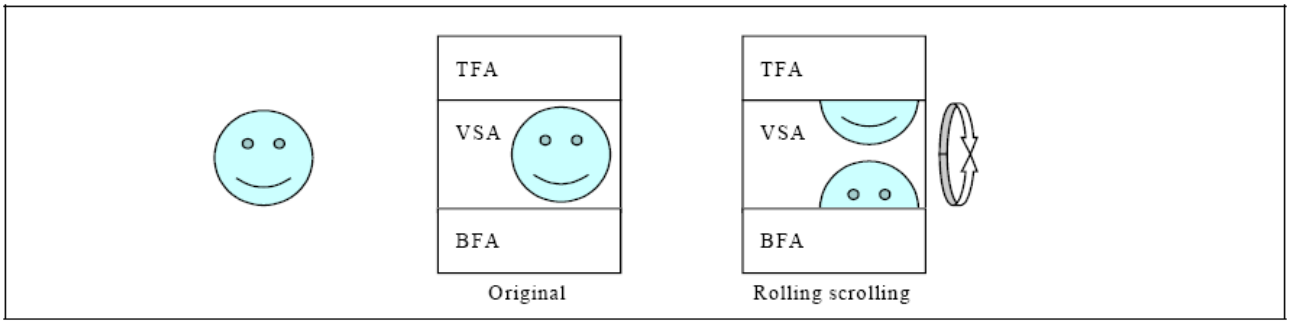
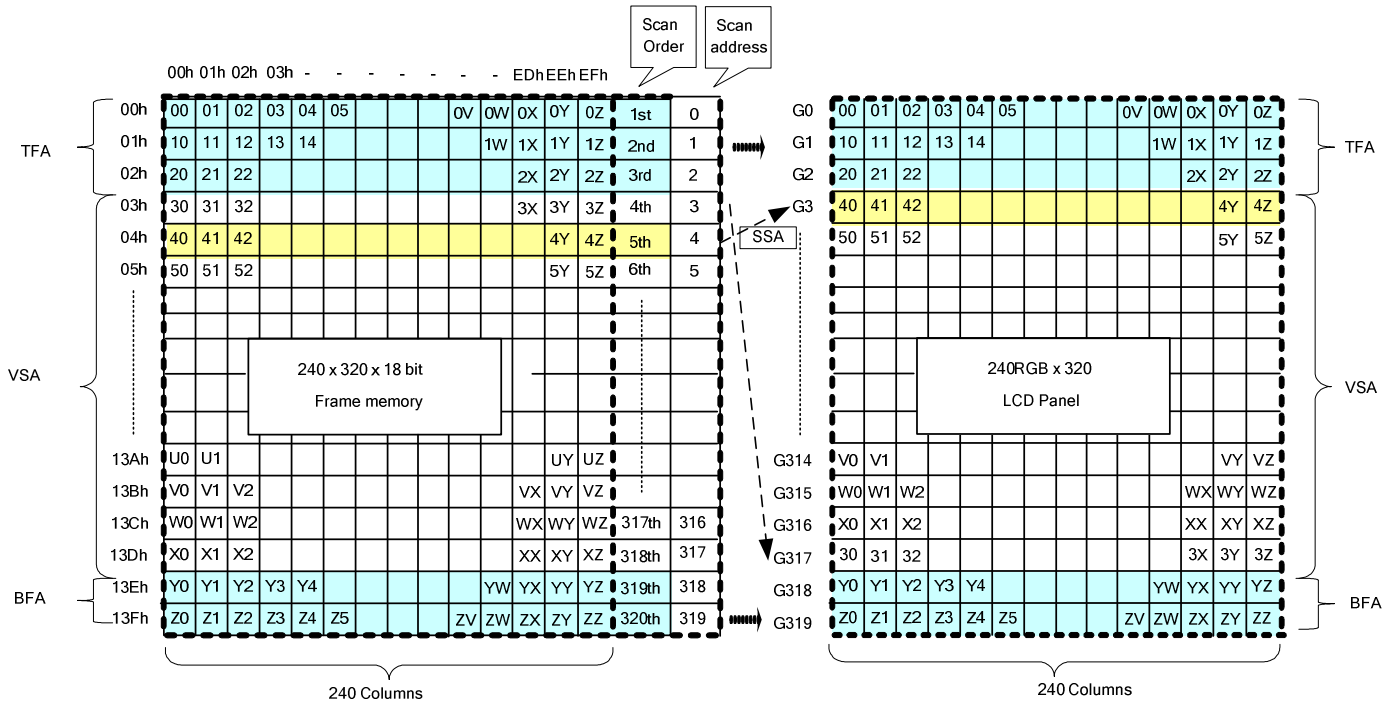


Figure 34 Rolling Scroll Definition

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) =320. In this case, ‘rolling’ scrolling is applied as shown below. All the memory contents will be used.

Example1) Panel size=240 x 320, TFA =3, VSA=315, BFA=2, SSA=4, MADCTR ML=0: Rolling Scroll



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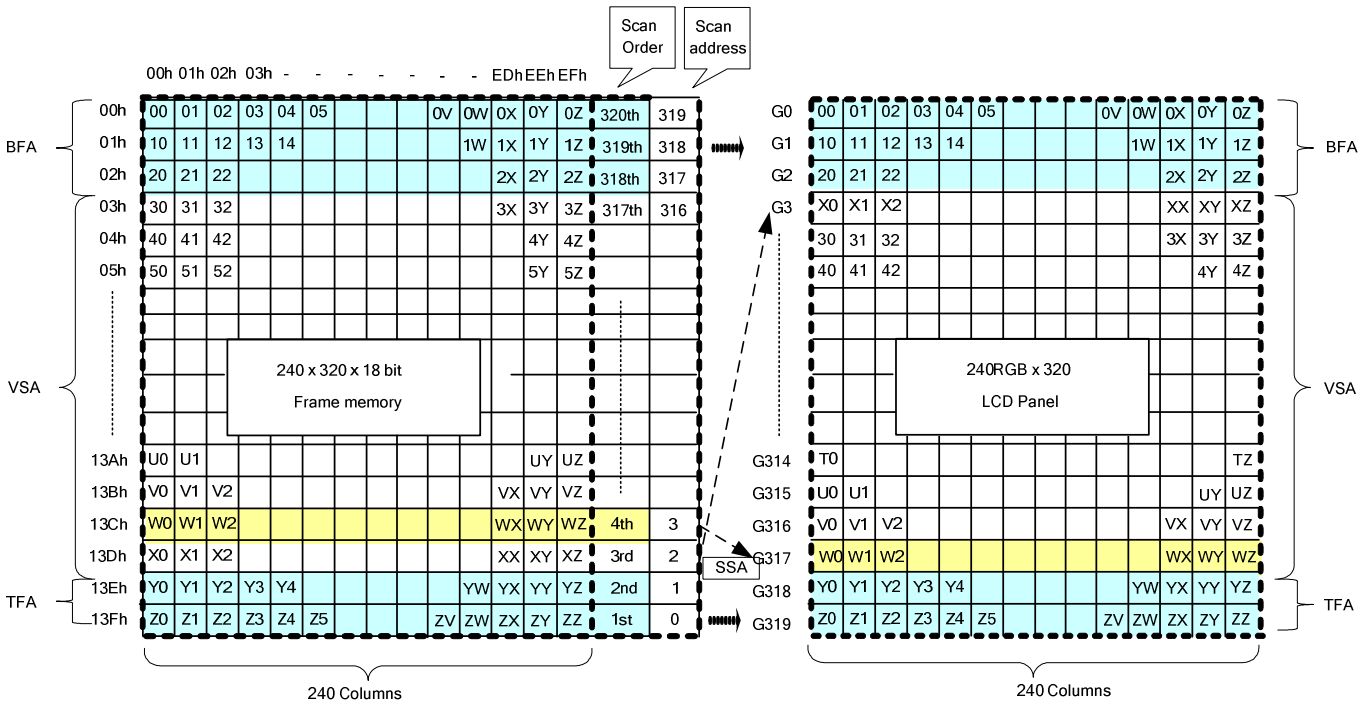
Example2) Panel size=132 x 132, TFA =2, VSA=315, BFA=3, SSA=4, MADCTR ML=1: Rolling Scroll (TFA and BFA are exchanged)



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8.14.2 Vertical Scroll Example

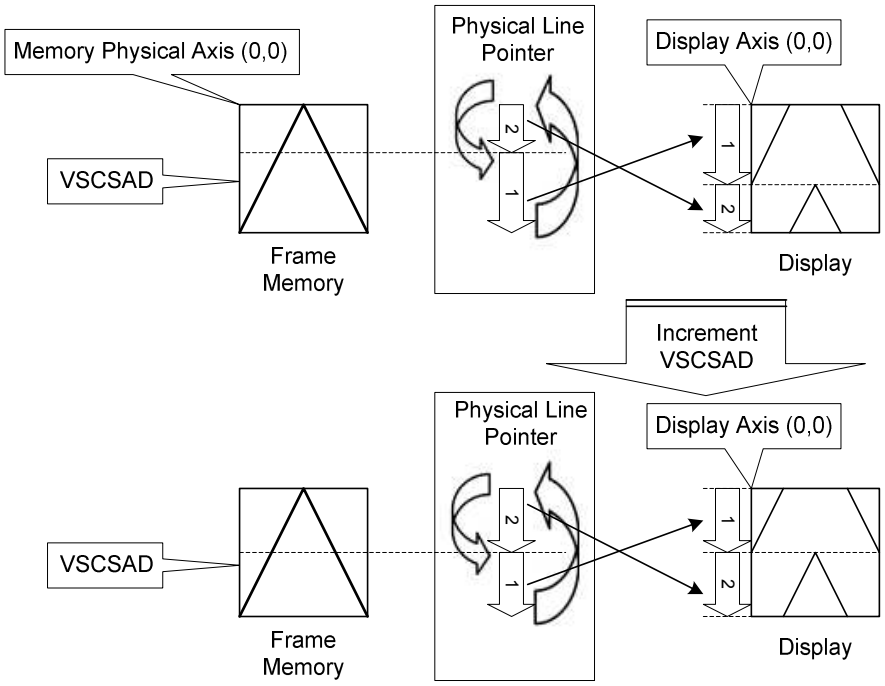
There are 2 types of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

Case 1: TFA + VSA + BFA<320

N/A. Do not set TFA + VSA + BFA<320. In that case, unexpected picture will be shown.

Case 2: TFA + VSA + BFA=320 (Rolling Scrolling)

Example1) When MADCTR parameter ML=”0”, TFA=0, VSA=320, BFA=0 and VSCSAD=40.



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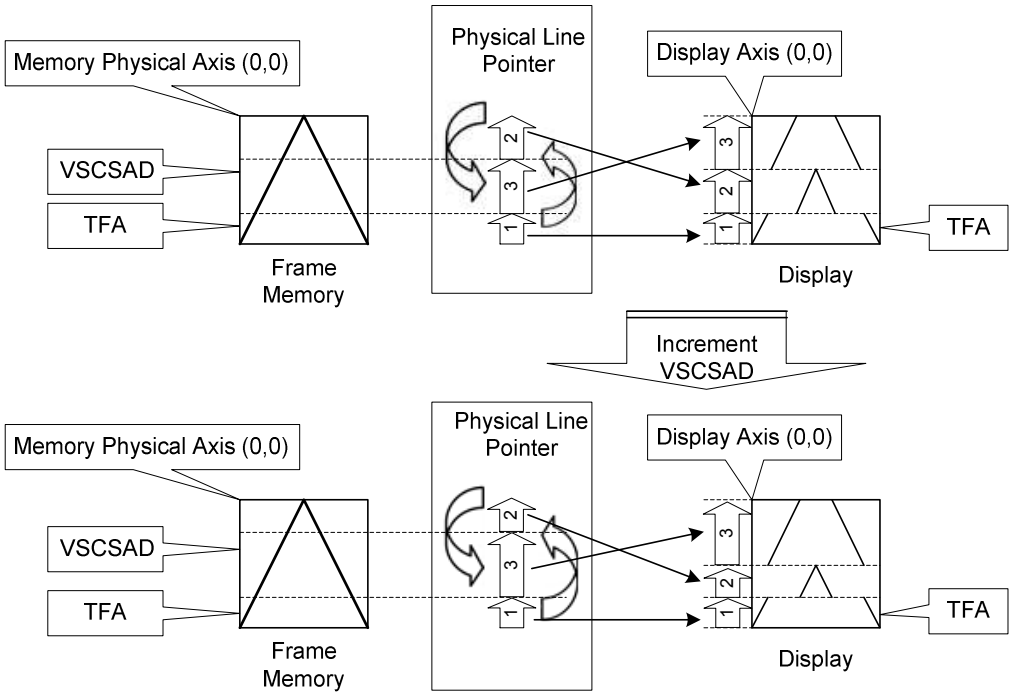
Example2) When MADCTR parameter ML="1", TFA=10, VSA=310, BFA=0 and VSCSAD=30.



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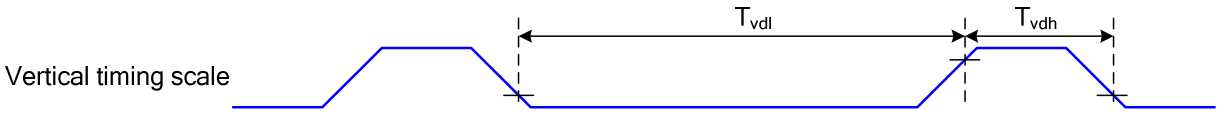
8.15 Tearing Effect

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

8.15.1 Tearing effect line modes

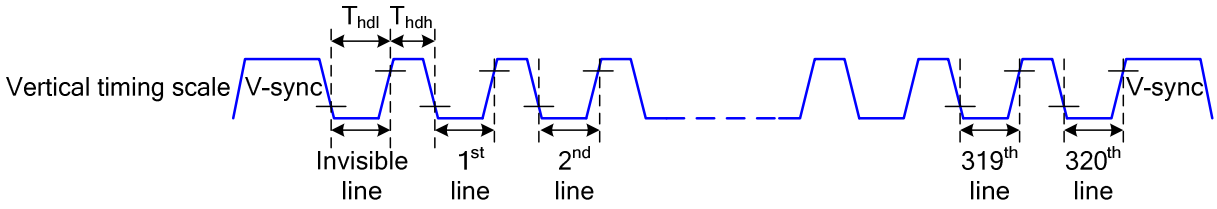
Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:



tvdh= The LCD display is not updated from the Frame Memory

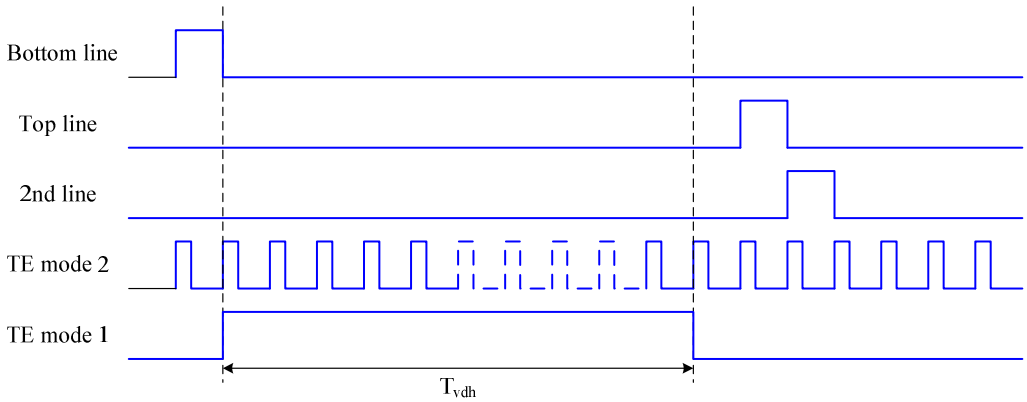
tvdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 320 H-sync pulses per field.



thdh= The LCD display is not updated from the Frame Memory

thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)



Note: During Sleep In Mode, the Tearing Output Pin is active Low.

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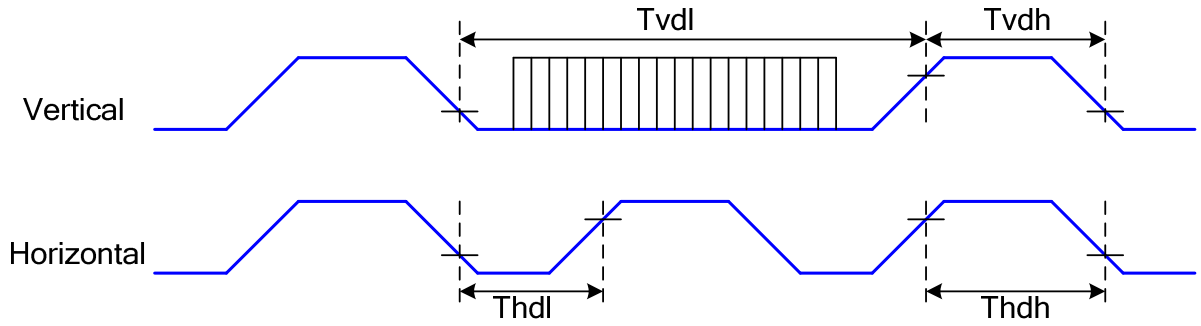
8.15.2 Tearign effect line timings

The Tearing Effect signal is described below:

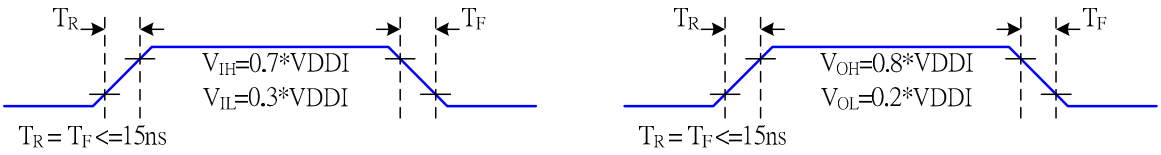


Symbol	Parameter	min	max	unit	description
tvdl	Vertical Timing Low Duration	13	-	ms	
tvdh	Vertical Timing High Duration	1000	-	µs	
thdl	Horizontal Timing Low Duration	33	-	µs	
thdh	Horizontal Timing Low Duration	25	500	µs	

Table 17 AC characteristics of Tearing Effect Signal Idle Mode Off (Frame Rate = 60 Hz, Ta=25°C)

Note: The timings in Table 15 apply when MADCTL ML=0 and ML=1

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

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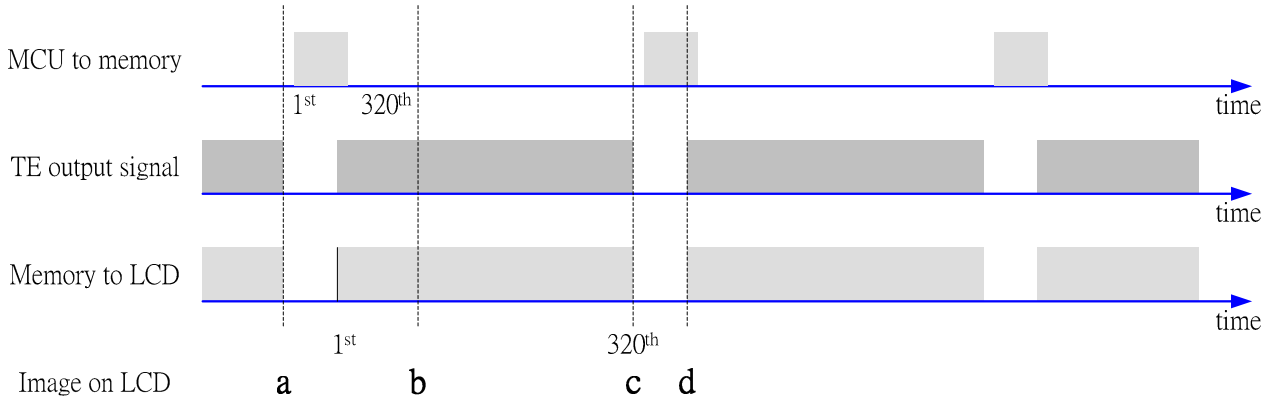
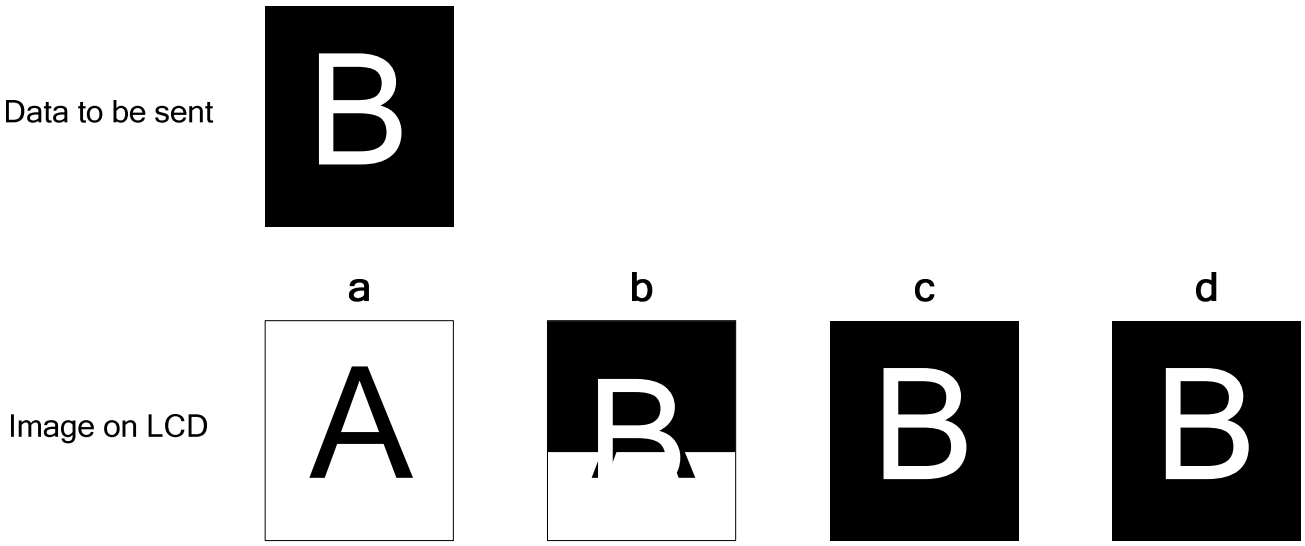
8.15.3 Example 1: MPU Write is faster than panel read



Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



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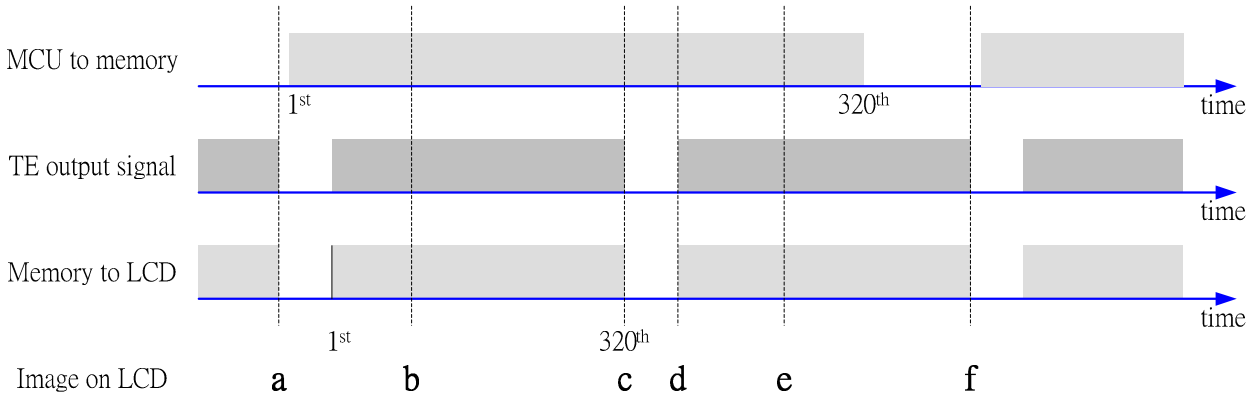
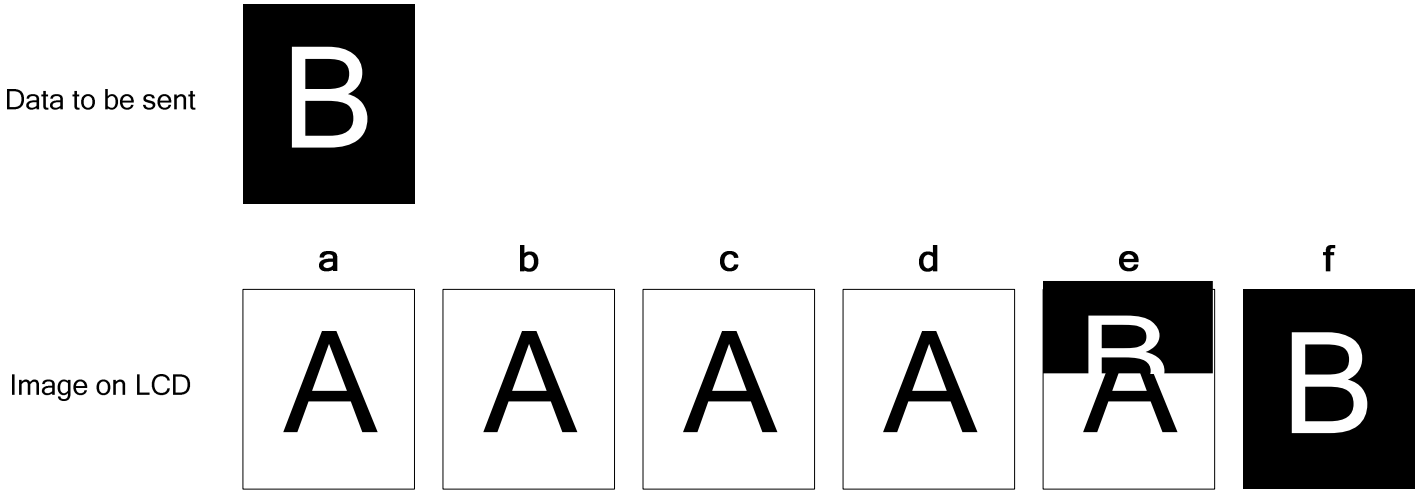
8.15.4 Example 2: MPU write is slower than panel read



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.



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8.16 Power ON/OFF Sequence

VDDI and VDD can be applied in any order.

VDD and VDDI can be power down in any order.

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

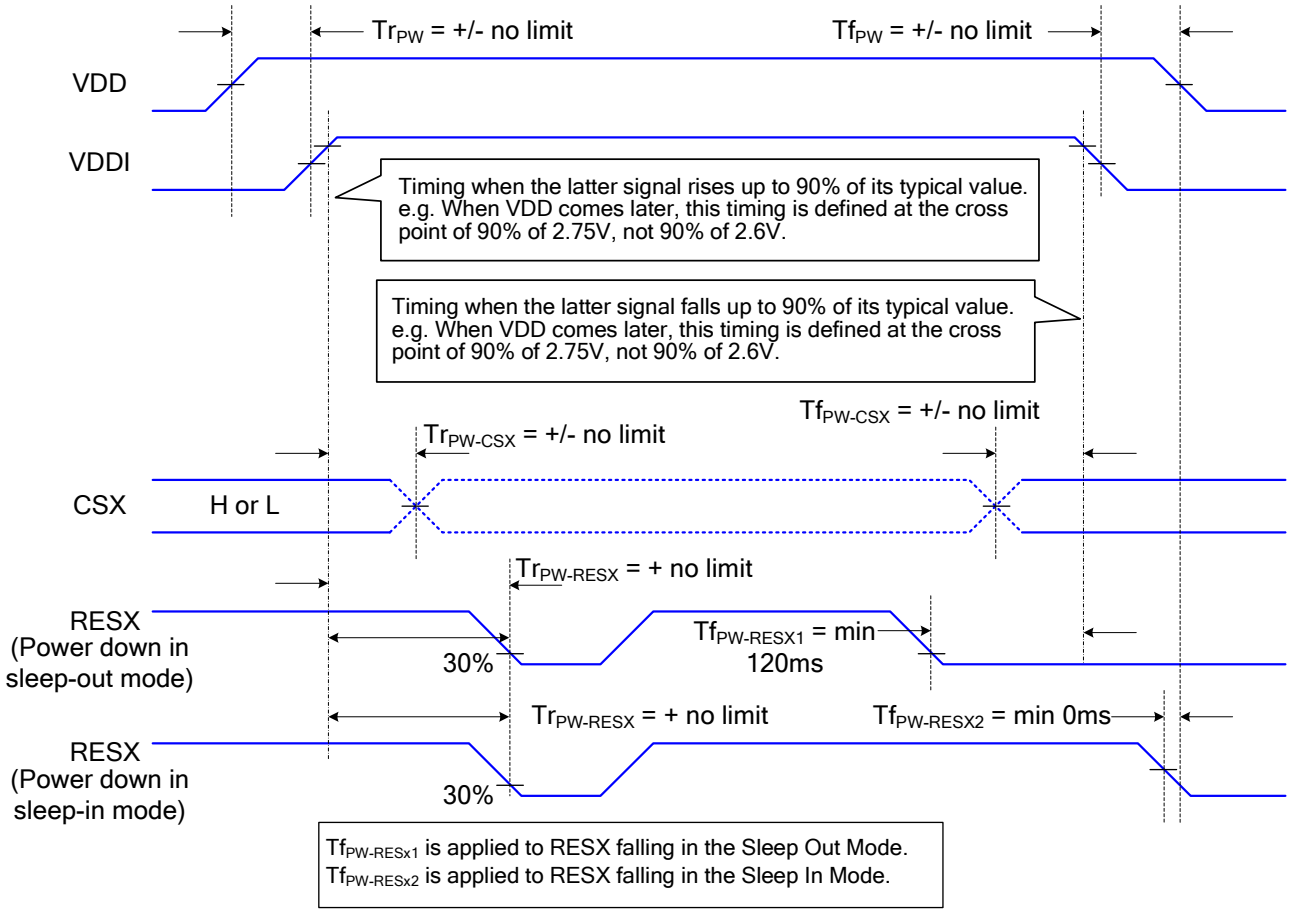
Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below



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8.16.1 Uncontrolled Power Off

The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface.

If uncontrolled power-off happened, the display will go blank and there will not any visible effect on the display (blank display) and remains blank until “Power On Sequence” powers it up.

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8.17 Power Level Definition

8.17.1 Power Level

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
In this mode, the display is able to show maximum 262,144 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out.
In this mode part of the display is used with maximum 262,144 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.
In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out.
In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode
In this mode, the DC: DC converter, internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

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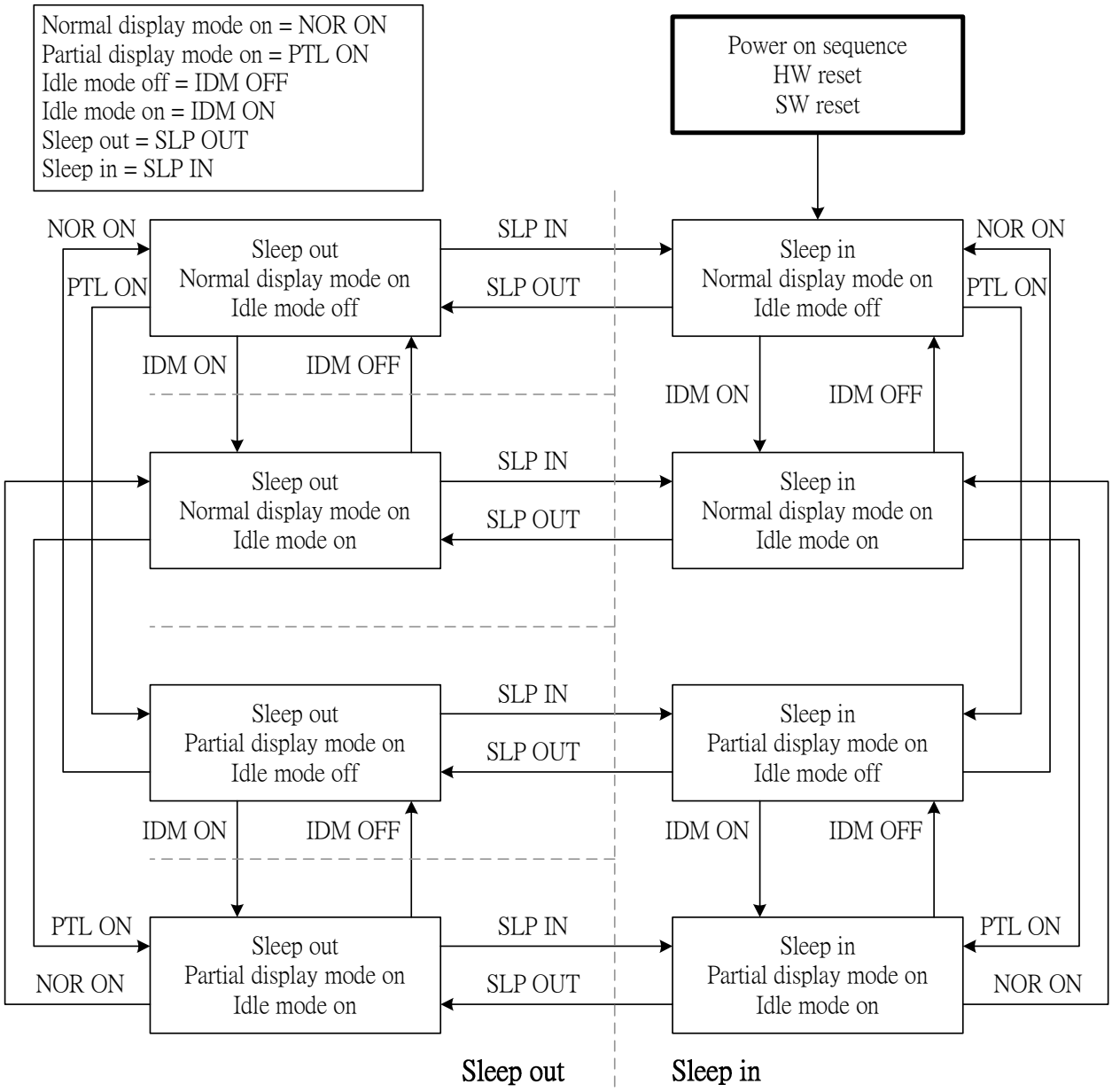
8.18 Power Flow Chart



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8.19 Gamma Correction

ST7789VW incorporate the gamma correction function to display 262,244 colors for the LCD panel. The gamma correction is performed with 3 groups of registers, which are gradient adjustment, contrast adjustment and fine- adjustment registers for positive and negative polarities, and RGB can be adjusted individually.

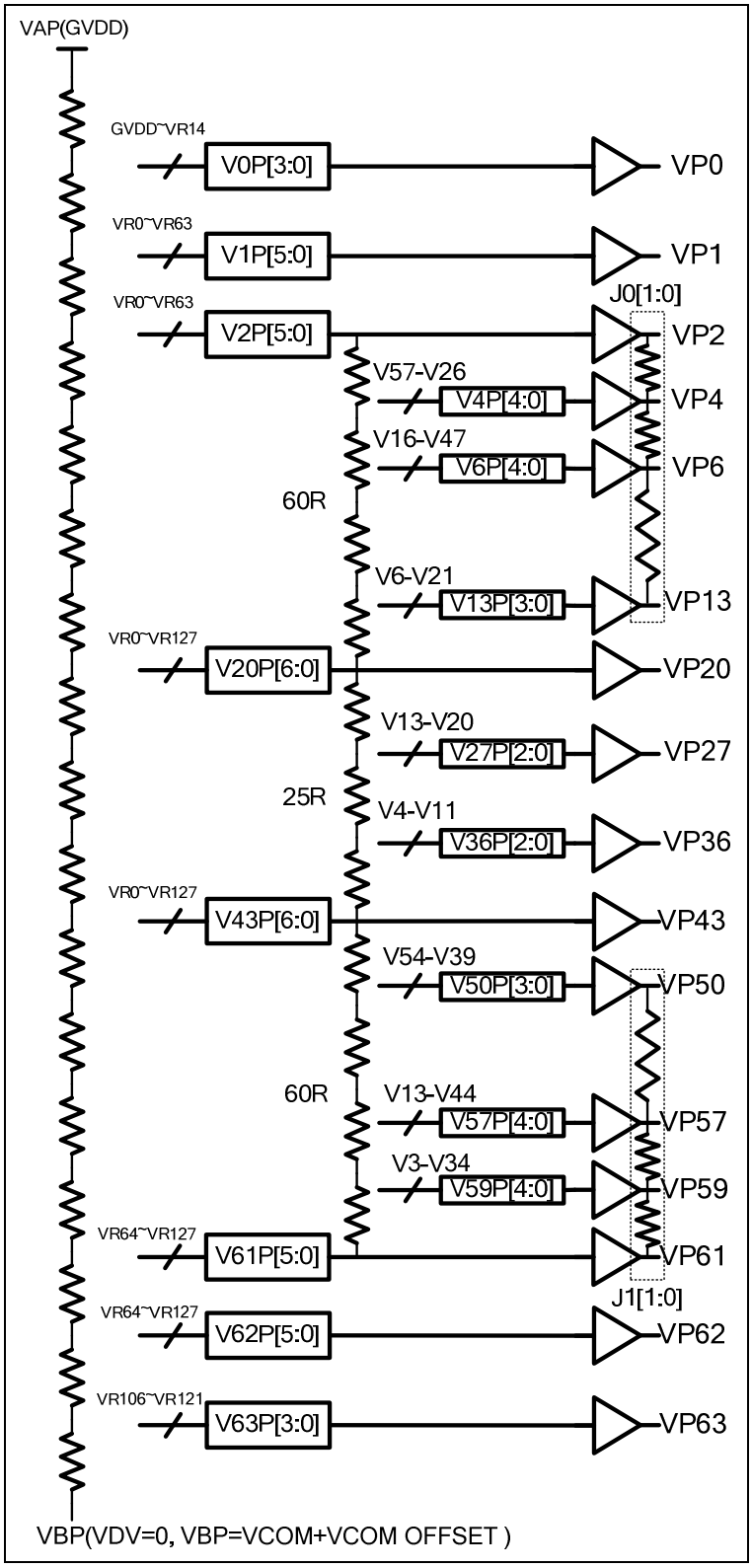

Figure 35 Gray scale Voltage Generation (Positive)

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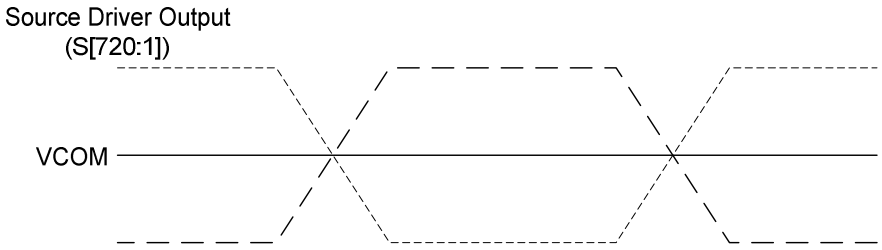

Figure 36 Relationship between Source Output and VCOM

Percentage adjustment:

J0P[1:0], J1P[1:0], J0N[1:0], J1N[1:0] these register are used to adjust the voltage level of interpolation point. The following table is the detail description.

J0P[1:0]/J0N[1:0]:

	00h	01h	02h	03h
VP3/VN3	50%	56%	50%	60%
VP5/VN5	50%	44%	50%	42%
VP7/VN7	86%	71%	80%	66%
VP8/VN8	71%	57%	63%	49%
VP9/VN9	57%	40%	49%	34%
VP10/VN10	43%	29%	34%	23%
VP11/VN11	29%	17%	20%	14%
VP12/VN12	14%	6%	9%	6%

J1P[1:0]/J1N[1:0]:

	00h	01h	02h	03h
VP51/VN51	86%	86%	86%	89%
VP52/VN52	71%	71%	77%	80%
VP53/VN53	57%	60%	63%	69%
VP54/VN54	43%	46%	46%	51%
VP55/VN55	29%	34%	31%	37%
VP56/VN56	14%	17%	14%	20%
VP58/VN58	50%	56%	47%	47%
VP60/VN60	50%	50%	50%	53%

Table 18 voltage level percentage adjustment description

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Source voltage of positive gamma level

Gamma level	Related Register	Formula
VP0	V0P[3:0]	(VAP-VBP)*(129R-V0P[3:0]R)/129R+VBP
VP1	V1P[5:0]	(VAP-VBP)*(128R-V1P[5:0]R)/129R+VBP
VP2	V2P[5:0]	(VAP-VBP)*(128R-V2P[5:0]R)/129R+VBP
VP3	J0P[1:0]	(VP2-VP4)*J0P[1:0]+VP4
VP4	V4P[4:0]	(VP2-VP20)*(57R-V4P[4:0])/60R+VP20
VP5	J0P[1:0]	(VP4-VP6)*J0P[1:0]+VP6
VP6	V6P[4:0]	(VP2-VP20)*(47R-V6P[4:0])/60R+VP20
VP7	J0P[1:0]	(VP6-VP13)*J0P[1:0]+VP13
VP8	J0P[1:0]	(VP6-VP13)*J0P[1:0]+VP13
VP9	J0P[1:0]	(VP6-VP13)*J0P[1:0]+VP13
VP10	J0P[1:0]	(VP6-VP13)*J0P[1:0]+VP13
VP11	J0P[1:0]	(VP6-VP13)*J0P[1:0]+VP13
VP12	J0P[1:0]	(VP6-VP13)*J0P[1:0]+VP13
VP13	V13P[3:0]	(VP2-VP20)*(21R-V13P[3:0])/60R+VP20
VP14	--	(VP13-VP20)/(20-13)*(20-14)+VP20
VP15	--	(VP13-VP20)/(20-13)*(20-15)+VP20
VP16	--	(VP13-VP20)/(20-13)*(20-16)+VP20
VP17	--	(VP13-VP20)/(20-13)*(20-17)+VP20
VP18	--	(VP13-VP20)/(20-13)*(20-18)+VP20
VP19	--	(VP13-VP20)/(20-13)*(20-19)+VP20
VP20	V20P[6:0]	(VAP-VBP)*(128R-V20P[6:0]R)/129R+VBP
VP21	--	(VP20-VP27)/(27-20)*(27-21)+VP27
VP22	--	(VP20-VP27)/(27-20)*(27-22)+VP27
VP23	--	(VP20-VP27)/(27-20)*(27-23)+VP27
VP24	--	(VP20-VP27)/(27-20)*(27-24)+VP27
VP25	--	(VP20-VP27)/(27-20)*(27-25)+VP27
VP26	--	(VP20-VP27)/(27-20)*(27-26)+VP27
VP27	V27P[2:0]	(VP20-VP43)*(20R-V27P[2:0])/25R+VP43
VP28	--	(VP27-VP36)/(36-27)*(36-28)+VP36
VP29	--	(VP27-VP36)/(36-27)*(36-29)+VP36
VP30	--	(VP27-VP36)/(36-27)*(36-30)+VP36
VP31	--	(VP27-VP36)/(36-27)*(36-31)+VP36
VP32	--	(VP27-VP36)/(36-27)*(36-32)+VP36
VP33	--	(VP27-VP36)/(36-27)*(36-33)+VP36
VP34	--	(VP27-VP36)/(36-27)*(36-34)+VP36
VP35	--	(VP27-VP36)/(36-27)*(36-35)+VP36
VP36	V36P[2:0]	(VP20-VP43)*(11R-V36P[2:0])/25R+VP43
VP37	--	(VP36-VP43)/(43-36)*(43-37)+VP43
VP38	--	(VP36-VP43)/(43-36)*(43-38)+VP43
VP39	--	(VP36-VP43)/(43-36)*(43-39)+VP43
VP40	--	(VP36-VP43)/(43-36)*(43-40)+VP43
VP41	--	(VP36-VP43)/(43-36)*(43-41)+VP43
VP42	--	(VP36-VP43)/(43-36)*(43-42)+VP43
VP43	V43P[6:0]	(VAP-VBP)*(128R-V43P[6:0]R)/129R+VBP
VP44	--	(VP43-VP50)/(50-43)*(50-44)+VP50
VP45	--	(VP43-VP50)/(50-43)*(50-45)+VP50
VP46	--	(VP43-VP50)/(50-43)*(50-46)+VP50
VP47	--	(VP43-VP50)/(50-43)*(50-47)+VP50
VP48	--	(VP43-VP50)/(50-43)*(50-48)+VP50
VP49	--	(VP43-VP50)/(50-43)*(50-49)+VP50
VP50	V50P[3:0]	(VP43-VP61)*(54R-V50P[3:0])/60R+VP61
VP51	J1P[1:0]	(V5P0-VP57)*J1P[1:0]+VP57

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VP52	J1P[1:0]	(VP50-VP57)*J1P[1:0]+VP57
VP53	J1P[1:0]	(VP50-VP57)*J1P[1:0]+VP57
VP54	J1P[1:0]	(VP50-VP57)*J1P[1:0]+VP57
VP55	J1P[1:0]	(VP50-VP57)*J1P[1:0]+VP57
VP56	J1P[1:0]	(VP50-VP57)*J1P[1:0]+VP57
VP57	V57P[4:0]	(VP43-VP61)*(44R-V57P[4:0])/60R+VP61
VP58	J1P[1:0]	(VP57-VP59)*J1P[1:0]+VP59
VP59	V59P[4:0]	(VP43-VP61)*(34R-V59P[4:0])/60R+VP61
VP60	J1P[1:0]	(VP59-VP61)*J1P[1:0]+VP61
VP61	V61P[5:0]	(VAP-VBP)*(64R-V61P[5:0]R)/129R+VBP
VP62	V62P[5:0]	(VAP-VBP)*(64R-V62P[5:0]R)/129R+VBP
VP63	V63P[3:0]	(VAP-VBP)*(23R-V63P[3:0]R)/129R+VBP

Source voltage of negative gamma level

Gamma level	Related Register	Formula
VN0	V0N[3:0]	VBN-(VBN-VAN)*(129R-V0N[3:0]R)/129R
VN1	V1N[5:0]	VBN-(VBN-VAN)*(128R-V1N[5:0]R)/129R
VN2	V2N[5:0]	VBN-(VBN-VAN)*(128R-V2N[5:0]R)/129R
VN3	J0N[1:0]	(VN2-VN4)*J0N[1:0]+VN4
VN4	V4N[4:0]	(VN2-VN20)*(57R-V4N[4:0])/60R+VN20
VN5	J0N[1:0]	(VN4-VN6)*J0N[1:0]+VN6
VN6	V6N[4:0]	(VN2-VN20)*(47R-V6N[4:0])/60R+VN20
VN7	J0N[1:0]	(VN6-VN13)*J0N[1:0]+VN13
VN8	J0N[1:0]	(VN6-VN13)*J0N[1:0]+VN13
VN9	J0N[1:0]	(VN6-VN13)*J0N[1:0]+VN13
VN10	J0N[1:0]	(VN6-VN13)*J0N[1:0]+VN13
VN11	J0N[1:0]	(VN6-VN13)*J0N[1:0]+VN13
VN12	J0N[1:0]	(VN6-VN13)*J0N[1:0]+VN13
VN13	V13N[3:0]	(VN2-VN20)*(21R-V13N[3:0])/60R+VN20
VN14	--	(VN13-VN20)/(20-13)*(20-14)+VN20
VN15	--	(VN13-VN20)/(20-13)*(20-15)+VN20
VN16	--	(VN13-VN20)/(20-13)*(20-16)+VN20
VN17	--	(VN13-VN20)/(20-13)*(20-17)+VN20
VN18	--	(VN13-VN20)/(20-13)*(20-18)+VN20
VN19	--	(VN13-VN20)/(20-13)*(20-19)+VN20
VN20	V20N[6:0]	VBN-(VBN-VAN)*(128R-V20N[6:0]R)/129R
VN21	--	(VN20-VN27)/(27-20)*(27-21)+VN27
VN22	--	(VN20-VN27)/(27-20)*(27-22)+VN27
VN23	--	(VN20-VN27)/(27-20)*(27-23)+VN27
VN24	--	(VN20-VN27)/(27-20)*(27-24)+VN27
VN25	--	(VN20-VN27)/(27-20)*(27-25)+VN27
VN26	--	(VN20-VN27)/(27-20)*(27-26)+VN27
VN27	V27N[2:0]	(VN20-VN43)*(20R-V27N[2:0])/25R+VN43
VN28	--	(VN27-VN36)/(36-27)*(36-28)+VN36
VN29	--	(VN27-VN36)/(36-27)*(36-29)+VN36
VN30	--	(VN27-VN36)/(36-27)*(36-30)+VN36
VN31	--	(VN27-VN36)/(36-27)*(36-31)+VN36
VN32	--	(VN27-VN36)/(36-27)*(36-32)+VN36
VN33	--	(VN27-VN36)/(36-27)*(36-33)+VN36
VN34	--	(VN27-VN36)/(36-27)*(36-34)+VN36
VN35	--	(VN27-VN36)/(36-27)*(36-35)+VN36
VN36	V36N[2:0]	(VN20-VN43)*(11R-V36N[2:0])/25R+VN43
VN37	--	(VN36-VN43)/(43-36)*(43-37)+VN43

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VN38	--	(VN36-VN43)/(43-36)*(43-38)+VN43
VN39	--	(VN36-VN43)/(43-36)*(43-39)+VN43
VN40	--	(VN36-VN43)/(43-36)*(43-40)+VN43
VN41	--	(VN36-VN43)/(43-36)*(43-41)+VN43
VN42	--	(VN36-VN43)/(43-36)*(43-42)+VN43
VN43	V43N[6:0]	VBN-(VBN-VAN)*(128R-V43N[6:0]R)/129R
VN44	--	(VN43-VN50)/(50-43)*(50-44)+VN50
VN45	--	(VN43-VN50)/(50-43)*(50-45)+VN50
VN46	--	(VN43-VN50)/(50-43)*(50-46)+VN50
VN47	--	(VN43-VN50)/(50-43)*(50-47)+VN50
VN48	--	(VN43-VN50)/(50-43)*(50-48)+VN50
VN49	--	(VN43-VN50)/(50-43)*(50-49)+VN50
VN50	V50N[3:0]	(VN43-VN61)*(54R-V50N[3:0])/60R+VN61
VN51	J1N[1:0]	(V5N0-VN57)*J1N[1:0]+VN57
VN52	J1N[1:0]	(VN50-VN57)*J1N[1:0]+VN57
VN53	J1N[1:0]	(VN50-VN57)*J1N[1:0]+VN57
VN54	J1N[1:0]	(VN50-VN57)*J1N[1:0]+VN57
VN55	J1N[1:0]	(VN50-VN57)*J1N[1:0]+VN57
VN56	J1N[1:0]	(VN50-VN57)*J1N[1:0]+VN57
VN57	V57N[4:0]	(VN43-VN61)*(44R-V57N[4:0])/60R+VN61
VN58	J1N[1:0]	(VN57-VN59)*J1N[1:0]+VN59
VN59	V59N[4:0]	(VN43-VN61)*(34R-V59N[4:0])/60R+VN61
VN60	J1N[1:0]	(VN59-VN61)*J1N[1:0]+VN61
VN61	V61N[5:0]	VBN-(VBN-VAN)*(64R-V61N[5:0]R)/129R
VN62	V62N[5:0]	VBN-(VBN-VAN)*(64R-V62N[5:0]R)/129R
VN63	V63N[3:0]	VBN-(VBN-VAN)*(23R-V63N[3:0]R)/129R

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8.20 Gray voltage generator for digital gamma correction

ST7789VW digital gamma function can implement the RGB gamma correction independently. ST7789VW utilizes look-up table of digital gamma to change ram data, and then display the changed data from source driver. The following diagram shows the data flow of digital gamma.

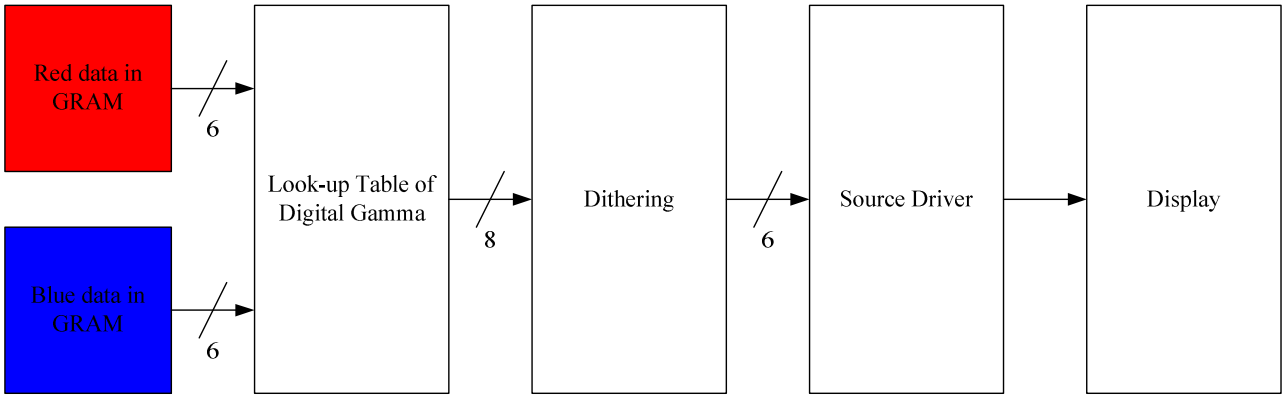

Figure 37 Block diagram of digital gamma

There are 2 registers and each register has 64 bytes to set R, G, B gamma independently. When bit DGMEN be set to 1, R and B gamma will be mapped via look-up table of digital gamma to gray level voltage.

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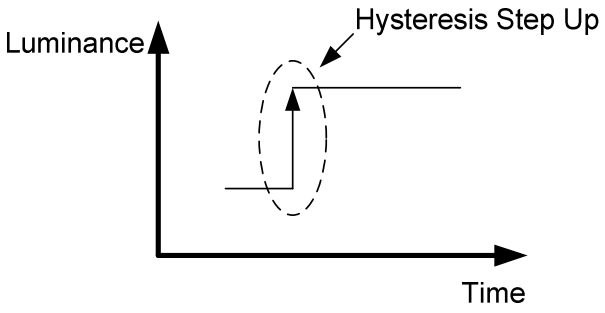
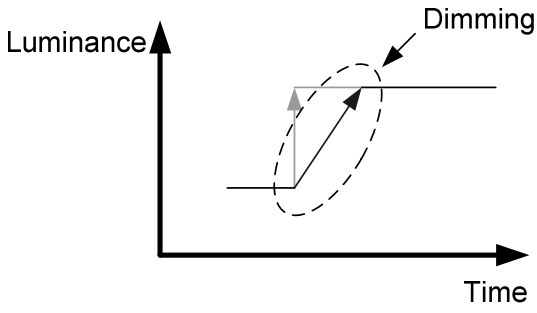
8.21 Display Dimming

8.21.1 General Description

A dimming function (how fast to change the brightness from old to new level and what are brightness levels during the change) is used when changing from one brightness level to another. This dimming function curve is the same in increment and decrement. The basic idea is described below.



Without Dimming



With Dimming

Dimming function can be enable and disable. See “Write CTRL Display (53h)” (bit DD) for more information.

8.21.2 Dimming Requirement

Dimming function in the display module should be implemented so that 400-600ms is used for the transition between the original brightness value and the target brightness value. The transferring time steps between these two brightness values are equal making the transition linear.

The dimming function is working similarly in both upward and downward directions.

An upward example is illustrate below

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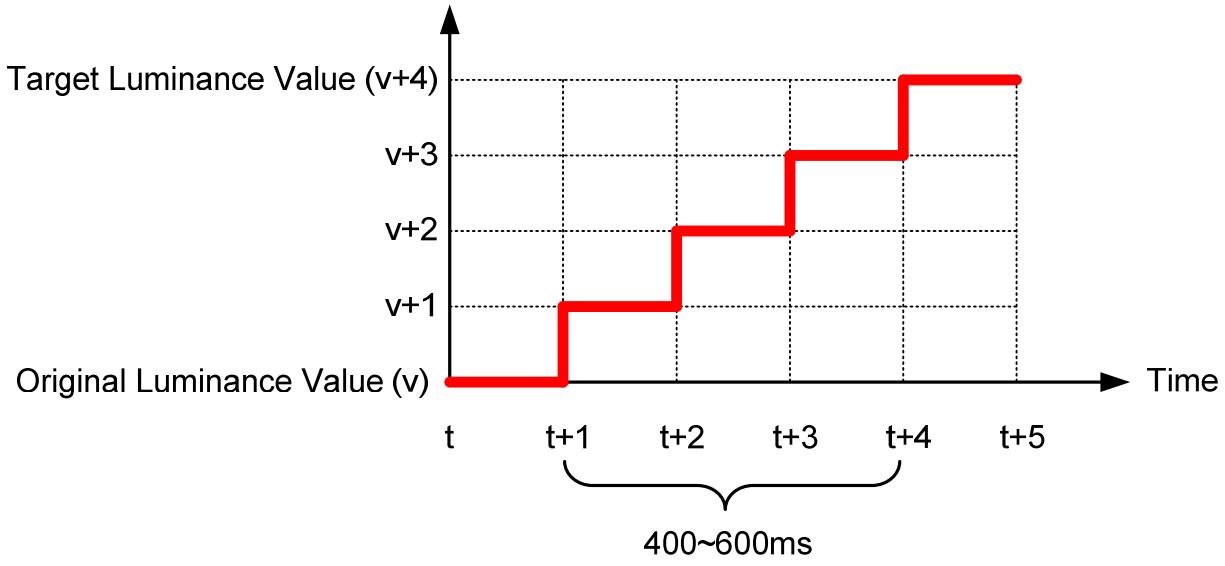

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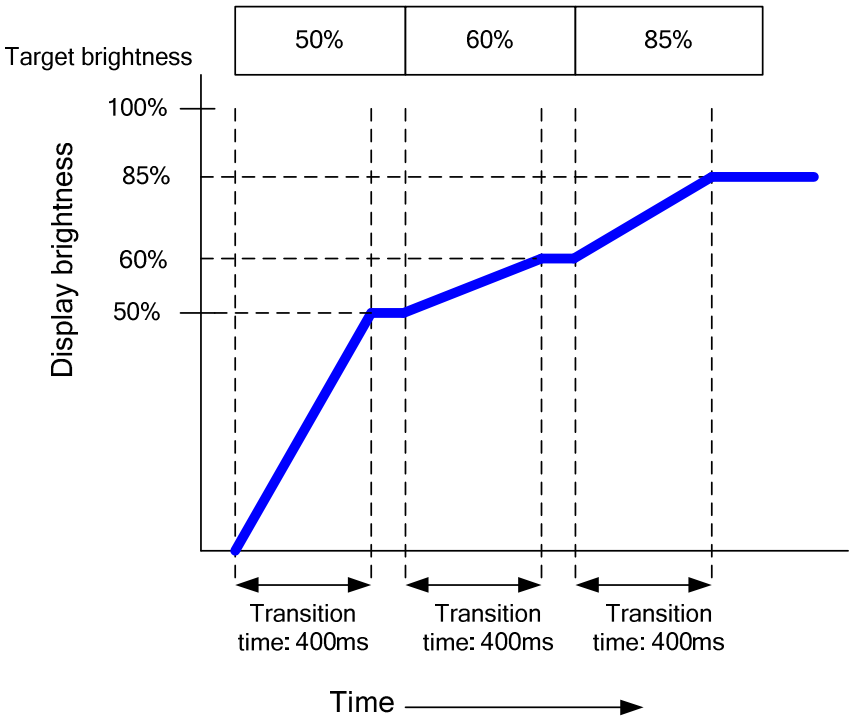
8.21.3 Definition of brightness transition time

- Shorter transition time than 500ms.

  There is some stable time between transitions. Below drawing is for transition time: 400ms.



- Longer transition time than 500ms

  There is no any stable time between transitions. Below drawing is for transition time: 600ms.

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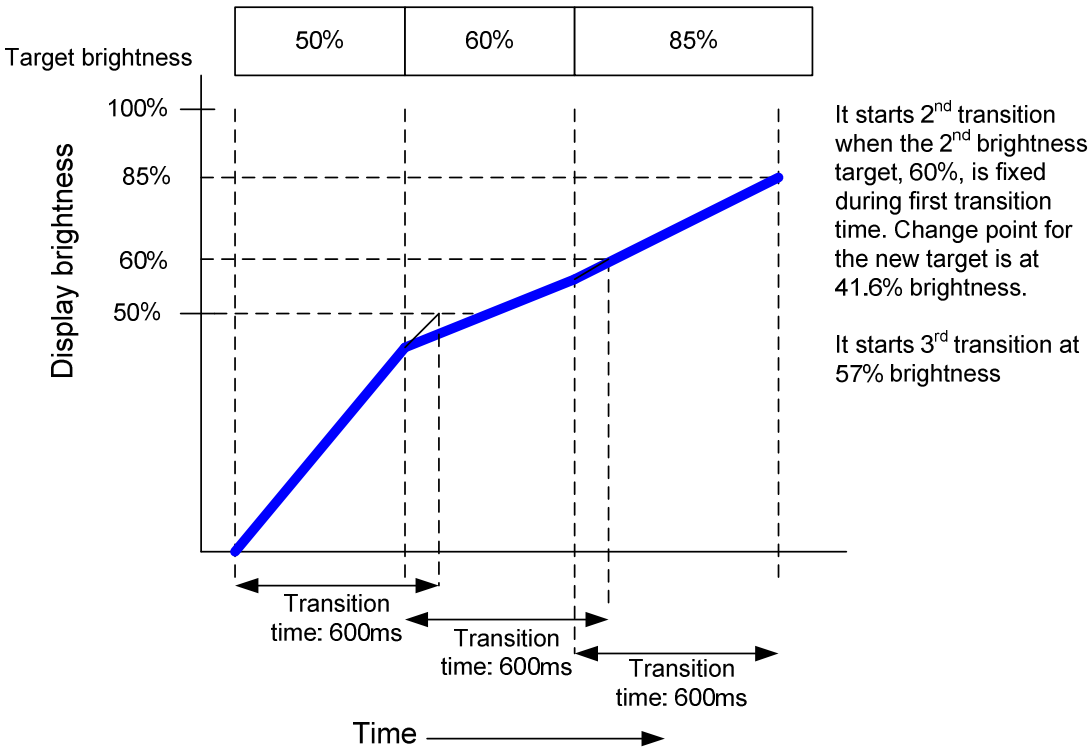

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8.22 Content Adaptive Brightness Control (CABC)

8.22.1 Definition of CABC

A Content Adaptive Brightness Control function can be used to reduce the power consumption of the luminance source. Content adaptation means that content gray level scale can be increased while simultaneously lowering brightness of the backlight to achieve same perceived brightness. The adjusted gray level scale and thus the power consumption reduction

Definition of Modes and target power reduction ratio:

- Off mode: Content Adaptive Brightness Control functionality is totally off.
- UI [User interface] image mode: Optimized for UI image. It is kept image quality as much as possible. Target power consumption reduction ratio: 10% or less.
- Still picture mode: Optimized for still picture. Some image quality degradation would be acceptable. Target power consumption reduction ratio: more than 30%.
- Moving image mode: Optimized for moving image. It is focused on the biggest power reduction with image quality degradation. Target power consumption reduction ratio: more than 30%.

Note 1: Updating partial area of the image data should be supported by CABC functionality.
Note 2: Processing power consumption of CABC should be minimized.
Note 3: Customer need program OTP GAMMA when using CABC.

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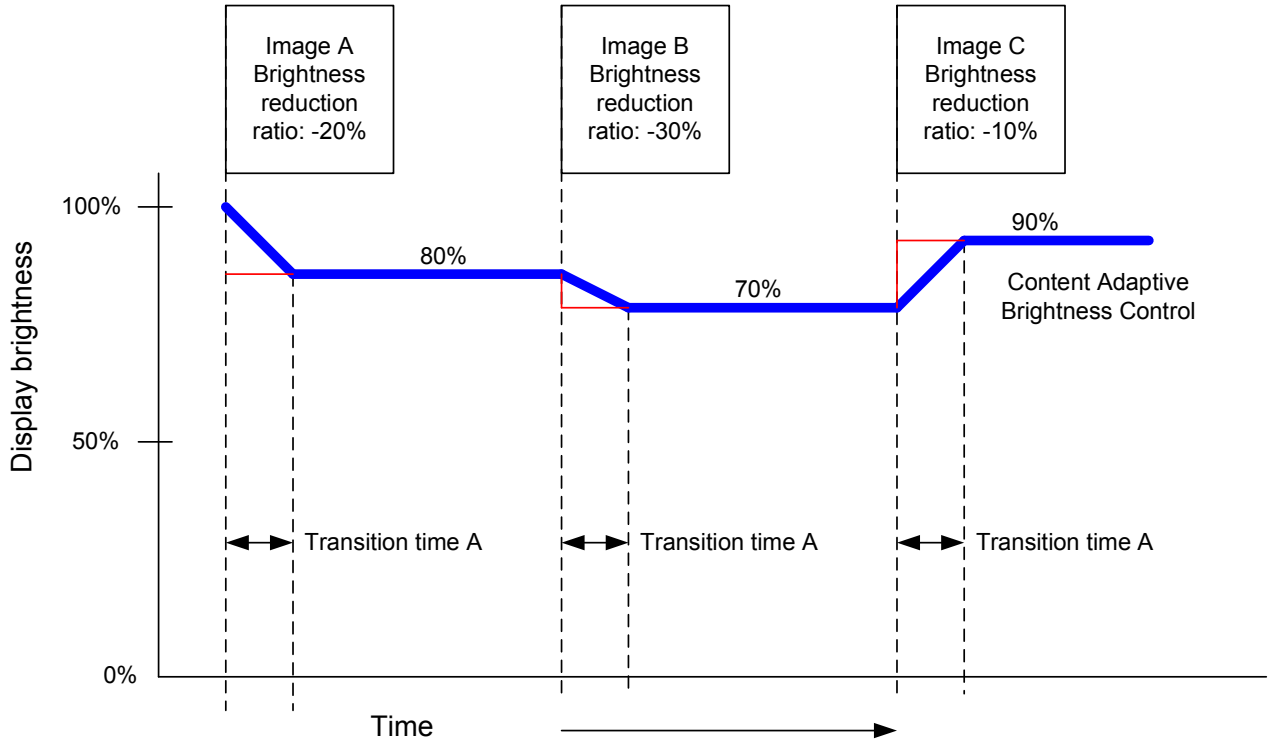
The transition time for dimming function is illustrated below.

- Content Adaptive Brightness Control

Display brightness is changed, according to the image contents. The following graph mentions the case of displaying three different images.

- Image A: -20% brightness reduction
- Image B: -30% brightness reduction
- Image C: -30% brightness reduction

Transition time from the previous image to the current displayed image is “transition time A”.



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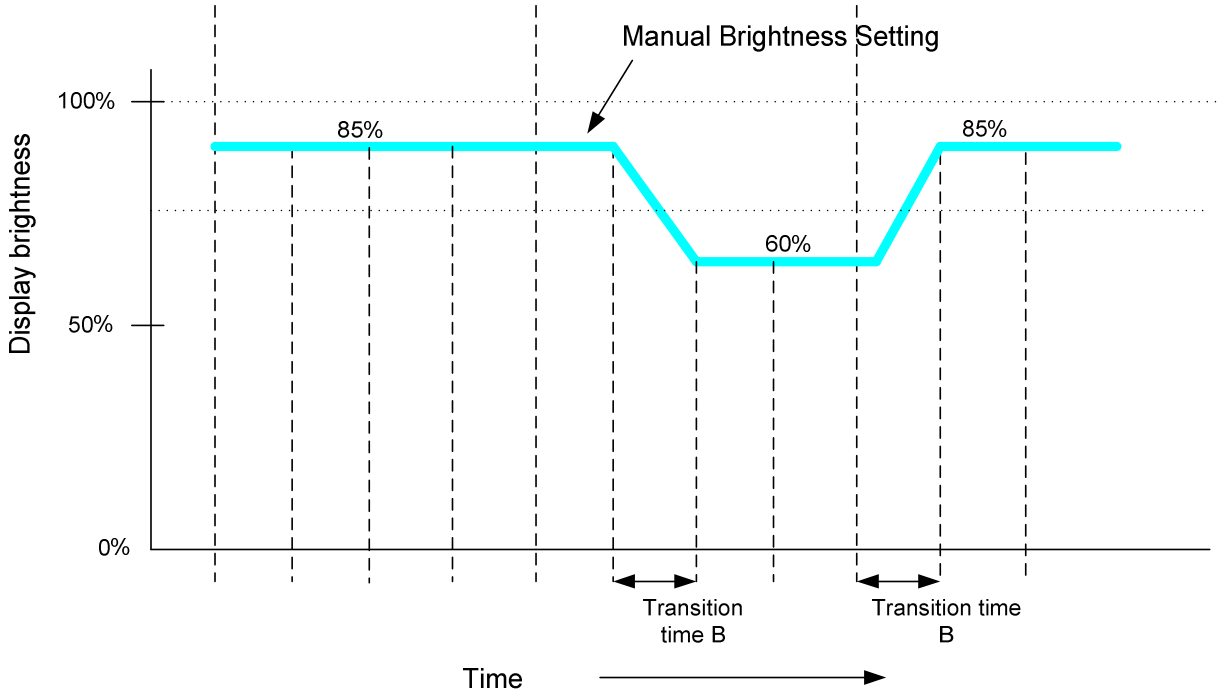
- Manual brightness setting and Dimming function



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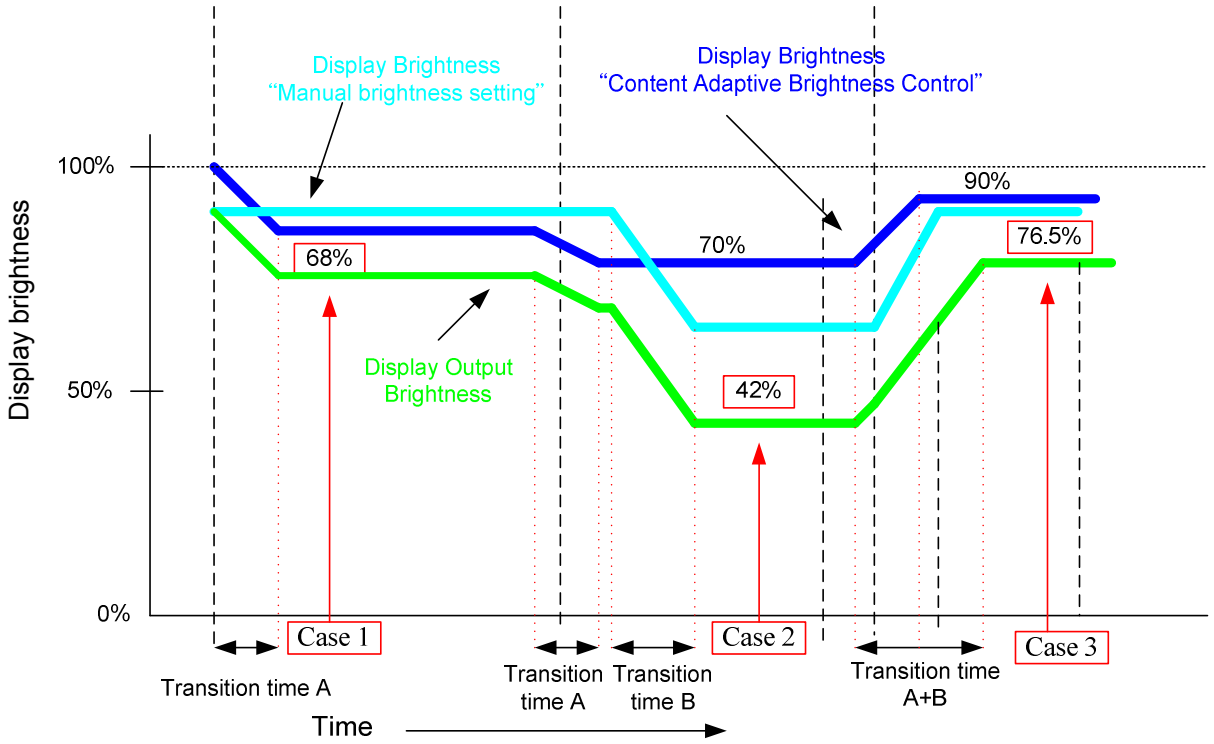
- Combine Display brightness

Green line in the following graph is for the output brightness of display. It is combined with both display brightness, which are defined in the above graphs.

Maximum transition time is transition time A+B.



Brightness level calculates with the following formula.

Display Output brightness = Manual Brightness setting * CABC brightness ratio

	Manual Brightness setting	Brightness ratio [CABC]	Display Output brightness
Case 1	85%	80%	68%
Case 2	60%	70%	42%
Case 3	85%	90%	76.5%

Transition time from the current brightness to target brightness is A+B in the worst case.

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8.22.2 Minimum brightness setting of CABC function

CABC function is automatically reduced backlight brightness based on image contents. In the case of the combination with the LABC or manual brightness setting, display brightness is too dark. It must affect to image quality degradation. CABC minimum brightness setting is to avoid too much brightness reduction. When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. If CABC algorithm works without any abnormal visual effect, image processing function can operate even when the brightness can not be changed.

This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

When display brightness is turned off (BCTRL=0 of “9.1.39 Write CTRL Display (53h)”), CABC minimum brightness setting is ignored. “9.1.44 Read CABC minimum brightness (5Fh)” always read the setting value of “9.1.43 Write CABC minimum brightness (5Eh)”.

	WRCABC (55h)	Function	RDCABCMB (5Fh)	Image
Sleep-in		NA	WRCABCMB (5Eh)	
CABC off	00b	Disable	WRCABCMB (5Eh)	Original
CABC on	01b/10b/11b	Enable	WRCABCMB (5Eh)	CABC modified

Brightness level calculates with the following formula.

Display Output Brightness = Manual brightness setting * CABC brightness ratio

Below drawing is for the explanation of the CABC minimum brightness setting.

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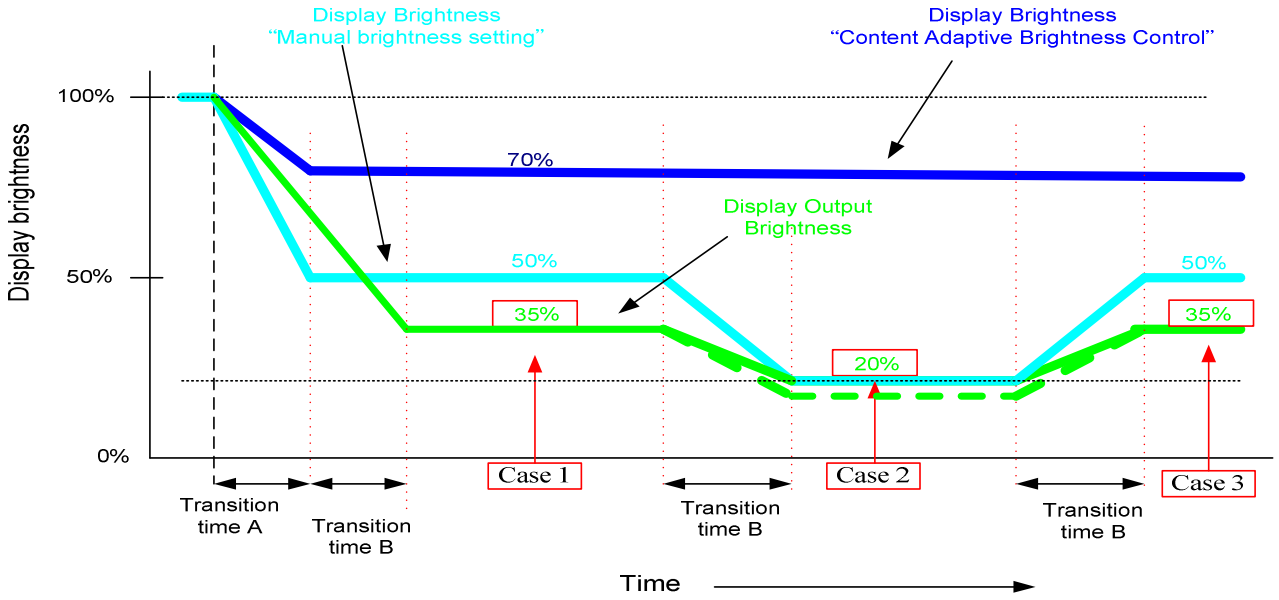

CABC minimum brightness value = 51 (33h: 20% display brightness)

	Display Brightness [manual setting]	Brightness ratio [CABC]	Calculation result of the display brightness formula	Display Output Brightness	Image
Case 1	50%	70%	35%	35%	CABC modified
Case 2	20%	70%	14%	20%	CABC modified
Case 3	50%	70%	35%	35%	CABC modified

At the case 2, the calculation result of the display brightness is 14%. CABC minimum brightness value is set to 20% brightness. Actual display brightness is 20% as the CABC minimum brightness setting.

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9 COMMAND

9.1 System Function Command Table 1

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)	No operation
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)	Software reset
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)	Read display ID
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		ID1 read
	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		ID2 read
	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		ID3 read
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)	Read display status
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24		-
	1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON		-
	1	1	↑	-	ST15	ST14	INVON	ST12	ST11	DISON	TEON	GCS2		-
	1	1	↑	-	GCS1	GCS0	TEM	ST4	ST3	ST2	ST1	ST0		-
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)	Read display power
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	0	0		
RDD MADCTL	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)	Read display
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	MY	MX	MV	ML	RGB	MH	0	0		-
RDD COLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)	Read display pixel
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	0	D6	D5	D4	0	D2	D1	D0		-
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)	Read display image
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	VSSON	0	INVON	0	0	GC2	GC1	GC0		-
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)	Read display signal
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read

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Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	1	↑	-	TEON	TEM	0	0	0	0	0	0		-
RDDSDR	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)	Read display self-diagnostic result
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	D7	D6	0	0	0	0	0	0		-
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)	Sleep in
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)	Sleep out
PTLON	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)	Partial mode on
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)	Partial off (Normal)
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)	Display inversion off
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)	Display inversion on
GAMSET	0	↑	1	-	0	0	1	0	0	0	0	1	(26h)	Display inversion on
	1	↑	1	-	0	0	0	0	GC3	GC2	GC1	GC0		
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)	Display off
DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)	Display on
CASET	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)	Column address set
	1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8		X address start: 0≦XS≦X
	1	↑	1		XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0		
	1	↑	1		XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8		X address start: S≦XE≦X
	1	↑	1		XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0		
RASET	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)	Row address set
	1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8		Y address start: 0≦YS≦Y
	1	↑	1		YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0		
	1	↑	1		YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8		Y address start: S≦YE≦Y
	1	↑	1		YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0		
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)	Memory write
	1	↑	1	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Write data
	1	↑	1	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	↑	1	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
RAMRD	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)	Memory read

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Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Read data
	1	1	↑	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	1	↑	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
PTLAR	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)	Partial sart/end address set
	1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8		Partial start address: (0, 1,2, ..P)
	1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0		
	1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8		Partial end address (0, 1,2, 3, , P)
	1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0		
VSCRDEF	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)	Vertical scrolling definition
	1	↑	1	-	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8		
	1	↑	1	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0		
	1	↑	1	-	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8		
	1	↑	1	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0		
	1	↑	1	-	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8		
	1	↑	1	-	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0		
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)	Tearing effect line off
TEON	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)	Tearing effect line on
	1	↑	1	-	-	-	-	-	-	-	-	TEM		
MADCTL	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)	Memory data access control
	1	↑	1	-	MY	MX	MV	ML	RGB	0	0	0		-
VSCRSADD	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)	Vertical scrolling start address
	1	↑	1	-	VSP15	VSP14	VSP13	VSP12	VSP11	VSP10	VSP9	VSP8		
	1	↑	1	-	VSP7	VSP6	VSP5	VSP4	VSP3	VSP2	VSP1	VSP0		
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)	Idle mode off
IDMON	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)	Idle mode on

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Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
COLMOD	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)	Interface pixel format
	1	↑	1	-	0	D6	D5	D4	0	D2	D1	D0		Interface format
RAMWRC	0	↑	1	-	0	0	1	1	1	1	0	0	(3Ch)	Memory write continue
	1	↑	1	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Write data
	1	↑	1	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	↑	1	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
RAMRDC	0	↑	1	-	0	0	1	1	1	1	1	0	(3Eh)	Memory read continue
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		
	1	1	↑	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	1	↑	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
TESCAN	0	↑	1	-	0	1	0	0	0	1	0	0	(44h)	Set tear scanline
	1	↑	1	-	N15	N14	N13	N12	N11	N10	N9	N8		
	1	↑	1	-	N7	N6	N5	N4	N3	N2	N1	N0		
RDTESCAN	0	↑	1	-	0	1	0	0	0	1	0	1	(45h)	Get scanline
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	-	-	-	-	-	-	N9	N8		
	1	1	↑	-	N7	N6	N5	N4	N3	N2	N1	N0		
WRDISBV	0	↑	1	-	0	1	0	1	0	0	0	1	(51h)	Write display brightness
	1	↑	1	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0		
RDDISBV	0	↑	1	-	0	1	0	1	0	0	1	0	(52h)	Read display brightness value
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0		
WRCTRLD	0	↑	1	-	0	1	0	1	0	0	1	1	(53h)	Write CTRL display
	1	↑	1	-	0	0	BCTRL	0	DD	BL	0	0		
RDCTRLD	0	↑	1	-	0	1	0	1	0	1	0	0	(54h)	Read CTRL value dsiplay
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	0	0	BCTRL	0	DD	BL	0	0		

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Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
WRCACE	0	↑	1	-	0	1	0	1	0	1	0	1	(55h)	Write content adaptive brightness control and Color enhancemnet
	1	↑	1	-	CECTRL	0	CE1	CE0	0	0	C1	C0		
RDCABC	0	↑	1	-	0	1	0	1	0	1	1	0	(56h)	Read content adaptive brightness control
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	0	CECTRL	0	0	0	0	C1	C0		
WRCABCMB	0	↑	1	-	0	1	0	1	1	1	1	0	(5Eh)	Write CABC minimum brightness
	1	↑	1	-	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0		
RDCABCMB	0	↑	1	-	0	1	0	1	1	1	1	1	(5Fh)	Read CABC minimum brightness
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0		
RDABCSDR	0	↑	1	-	0	1	1	0	1	0	0	0	(68h)	Read Automatic Brightness Control Self-Diagnostic Result
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	D7	D6	0	0	0	0	0	0		-
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)	Read ID1
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		Read parameter
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)	Read ID2
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		Read parameter
RDID3	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)	Read ID3

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Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		Read parameter

Table 19 System Function Command List

"-": Don't care

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9.1.1 NOP (00h)

<table>
<tr><td>00H</td><td colspan="13">NOP (No Operation)</td></tr>
<tr><td>Inst / Para</td><td>D/CX</td><td>WRX</td><td>RDX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>NOP</td><td>0</td><td>↑</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>(00h)</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td><td>-</td></tr>
<tr><td>Description</td><td colspan="13">This command is empty command.</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"></td></tr>
</table>

Note: "-"Don't care

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9.1.2 SWRESET (01h): Software Reset

01H	SWRESET (Software Reset)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)
Parameter	No Parameter												-
Description	"-" Don't care -The display module performs a software reset, registers are written with their SW reset default values. -Frame memory contents are unaffected by this command.												
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display suppliers' factory default values to the registers during this 5msec. If software reset is sent during sleep in mode, it will be necessary to wait 120msec before sending sleep out command. Software reset command cannot be sent during sleep out sequence.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

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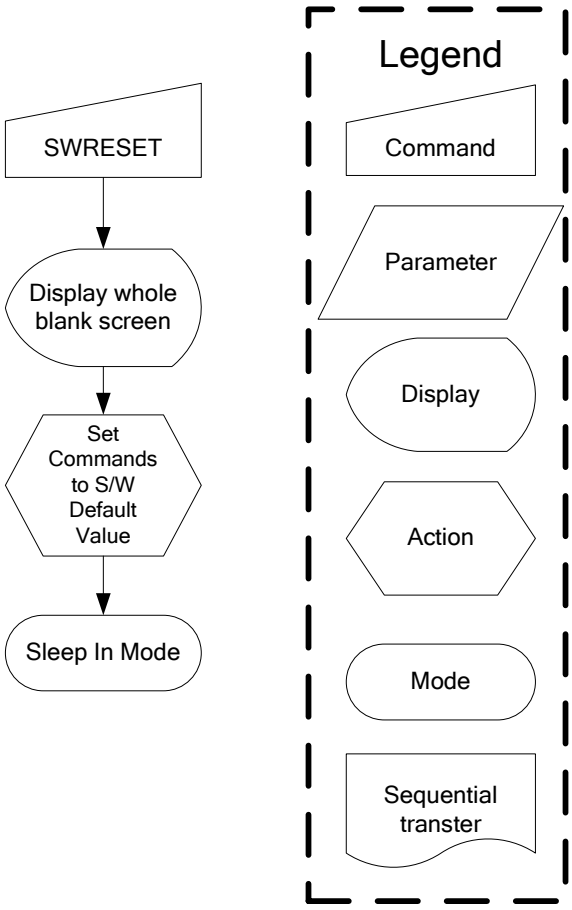
Flow Chart



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9.1.3 RDDID (04h): Read Display ID

04H	RDDID (Read Display ID)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	
3rd parameter	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
4th parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	

Description

-This read byte returns 24-bit display identification information.

-The 1st parameter is dummy data

-The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID.

-The 3rd parameter (ID26 to ID20): LCD module/driver version ID

-The 4th parameter (ID37 to UD30): LCD module/driver ID.

-Commands RDID1/2/3(Dah, DBh, DCh) read data correspond to the parameters 2,3,4 of the command 04h, respectively.

"-" Don't care

Restriction

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	ID1	ID2	ID3
Power On Sequence	0x85	0x85	0x52
S/W Reset	0x85	0x85	0x52
H/W Reset	0x85	0x85	0x52

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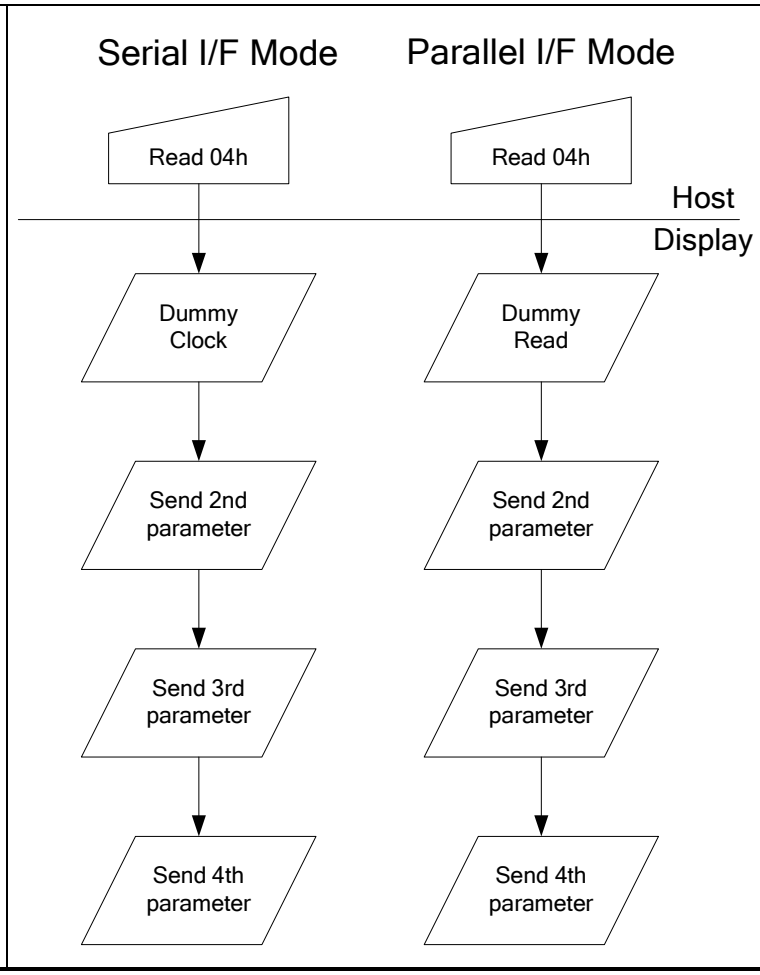
Flow Chart



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9.1.4 RDDST (09h): Read Display Status

09H	RDDST (Read Display Status)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24	
3rd parameter	1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON	
4th parameter	1	1	↑	-	ST15	ST14	INVON	ST12	ST11	DISON	TEON	GCS2	
5th parameter	1	1	↑	-	GCS1	GCS0	TEM	ST4	ST3	ST2	ST1	ST0	

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
BSTON	Booster Voltage Status	'1' =Booster on, '0' =Booster off
MY	Row Address Order (MY)	'1' =Decrement, (Bottom to Top, when MADCTL (36h) D7='1') '0' =Increment, (Top to Bottom, when MADCTL (36h) D7='0')
MX	Column Address Order (MX)	'1' =Decrement, (Right to Left, when MADCTL (36h) D6='1') '0' =Increment, (Left to Right, when MADCTL (36h) D6='0')
MV	Row/Column Exchange (MV)	'1' = Row/column exchange, (when MADCTL (36h) D5='1') '0' = Normal, (when MADCTL (36h) D5='0'
ML	Scan Address Order (ML)	'0' =Decrement, (LCD refresh Top to Bottom, when MADCTL (36h) D4='0') '1'=Increment, (LCD refresh Bottom to Top, when MADCTL (36h) D4='1')
RGB	RGB/ BGR Order (RGB)	'1' =BGR, (When MADCTL (36h) D3='1') '0' =RGB, (When MADCTL (36h) D3='0')
MH	Horizontal Order	'0' =Decrement, (LCD refresh Left to Right, when MADCTL (36h) D2='0') '1' =Increment, (LCD refresh Right to Left, when MADCTL (36h) D2='1')
ST24	For Future Use	'0'
ST23	For Future Use	'0'
IFPF2 IFPF1 IFPF0	Interface Color Pixel Format Definition	"011" = 12-bit / pixel, "101" = 16-bit / pixel, "110" = 18-bit / pixel, "111" = 16M truncated, others are not defined.
IDMON	Idle Mode On/Off	'1' = On, "0" = Off
PTLON	Partial Mode On/Off	'1' = On, "0" = Off

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	SLPOUT	Sleep In/Out	'1' = Out, "0" = In
	NORON	Display Normal Mode On/Off	'1' = Normal Display, '0' = Partial Display
	ST15	Vertical Scrolling Status (Not Used)	'1' = Scroll on,"0" = Scroll off
	ST14	Horizontal Scroll Status (Not Used)	'0'
	INVON	Inversion Status	'1' = On, "0" = Off
	ST12	All Pixels On (Not Used)	'0'
	ST11	All Pixels Off (Not Used)	'0'
	DISON	Display On/Off	'1' = On, "0" = Off
	TEON	Tearing effect line on/off	'1' = On, "0" = Off
	GCSEL2	Gamma Curve Selection	"000" = GC0
	GCSEL1		"001" = GC1
	GCSEL0		"010" = GC2 "011" = GC3 "100" to "111" = Not defined
	TEM	Tearing effect line mode	'0' = mode1, '1' = mode2
	ST4	For Future Use	'0'
	ST3	For Future Use	'0'
	ST2	For Future Use	'0'
	ST1	For Future Use	'0'
	ST0	For Future Use	'0'

"-" Don't care

Restriction

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (ST31 to ST0)			
	ST[31-24]	ST[23-16]	ST[15-8]	ST[7-0]
Power On Sequence	0000-0000	0110-0001	0000-0000	0000-0000
S/W Reset	0xxx-xx00	0xxx-0001	0000-0000	0000-0000
H/W Reset	0000-0000	0110-0001	0000-0000	0000-0000

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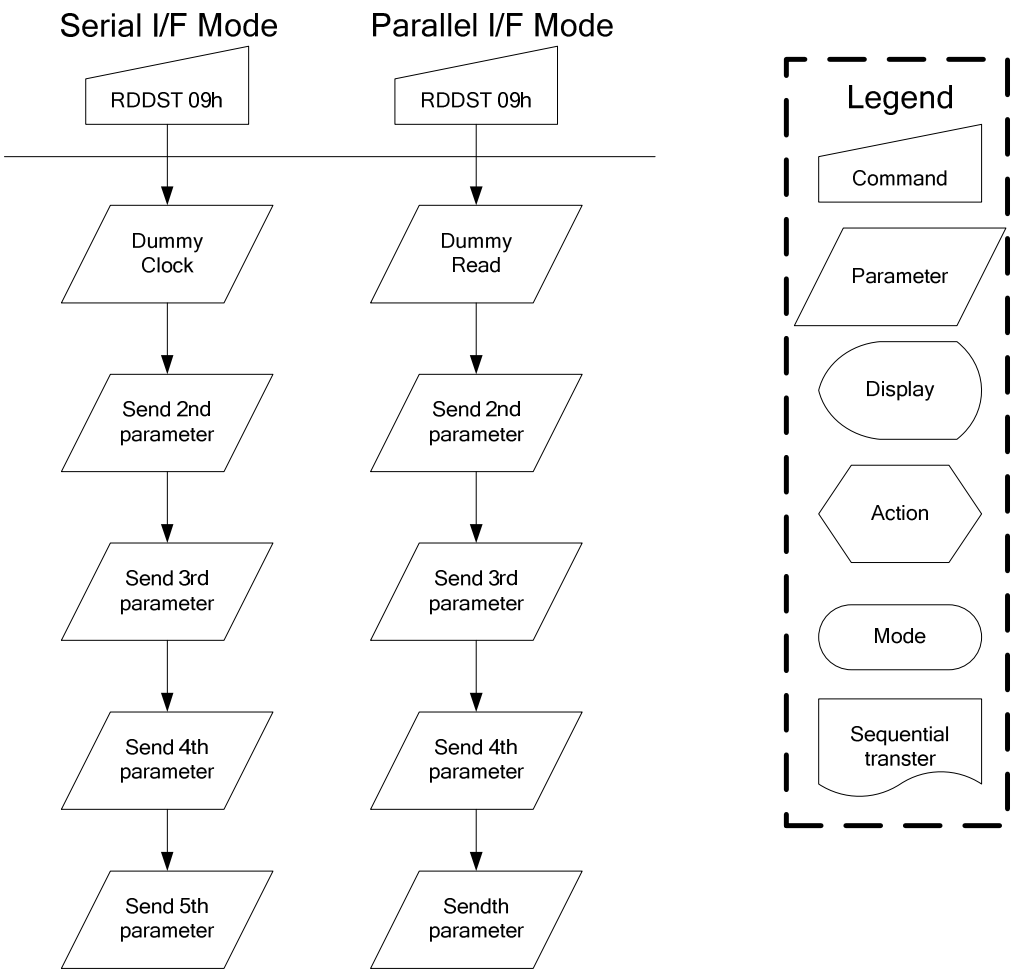
Flow Chart	

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9.1.5 RDDPM (0Ah): Read Display Power Mode

0AH	RDDPM (Read Display Power Mode)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	D1	D0	

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
BSTON	Booster Voltage Status	'1' =Booster on, '0' =Booster off
IDMON	Idle mode on/off	'1' = Idle Mode On, '0' = Idle Mode Off
PTLON	Partial mode on/off	'1' =Partial mode on, '0' =Partial mode off,
SLPOUT	Sleep in/out	'1' =Sleep out, '0' =Sleep in,
NORON	Display normal mode on/off	'1' = Normal display, '0' = Partial display,
DISON	Display on/off	'1' =Display on, '0' =Display off,
D1	Not Used	"0"
D0	Not Used	"0"

"-" Don't care

Restriction

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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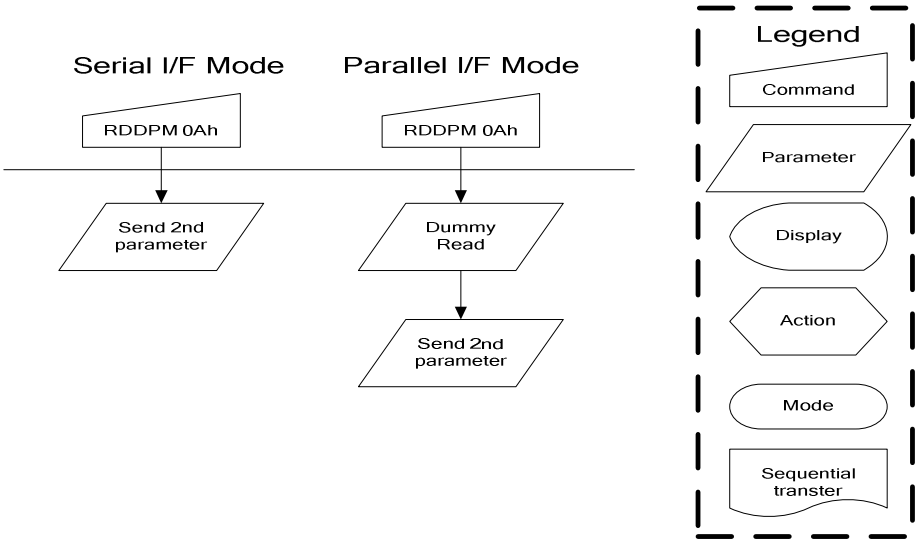
Default

Status	Default Value (D7 to D0)
Power On Sequence	0000-1000(08h)
S/W Reset	0000-1000(08h)
H/W Reset	0000-1000(08h)

Flow Chart



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9.1.6 RDDMADCTL (0Bh): Read Display MADCTL

0BH	RDDMADCTL (Read Display MADCTL)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDMADCTL	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	MY	MX	MV	ML	RGB	MH	D1	D0	

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
MY	Row Address Order (MY)	'1' =Decrement, (Bottom to Top, when MADCTL (36h) D7='1') '0' =Increment, (Top to Bottom, when MADCTL (36h) D7='0')
MX	Column Address Order (MX)	'1' =Decrement, (Right to Left, when MADCTL (36h) D6='1') '0' =Increment, (Left to Right, when MADCTL (36h) D6='1')
MV	Row/Column Exchange (MV)	'1' = Row/column exchange, (when MADCTL (36h) D5='1') '0' = Normal, (when MADCTL (36h) D5='0'
ML	Scan Address Order (ML)	'0' =Decrement, (LCD refresh Top to Bottom, when MADCTL (36h) D4='0') '1'=Increment, (LCD refresh Bottom to Top, when MADCTL (36h) D4='1')
RGB	RGB/ BGR Order (RGB)	'1' =BGR, (When MADCTL (36h) D3='1') '0' =RGB, (When MADCTL (36h) D3='0')
MH	Horizontal Order	'0' =Decrement, (LCD refresh Left to Right, when MADCTL (36h) D2='0') '1' =Increment, (LCD refresh Right to Left, when MADCTL (36h) D2='1')
D1	Not used	'0'
D0	Not used	'0'

"-" Don't care

Restriction

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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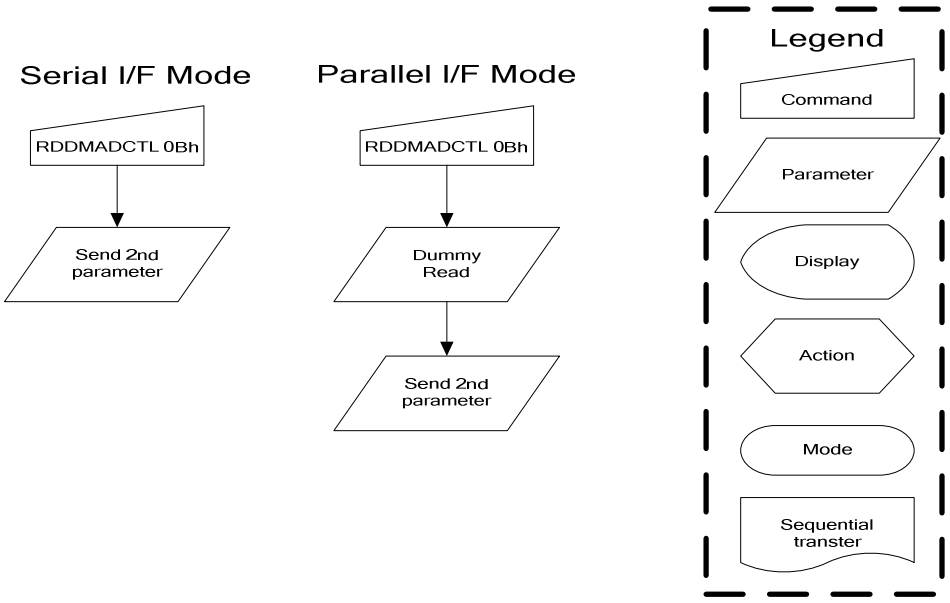
Default

Status	Default Value (D7 to D0)
Power On Sequence	0000-0000 (00h)
S/W Reset	No change
H/W Reset	0000-0000 (00h)

Flow Chart



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9.1.7 RDDCOLMOD (0Ch): Read Display Pixel Format

<table>
<tr><td>0CH</td><td colspan="13">RDDCOLMOD (Read Display Pixel Format)</td></tr>
<tr><td>Inst / Para</td><td>D/CX</td><td>WRX</td><td>RDX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>RDDCOLMOD</td><td>0</td><td>↑</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>(0Ch)</td></tr>
<tr><td>1st parameter</td><td>1</td><td>1</td><td>↑</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>1</td><td>↑</td><td>-</td><td>0</td><td>D6</td><td>D5</td><td>D4</td><td>0</td><td>D2</td><td>D1</td><td>D0</td><td></td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>-</td><td>Set to ‘0’</td></tr>
<tr><td>D6</td><td rowspan="3">RGB interface color format</td><td rowspan="3">‘101’ = 16 bit/pixel
‘110’ = 18 bit/pixel</td></tr>
<tr><td>D5</td></tr>
<tr><td>D4</td></tr>
<tr><td>D3</td><td>-</td><td>Set to ‘0’</td></tr>
<tr><td>D2</td><td rowspan="3">Control interface color format</td><td rowspan="3">‘101’ = 16 bit/pixel
‘110’ = 18 bit/pixel</td></tr>
<tr><td>D1</td></tr>
<tr><td>D0</td></tr>
</table>
Others are no define and invalid
“-“ Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>0000-0110 (18 bit/pixel)</td></tr>
<tr><td>S/W Reset</td><td>No change</td></tr>
<tr><td>H/W Reset</td><td>0000-0110 (18 bit/pixel)</td></tr>
</table>
</td></tr>
</table>

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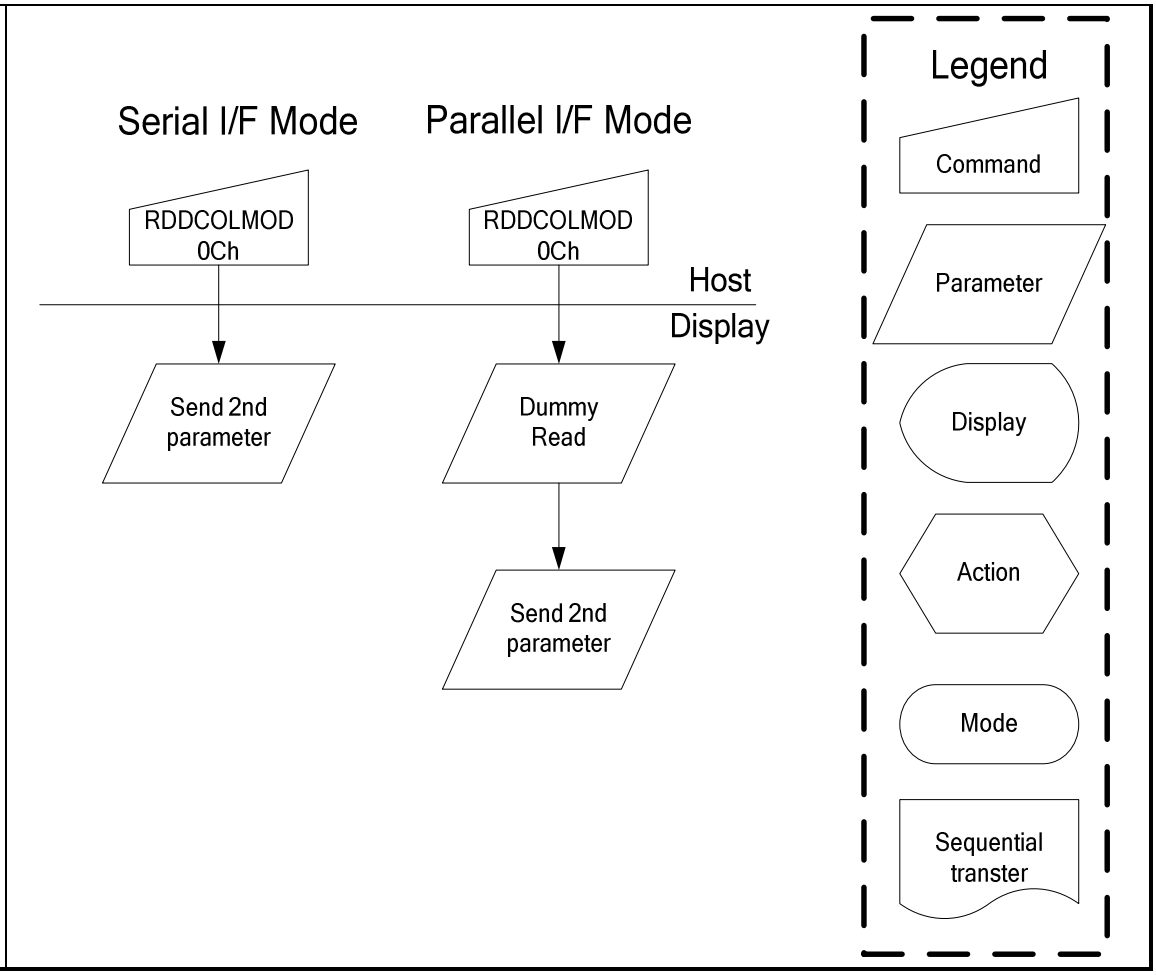
Flow Chart



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9.1.8 RDDIM (0Dh): Read Display Image Mode

0DH	RDDIM (Read Display Image Mode)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	VSSON	0	INVON	0	0	GC2	GC1	GC0	

Description

This command indicates the current status of the display as described in the table below:

-VSSON: Vertical scrolling on/off

-INVON: Inversion on/off

Gamma Curve Selection	GC2	GC1	GC0	Gamma set (26h) Parameter
Gamma curve 1	0	0	0	GC0
Gamma curve 2	0	0	1	GC1
Gamma curve 3	0	1	0	GC2
Gamma curve 4	0	1	1	GC3
Not Defined	1	0	0	Not Defined
Not Defined	1	0	1	Not Defined
Not Defined	1	1	0	Not Defined
Not Defined	1	1	1	Not Defined

Others are no define and invalid

"-" Don't care

Restriction

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000-0000
S/W Reset	0000-0000

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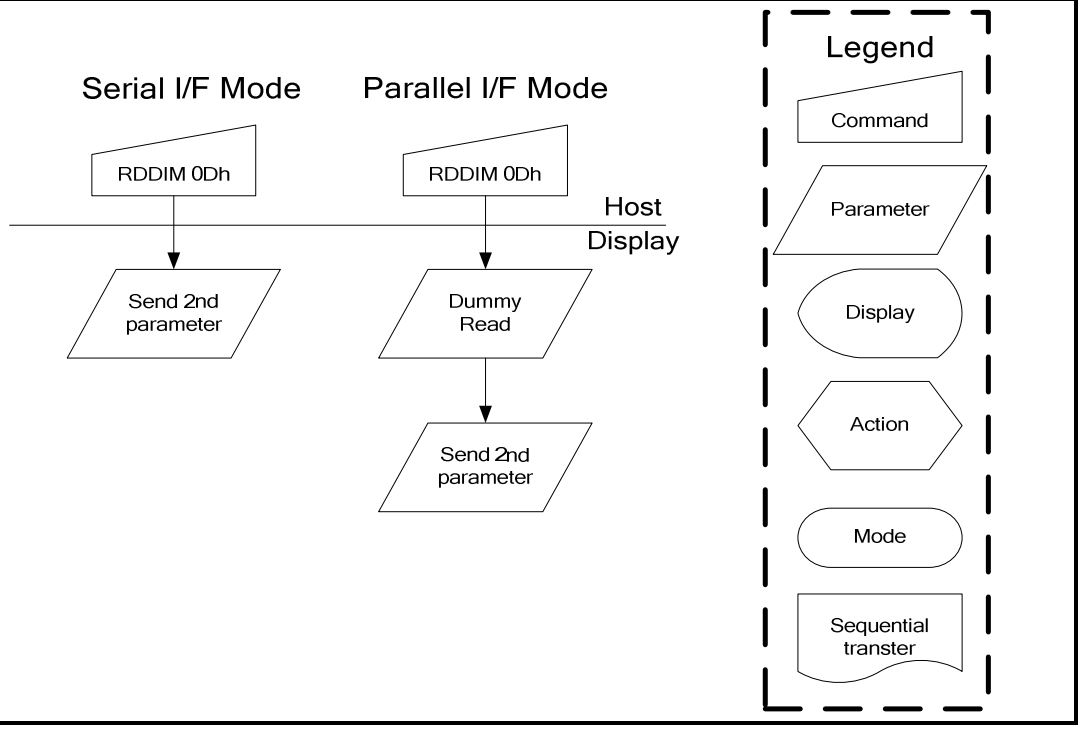
	H/W Reset: 0000-0000
Flow Chart	

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9.1.9 RDDSM (0Eh): Read Display Signal Mode

0EH	RDDSM (Read Display Signal Status)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	TEON	TEM	0	0	0	0	0	0	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
TEON	Tearing effect line on/off	'1' = ON, '0' = OFF,
TEM	Tearing effect line mode	'1' = mode2, '0' = mode1,

"-" Don't care

Restriction

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000-0000
S/W Reset	0000-0000
H/W Reset	0000-0000

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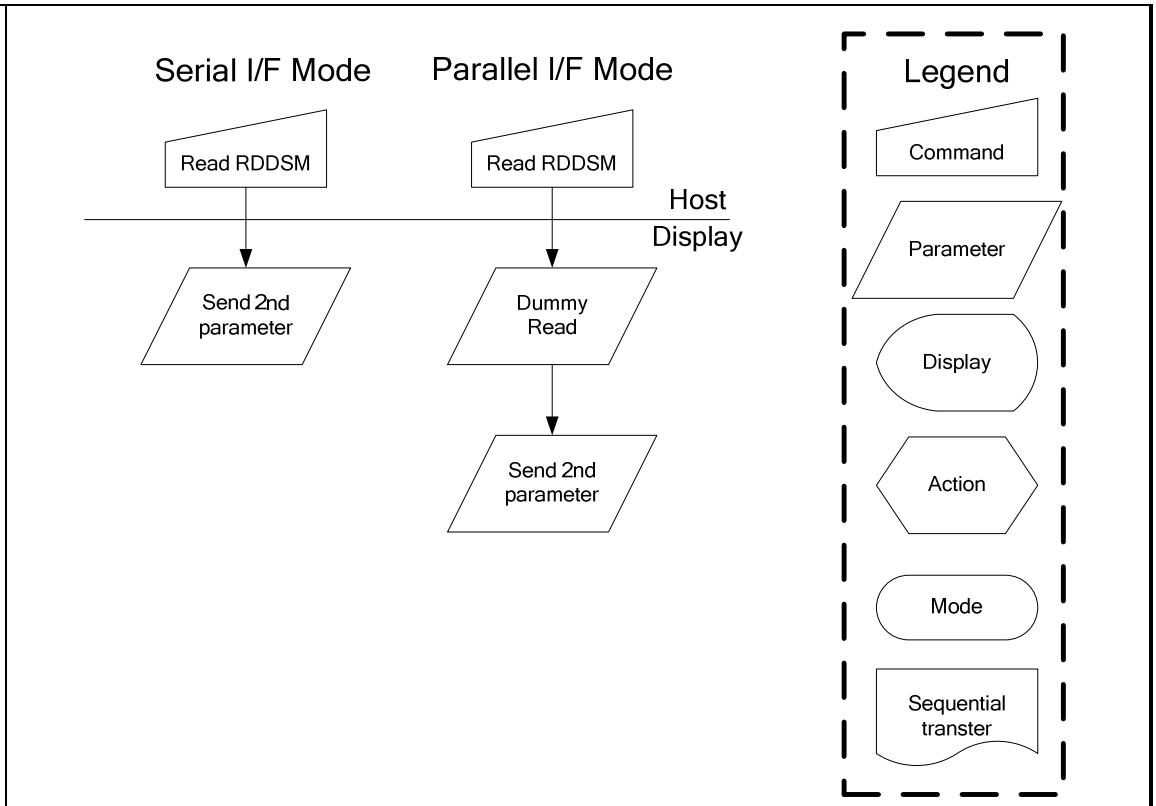
Flow Chart



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9.1.10 RDDSDR (0Fh): Read Display Self-Diagnostic Result

09H	RDDSDR (Read Display Self-Diagnostic Result)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDSDR	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	D6	0	0	0	0	0	0	-
Description	This command indicates the current status of the display self-diagnostic result after sleep out command as described below: -D7: Register loading detection -D6: Functionality detection "-" Don't care												
Restriction													

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000-0000
S/W Reset	0000-0000
H/W Reset	0000-0000

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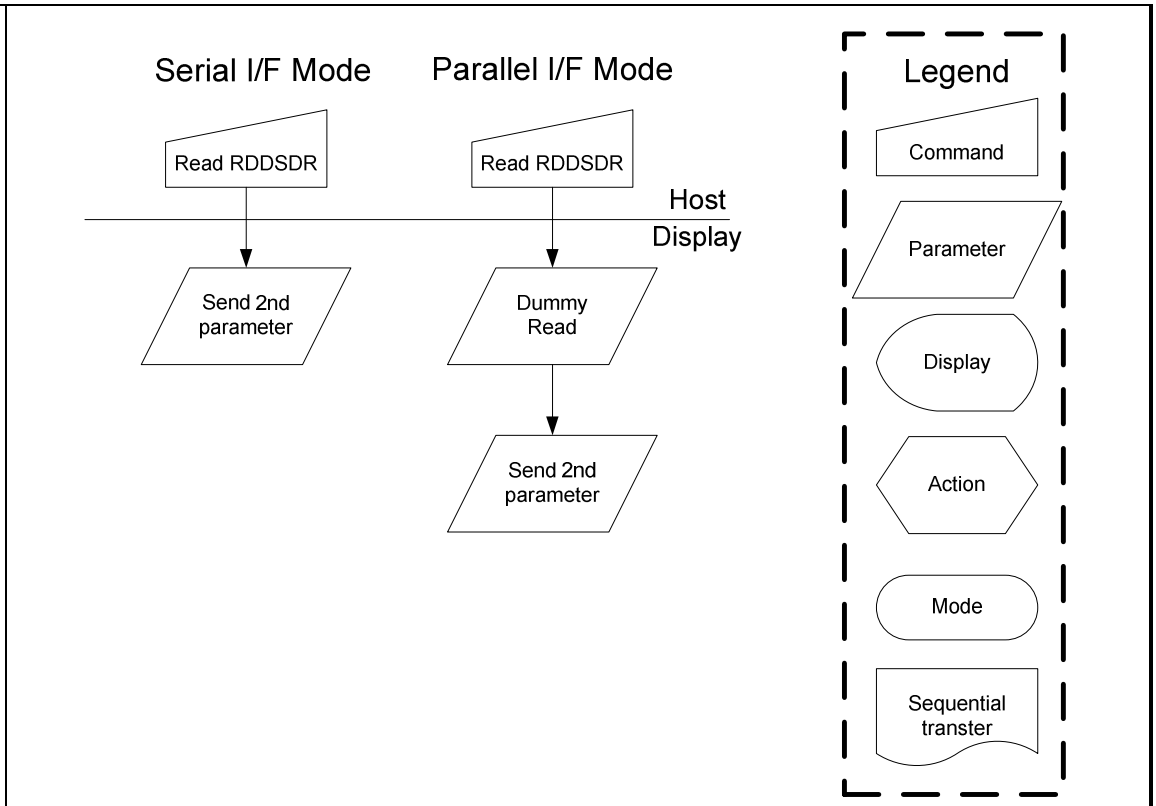
Flow Chart



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9.1.11 SLPIN (10h): Sleep in

10H	SLPIN (Sleep In)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)
parameter	No Parameter												
Description	-This command causes the LCD module to enter the minimum power consumption mode. -In this mode the DC/DC converter is stopped, internal oscillator is stopped, and panel scanning is stopped. -MCU interface and memory are still working and the memory keeps its contents. "-" Don't care												
Restriction	-This command has no effect when module is already in sleep in mode. Sleep in mode can only be left by the sleep out command (11h). -It will be necessary to wait 5msec before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize. -It will be necessary to wait 120msec after sending sleep out command (when in sleep in mode) before sending an sleep in command.												
Register availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

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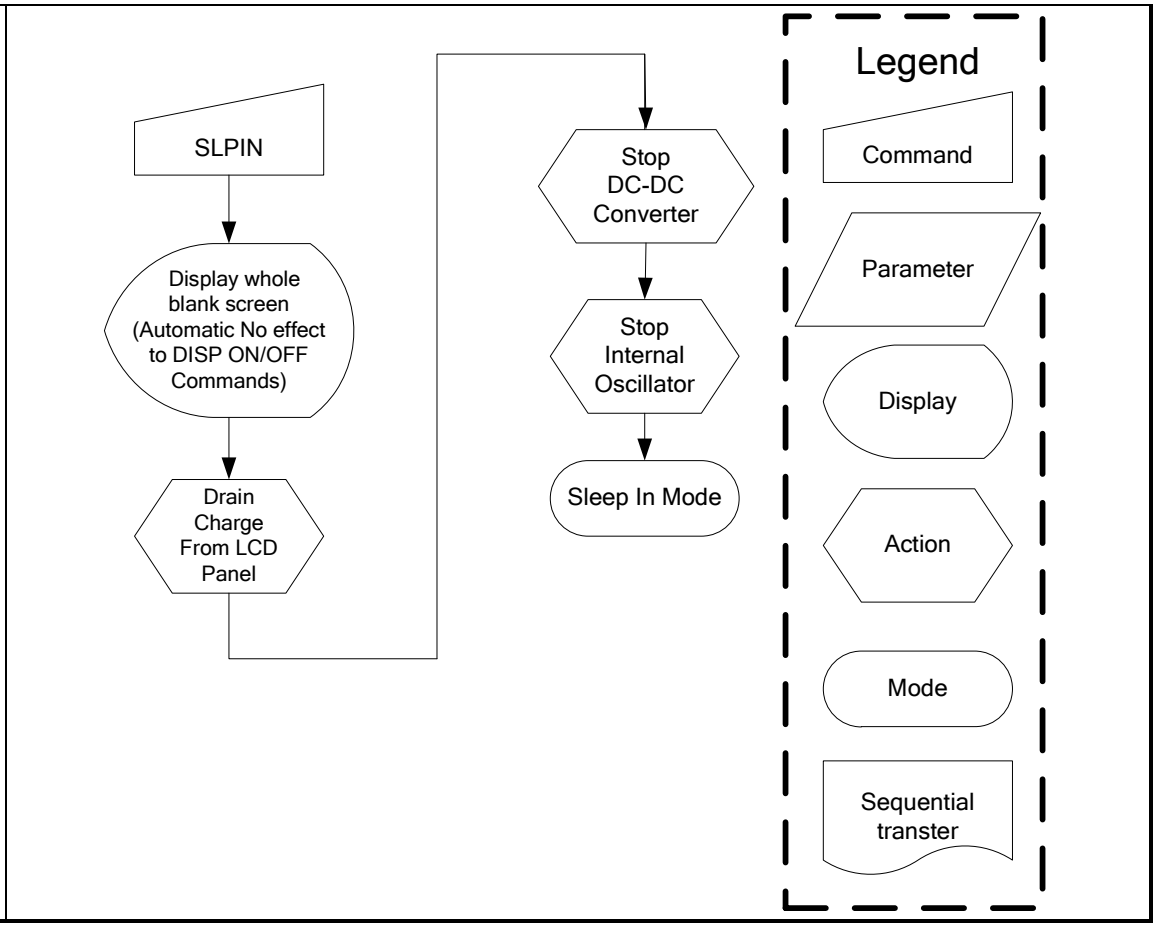
Flow Chart



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9.1.12 SLPOUT (11h): Sleep Out

11H	SLPOUT (Sleep Out)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)
parameter	No Parameter												
Description	-This command turn off sleep mode. -In this mode the DC/DC converter is enable, internal display oscillator is started, and panel scanning is started.												
Restriction	-This command has no effect when module is already in sleep out mode. Sleep out mode can only be left by the sleep in command (10h). -It will be necessary to wait 5msec before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize. -It will be necessary to wait 120msec after sending sleep out command (when in sleep in mode) before sending an sleep in command. -The display module runs the self-diagnostic functions after this command is received.												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

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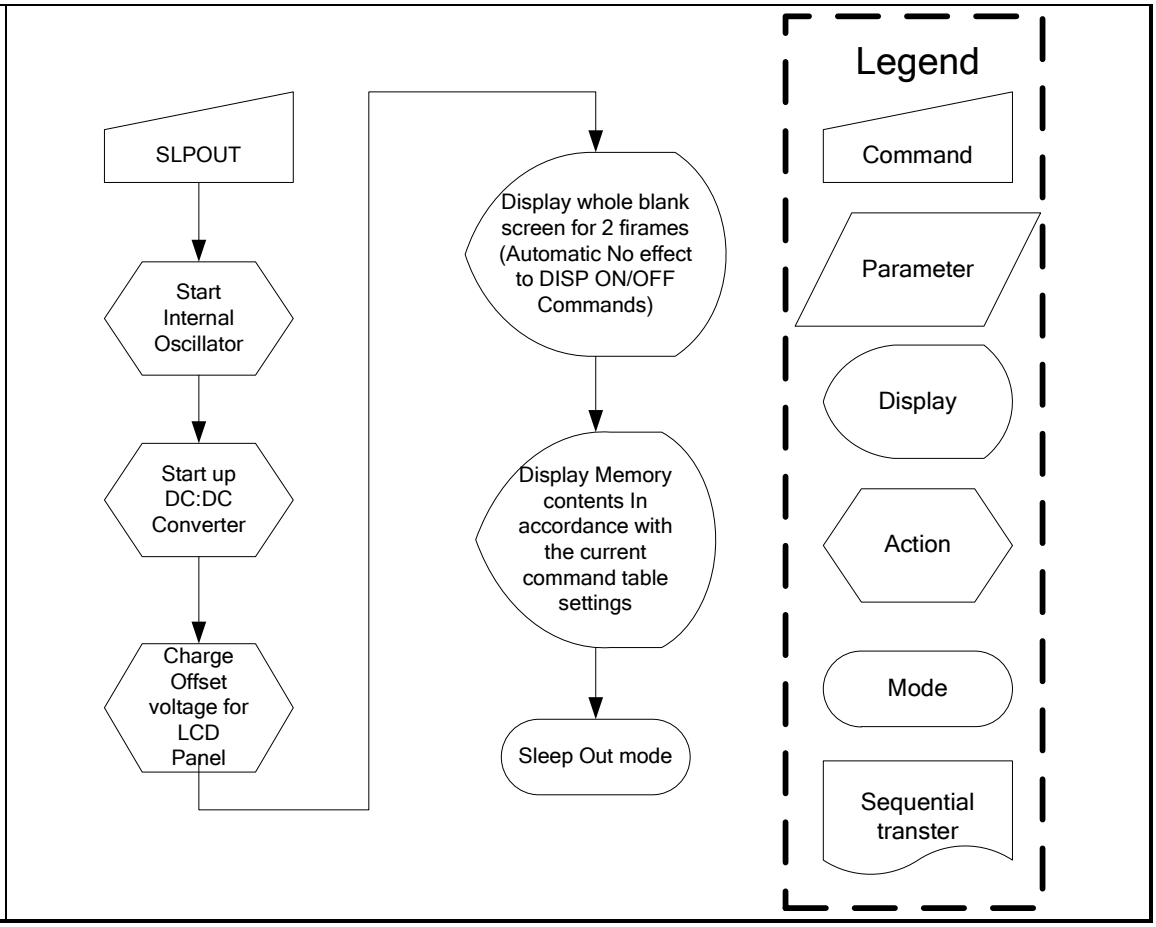
Flow Chart



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9.1.13 PTLON (12h): Partial Display Mode On

<table>
<tr><td>12H</td><td colspan="13">PTLON (Partial Display Mode On)</td></tr>
<tr><td>Inst / Para</td><td>D/CX</td><td>WRX</td><td>RDX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>PTLON</td><td>0</td><td>↑</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>(12h)</td></tr>
<tr><td>parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">-This command turns on Partial mode. The partial mode window is described by the Partial Area command (30h)
-To leave Partial mode, the Normal Display Mode On command (13h) should be written.
“-“ Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when partial mode is active.</td></tr>
<tr><td>Register availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal display mode on</td></tr><tr><td>S/W Reset</td><td>Normal display mode on</td></tr><tr><td>H/W Reset</td><td>Normal display mode on</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area (30h)</td></tr>
</table>

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9.1.14 NORON (13h): Normal Display Mode On

12H	NORON (Normal Display Mode On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)
parameter	No Parameter												
Description	-This command turns the display to normal mode. -Normal display mode on means partial mode off. -Exit from NORON by the partial mode on command. "-" Don't care												
Restriction	This command has no effect when normal display mode is active.												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal display mode on
S/W Reset	Normal display mode on
H/W Reset	Normal display mode on

Flow Chart: See partial area description for details of when to use this command.

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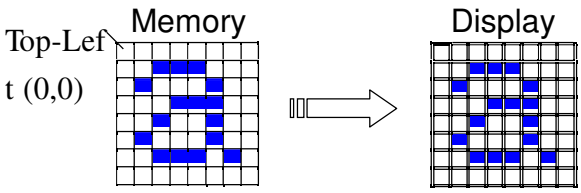
9.1.15 INVOFF (20h): Display Inversion Off

20H	INVOFF (Display Inversion Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)
parameter	No Parameter												
Description	-This command is used to recover from display inversion mode. "-" Don't care (Example)  												
Restriction	This command has no effect when module is already in inversion off mode.												
Register availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display inversion off
S/W Reset	Display inversion off
H/W Reset	Display inversion off

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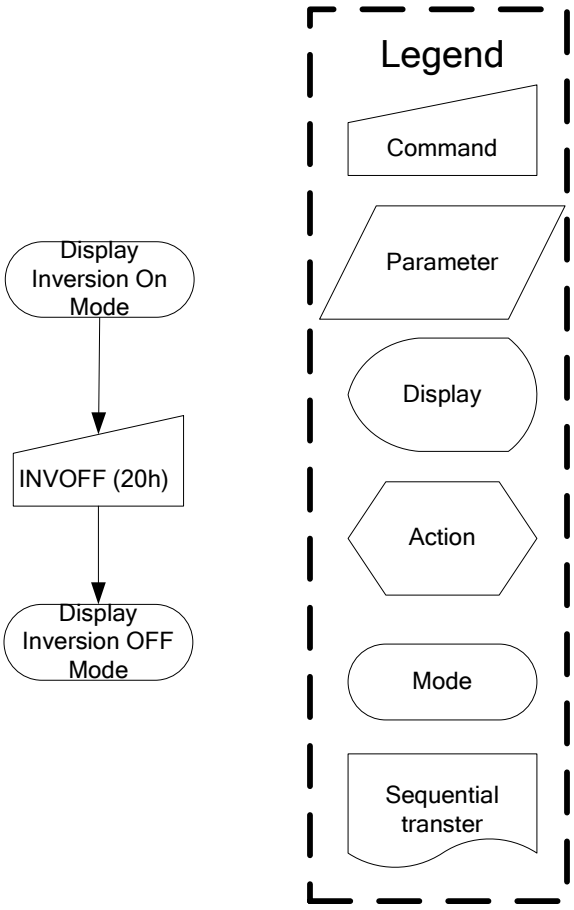
Flow Chart



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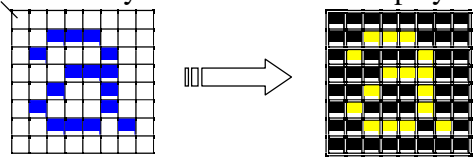
9.1.16 INVON (21h): Display Inversion On

21H	INVON (Display Inversion On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)
parameter	No Parameter												
Description	-This command is used to recover from display inversion mode. "-" Don't care (Example) Top-Left (0,0) Memory → Display 												
Restriction	This command has no effect when module is already in inversion on mode.												
Register availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display inversion off
S/W Reset	Display inversion off
H/W Reset	Display inversion off

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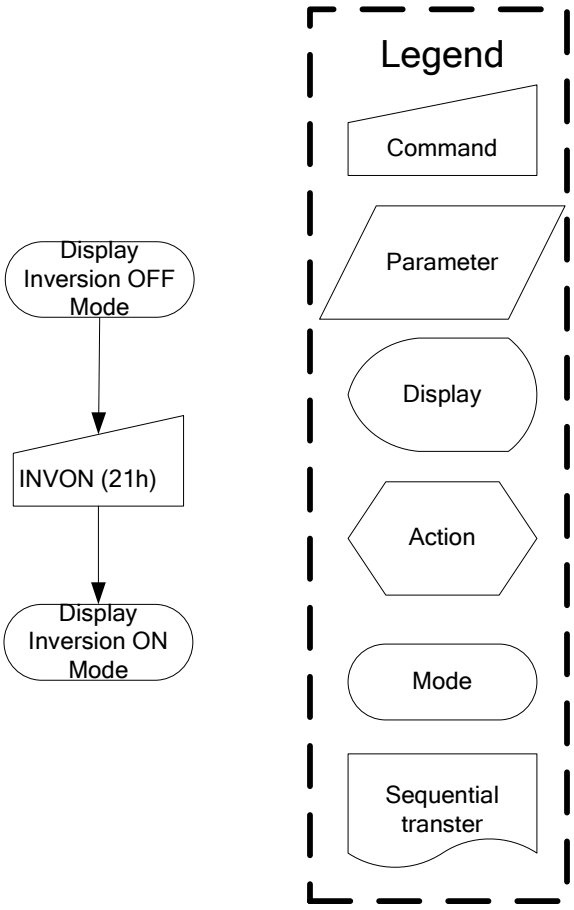
Flow Chart



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9.1.17 GAMSET (26h): Gamma Set

<table>
<tr><td>26H</td><td colspan="13">GAMSET (Gamma Set)</td></tr>
<tr><td>Inst / Para</td><td>D/CX</td><td>WRX</td><td>RDX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>GAMSET</td><td>0</td><td>↑</td><td>1</td><td>-</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>(26h)</td></tr>
<tr><td>parameter</td><td>1</td><td>↑</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>GC3</td><td>GC2</td><td>GC1</td><td>GC0</td><td></td></tr>
<tr><td>1. Description</td><td colspan="13">-This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table.
<table>
<tr><th>GC [7:0]</th><th>Parameter</th><th>Curve Selected</th></tr>
<tr><td>01h</td><td>GC0</td><td>Gamma Curve 1 (G2.2)</td></tr>
<tr><td>02h</td><td>GC1</td><td>Gamma Curve 2 (G1.8)</td></tr>
<tr><td>04h</td><td>GC2</td><td>Gamma Curve 3 (G2.5)</td></tr>
<tr><td>08h</td><td>GC3</td><td>Gamma Curve 4 (G1.0)</td></tr>
</table>
Note: All other values are undefined.</td></tr>
<tr><td>Restriction</td><td colspan="13">Values of GC[7:0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.</td></tr>
<tr><td>Register availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>0x01</td></tr>
<tr><td>S/W Reset</td><td>0x01</td></tr>
<tr><td>H/W Reset</td><td>0x01</td></tr>
</table>
</td></tr>
</table>

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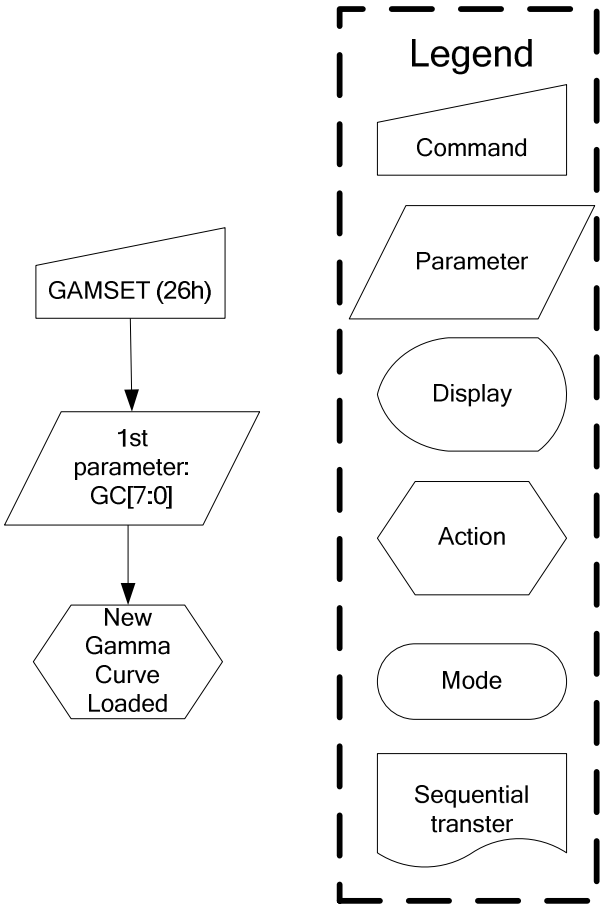
Flow Chart	

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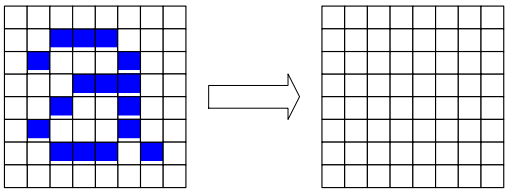
9.1.18 DISPOFF (28h): Display Off

28H	DISPOFF (Display Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)
parameter	No Parameter												
Description	- This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. - This command makes no change of contents of frame memory. - This command does not change any other status. - There will be no abnormal visible effect on the display. - Exit from this command by Display On (29h) **(Example)** **Memory** **Display** 												
Restriction	This command has no effect when module is already in display off mode.												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

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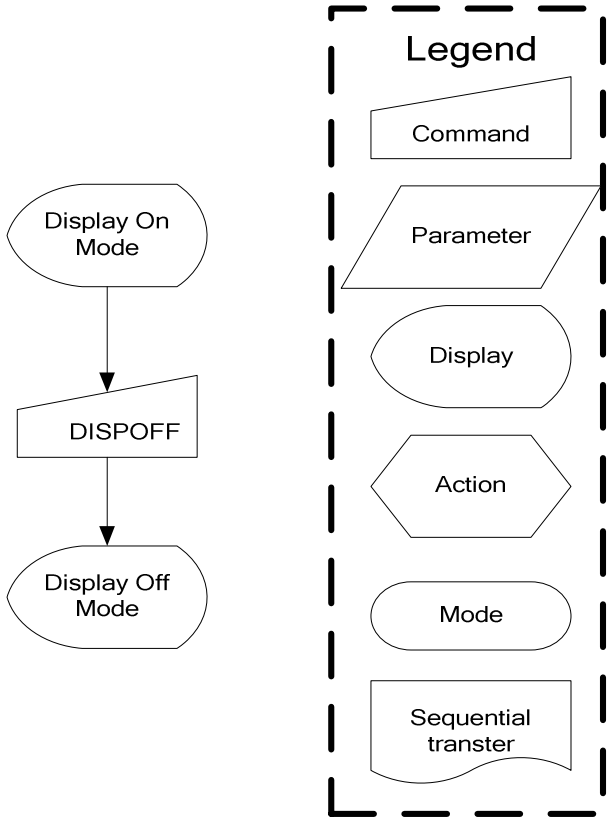
Flow Chart	

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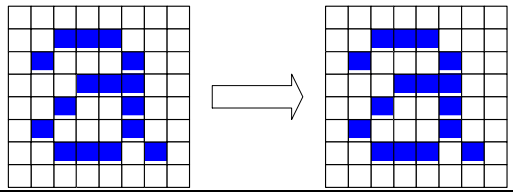
9.1.19 DISPON (29h): Display On

29H	DISPON (Display On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)
parameter	No Parameter												
Description	- This command is used to recover from DISPLAY OFF mode. - Output from the Frame Memory is enabled. - This command makes no change of contents of frame memory. - This command does not change any other status. **(Example)** **Memory** → **Display** 												
Restriction	This command has no effect when module is already in display on mode.												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

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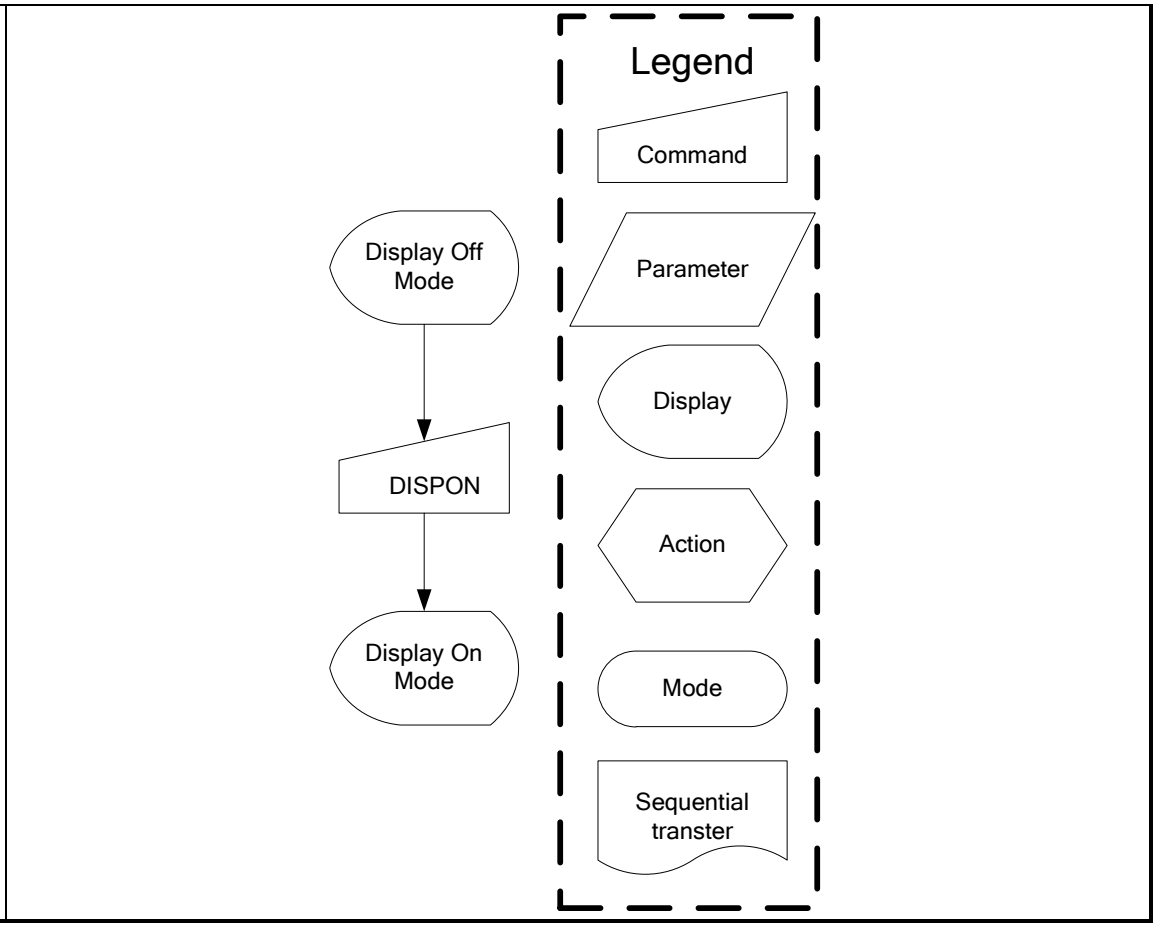
Flow Chart



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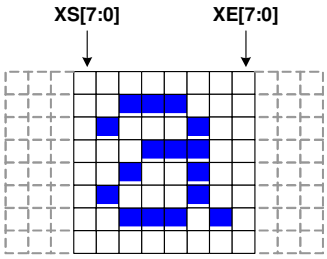
9.1.20 CASET (2Ah): Column Address Set

2AH	CASET (Column Address Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CASET	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)
1st parameter	1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	
2nd parameter	1	↑	1	-	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
3rd parameter	1	↑	1	-	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	
4th parameter	1	↑	1	-	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	

2. Description

-The value of XS [7:0] and XE [7:0] are referred when RAMWR command comes.

-Each value represents one column line in the Frame Memory.



Restriction

XS [15:0] always must be equal to or less than XE [15:0]

When XS [15:0] or XE [15:0] is greater than maximum address like below, data of out of range will be ignored.

(Parameter range: 0 < XS [15:0] < XE [15:0] < 239 (00Efh)): MV="0")

(Parameter range: 0 < XS [15:0] < XE [15:0] < 319 (013Fh)): MV="1")

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	XS[15:0]=0x00	XE[15:0]=0xEF
S/W Reset	XS[15:0]=0x00	When MV=0: XE[15:0]=00Efh, When MV=1: XE[15:0]=013Fh
H/W Reset	XS[15:0]=0x00	XE[15:0]=0xEF

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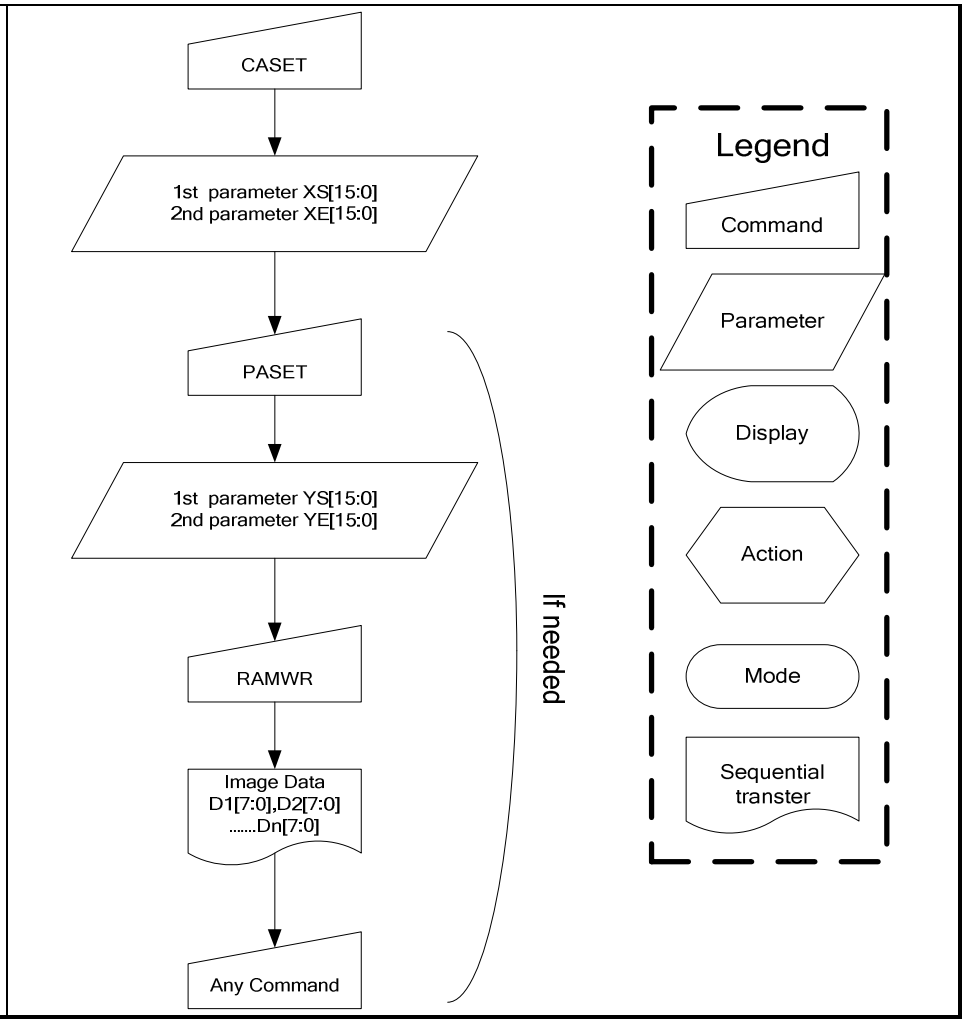
Flow Chart



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9.1.21 RASET (2Bh): Row Address Set

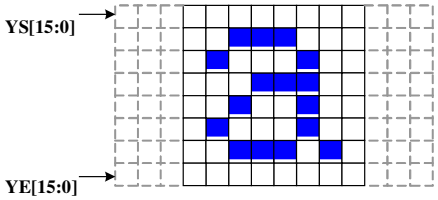
2BH	RASET (Row Address Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RASET	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)
1st parameter	1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	
2nd parameter	1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
3rd parameter	1	↑	1	-	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	
4th parameter	1	↑	1	-	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	

3. Description

-This command is used to defined area of frame memory where MCU can access.

-The value of YS [15:0] and YE [15:0] are referred when RAMWR command comes.

-Each value represents one page line in the Frame Memory.



Restriction

YS [15:0] always must be equal to or less than YE [15:0]

When YS [15:0] or YE [15:0] is greater than maximum address like below, data of out of range will be ignored.

(Parameter range: 0 < YS [15:0] < YE [15:0] < 319 (013fh)): MV="0")

(Parameter range: 0 < YS [15:0] < YE [15:0] < 239 (00EFh)): MV="1")

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	YS[15:0]=0000h	YE[15:0]=013Fh
S/W Reset	YS[15:0]=0000h	When MV=0: YE[15:0]=013Fh, When MV=1: YE[15:0]=00Efh
H/W Reset	YS[15:0]=0000h	YE[15:0]=013Fh

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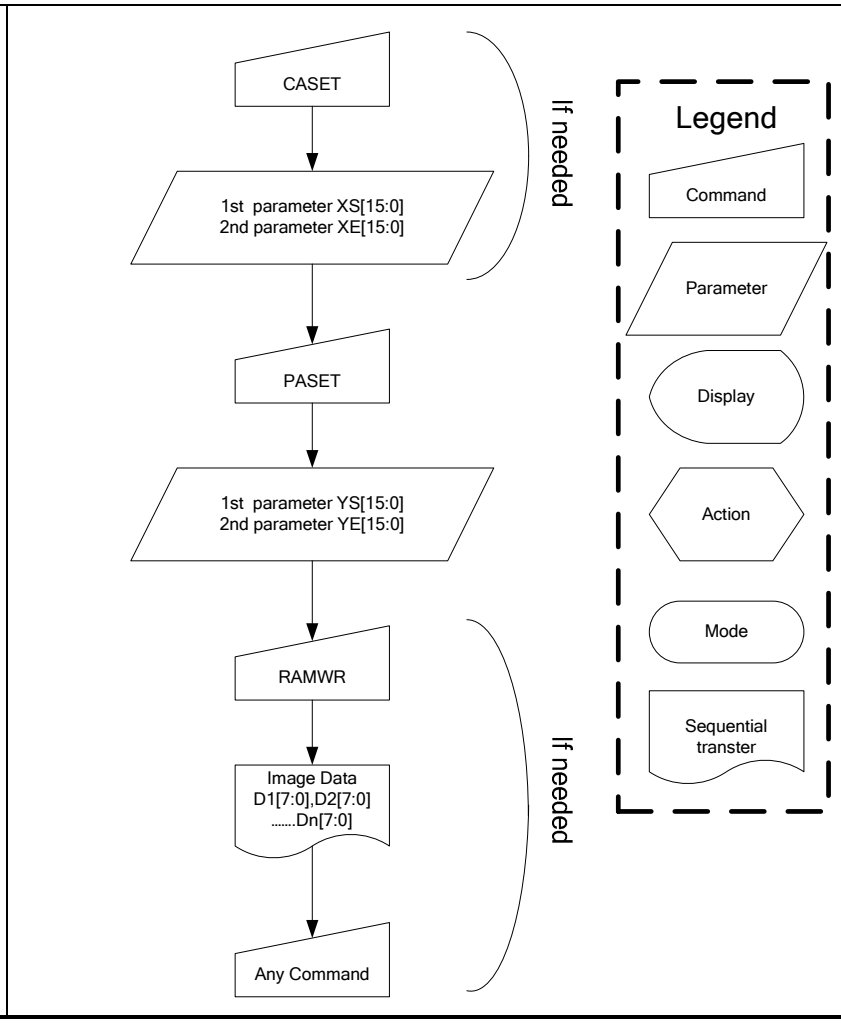
Flow Chart	

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9.1.22 RAMWR (2Ch): Memory Write

2CH	RAMWR (Memory Write)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)
1st parameter	1	↑	1	D1[17]-1[8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	
…	1	↑	1	Dx[17]-x[8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	
N parameter	1	↑	1	Dn[17]-n[8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	
Description	-This command is used to transfer data from MCU to frame memory. -When this command is accepted, the column register and the page register are reset to the start column/start page positions. -The start column/start page positions are different in accordance with MADCTL setting. -Sending any other command can stop frame write.												
Restriction													

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

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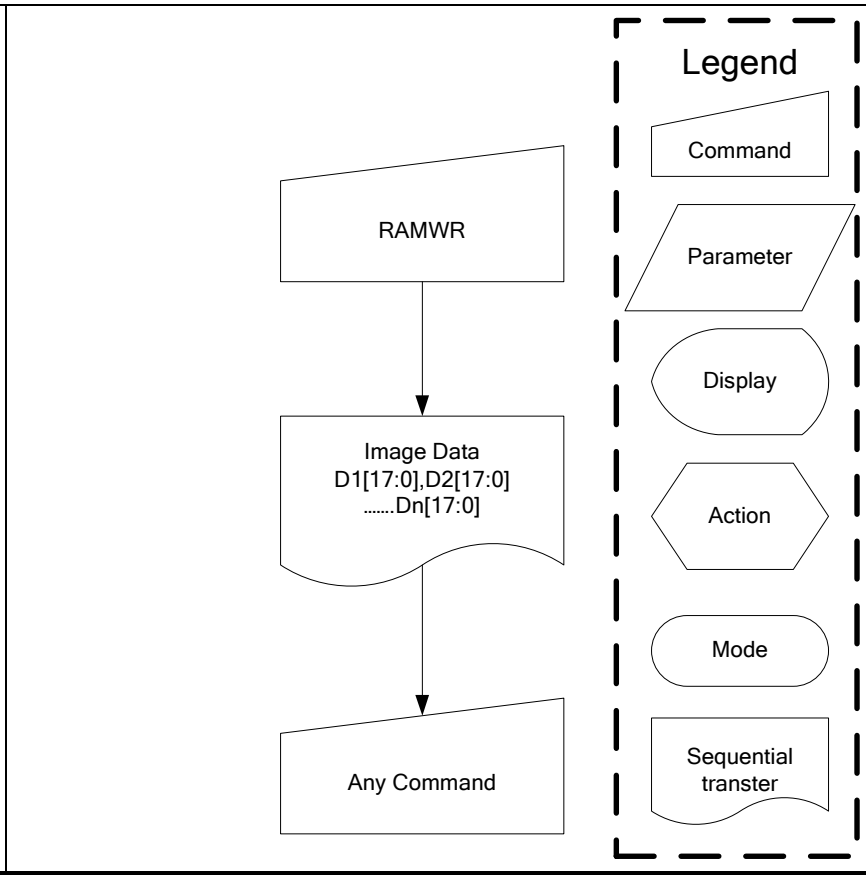
Flow Chart	

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9.1.23 RAMRD (2Eh): Memory Read

2EH	RAMRD (Memory Read)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMRD	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
:	1	1	↑	:	:	:	:	:	:	:	:	:	
(N+1)th parameter	1	1	↑	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
Description	-This command is used to transfer data from frame memory to MCU. -When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions. -The Start Column/Start Row positions are different in accordance with MADCTL setting. -Then D[17:0] is read back from the frame memory and the column register and the row register incremented -Frame Read can be cancelled by sending any other command. -The data color coding is fixed to 18-bit in reading function. Please see section 9.8 “Data color coding” for color coding (18-bit cases), when there is used 8, 9, 16 and 18-bit data lines for image data. Note1: The Command 3Ah should be set to 66h when reading pixel data from frame memory.												
Restriction													
Register availability													
Default													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

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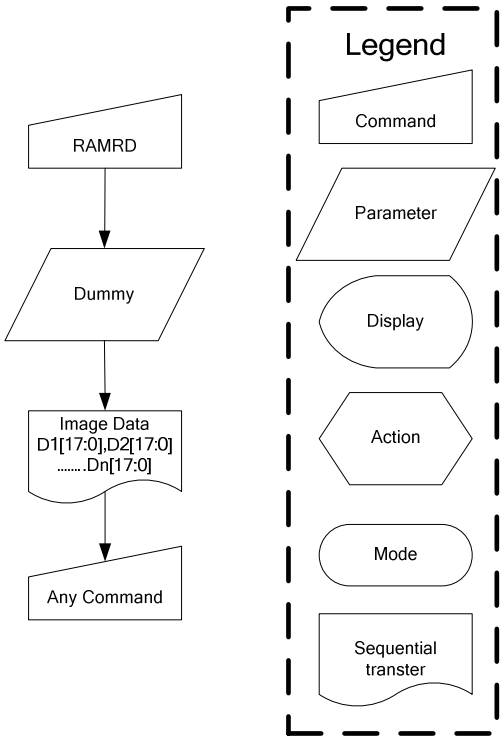
Flow Chart	

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9.1.24 PTLAR (30h): Partial Area

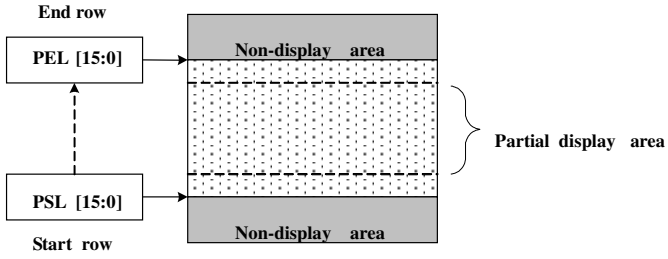
30H	PTLAR (Partial Area)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PTLAR	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)
1st parameter	1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	
2nd parameter	1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	
3rd parameter	1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	
4th parameter	1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	

Description

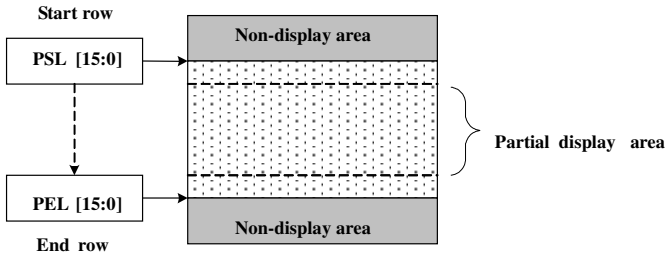
-This command defines the partial mode's display area.

-There are 4 parameters associated with this command, the first defines the Start Row (PSL) and the second the End Row (PEL), as illustrated in the figures below. PSL and PEL refer to the Frame Memory row address counter.

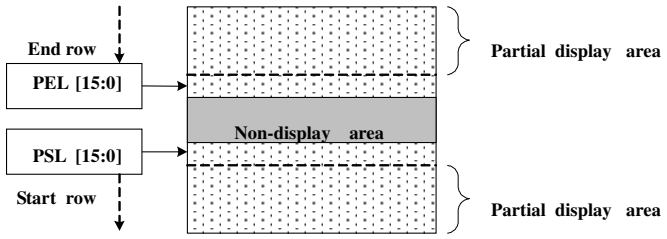
-If End Row > Start Row, when MADCTL ML='1'



-If End Row > Start Row, when MADCTL ML='0'



-If End Row < Start Row, when MADCTL ML='0'



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	-If End Row = Start Row then the Partial Area will be one row deep.
Restriction	Each detail initial value by the display resolution will be updated.

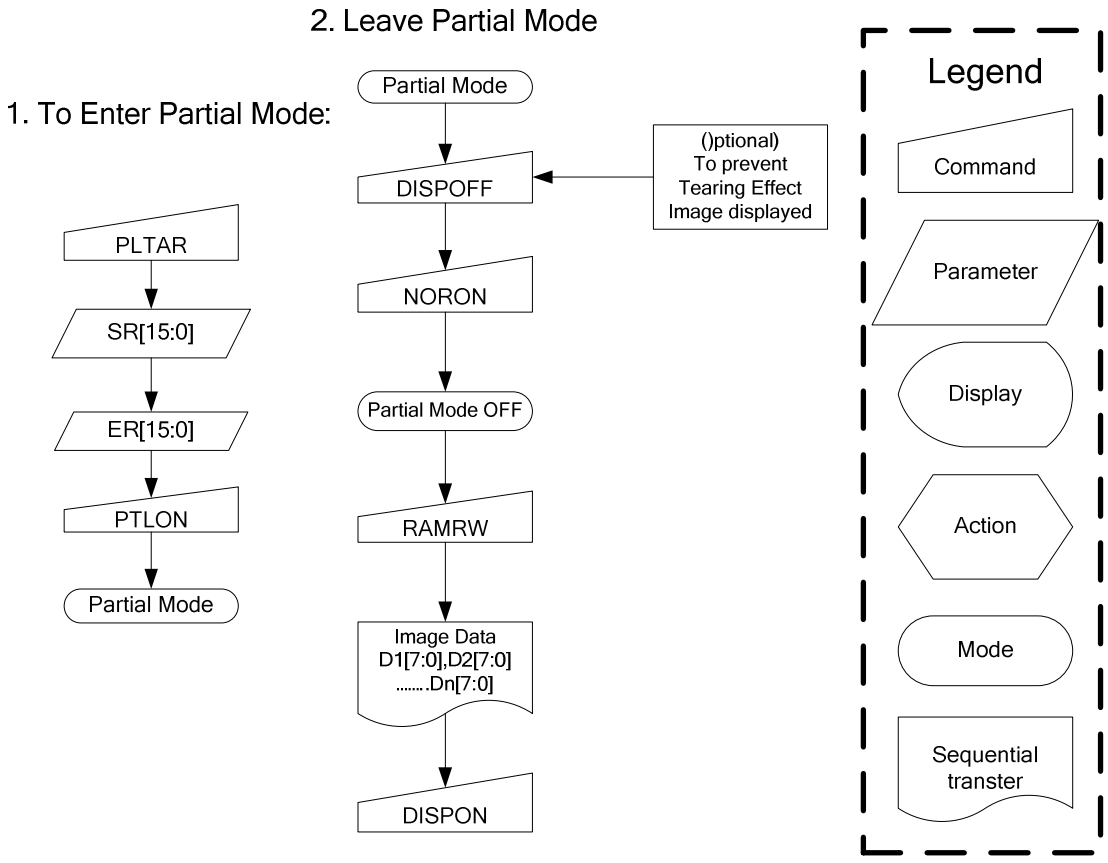
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	PSL[15:0]=0000h, PEL=013Fh
S/W Reset	PSL[15:0]=0000h, PEL=013Fh
H/W Reset	PSL[15:0]=0000h, PEL=013Fh

Flow Chart



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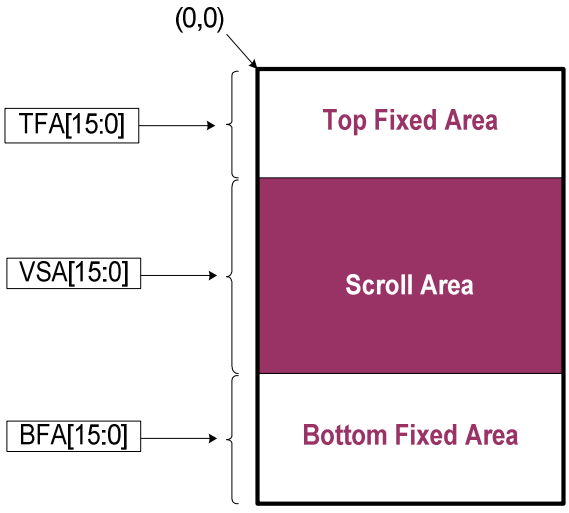
9.1.25 VSCRDEF (33h): Vertical Scrolling Definition

33H	(Vertical Scrolling Definition)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VSCRDEF	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)
1st parameter	1	↑	1	-	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8	
2nd parameter	1	↑	1	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	
3rd parameter	1	↑	1	-	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8	
4th parameter	1	↑	1	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	
5th parameter	1	↑	1		BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8	
6th parameter	1	↑	1		BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	
Description	-This command just defines the Vertical Scrolling Area of the display and not performs vertical scroll -When MADCTL MV=0 -The 1st & 2nd parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display). -The 3rd & 4th parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address) The first line appears immediately after the bottom most line of the Top Fixed Area. -The 4th & 5th parameter BFA [6:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer  												
Restriction	The condition is TFA+VSA+BFA = 320, otherwise Scrolling mode is undefined.												

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<table>
<tr><td></td><td>In Vertical Scrolling Mode, MADCTL parameter MV should be set to ‘0’ – this only affects the Frame Memory write.</td></tr>
<tr><td>Register availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th colspan="3">Default Value</th></tr>
<tr><td>Power On Sequence</td><td>TFA[15:0] = 0000h</td><td>VSA[0:15] = 0140h</td><td>BFA[15:0] = 0000h</td></tr>
<tr><td>S/W Reset</td><td>TFA[15:0] = 0000h</td><td>VSA[0:15] = 0140h</td><td>BFA[15:0] = 0000h</td></tr>
<tr><td>H/W Reset</td><td>TFA[15:0] = 0000h</td><td>VSA[0:15] = 0140h</td><td>BFA[15:0] = 0000h</td></tr>
</table>
</td></tr>
</table>

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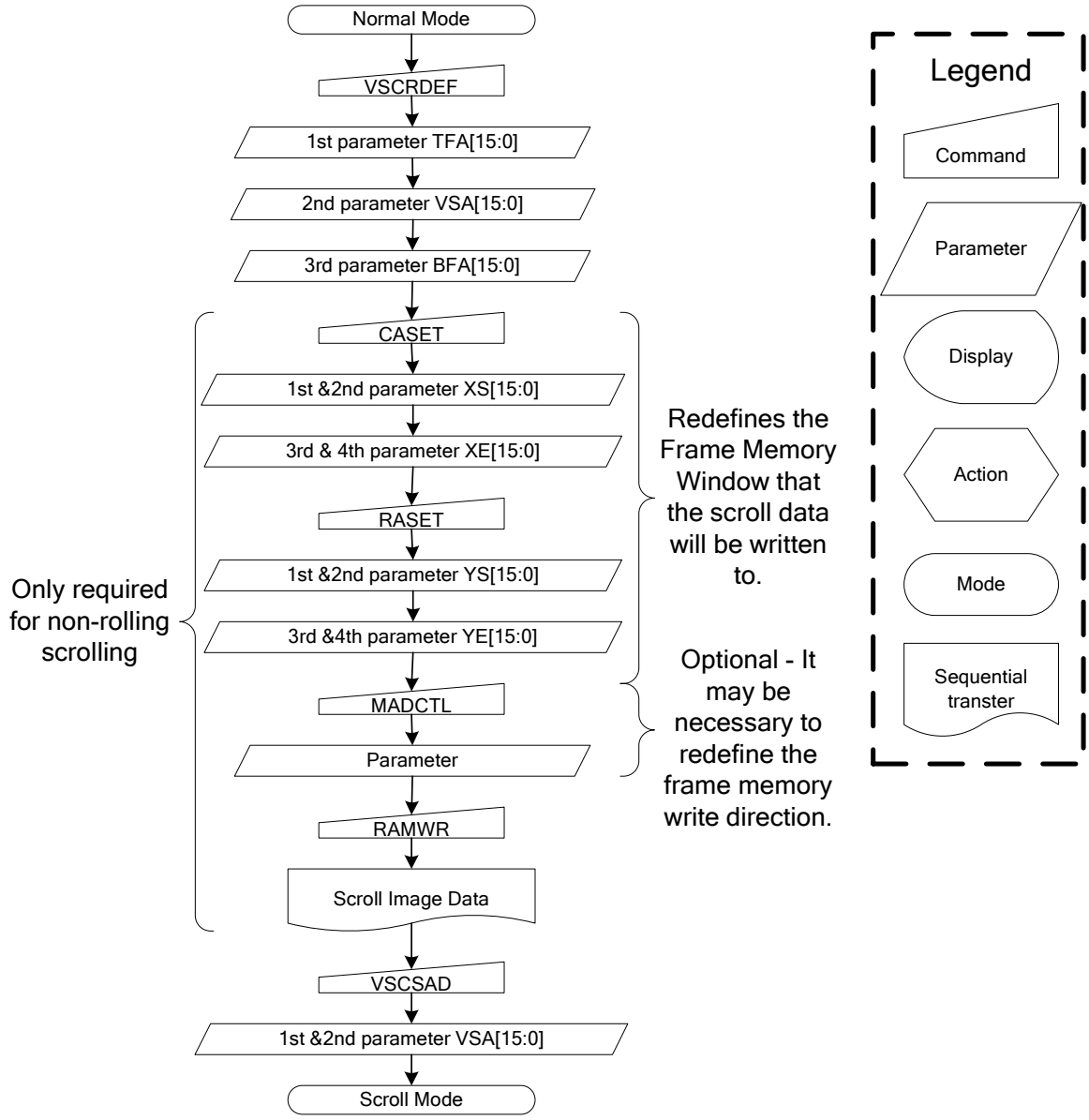
Flow Chart

1. TO Enter Vertical Scroll Mode:



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9.1.26 TEOFF (34h): Tearing Effect Line OFF

34H	TEOFF (Tearing Effect Line OFF)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)
parameter	No Parameter												
Description	-This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.												
Restriction	This command has no effect when tearing effect output is already off..												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
S/W Reset	Off
H/W Reset	Off

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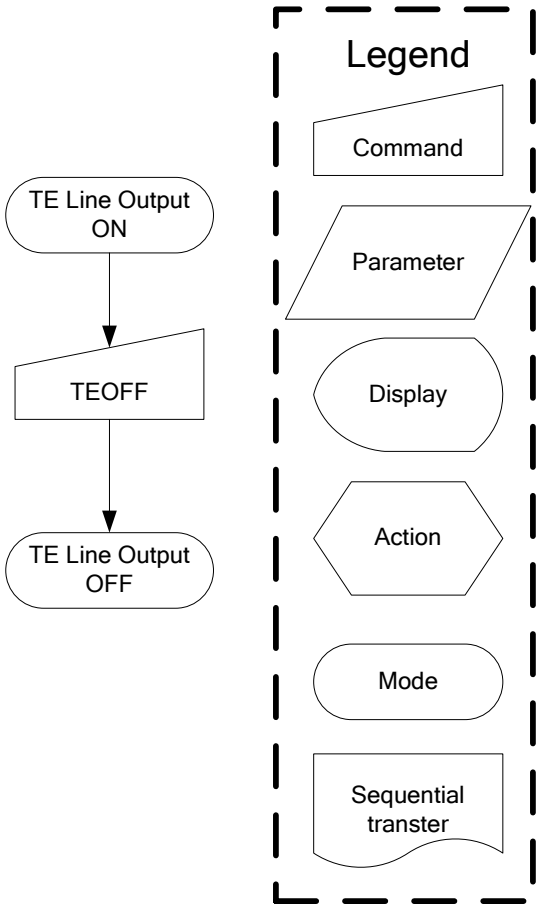
Flow Chart



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9.1.27 TEON (35h): Tearing Effect Line On

35H	TEON (Tearing Effect Line On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TEON	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)
parameter	1	↑	1	-	0	0	0	0	0	0	0	TEM	

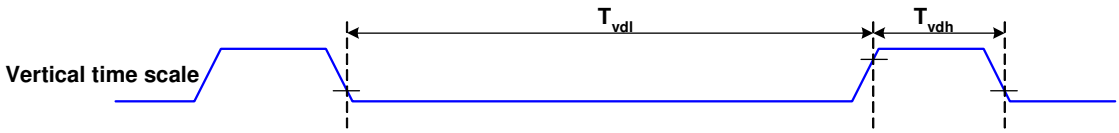
Description

-This command is used to turn ON the Tearing Effect output signal from the TE signal line.

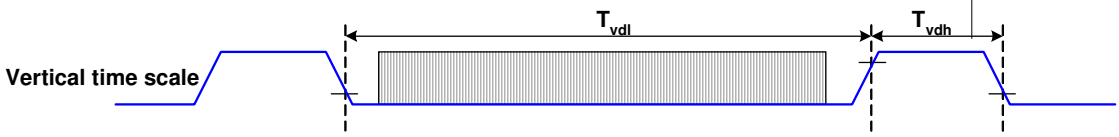
-This output is not affected by changing MADCTL bit ML.

-The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line:

-When TEM =’0’: The Tearing Effect output line consists of V-Blanking information only



-When TEM =’1’: The Tearing Effect output Line consists of both V-Blanking and H-Blanking information



Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

This command has no effect when tearing effect output is already on.

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
S/W Reset	Off
H/W Reset	Off

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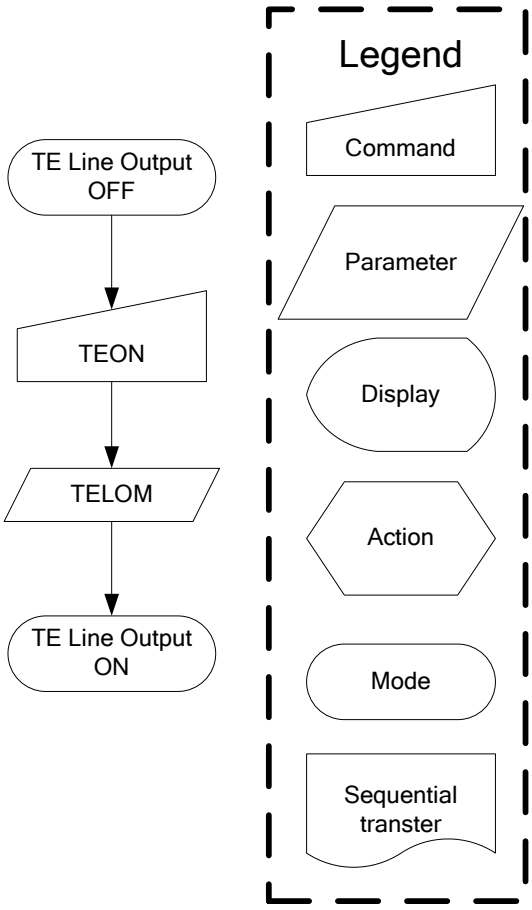
Flow Chart	

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9.1.28 MADCTL (36h): Memory Data Access Control

36H	MADCTL (Memory Data Access Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MADCTL	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)
parameter	1	↑	1	-	MY	MX	MV	ML	RGB	MH	-	-	

Description

-This command defines read/ write scanning direction of frame memory.

Bit	NAME	DESCRIPTION
D7	MY	Page Address Order
D6	MX	Column Address Order
D5	MV	Page/Column Order
D4	ML	Line Address Order
D3	RGB	RGB/BGR Order
D2	MH	Display Data Latch Order

-Bit Assignment

Bit D7- Page Address Order

"0" = Top to Bottom (When MADCTL D7="0").

"1" = Bottom to Top (When MADCTL D7="1").

Bit D6- Column Address Order

"0" = Left to Right (When MADCTL D6="0").

"1" = Right to Left (When MADCTL D6="1").

Bit D5- Page/Column Order

"0" = Normal Mode (When MADCTL D5="0").

"1" = Reverse Mode (When MADCTL D5="1")

Note: Bits D7 to D5, alse refer to section 8.12 Address Control

Bit D4- Line Address Order

"0" = LCD Refresh Top to Bottom (When MADCTL D4="0")

"1" = LCD Refresh Bottom to Top (When MADCTL D4="1")

Bit D3- RGB/BGR Order

"0" = RGB (When MADCTL D3="0")

"1" = BGR (When MADCTL D3="1")

Bit D2- Display Data Latch Data Order

"0" = LCD Refresh Left to Right (When MADCTL D2="0")

"1" = LCD Refresh Right to Left (When MADCTL D2="1")

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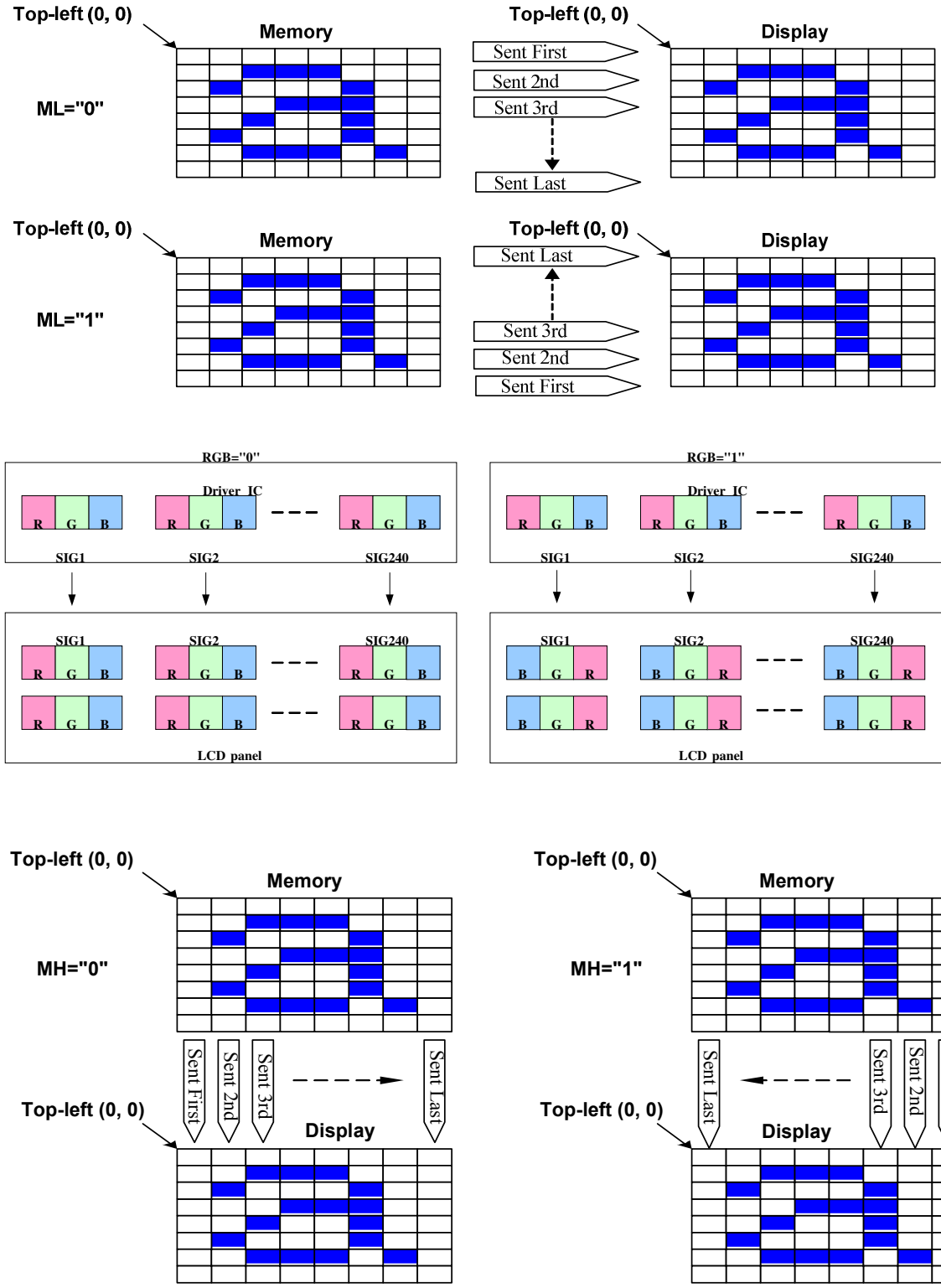

Restriction	
Register	

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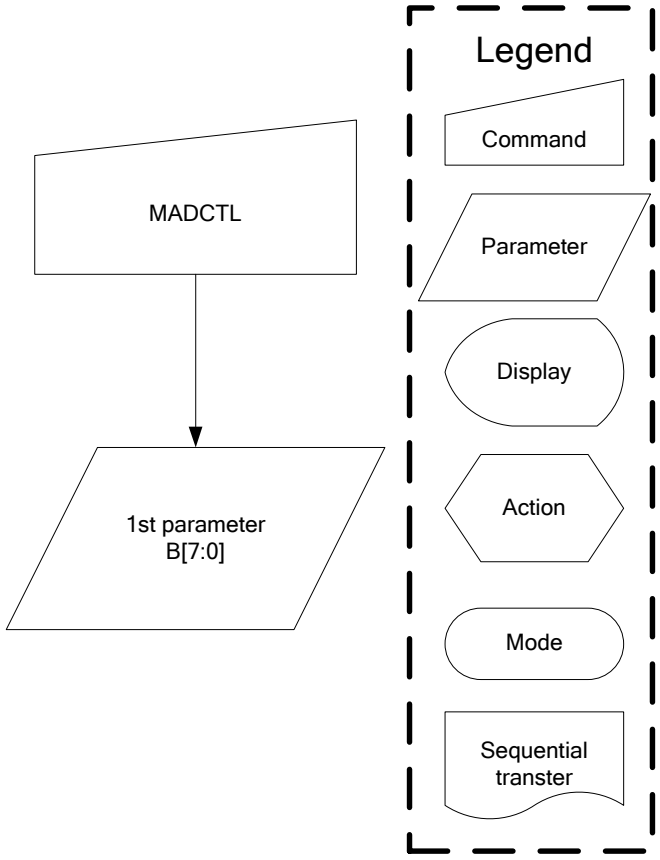
availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	No change
H/W Reset	0000h

Flow Chart



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9.1.29 VSCSAD (37h): Vertical Scroll Start Address of RAM

37H	VSCSAD (Vertical Scroll Start Address of RAM)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VSCSAD	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)
1ST parameter	1	↑	1	-	VSP15	VSP14	VSP13	VSP12	VSP11	VSP10	VSP9	VSP8	
2ND parameter	1	↑	1	-	VSP7	VSP6	VSP5	VSP4	VSP3	VSP2	VSP1	VSP0	

Description

-This command is used together with Vertical Scrolling Definition (33h).

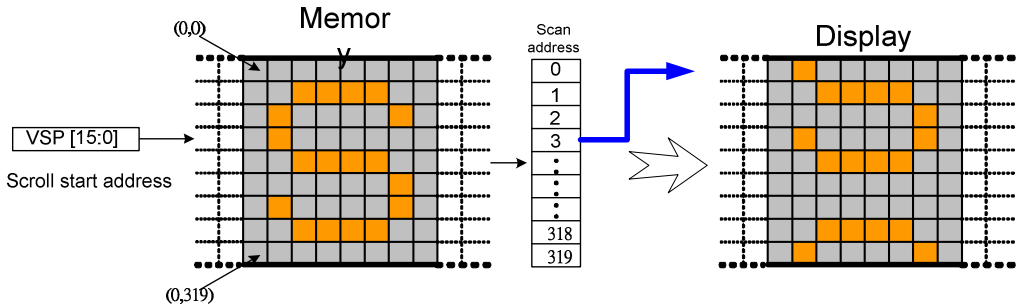
-These two commands describe the scrolling area and the scrolling mode.

-The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:

When ML=0

Example:

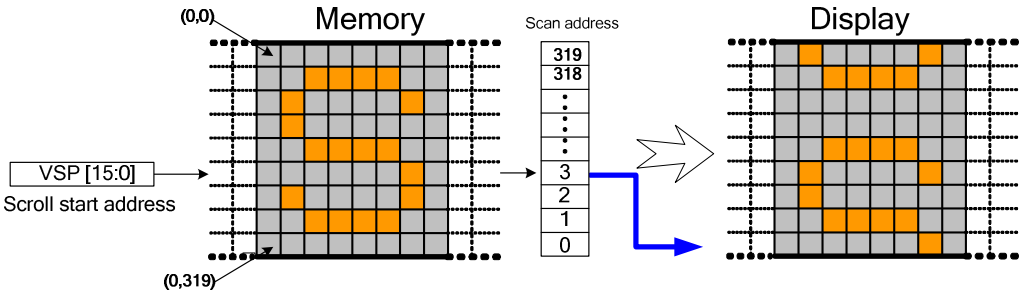
When Top Fixed Area = Bottom Fixed Area = 00, vertical Scrolling Area = 320 and VSP = '3'



When ML=1

Example:

When Top Fixed Area = Bottom Fixed Area = 00, vertical Scrolling Area = 320 and VSP = '3'



NOTE: When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.

VSP refers to the Frame Memory line Pointer

Restriction

Since the value of the vertical scrolling start address is absolute (with reference to the frame memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h)- otherwise undesirable image will be displayed on the panel)

Register

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availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart

See Vertical Scrolling Definition (33h) description

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9.1.30 IDMOFF (38h): Idle Mode Off

<table>
<tr><td>38H</td><td colspan="13">IDMOFF (Idle Mode Off)</td></tr>
<tr><td>Inst / Para</td><td>D/CX</td><td>WRX</td><td>RDX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>IDMOFF</td><td>0</td><td>↑</td><td>1</td><td>-</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>(38h)</td></tr>
<tr><td>parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">-This command is used to recover from Idle mode on.
-In the idle off mode,
1. LCD can display 4096, 65k or 262k colors.
2. Normal frame frequency is applied.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode</td></tr>
<tr><td>Register availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Idle mode off</td></tr><tr><td>S/W Reset</td><td>Idle mode off</td></tr><tr><td>H/W Reset</td><td>Idle mode off</td></tr></table></td></tr>
</table>

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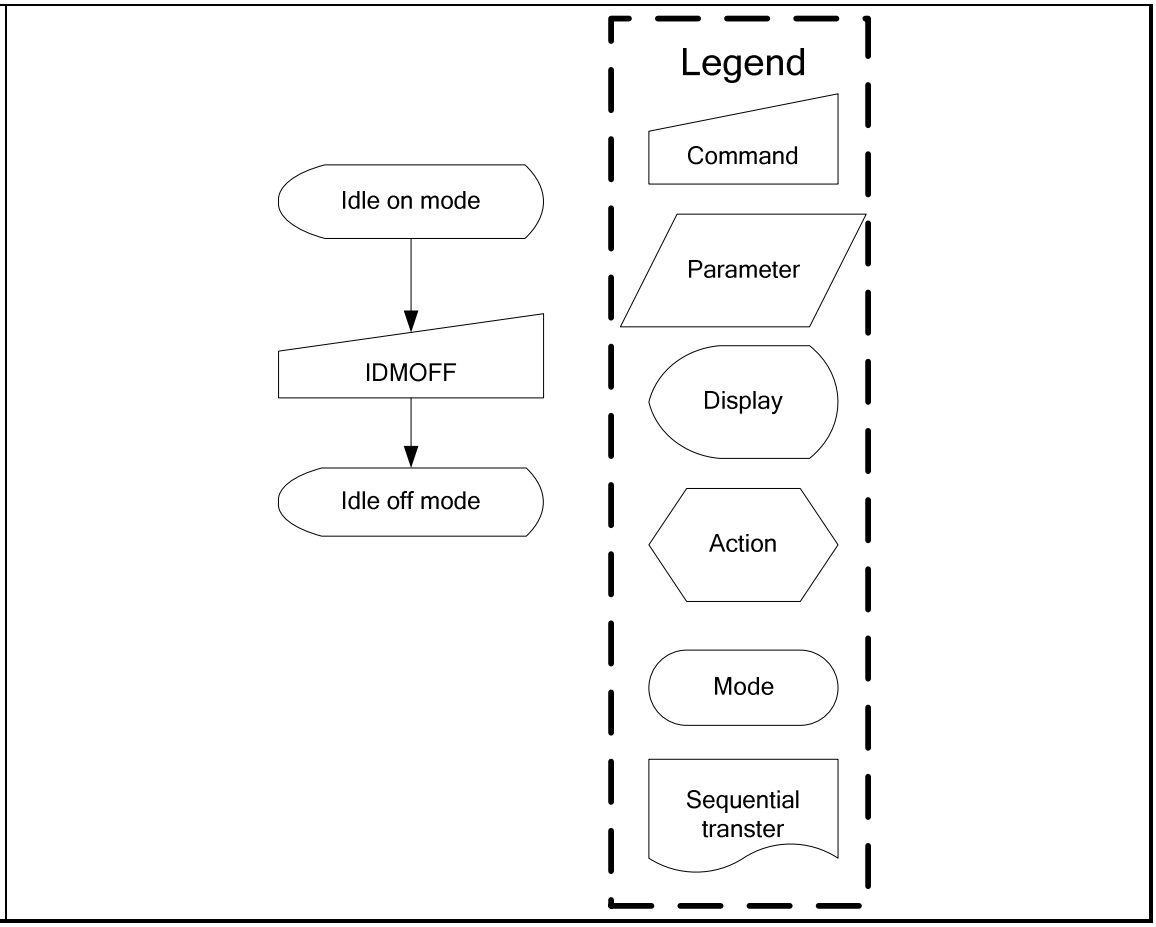
Flow Chart	

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9.1.31 IDMON (39h): Idle mode on

39H	IDMON (Idle Mode On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IDMON	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)
parameter	No Parameter												

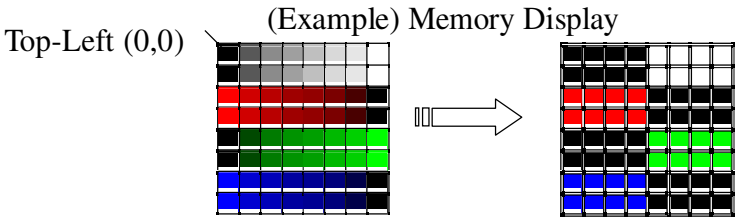
Description

-This command is used to enter into Idle mode on.

-There will be no abnormal visible effect on the display mode change transition.

-In the idle on mode,

1. Color expression is reduced. The primary and the secondary colors using MSB of each R,G and B in the Frame Memory, 8 color depth data is displayed.
2. 8-Color mode frame frequency is applied.
3. Exit from IDMON by Idle Mode Off (38h) command



Color	R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B4 B1 B0
Black	0xxxxx	0xxxxx	0xxxxx
Blue	0xxxxx	0xxxxx	1xxxxx
Red	1xxxxx	0xxxxx	0xxxxx
Magenta	1xxxxx	0xxxxx	1xxxxx
Green	0xxxxx	1xxxxx	0xxxxx
Cyan	0xxxxx	1xxxxx	1xxxxx
Yellow	1xxxxx	1xxxxx	0xxxxx
White	1xxxxx	1xxxxx	1xxxxx

Restriction: This command has no effect when module is already in idle off mode

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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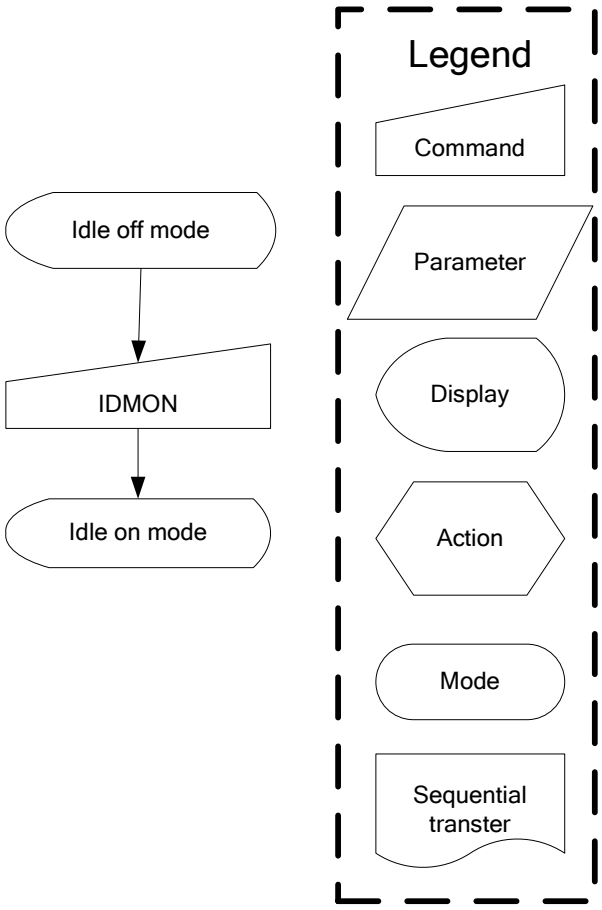
Default

Status	Default Value
Power On Sequence	Idle mode off
S/W Reset	Idle mode off
H/W Reset	Idle mode off

Flow Chart



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9.1.32 COLMOD (3Ah): Interface Pixel Format

3AH	COLMOD (Interface Pixel Format)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
COLMOD	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)
1st Parameter	1	↑	1	-	0	D6	D5	D4	0	D2	D1	D0	

Description

This command is used to define the format of RGB picture data, which is to be transferred via the MCU interface. The formats are shown in the table:

1st parameter:

Bit	Description	
D7	-	Set to '0'
D6	RGB interface color format	'101' = 65K of RGB interface '110' = 262K of RGB interface
D5		
D4		
D3	-	Set to '0'
D2	Control interface color format	'011' = 12bit/pixel '101' = 16bit/pixel '110' = 18bit/pixel '111' = 16M truncated
D1		
D0		

Note1: In 12-bit/Pixel, 16-bit/Pixel or 18-bit/Pixel mode, the LUT is applied to transfer data into the Frame Memory.
Note2: The Command 3Ah should be set at 55h when writing 16-bit/pixel data into frame memory, but 3Ah should be re-set to 66h when reading pixel data from frame memory.

Restriction

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	18bit/pixel
S/W Reset	No change
H/W Reset	18bit/pixel

Flow Chart

See Vertical Scrolling Definition (33h) description

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9.1.33 WRMEMC (3Ch): Write Memory Continue

3CH	WRMEMC (Write Memory Continue)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRMEMC	0	↑	1	-	0	0	1	1	1	1	0	0	(3Ch)
1ST parameter	1	↑	1	D1[17]-D1[8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	
⋮	1	↑	1	Dx[17]-Dx[8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	
Nth parameter	1	↑	1	Dn[17]-Dn[8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	

Description

-This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write memory continue or memory write command.

-If MV=0:

Data is written continuing from the pixel location after the write range of the previous memory write or write memory continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the end column (XE) value. The column register is then reset to XS and the page register is incremented. Pixels are written to the frame memory until the page register equals the end page (YE) value and the column register equals the XE value, or the host processor sends another command. If the number of pixels exceeds (XE-XS+1)*(YE-YS+1) the extra pixels are ignored.

If MV=1:

Data is written continuing from the pixel location after the write range of the previous memory write or write memory continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the end page (YE) value. The page register is then reset to YS and the column register is incremented. Pixels are written to the frame memory until the column register equals the end column (XE) value and the page register equals the YE value, or the host processor sends another command. If the number of pixels exceeds (XE-XS+1)*(YE-YS+1) the extra pixels are ignored.

Restriction

A memory write should follow a column address set or page address set to define the write address. Otherwise, data written with write memory continue is written to undefined addresses.

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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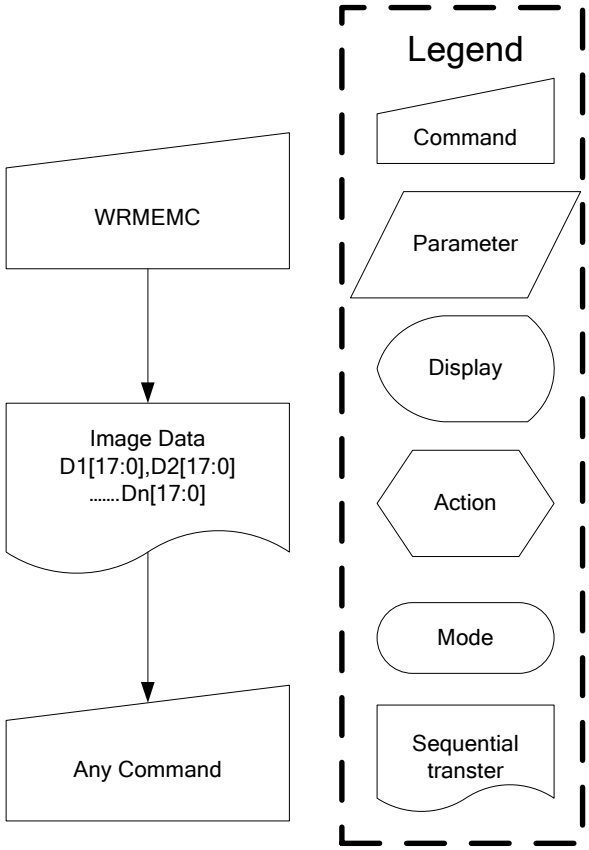
Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart



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9.1.34 RDMEMC (3Eh): Read Memory Continue

3EH	RDMEMC (Read Memory Continue)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDMEMC	0	↑	1	-	0	0	1	1	1	1	1	0	(3Eh)
1ST parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	D1[17]-D1[8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	
⋮	1	1	↑	Dx[17]-Dx[8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	
Nth parameter	1	1	↑	Dn[17]-Dn[8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	

Description

-This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous read memory continue or memory read command.

-If MV=0:

Pixels are read continuing from the pixel location after the read range of the previous memory read or read memory continue. The column register is then incremented and pixels are read from the frame memory until the column register equals the end column (XE) value. The column register is then reset to XS and the page register is incremented. Pixels are read from the frame memory until the page register equals the end page (YE) value and the column register equals the XE value, or the host processor sends another command.

If MV=1:

Pixels are read continuing from the pixel location after the read range of the previous memory read or read memory continue. The page register is then incremented and pixels are read from the frame memory until the page register equals the end page (YE) value. The page register is then reset to YS and the column register is incremented. Pixels are read from the frame memory until the column register equals the end column (XE) value and the page register equals the YE value, or the host processor sends another command.

Restriction

Regardless of the color mode set in interface pixel format, the pixel format returned by read memory continue is always 18-bit so there is no restriction on the length of data

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared

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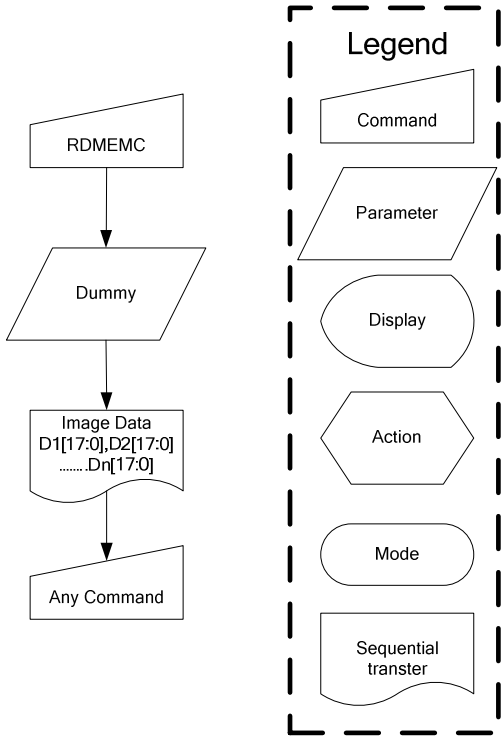
	H/W Reset | Contents of memory is not cleared
Flow Chart	

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9.1.35 STE (44h): Set Tear Scanline

44H	STE (Set Tear ScanLine)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
STE	0	↑	1	-	0	1	0	0	0	1	0	0	(44h)
1st parameter	1	↑	1	-	N15	N14	N13	N12	N11	N10	N9	N8	
2nd parameter	1	↑	1	-	N7	N6	N5	N4	N3	N2	N1	N0	

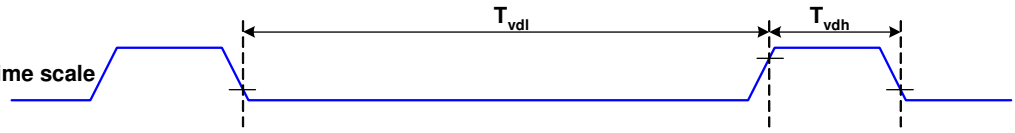
Description

-This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N. The TE signal is not affected by changing MV.

-The tearing effect line on has one parameter that describes the tearing effect output line mode.

-The tearing effect output line consist of V-blanking information only.

Vertical time scale



Note that set tear scanline with N=0 is equivalent to tearing effect line on with TEM=0.

The tearing effect output line shall be active low when the display module is in sleep mode

Restriction

This command takes affect on the frame following the current frame. Therefore, if the tear effect (TE) output is already on, the TE output shall continue to operate as programmed by the previous tearing effect line on or set tear scanline command until the end of the frame

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

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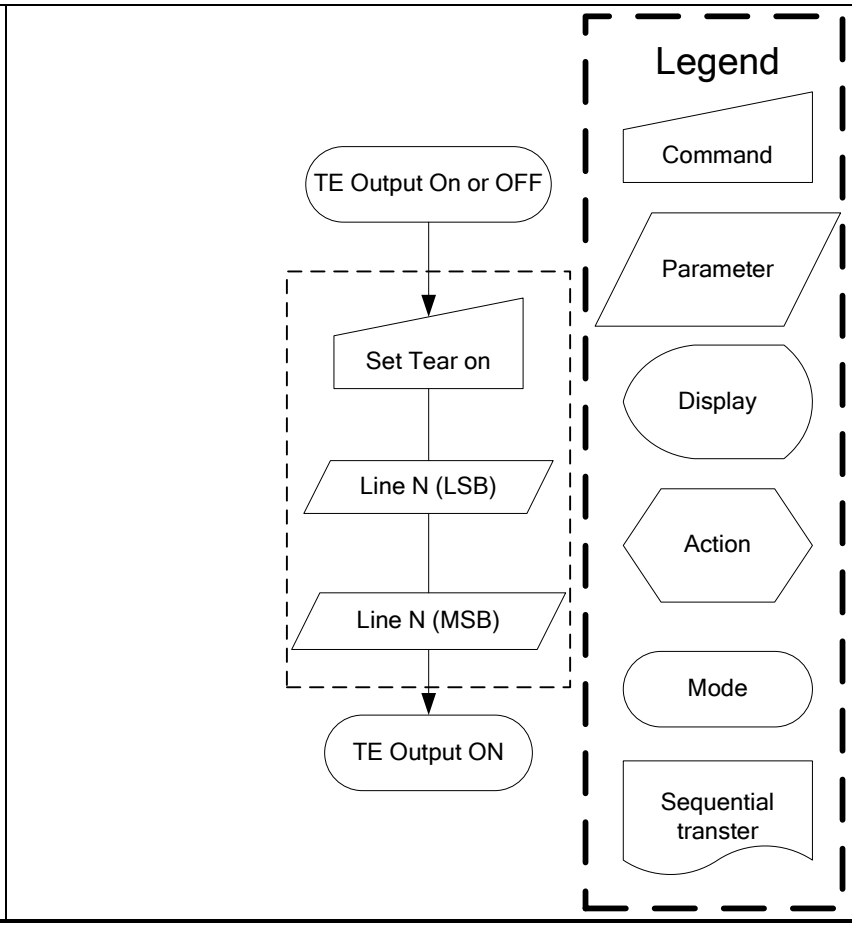
Flow Chart



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9.1.36 GSCAN (45h): Get Scanline

45H	GSCAN (Get ScanLine)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GSCAN	0	↑	1	-	0	1	0	0	0	1	0	1	(45h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	N15	N14	N13	N12	N11	N10	N9	N8	
3rd parameter	1	1	↑	-	N7	N6	N5	N4	N3	N2	N1	N0	
Description	-The display module returns the current scanline ,N, used to update the display device. The total number of scanlines on a display device is defined as VSYNC+VBP+VACT+VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0. -When in sleep in mode, the value returned by get scanline is undefined.												
Restriction	-												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

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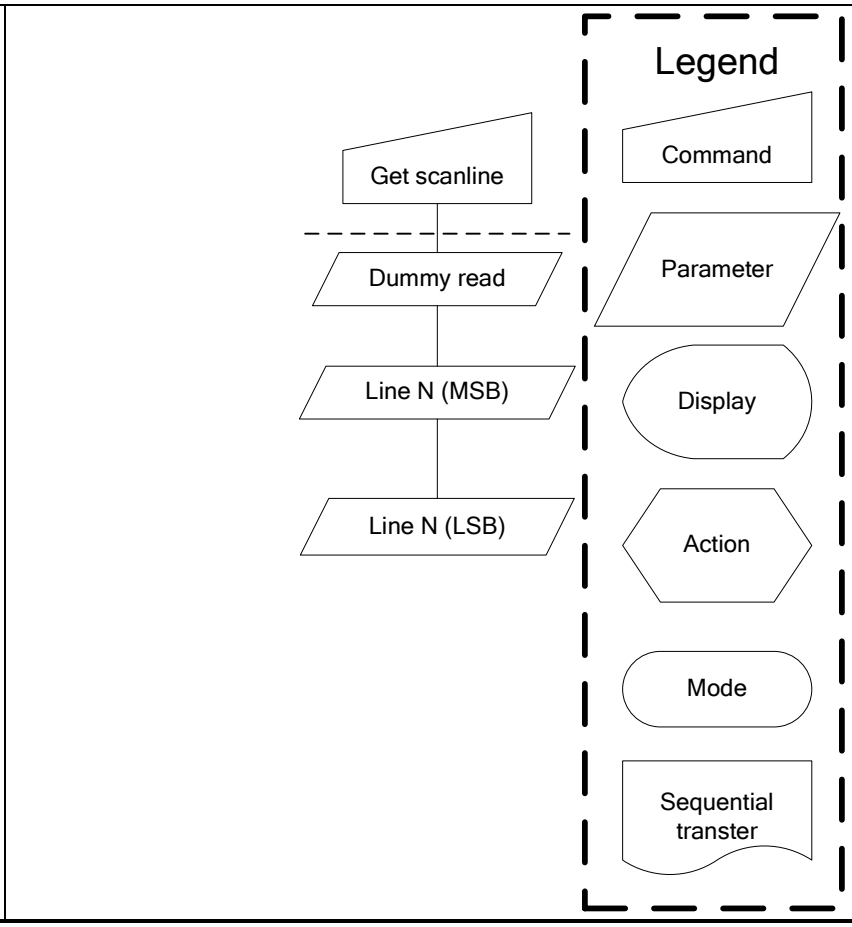
Flow Chart	

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9.1.37 WRDISBV (51h): Write Display Brightness

51H	WRDISBV (Write Display Brightness)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRDISBV	0	↑	1	-	0	1	0	1	0	0	0	1	(51h)
Parameter	1	↑	1	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	
Description	-This command is used to adjust the brightness value of the display. -It should be checked what the relationship between this written value and output brightness of the display is. This relationship is defined on the display module specification. -In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.												
Restriction													

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

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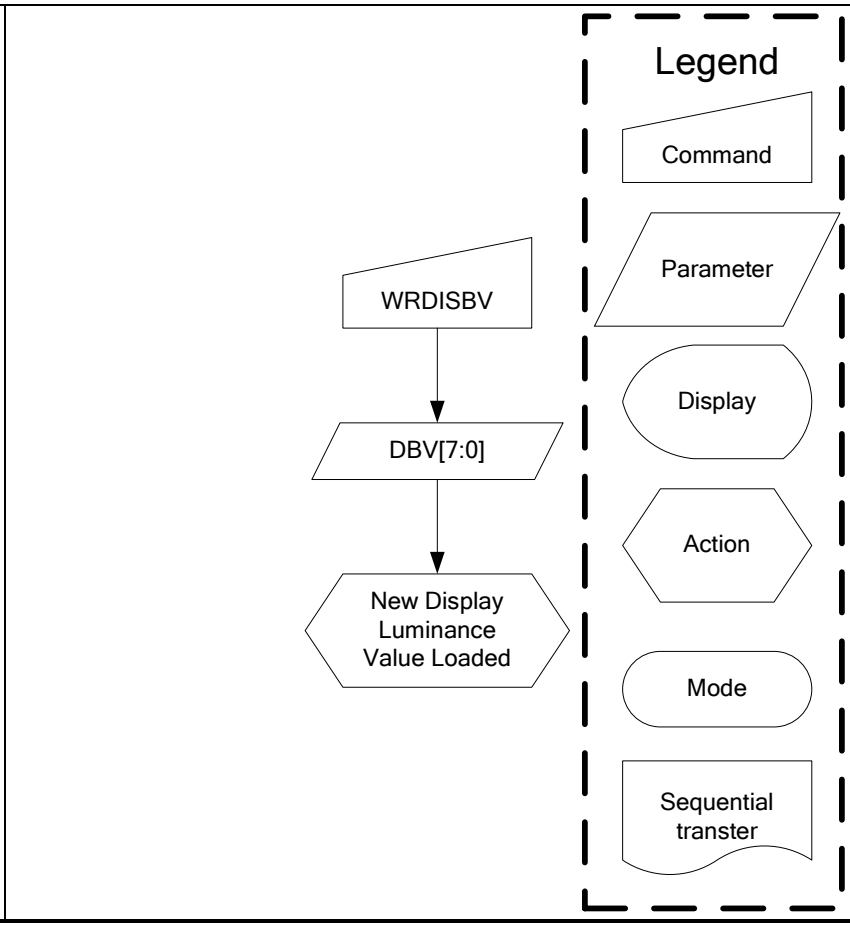
Flow Chart	

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9.1.38 RDDISBV (52h): Read Display Brightness Value

52H	RDDISBV (Read Display Brightness Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDISBV	0	↑	1	-	0	1	0	1	0	0	1	0	(52h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	
Description	-This command returns the brightness value of the display. -It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification is. -In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. -DBV[7:0] is reset when display is in sleep in mode. -DBV[7:0] is '0' when bit BCTRL of write CTRL display command (53h) is '0' -DBV[7:0] IS manual set brightness specified with write CTRL display command (53h) when bit BCTRL is '1'												
Restriction	-												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

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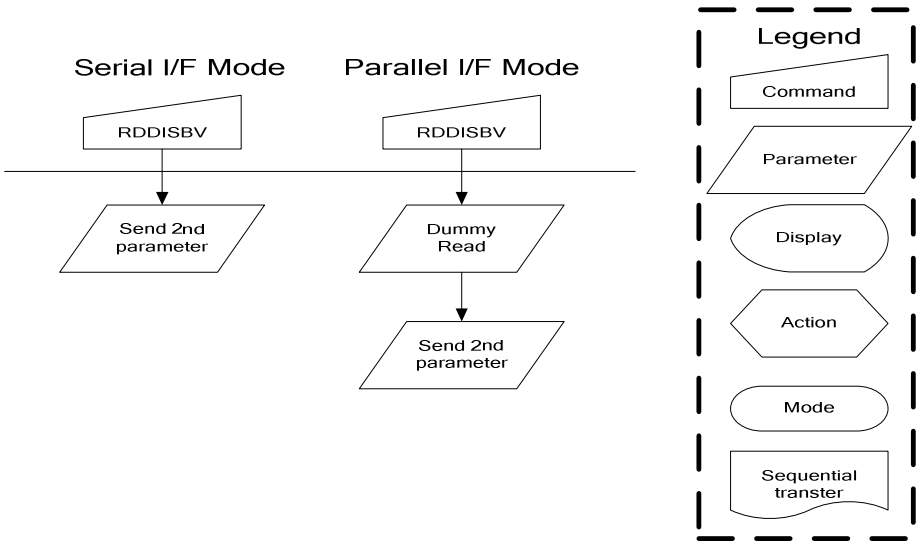
Flow Chart	

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9.1.39 WRCTRLD (53h): Write CTRL Display

53H	WRCTRLD (Write CTRL Display)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRCTRLD	0	↑	1	-	0	1	0	1	0	0	1	1	(53h)
Parameter	1	↑	1	-	0	0	BCTRL	0	DD	BL	0	0	
Description	-This command is used to control display brightness. -BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off (Brightness register are 00h, DBV[7:0]) 1 = On (Brightness register are active, according to the other parameters.) -DD: Display Dimming (Only for manual brightness setting) DD = 0: Display Dimming is off. DD = 1: Display Dimming is on. -BL: Backlight Control On/Off 0 = Off (Completely turn off backlight circuit. Control lines must be low.) 1 = On -Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1. -When BL bit changed from 'on' to 'off', backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.												
Restriction													

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

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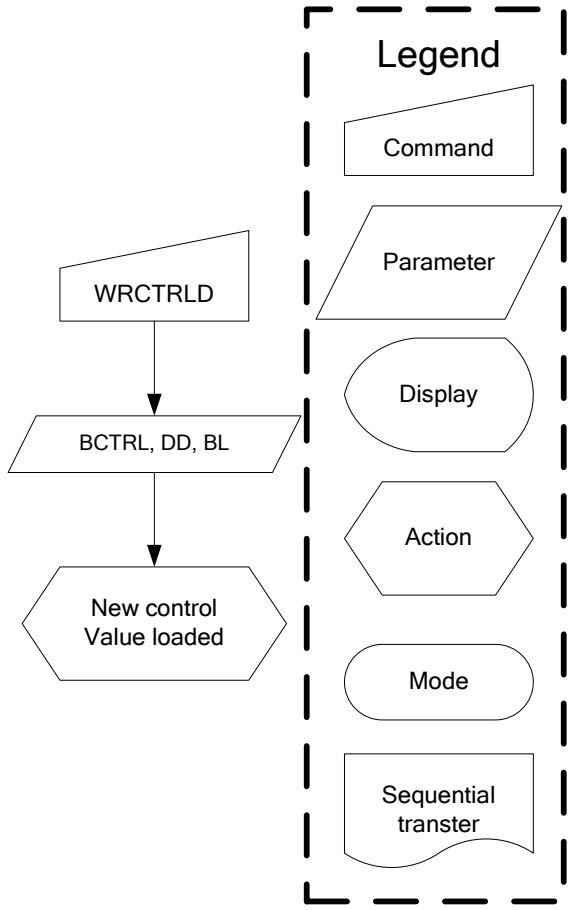
Flow Chart	

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9.1.40 RDCTRLD (54h): Read CTRL Value Display

54H	RDCTRLD (Read CTRL value Display)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDCTRLD	0	↑	1	-	0	1	0	1	0	1	0	0	(54h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	0	0	BCTRL	0	DD	BL	0	0	

Description

-This command returns ambient light and brightness control values..

-BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.

0 = Off

1 = On

-DD: Display Dimming (Only for manual brightness setting)

DD = 0

DD = 1

-BL: Backlight Control On/Off

0 = Off

1 = On

Restriction

-

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

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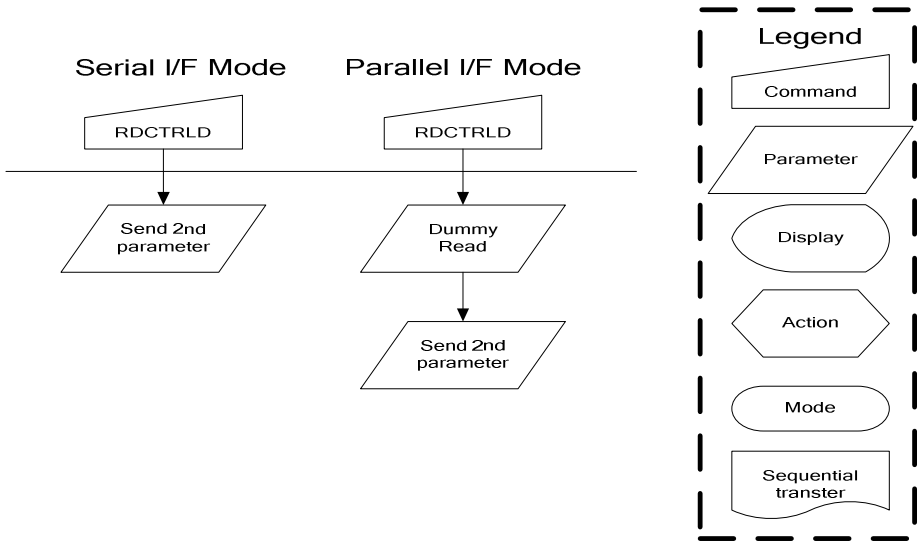
Flow Chart	

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9.1.41 WRCACE (55h): Write Content Adaptive Brightness Control and Color Enhancement

55H	WRCACE (Write Content Adaptive Brightness Control and Color Enhancement)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRCACE	0	↑	1	-	0	1	0	1	0	1	0	1	(55h)
Parameter	1	↑	1	-	CECTRL	0	CE1	CE0	0	0	C1	C0	

Description

-This command is used to set parameters for image content based adaptive brightness control functionality and Color Enhancement function.

-There is possible to used 4 different modes for content adaptive image functionality, which are defined on a table below.

C1	C0	Function
0	0	Off
0	1	User Interface Mode
1	0	Still Picture
1	1	Moving Image

-CECTRL: Color Enhancement Control Bit:

CECTRL=0: Color Enhancement Off.

CECTRL=1: Color Enhancement On.

-There are three color enhancement levels can be set.

CE1	CE0	Color enhancement level
0	0	Low enhancement
0	1	Medium enhancement
1	1	High enhancement

'-': Don't care

Restriction

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

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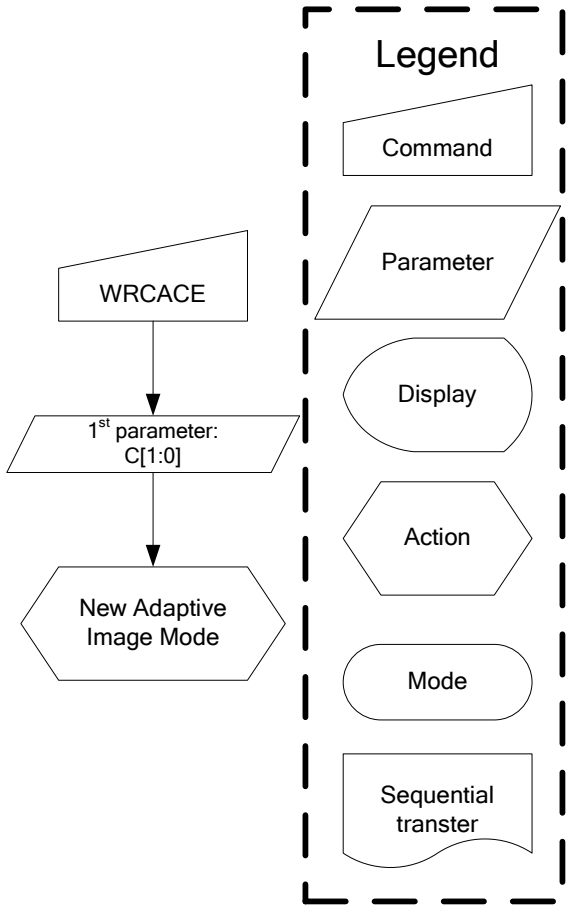
Flow Chart	

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9.1.42 RDCABC (56h): Read Content Adaptive Brightness Control

56H	RDCABC (Read Content Adaptive Brightness Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDCABC	0	↑	1	-	0	1	0	1	0	1	1	0	(56h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	0	0	0	0	0	0	C1	C0	

Description

-This command is used to read the settings for image content based adaptive brightness control functionality.

-There is possible to used 4 different modes for content adaptive image functionality, which are defined on a table below.

C1	C0	Function
0	0	Off
0	1	User Interface Mode
1	0	Still Picture
1	1	Moving Image

'-': Don't care

Restriction

-

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

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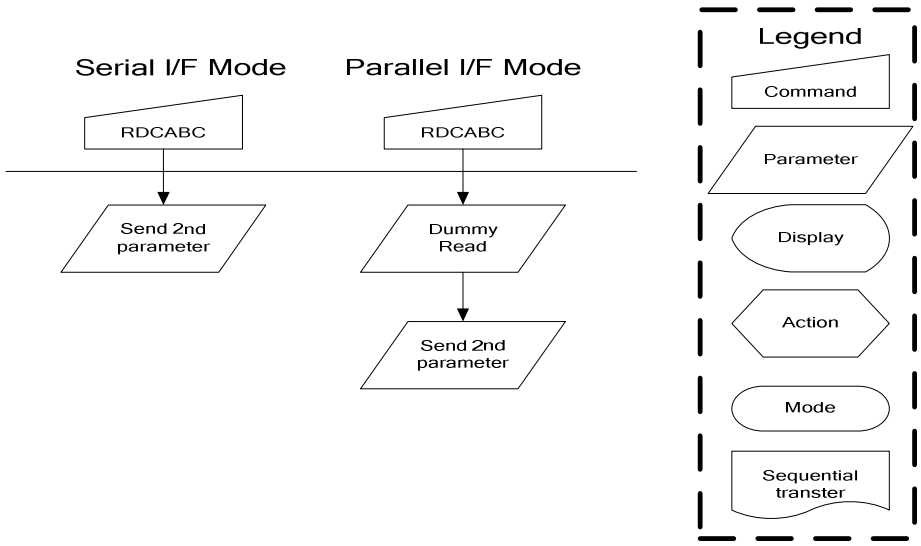
Flow Chart	

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9.1.43 WRCABCMB (5Eh): Write CABC Minimum Brightness

5EH	WRCABCMB (Write CABC Minimum Brightness)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRCABCMB	0	↑	1	-	0	1	0	1	1	1	1	0	(5Eh)
Parameter	1	↑	1	-	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	
Description	-This command is used to set the minimum brightness value of the display for CABC function. -In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the brightness for CABC. '-': Don't care												
Restriction													

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

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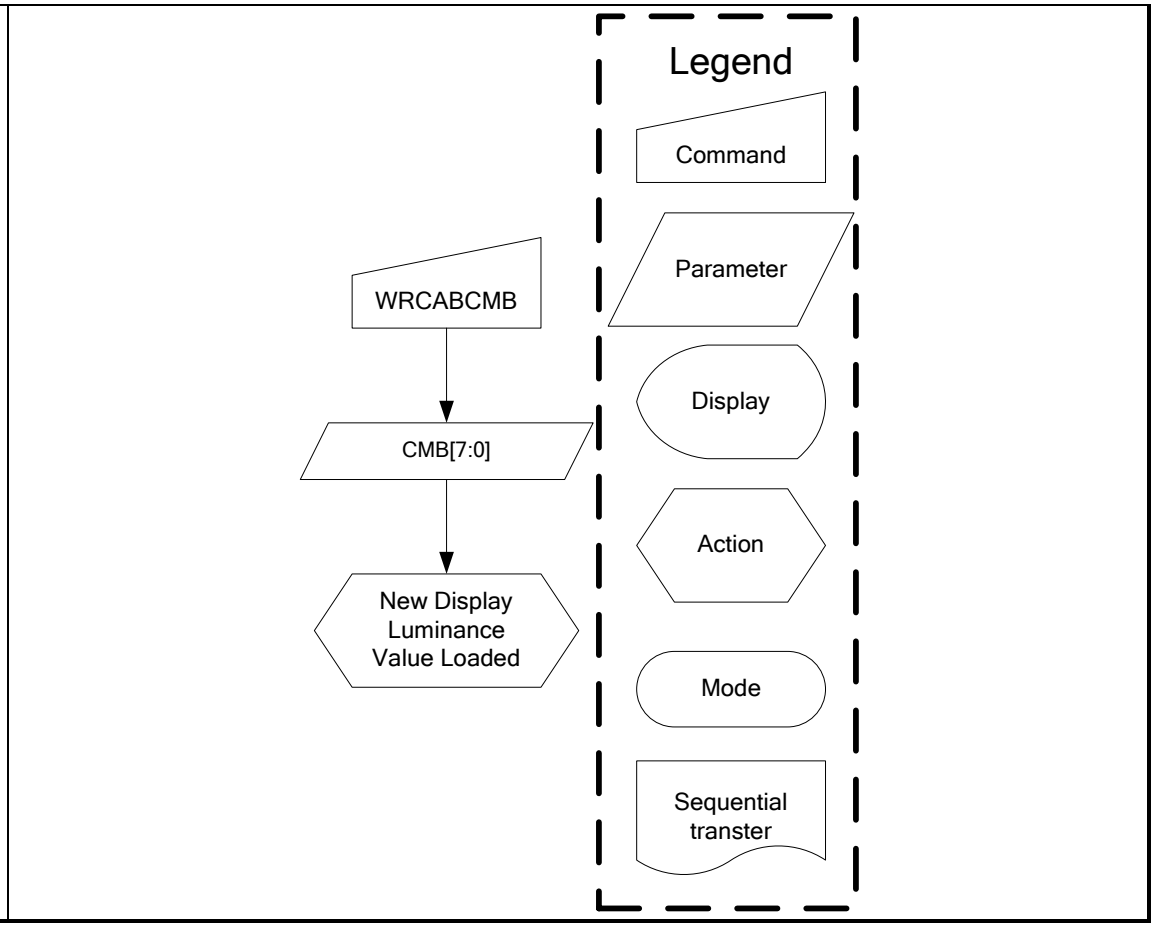
Flow Chart	

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9.1.44 RDCABCMB (5Fh): Read CABC Minimum Brightness

5FH	RDCABCMB (Read CABC Minimum Brightness)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDCABCMB	0	↑	1	-	0	1	0	1	1	1	1	1	(5Fh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	
Description	-This command returns the minimum brightness value of CABC function. -In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the brightness for CABC. '-': Don't care												
Restriction	-												

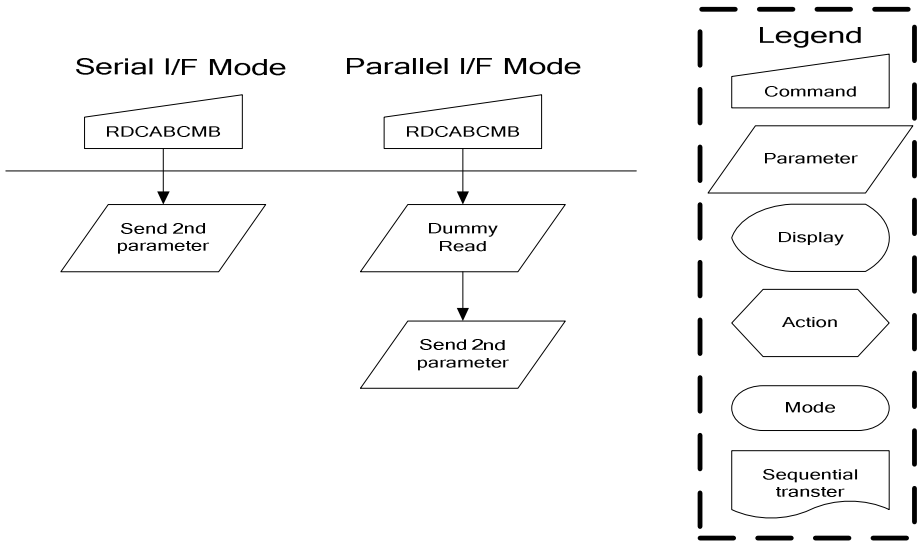
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart



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9.1.45 RDABCSDR (68h): Read Automatic Brightness Control Self-Diagnostic Result

68H	RDABCSDR (Read Automatic Brightness Control Self-Diagnostic Result)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDABCSDR	0	↑	1	-	0	1	1	0	1	0	0	0	(68h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	D6	0	0	0	0	0	0	-

Description

This command indicates the current status of the display self-diagnostic results for automatic brightness control after sleep out -command as described below:

-D7: Register loading detection

-D6: Functionality detection

"-" Don't care

Restriction

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

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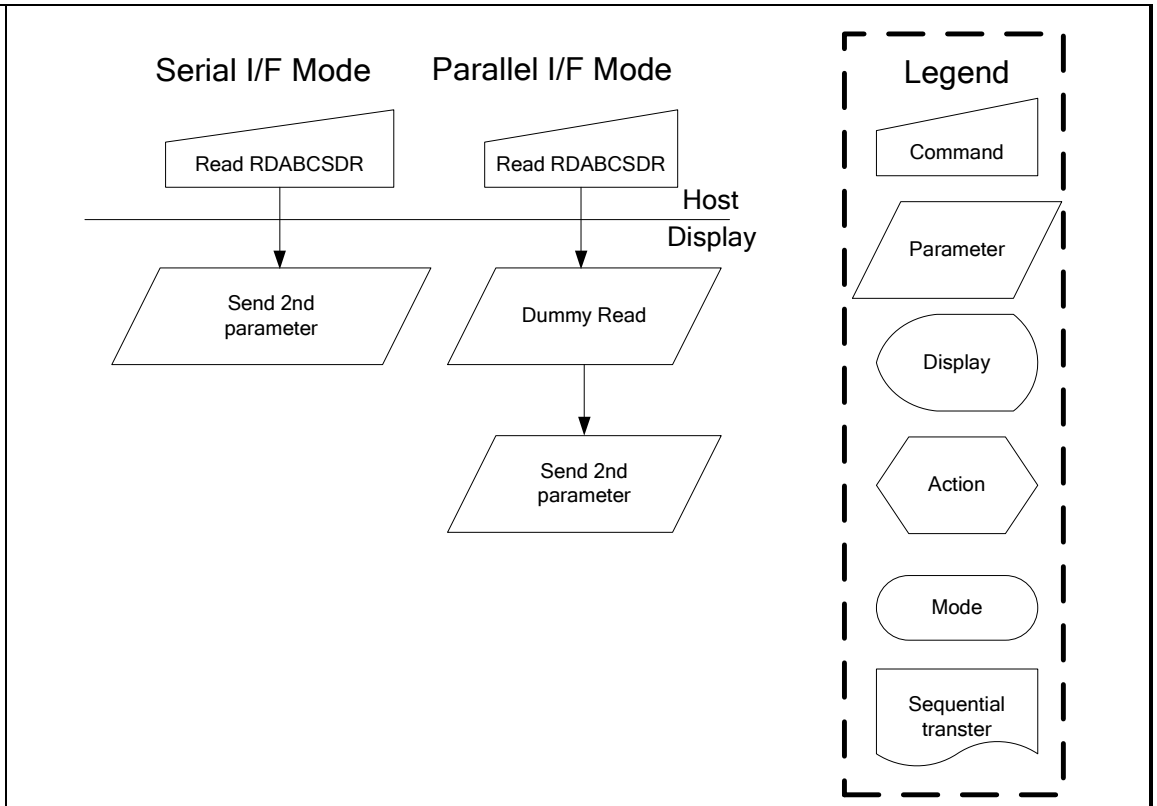
Flow Chart



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9.1.46 RDID1 (DAh): Read ID1

DAH	RDID1 (Read ID1)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(Dah)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	
Description	-This read byte identifies the LCD module's manufacturer.												
Restriction	-												

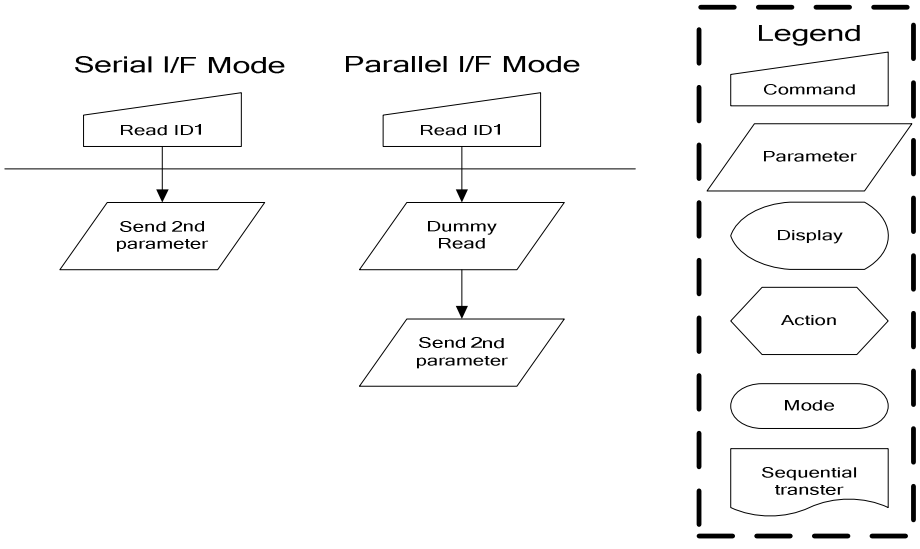
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	85h
S/W Reset	85h
H/W Reset	85h

Flow Chart



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9.1.47 RDID2 (DBh): Read ID2

DBH	RDID2 (Read ID2)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
Description	This read byte is used to track the LCD module/driver IC version. '-': Don't care.												
Restriction	-												

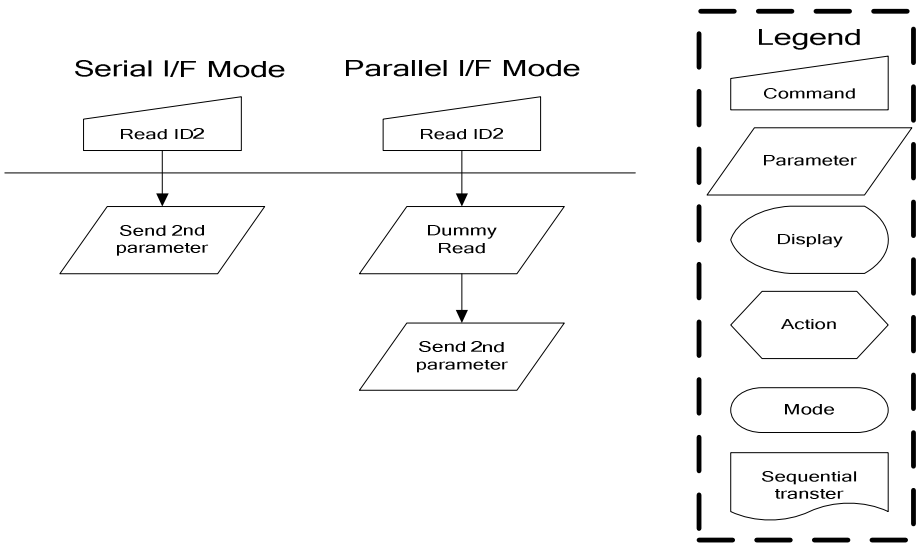
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	85h
S/W Reset	85h
H/W Reset	85h

Flow Chart



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9.1.48 RDID3 (DCh): Read ID3

DCH	RDID3 (Read ID3)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID3	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	
Description	This read byte identifies the LCD module/driver.												
Restriction	-												

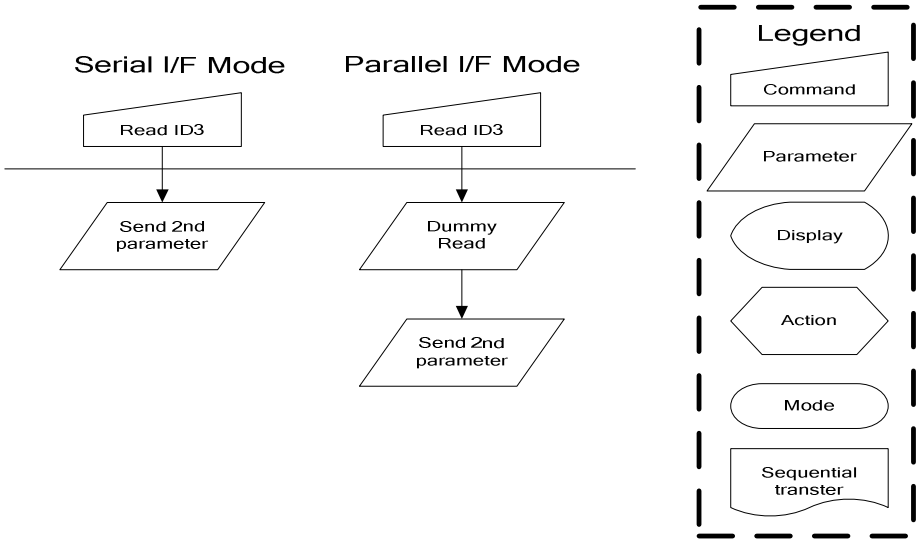
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	52h
S/W Reset	52h
H/W Reset	52h

Flow Chart



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9.2 System Function Command Table 2

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
RAMCTRL	0	↑	1	-	1	0	1	1	0	0	0	0	(B0h)	RAM Control
	1	↑	1	-	0	0	0	RM	0	0	DM1	DM0		
	1	↑	1	-	1	1	EPF1	EPF0	ENDIAN	RIM	MDT1	MDT0		
RGBCTRL	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)	RGB Control
	1	↑	1	-	WO	RCM1	RCM0	0	VSPL	HSPL	DPL	EPL		
	1	↑	1	-	0	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0		
	1	↑	1	-	0	0	0	HBP4	HBP3	HBP2	HBP1	HBP0		
PORCTRL	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)	Porch control
	1	↑	1	-	0	BPA6	BPA5	BPA4	BPA3	BPA2	BPA1	BPA0		
	1	↑	1	-	0	FPA6	FPA5	FPA4	FPA3	FPA2	FPA1	FPA0		
	1	↑	1	-	0	0	0	0	0	0	0	PSEN		
	1	↑	1		BPB3	BPB2	BPB1	BPB0	FPB3	FPB2	FPB1	FPB0		
	1	↑	1		BPC3	BPC2	BPC1	BPC0	FPC3	FPC2	FPC1	FPC0		
FRCTRL1	0	↑	1	-	1	0	1	1	0	0	1	1	(B3h)	Frame Rate Control 1
	1	↑	1	-	0	0	0	FRSEN	0	0	DIV1	DIV0		
	1	↑	1	-	NLB2	NLB1	NLB0	RTNB4	RTNB3	RTNB2	RTNB1	RTNB0		
	1	↑	1	-	NLC2	NLC1	NLC0	RTNC4	RTNC3	RTNC2	RTNC1	RTNC0		
PARCTRL	0	↑	1	-	1	0	1	1	0	1	0	1	(B5h)	Partial control
	1	↑	1	-	NDL	0	0	PTGISC	ISC3	ISC2	ISC1	ISC0		
GCTRL	0	↑	1	-	1	0	1	1	0	1	1	1	(B7h)	Gate control
	1	↑	1	-	0	VGHS2	VGHS1	VGHS0	0	VGLS2	VGLS1	VGLS0		
GTADJ	0	↑	1	-	1	0	1	1	1	0	0	0	(B8h)	Gate on timing adjustment
	1	↑	1	-	0	0	1	0	1	0	1	0		
	1	↑	1	-	0	0	1	0	1	0	1	1		
	1	↑	1	-	0	0	GTA5	GTA4	GTA3	GTA2	GTA1	GTA0		
	1	↑	1	-	GOFR3	GOFR2	GOFR1	GOFR0	GOF3	GOF2	GOF1	GOF0		
DGMEN	0	↑	1	-	1	0	1	1	1	0	1	0	(BAh)	Digital Gamma Enable
	1	↑	1	-	0	0	0	0	0	DGMEN	0	0		
VCOMS	0	↑	1	-	1	0	1	1	1	0	1	1	(BBh)	VCOM Setting
	1	↑	1	-	0	0	VCOMS5	VCOMS4	VCOMS3	VCOMS2	VCOMS1	VCOMS0		
POWSAVE	0	↑	1	-	1	0	1	1	1	1	0	0	(BCh)	Power saving mode
	1	↑	1	-	1	1	1	0	1	1	NS	IS		

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Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
DLPOFFSAVE	0	↑	1	-	1	0	1	1	1	1	0	1	(BDh)	Display off power save
	1	↑	1	-	1	1	1	1	1	1	1	DOFSAVE		
LCMCTRL	0	↑	1	-	1	1	0	0	0	0	0	0	(C0h)	LCM Control
	1	↑	1	-	0	XMY	XBGR	XINV	XMX	XMH	XMV	XGS		
IDSET	0	↑	1	-	1	1	0	0	0	0	0	1	(C1h)	ID Setting
	1	↑	1	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		
	1	↑	1	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		
	1	↑	1	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		
VDVVRHEN	0	↑	1	-	1	1	0	0	0	0	1	0	(C2h)	VDV and VRH Command Enable
	1	↑	1	-	0	0	0	0	0	0	0	CMDEN		
	1	↑	1	-	1	1	1	1	1	1	1	1		
VRHS	0	↑	1		1	1	0	0	0	0	1	1	(C3h)	VRH Set
	1	↑	1		0	0	VRHS5	VRHS4	VRHS3	VRHS2	VRHS1	VRHS0		
VDVSET	0	↑	1	-	1	1	0	0	0	1	0	0	(C4h)	VDV Setting
	1	↑	1	-	0	0	VDVS5	VDVS4	VDVS3	VDVS2	VDVS1	VDVS0		
VCMOFSET	0	↑	1	-	1	1	0	0	0	1	0	1	(C5h)	VCOM Offset Set
	1	↑	1	-	0	0	VCMOFS5	VCMOFS4	VCMOFS3	VCMOFS2	VCMOFS1	VCMOFS0		
FRCTR2	0	↑	1		1	1	0	0	0	1	1	0	(C6h)	FR Control 2
	1	↑	1		NLA2	NLA1	NLA0	RTNA4	RTNA3	RTNA2	RTNA1	RTNA0		
CABCCTRL	0	↑	1	-	1	1	0	0	0	1	1	1	(C7h)	CABC Control
	1	↑	1	-	0	0	0	0	LEDONREV	DPOFPWM	PWMFIX	PWMPOL		
REGSEL1	0	↑	1	-	1	1	0	0	1	0	0	0	(C8h)	Register value selection1
	1	↑	1	-	0	0	0	0	1	0	0	0		
REGSEL2	0	↑	1	-	1	1	0	0	1	0	1	0	(CAh)	Register value selection2
	1	↑	1	-	0	0	0	0	1	1	1	1		
PWMFRSEL	0	↑	1	-	1	1	0	0	1	1	0	0	(CCh)	PWM Frequency Selection
	1	↑	1	-	0	0	CS2	CS1	CS0	CLK2	CLK1	CLK0		
PWCTRL1	0	↑	1	-	1	1	0	1	0	0	0	0	(D0h)	Power Control 1
	1	↑	1	-	1	0	1	0	0	1	0	0		
	1	↑	1	-	AVDD1	AVDD0	AVCL1	AVCL0	0	0	VDS1	VDS0		

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Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
VAPVANEN	0	↑	1	-	1	1	0	1	0	0	1	0	(D2h)	Enable VAP/VAN signal output
	1	↑	1	-	0	1	0	0	1	1	0	0		
CMD2EN	0	↑	1	-	1	1	0	1	1	1	1	1	(DFh)	Command 2 Enable
	1	↑	1	-	0	1	0	1	1	0	1	0	(5Ah)	
	1	↑	1	-	0	1	1	0	1	0	0	1	(69h)	
	1	↑	1	-	0	0	0	0	0	0	1	0	(02h)	
	1	↑	1	-	0	0	0	0	0	0	0	EN		
PVGAMCTRL	0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)	Positive Voltage Gamma Control
	1	↑	1	-	V63P3	V63P2	V63P1	V63P0	V0P3	V0P2	V0P1	V0P0		
	1	↑	1	-	0	0	V1P5	V1P4	V1P3	V1P2	V1P1	V1P0		
	1	↑	1	-	0	0	V2P5	V2P4	V2P3	V2P2	V2P1	V2P0		
	1	↑	1	-	0	0	0	V4P4	V4P3	V4P2	V4P1	V4P0		
	1	↑	1	-	0	0	0	V6P4	V6P3	V6P2	V6P1	V6P0		
	1	↑	1	-	0	0	J0P1	J0P0	V13P3	V13P2	V13P1	V13P0		
	1	↑	1	-	0	V20P6	V20P5	V20P4	V20P3	V20P2	V20P1	V20P0		
	1	↑	1	-	0	V36P2	V36P1	V36P0	0	V27P2	V27P1	V27P0		
	1	↑	1	-	0	V43P6	V43P5	V43P4	V43P3	V43P2	V43P1	V43P0		
	1	↑	1	-	0	0	J1P1	J1P0	V50P3	V50P2	V50P1	V50P0		
	1	↑	1	-	0	0	0	V57P4	V57P3	V57P2	V57P1	V57P0		
	1	↑	1	-	0	0	0	V59P4	V59P3	V59P2	V59P1	V59P0		
	1	↑	1	-	0	0	V61P5	V61P4	V61P3	V61P2	V61P1	V61P0		
	1	↑	1	-	0	0	V62P5	V62P4	V62P3	V62P2	V62P1	V62P0		
NVGAMCTRL	0	↑	1	-	1	1	1	0	0	0	0	1	(E1h)	Negative Voltage Gamma Control
	1	↑	1	-	V63N3	V63N2	V63N1	V63N0	V0N3	V0N2	V0N1	V0N0		
	1	↑	1	-	0	0	V1N5	V1N4	V1N3	V1N2	V1N1	V1N0		
	1	↑	1	-	0	0	V2N5	V2N4	V2N3	V2N2	V2N1	V2N0		
	1	↑	1	-	0	0	0	V4N4	V4N3	V4N2	V4N1	V4N0		
	1	↑	1	-	0	0	0	V6N4	V6N3	V6N2	V6N1	V6N0		

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Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	↑	1	-	0	0	J0N1	J0N0	V13N3	V13N2	V13N1	V13N0		
	1	↑	1		0	V20N6	V20N5	V20N4	V20N3	V20N2	V20N1	V20N0		
	1	↑	1		0	V36N2	V36N1	V36N0	0	V27N2	V27N1	V27N0		
	1	↑	1		0	V43N6	V43N5	V43N4	V43N3	V43N2	V43N1	V43N0		
	1	↑	1		0	0	J1N1	J1N0	V50N3	V50N2	V50N1	V50N0		
	1	↑	1		0	0	0	V57N4	V57N3	V57N2	V57N1	V57N0		
	1	↑	1		0	0	0	V59N4	V59N3	V59N2	V59N1	V59N0		
	1	↑	1		0	0	V61N5	V61N4	V61N3	V61N2	V61N1	V61N0		
	1	↑	1		0	0	V62N5	V62N4	V62N3	V62N2	V62N1	V62N0		
DGMLUTR	0	↑	1	-	1	1	1	0	0	0	1	0	(E2h)	Digital Gamma Look-up Table for Red
	1	↑	1	-	DGM_LUT_R00[7:0]									
	1	↑	1	-	DGM_LUT_R01[7:0]									
	1	↑	1	-	⋮									
	1	↑	1	-	DGM_LUT_R30[7:0]									
	1	↑	1	-	DGM_LUT_R31[7:0]									
	1	↑	1	-	⋮									
	1	↑	1	-	DGM_LUT_R62[7:0]									
	1	↑	1	-	DGM_LUT_R63[7:0]									
DGMLUTB	0	↑	1	-	1	1	1	0	0	0	1	1	(E3h)	Digital Gamma Look-up Table for Blue
	1	↑	1	-	DGM_LUT_B00[7:0]									
	1	↑	1	-	DGM_LUT_B01[7:0]									
	1	↑	1	-	⋮									
	1	↑	1	-	DGM_LUT_B30[7:0]									
	1	↑	1	-	DGM_LUT_B31[7:0]									
	1	↑	1	-	⋮									
	1	↑	1	-	DGM_LUT_B62[7:0]									
	1	↑	1	-	DGM_LUT_B63[7:0]									
GATECTRL	0	↑	1	-	1	1	1	0	0	1	0	0	(E4h)	Gate control
	1	↑	1	-	0	0	NL5	NL4	NL3	NL2	NL1	NL0		

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Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	↑	1	-	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0		
	1	↑	1	-	0	0	0	TMG	0	SM	0	GS		
SPI2EN	0	↑	1	-	1	1	1	0	0	1	1	1	(E7h)	SPI2
	1	↑	1	-	0	0	0	SPI2EN	0	0	0	SPIRD		enable
PWCTRL2	0	↑	1	-	1	1	1	0	1	0	0	0	(E8h)	Power
	1	↑	1	-	1	0	SBCLK1	SBCLK0	0	0	STP14CK1	STP14CK0		Control 2
EQCTRL	0	↑	1	-	1	1	1	0	1	0	0	1	(E9h)	
	1	↑	1	-	0	0	0	SEQ4	SEQ3	SEQ2	SEQ1	SEQ0		Equalize
	1	↑	1	-	0	0	0	SPRET4	SPRET3	SPRET2	SPRET1	SPRET0		Time
	1	↑	1	-	0	0	0	0	GEQ3	GEQ2	GEQ1	GEQ0		Control
PROMCTRL	0	↑	1	-	1	1	1	0	1	1	0	0	(ECh)	Program
	1	↑	1	-	0	0	0	0	0	0	0	1		Control
PROMEN	0	↑	1	-	1	1	1	1	1	0	1	0	(FAh)	
	1	↑	1	-	0	1	0	1	1	0	1	0		Program
	1	↑	1	-	0	1	1	0	1	0	0	1		Mode
	1	↑	1	-	1	1	1	0	1	1	1	0		Enable
	1	↑	1	-	0	0	0	0	0	PROMEN	0	0		
NVMSET	0	↑	1	-	1	1	1	1	1	1	0	0	(FCh)	
	1	↑	1	-	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0		NVM
	1	↑	1	-	D7	D6	D5	D4	D3	D2	D1	D0		Setting
PROMACT	0	↑	1	-	1	1	1	1	1	1	1	0	(FEh)	
	1	↑	1	-	0	0	0	1	1	0	0	1		Program
	1	↑	1	-	1	0	1	0	0	1	0	1		Action

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9.2.1 RAMCTRL (B0h): RAM Control

B0H	RAMCTR (RAM Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMCTRL	0	↑	1	-	1	0	1	1	0	0	0	0	(B0h)
1st Parameter	1	↑	1	-	0	0	0	RM	0	0	DM1	DM0	
2nd Parameter	1	↑	1	-	1	1	EPF1	EPF0	ENDIAN	RIM	MDT1	MDT0	

Description

RM : ram access selection.

RM="0" : Ram access from MCU interface

RM="1" : Ram access from RGB interface

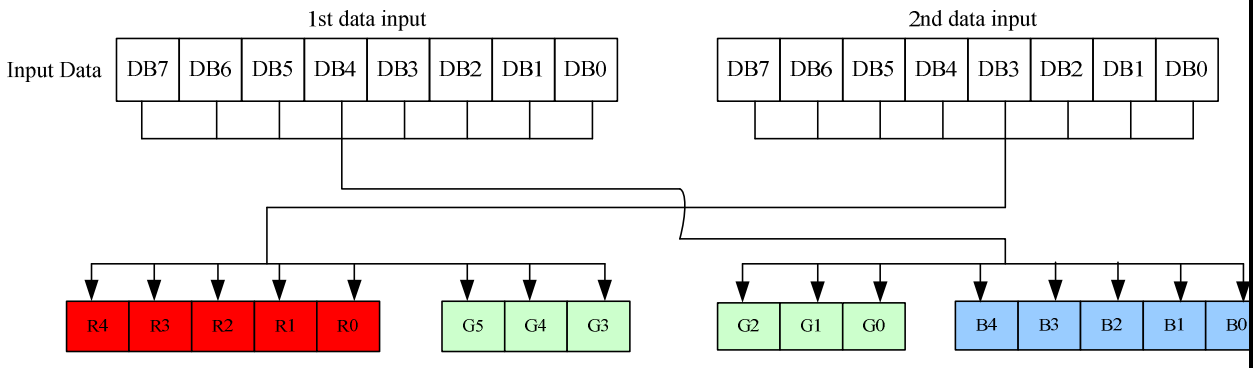
DM[1:0] : Display operation selection.

DM[1:0]	Mode
00h	MCU interface
01h	RGB interface
10h	VSYNC interface
11h	Reserved

ENDIAN :

ENDIAN	Mode
0	Normal (MSB first)
1	Little Endian (LSB first)

Note: Little Endian only can be supported in 65K 8-bit and 9-bit interface.



MDT[1:0] : Method of pixel data transfer.

Please refer to **section 8.8 Data Color Coding**

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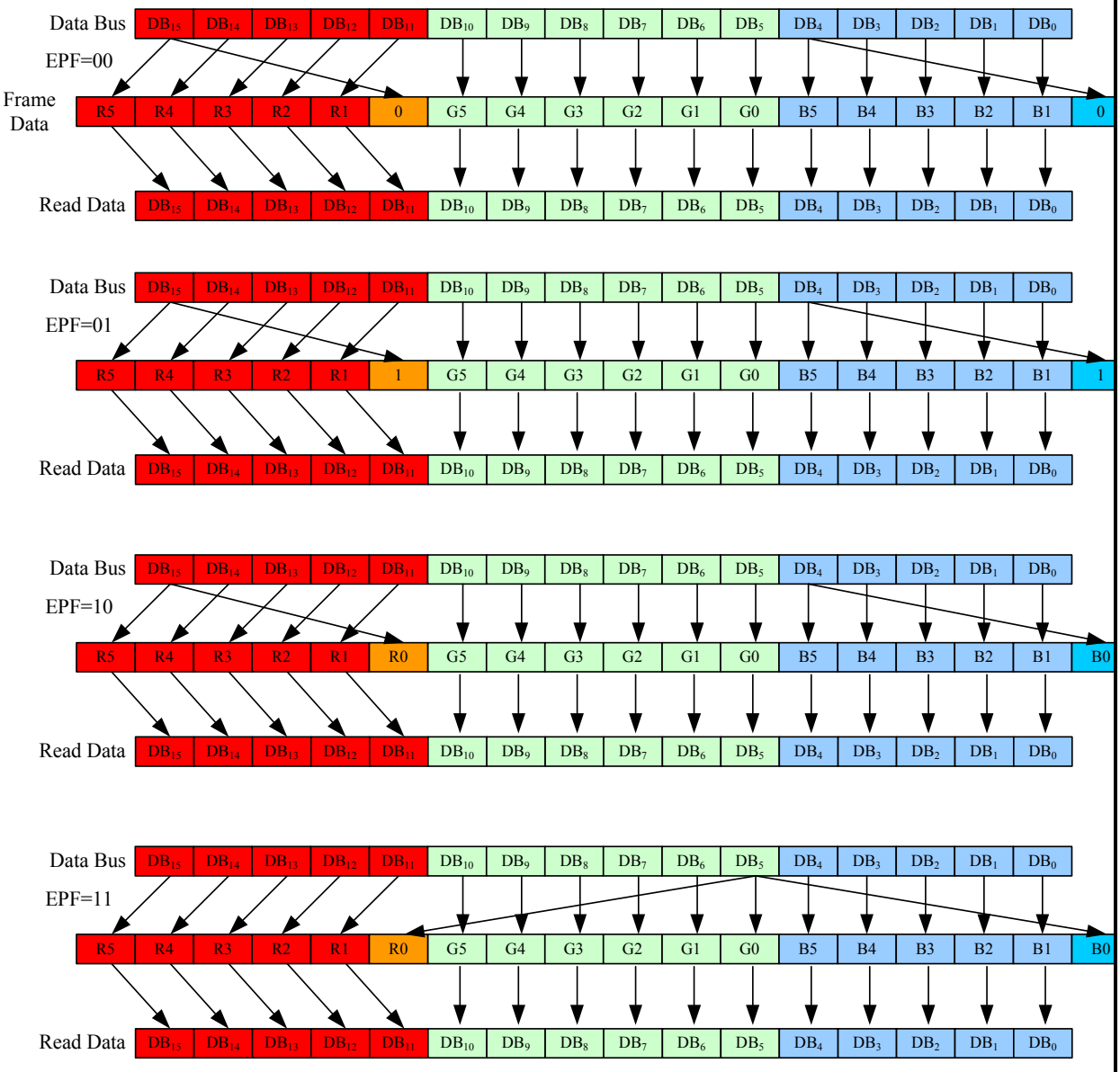
RIM: Specify RGB interface bus width.

RIM=”0”: 18 bit bus width.

RIM=”1”: 6 bit bus width

EPF[1:0] : Data translate of 65k and 4k to frame data.

65K data formate:



Register Availability

Status	Availability

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		Normal Mode On, Idle Mode Off, Sleep Out	Yes
		Normal Mode On, Idle Mode On, Sleep Out	Yes
		Partial Mode On, Idle Mode Off, Sleep Out	Yes
		Partial Mode On, Idle Mode On, Sleep Out	Yes
		Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h/F0h
S/W Reset	00h/F0h
H/W Reset	00h/F0h

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9.2.2 RGBCTRL (B1h): RGB Interface Control

B1H	RGBCTRL (RGB Interface Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RGBCTRL	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)
1st parameter	1	↑	1	-	WO	RCM1	RCM0	0	VSPL	HSPL	DPL	EPL	
2nd parameter	1	↑	1	-	0	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	
3rd parameter	1	↑	1	-	0	0	0	HBP4	HBP3	HBP2	HBP1	HBP0	

Description

WO: Direct RGB mode.

WO	Mode
0	Memory
1	Shift register

RCM[1:0]: RGB I/F enable mode selection.

RCM[1:0]	Mode
00	MCU interface
01	
10	RGB DE mode
11	RGB HV mode

VSPL : Sets the signal polarity of the VSYNC pin.

VSPL="0", Low active

VSPL="1", High active

HSPL : Sets the signal polarity of the HSYNC pin.

HSPL="0", Low active

HSPL="1", High active

DPL : Sets the signal polarity of the DOTCLK pin.

DPL = "0" The data is input on the positive edge of DOTCLK

DPL = "1" The data is input on the negative edge of DOTCLK

EPL : Sets the signal polarity of the ENABLE pin.

EPL = "0" The data DB17-0 is written when ENABLE = "1". Disable data write operation when ENABLE = "0".

EPL = "1" The data DB17-0 is written when ENABLE = "0". Disable data write operation when ENABLE = "1".

VBP[6:0]: RGB interface Vsync back porch setting. Minimum setting is 0x02.

HBP[4:0]: RGB interface Hsync back porch setting. Please refer to the section 8.9.3 for minimum setting.

Register Availability

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		Status	Availability
		Normal Mode On, Idle Mode Off, Sleep Out	Yes
		Normal Mode On, Idle Mode On, Sleep Out	Yes
		Partial Mode On, Idle Mode Off, Sleep Out	Yes
		Partial Mode On, Idle Mode On, Sleep Out	Yes
		Sleep In	Yes

Default		Status	Default Value
		Power On Sequence	40h/02h/14h
		S/W Reset	40h/02h/14h
		H/W Reset	40h/02h/14h

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9.2.3 PORCTRL (B2h): Porch Setting

B2H	PORCTRL (Porch Setting)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PORCTRL	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)
1st parameter	1	↑	1	-	0	BPA6	BPA5	BPA4	BPA3	BPA2	BPA1	BPA0	
2nd parameter	1	↑	1	-	0	FPA6	FPA5	FPA4	FPA3	FPA2	FPA1	FPA0	
3rd parameter	1	↑	1	-	0	0	0	0	0	0	0	PSEN	
4th parameter	1	↑	1	-	BPB3	BPB2	BPB1	BPB0	FPB3	FPB2	FPB1	FPB0	
5th parameter	1	↑	1	-	BPC3	BPC2	BPC1	BPC0	FPC3	FPC2	FPC1	FPC0	

Description

BPA[6:0]: Back porch setting in normal mode. The minimum setting is 0x01.

FPA[6:0]: Front porch setting in normal mode. The minimum setting is 0x01.

PSEN: Enable separate porch control.

PSEN	**Mode**
0	Disable separate porch control
1	Enable separate porch control

BPB[3:0]: Back porch setting in idle mode. The minimum setting is 0x01.

FPB[3:0]: Front porch setting in idle mode. The minimum setting is 0x01.

BPC[3:0]: Back porch setting in partial mode. The minimum setting is 0x01.

FPC[3:0]: Front porch setting in partial mode. The minimum setting is 0x01.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0Ch/0Ch/00h/33h/33h
S/W Reset	0Ch/0Ch/00h/33h/33h
H/W Reset	0Ch/0Ch/00h/33h/33h

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9.2.4 FRCTRL1 (B3h): Frame Rate Control 1 (In partial mode/ idle colors)

B3H	FRCTRL1 (Frame rate control 1)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
FRCTRL1	0	↑	1	-	1	0	1	1	0	0	1	1	(B3h)
1st parameter	1	↑	1	-	0	0	0	FRSEN	0	0	DIV1	DIV0	
2nd parameter	1	↑	1	-	NLB2	NLB1	NLB0	RTNB4	RTNB3	RTNB2	RTNB1	RTNB0	
3rd parameter	1	↑	1	-	NLC2	NLC1	NLC0	RTNC4	RTNC3	RTNC2	RTNC1	RTNC0	

Description

FRSEN: Enable separate frame rate control.

When FRSEN=0, Frame rate of idle and partial mode are determined by C6h

When FRSEN=1, Frame rate of idle and partial mode are determined by B3h

FRSEN	Mode
0	Disable separate FR control
1	Enable separate FR control

DIV[1:0]: Frame rate divided control

DIV[1:0]	Mode
00	Divide by 1
01	Divide by 2
10	Divide by 4
11	Divide by 8

NLB[2:0]: Inversion selection in idle mode.

0x00: dot inversion.

0x07: column inversion.

RTNB[4:0]: Frame rate control in idle mode.

RTNB[4:0]	FR in idle mode (Hz)	RTNB[4:0]	FR in idle mode (Hz)
00h	119	10h	58
01h	111	11h	57
02h	105	12h	55
03h	99	13h	53
04h	94	14h	52
05h	90	15h	50
06h	86	16h	49
07h	82	17h	48
08h	78	18h	46
09h	75	19h	45

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	0Ah	72	1Ah	44
	0Bh	69	1Bh	43
	0Ch	67	1Ch	42
	0Dh	64	1Dh	41
	0Eh	62	1Eh	40
	0Fh	60	1Fh	39

Note:

1. If FRSEN=1, Frame rate in idle mode=10MHz/(320+(FPB[3:0]+BPB[3:0])*4)*(250+RTNB[4:0]*16).
2. FPB[6:0] and BPB[6:0] are in command B2h
3. In this frame rate table, FPB[3:0]=03h, BPB[3:0]=03h

NLC[2:0]: Inversion setting in partial mode.

0x00: dot inversion.

0x07: column inversion.

RTNC[4:0]: Frame rate control in partial mode. This setting is equal to RTNB.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h/0Fh/0Fh
S/W Reset	00h/0Fh/0Fh
H/W Reset	00h/0Fh/0Fh

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9.2.5 PARCTRL (B5h): Partial Control

B5H	PARCTRL (Partial Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PARCTRL	0	↑	1	-	1	0	1	1	0	1	0	1	(B5h)
Parameter	1	↑	1	-	NDL	0	0	PTGISC	ISC3	ISC2	ISC1	ISC0	

Description

NDL: Source output level in non display area in partial mode.

When NDL=0, source output level is V63.

When NDL=1, source output level is V0.

PTGISC: Non display area scan mode.

When PTGISC=0, non-display area is normal scan.

When PTGISC=1, non-display area is interval scan.

ISC[3:0]: non-display area scan cycle selection.

ISC[3:0]	Scan cycle for non-display area
00h	Normal scan
01h	Every 3 cycles scan 1 time
02h	Every 5 cycles scan 1 time
03h	Every 7 cycles scan 1 time
⋮	⋮
0Fh	Every 31 cycles scan 1 time

Note:

If 01h to 0fh of ISC[3:0] need to be set, PTGISC have to set to 1.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

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9.2.6 GCTRL (B7h): Gate Control

B7H	GCTRL (Gate Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GCTRL	0	↑	1	-	1	0	1	1	0	1	1	1	(B7h)
Parameter	1	↑	1	-	0	VGHS2	VGHS1	VGHS0	0	VGLS2	VGLS1	VGLS0	

Description

VGHS[2:0]: VGH Setting.

VGHS[2:0]	VGH (V)
00h	12.2
01h	12.54
02h	12.89
03h	13.26
04h	13.65
05h	14.06
06h	14.5
07h	14.97

VGLS[2:0]: VGL Setting.

VGLS[2:0]	VGL (V)
00h	-7.16
01h	-7.67
02h	-8.23
03h	-8.87
04h	-9.6
05h	-10.43
06h	-11.38
07h	-12.5

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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Default

Status	Default Value
Power On Sequence	35h
S/W Reset	35h
H/W Reset	35h

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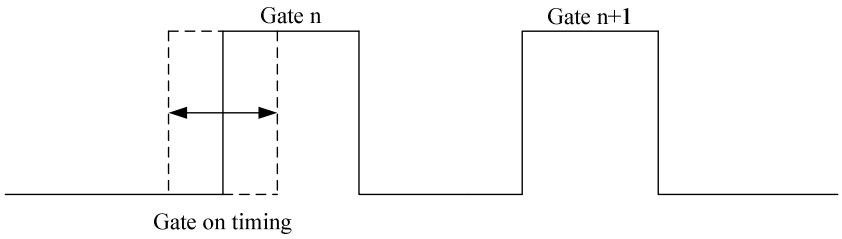
9.2.7 GTADJ (B8h): Gate On Timing Adjustment

B8H	GTADJ(Gate On Timing Adjustment)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GTADJ	0	↑	1	-	1	0	1	1	1	0	0	0	(B8h)
1st Parameter	1	↑	1	-	0	0	1	0	1	0	1	0	2Ah
2nd Parameter	1	↑	1	-	0	0	1	0	1	0	1	1	2Bh
3rd Parameter	1	↑	1	-	0	0	GTA5	GTA4	GTA3	GTA2	GTA1	GTA0	
4th Parameter	1	↑	1	-	GOFR3	GOFR2	GOFR1	GOFR0	GOF3	GOF2	GOF1	GOF0	

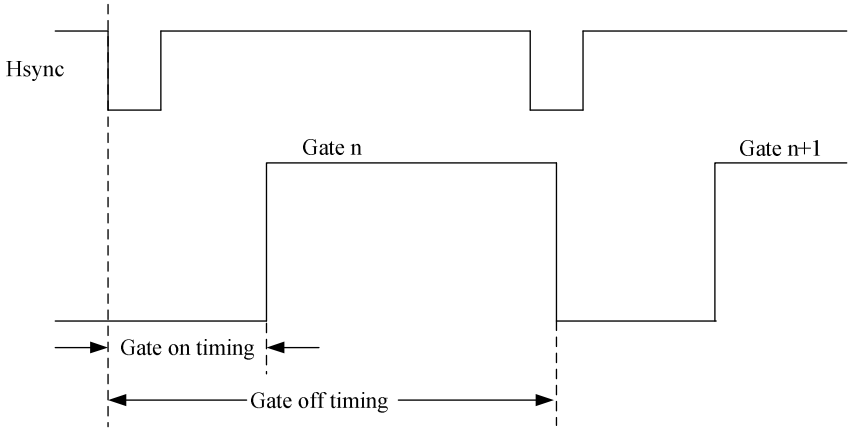
Description



GTA[5:0]: Gate on timing adjustment.

Gate on timing=300ns+GTA[5:0]*400ns

In RGB interface:



In 18bit RGB interface:

Gate on timing=7dotclk+GTA[5:0]*4dotclk

In 6bit RGB interface:

Gate on timing=7*3dotclk+GTA[5:0]*4*3dotclk

GOFR[3:0]: Gate off timing adjustment only for RGB interface

In 18bit RGB interface:

Gate off timing=516.5dotclk-16dotclk*GOFR[3:0]

In 6bit RGB interface:

Gate off timing=512*3dotclk-16dotclk*3*GOFR[3:0]

Note:

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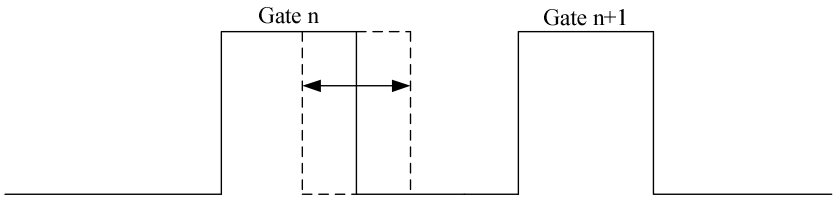
In rgb interface, if the setting of gate off timing is more than the number of dotclk in one line, the gate off timing is determined by hsync.



Gate off timing

GOF[3:0]: Gate off timing adjustment

Gate off timing=-GOF[3:0]*400ns

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	2Ah/2Bh/22h/75h
S/W Reset	2Ah/2Bh/22h/75h
H/W Reset	2Ah/2Bh/22h/75h

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9.2.8 DGMEN (BAh): Digital Gamma Enable

BAH	DGMEN (Digital Gamma Enable)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DGMEN	0	↑	1	-	1	0	1	1	1	0	1	0	(BAh)
Parameter	1	↑	1	-	0	0	0	0	0	DGMEN	0	0	
Description	**DGMEN:** "0": disable digital gamma. "1": enable digital gamma.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

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9.2.9 VCOMS (BBh): VCOM Setting

BBH	VCOMS (VCOM Setting)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VCOMS	0	↑	1	-	1	0	1	1	1	0	1	1	(BBh)
Parameter	1	↑	1	-	0	0	VCOM5	VCOM4	VCOM3	VCOM2	VCOM1	VCOM0	

Description

VCOMS[5:0]:

VCOMS[5:0]	VCOM (V)	VCOMS[5:0]	VCOM (V)
00h	0.1	20h	0.9
01h	0.125	21h	0.925
02h	0.15	22h	0.95
03h	0.175	23h	0.975
04h	0.2	24h	1.0
05h	0.225	25h	1.025
06h	0.25	26h	1.05
07h	0.275	27h	1.075
08h	0.3	28h	1.1
09h	0.325	29h	1.125
0Ah	0.35	2Ah	1.15
0Bh	0.375	2Bh	1.175
0Ch	0.4	2Ch	1.2
0Dh	0.425	2Dh	1.225
0Eh	0.45	2Eh	1.25
0Fh	0.475	2Fh	1.275
10h	0.5	30h	1.3
11h	0.525	31h	1.325
12h	0.55	32h	1.35
13h	0.575	33h	1.375
14h	0.6	34h	1.4
15h	0.625	35h	1.425
16h	0.65	36h	1.45
17h	0.675	37h	1.475
18h	0.7	38h	1.5
19h	0.725	39h	1.525
1Ah	0.75	3Ah	1.55
1Bh	0.775	3Bh	1.575
1Ch	0.8	3Ch	1.6

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	1Dh	0.825	3Dh	1.625
	1Eh	0.85	3Eh	1.65
	1Fh	0.875	3Fh	1.675

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	20h
S/W Reset	20h
H/W Reset	20h

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9.2.10 POWSAVE(BCh): Power Saving Mode

BCH	POWSAVE (Power Saving Mode)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
POWSAVE	0	↑	1	-	1	0	1	1	1	1	0	0	(BCh)
Parameter	1	↑	1	-	1	1	1	0	1	1	NS	IS	
Description	**NS:** Power save for normal mode. When NS=0, power consumption in normal mode will be saved. **IS:** Power save for Idle mode. When IS=0, power consumption in idle mode will be saved.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	FFh
S/W Reset	FFh
H/W Reset	FFh

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9.2.11 DLPOFFSAVE (BDh): Display off power save

BDH	DLPOFFSAVE (Display off power save)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DLPOFFSAVE	0	↑	1	-	1	0	1	1	1	1	0	1	(BDh)
Parameter	1	↑	1	-	1	1	1	1	1	1	1	DOFSAVE	
Description	**DOFSAVE:** Power save for display off mode. When DOFSAVE=0, power consumption in display off mode will be saved.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	FFh
S/W Reset	FFh
H/W Reset	FFh

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9.2.12 LCMCTRL (C0h): LCM Control

C0H	LCMCTRL (LCM Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
LCMCTRL	0	↑	1	-	1	1	0	0	0	0	0	0	(C0h)
1st parameter	1	↑	1	-	0	XMY	XBGR	XINV	XMX	XMH	XMV	XGS	
Description	**XMY:** XOR MY setting in command 36h. **XBGR:** XOR RGB setting in command 36h. **XREV:** XOR inverse setting in command 21h **XMH:** this bit can reverse source output order and only support for RGB interface without RAM mode **XMV:** XOR MV setting in command 36h **XMX:** XOR MX setting in command 36h. **XGS:** XOR GS setting in command E4h.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	2Ch
S/W Reset	2Ch
H/W Reset	2Ch

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9.2.13 IDSET (C1h): ID Code Setting

C1H	IDSET (ID Code Setting)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IDSET	0	↑	1	-	1	1	0	0	0	0	0	1	(C1h)
Parameter 1st	1	↑	1	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	
Parameter 2nd	1	↑	1	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
Parameter 3rd	1	↑	1	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	
Description	**ID1[7:0]:** ID1 Setting. **ID2[7:0]:** ID2 Setting. **ID3[7:0]:** ID3 Setting.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	85h/85h/52h
S/W Reset	85h/85h/52h
H/W Reset	85h/85h/52h

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9.2.14 VDVVRHEN (C2h): VDV and VRH Command Enable

C2H	VDVVRHEN (VDV and VRH Command Enable)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VDVVRHEN	0	↑	1	-	1	1	0	0	0	0	1	0	(C2h)
1st Parameter	1	↑	1	-	0	0	0	0	0	0	0	CMDEN	
2nd Parameter	1	↑	1	-	1	1	1	1	1	1	1	1	
Description	**CMDEN:** VDV and VRH command write enable. CMDEN="0": VDV and VRH register value comes from NVM. CMDEN="1", VDV and VRH register value comes from command write.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	01h/FFh
S/W Reset	01h/FFh
H/W Reset	01h/FFh

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9.2.15 VRHS (C3h): VRH Set

C3H	VRHS (VRH Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VRHS	0	↑	1	-	1	1	0	0	0	0	1	1	(C3h)
1st Parameter	1	↑	1	-	0	0	VRHS5	VRHS4	VRHS3	VRHS2	VRHS1	VRHS0	

Description

VRHS[5:0]: VRH Set.

VRHS[5:0]	VAP(GVDD) (V)	VRHS[5:0]	VAP(GVDD) (V)
00h	3.55+(vcom+vcom offset+vdv)	15h	4.6+(vcom+vcom offset+vdv)
01h	3.6+(vcom+vcom offset+vdv)	16h	4.65+(vcom+vcom offset+vdv)
02h	3.65+(vcom+vcom offset+vdv)	17h	4.7+(vcom+vcom offset+vdv)
03h	3.7+(vcom+vcom offset+vdv)	18h	4.75+(vcom+vcom offset+vdv)
04h	3.75+(vcom+vcom offset+vdv)	19h	4.8+(vcom+vcom offset+vdv)
05h	3.8+(vcom+vcom offset+vdv)	1Ah	4.85+(vcom+vcom offset+vdv)
06h	3.85+(vcom+vcom offset+vdv)	1Bh	4.9+(vcom+vcom offset+vdv)
07h	3.9+(vcom+vcom offset+vdv)	1Ch	4.95+(vcom+vcom offset+vdv)
08h	3.95+(vcom+vcom offset+vdv)	1Dh	5+(vcom+vcom offset+vdv)
09h	4+(vcom+vcom offset+vdv)	1Eh	5.05+(vcom+vcom offset+vdv)
0Ah	4.05+(vcom+vcom offset+vdv)	1Fh	5.1+(vcom+vcom offset+vdv)
0Bh	4.1+(vcom+vcom offset+vdv)	20h	5.15+(vcom+vcom offset+vdv)
0Ch	4.15+(vcom+vcom offset+vdv)	21h	5.2+(vcom+vcom offset+vdv)
0Dh	4.2+(vcom+vcom offset+vdv)	22h	5.25+(vcom+vcom offset+vdv)
0Eh	4.25+(vcom+vcom offset+vdv)	23h	5.3+(vcom+vcom offset+vdv)
0Fh	4.3+(vcom+vcom offset+vdv)	24h	5.35+(vcom+vcom offset+vdv)
10h	4.35+(vcom+vcom offset+vdv)	25h	5.4+(vcom+vcom offset+vdv)
11h	4.4+(vcom+vcom offset+vdv)	26h	5.45+(vcom+vcom offset+vdv)
12h	4.45+(vcom+vcom offset+vdv)	27h	5.5+(vcom+vcom offset+vdv)
13h	4.5+(vcom+vcom offset+vdv)	28h~3Fh	Reserved
14h	4.55+(vcom+vcom offset+vdv)	--	--

VRHS[5:0]	VAN(GVCL) (V)	VRHS[5:0]	VAN(GVCL) (V)
00h	-3.55+(vcom+vcom offset-vdv)	15h	-4.6+(vcom+vcom offset-vdv)
01h	-3.6+(vcom+vcom offset-vdv)	16h	-4.65+(vcom+vcom offset-vdv)
02h	-3.65+(vcom+vcom offset-vdv)	17h	-4.7+(vcom+vcom offset-vdv)
03h	-3.7+(vcom+vcom offset-vdv)	18h	-4.75+(vcom+vcom offset-vdv)
04h	-3.75+(vcom+vcom offset-vdv)	19h	-4.8+(vcom+vcom offset-vdv)
05h	-3.8+(vcom+vcom offset-vdv)	1Ah	-4.85+(vcom+vcom offset-vdv)

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	06h	-3.85+(vcom+vcom offset-vdv)	1Bh	-4.9+(vcom+vcom offset-vdv)
	07h	-3.9+(vcom+vcom offset-vdv)	1Ch	-4.95+(vcom+vcom offset-vdv)
	08h	-3.95+(vcom+vcom offset-vdv)	1Dh	-5+(vcom+vcom offset-vdv)
	09h	-4+(vcom+vcom offset-vdv)	1Eh	-5.05+(vcom+vcom offset-vdv)
	0Ah	-4.05+(vcom+vcom offset-vdv)	1Fh	-5.1+(vcom+vcom offset-vdv)
	0Bh	-4.1+(vcom+vcom offset-vdv)	20h	-5.15+(vcom+vcom offset-vdv)
	0Ch	-4.15+(vcom+vcom offset-vdv)	21h	-5.2+(vcom+vcom offset-vdv)
	0Dh	-4.2+(vcom+vcom offset-vdv)	22h	-5.25+(vcom+vcom offset-vdv)
	0Eh	-4.25+(vcom+vcom offset-vdv)	23h	-5.3+(vcom+vcom offset-vdv)
	0Fh	-4.3+(vcom+vcom offset-vdv)	24h	-5.35+(vcom+vcom offset-vdv)
	10h	-4.35+(vcom+vcom offset-vdv)	25h	-5.4+(vcom+vcom offset-vdv)
	11h	-4.4+(vcom+vcom offset-vdv)	26h	-5.45+(vcom+vcom offset-vdv)
	12h	-4.45+(vcom+vcom offset-vdv)	27h	-5.5+(vcom+vcom offset-vdv)
	13h	-4.5+(vcom+vcom offset-vdv)	28h~3Fh	Reserved
	14h	-4.55+(vcom+vcom offset-vdv)	--	--

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0Bh
S/W Reset	0Bh
H/W Reset	0Bh

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9.2.16 VDVS (C4h): VDV Set

C4H	VDVS (VDV Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VDVS	0	↑	1	-	1	1	0	0	0	1	0	0	(C4h)
1st Parameter	1	↑	1	-	0	0	VDVS5	VDVS4	VDVS3	VDVS2	VDVS1	VDVS0	

Description

VDVS[5:0]: VDV Set.

VDVS[5:0]	VDV (V)	VDVS[5:0]	VDV (V)
00h	-0.8	20h	0
01h	-0.775	21h	0.025
02h	-0.75	22h	0.05
03h	-0.725	23h	0.075
04h	-0.7	24h	0.1
05h	-0.675	25h	0.125
06h	-0.65	26h	0.15
07h	-0.625	27h	0.175
08h	-0.6	28h	0.2
09h	-0.575	29h	0.225
0Ah	-0.55	2Ah	0.25
0Bh	-0.525	2Bh	0.275
0Ch	-0.5	2Ch	0.3
0Dh	-0.475	2Dh	0.325
0Eh	-0.45	2Eh	0.35
0Fh	-0.425	2Fh	0.375
10h	-0.4	30h	0.4
11h	-0.375	31h	0.425
12h	-0.35	32h	0.45
13h	-0.325	33h	0.475
14h	-0.3	34h	0.5
15h	-0.275	35h	0.525
16h	-0.25	36h	0.55
17h	-0.225	37h	0.575
18h	-0.2	38h	0.6
19h	-0.175	39h	0.625
1Ah	-0.15	3Ah	0.65
1Bh	-0.125	3Bh	0.675
1Ch	-0.1	3Ch	0.7

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	1Dh	-0.075	3Dh	0.725
	1Eh	-0.05	3Eh	0.75
	1Fh	-0.025	3Fh	0.775

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	20h
S/W Reset	20h
H/W Reset	20h

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9.2.17 VCMOFSET (C5h): VCOM Offset Set

C5H	VCMOFSET (VCOM Offset Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VCMOFSET	0	↑	1	-	1	1	0	0	0	1	0	1	(C5h)
1st Parameter	1	↑	1	-	0	0	VCMOFS5	VCMOFS4	VCMOFS3	VCMOFS2	VCMOFS1	VCMOFS0	

Description

VCOM offset setting:

VCMOFS[5:0]	VCOM OFFSET (V)	VCMOFS[5:0]	VCOM OFFSET(V)
00h	-0.8	20h	0
01h	-0.775	21h	0.025
02h	-0.75	22h	0.05
03h	-0.725	23h	0.075
04h	-0.7	24h	0.1
05h	-0.675	25h	0.125
06h	-0.65	26h	0.15
07h	-0.625	27h	0.175
08h	-0.6	28h	0.2
09h	-0.575	29h	0.225
0Ah	-0.55	2Ah	0.25
0Bh	-0.525	2Bh	0.275
0Ch	-0.5	2Ch	0.3
0Dh	-0.475	2Dh	0.325
0Eh	-0.45	2Eh	0.35
0Fh	-0.425	2Fh	0.375
10h	-0.4	30h	0.4
11h	-0.375	31h	0.425
12h	-0.35	32h	0.45
13h	-0.325	33h	0.475
14h	-0.3	34h	0.5
15h	-0.275	35h	0.525
16h	-0.25	36h	0.55
17h	-0.225	37h	0.575
18h	-0.2	38h	0.6
19h	-0.175	39h	0.625
1Ah	-0.15	3Ah	0.65
1Bh	-0.125	3Bh	0.675
1Ch	-0.1	3Ch	0.7

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	1Dh	-0.075	3Dh	0.725
	1Eh	-0.05	3Eh	0.75
	1Fh	-0.025	3Fh	0.775

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	20h
S/W Reset	20h
H/W Reset	20h

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9.2.18 FRCTRL2 (C6h): Frame Rate Control in Normal Mode

C6H	FRCTRL2 (Frame Rate Control in Normal Mode)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
FRCTRL2	0	↑	1	-	1	1	0	0	0	1	1	0	(C6h)
1st Parameter	1	↑	1	-	NLA2	NLA1	NLA0	RTNA4	RTNA3	RTNA2	RTNA1	RTNA0	

Description

NLA[2 :0] : Inversion selection in normal mode.

0x00 : dot inversion.

0x07: column inversion.

RTNA[4:0]:

RTNA[4:0]	FR in normal mode (Hz)	RTNA[4:0]	FR in normal mode (Hz)
00h	119	10h	58
01h	111	11h	57
02h	105	12h	55
03h	99	13h	53
04h	94	14h	52
05h	90	15h	50
06h	86	16h	49
07h	82	17h	48
08h	78	18h	46
09h	75	19h	45
0Ah	72	1Ah	44
0Bh	69	1Bh	43
0Ch	67	1Ch	42
0Dh	64	1Dh	41
0Eh	62	1Eh	40
0Fh	60	1Fh	39

Note:

1. Frame rate=10MHz/(320+FPA[6:0]+BPA[6:0])*(250+RTNA[4:0]*16).
2. FPA[6:0] and BPA[6:0] are in command B2h
3. In this frame rate table, FPA[6:0]=0Ch, BPA[6:0]=0Ch

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

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	Sleep In: Yes
Default	

Status	Default Value
Power On Sequence	0Fh
S/W Reset	0Fh
H/W Reset	0Fh

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9.2.19 CABCCTRL (C7h): CABC Control

C7H	CABCCTRL (CABC Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CABCCTRL	0	↑	1	-	1	1	0	0	0	1	1	1	(C7h)
1st Parameter	1	↑	1	-	0	0	0	0	LEDONREV	DPOFPWM	PWMFIX	PWMPOL	

Description

LEDONREV: Reverse the status of LED_ON:

"0": keep the status of LED_ON.

"1": reverse the status of LED_ON.

DPOFPWM: initial state control of LEDPWM.

"0": The initial state of LEDPWM is low.

"1": The initial state of LEDPWM is high.

PWMFIX: LEDPWM fix control.

"0": LEDPWM control by CABC.

"1": fix LEDPWM in "ON" status.

PWMPOL: LEDPWM polarity control.

"0": polarity high.

"1": polarity low.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

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9.2.20 REGSEL1 (C8h): Register Value Selection 1

C8H	REGSEL1 (Register Value Selection 1)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
REGSEL1	0	↑	1	-	1	1	0	0	1	0	0	0	(C8h)
Parameter	1	↑	1	-	0	0	0	0	1	0	0	0	
Description	Reserved for testing												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	08h
S/W Reset	08h
H/W Reset	08h

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9.2.21 REGSEL2 (CAh): Register Value Selection 2

CAH	REGSEL2 (Register Value Selection 2)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
REGSEL2	0	↑	1	-	1	1	0	0	1	0	1	0	(Cah)
Parameter	1	↑	1	-	0	0	0	0	1	1	1	1	
Description	Reserved for testing												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0Fh
S/W Reset	0Fh
H/W Reset	0Fh

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9.2.22 PWMFRSEL (CCh): PWM Frequency Selection

CCH	PWMFRSEL (PWM Frequency Selection)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWMFRSEL	0	↑	1	-	1	1	0	0	1	1	0	0	(CCh)
1st Parameter	1	↑	1	-	0	0	CS2	CS1	CS0	CLK2	CLK1	CLK0	

Description

CS[2:0]/CLK[2:0]:

CLK[2:0] \ CS[2:0]	00h	01h	02h	03h	04h	05h
00h	39.2	78.7	158.7	322.6	666.7	1428.6
01h	19.6	39.4	79.4	161.3	333.3	714.3
02h	9.8	19.7	39.7	80.6	166.7	357.1
03h	4.9	9.8	19.8	40.3	83.3	178.6
04h	2.45	4.9	9.9	20.2	41.7	89.3
05h	1.23	2.5	5	10.1	20.8	44.6
06h	0.61	1.23	2.48	5	10.4	22.3
07h	0.31	0.62	1.24	2.5	5.2	11.2

Unit:kHz

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	02h
S/W Reset	02h
H/W Reset	02h

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9.2.23 PWCTRL1 (D0h): Power Control 1

D0H	PWCTRL (Power Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWCTRL	0	↑	1	-	1	1	0	1	0	0	0	0	(D0h)
1st Parameter	1	↑	1	-	1	0	1	0	0	1	0	0	
2nd Parameter	1	↑	1	-	AVDD1	AVDD0	AVCL1	AVCL0	0	0	VDS1	VDS0	

Description

AVDD[1:0]:

AVDD[1:0]	AVDD (V)
00h	6.4
01h	6.6
02h	6.8
03h	Reserved

AVCL[1:0]:

AVCL[1:0]	AVCL (V)
00h	-4.4
01h	-4.6
02h	-4.8
03h	-5.0

VDS[1:0]:

VDS[1:0]	VDDS (V)
00h	2.19
01h	2.3
02h	2.4
03h	2.51

VDDS: Power of source OP

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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Default	

Status	Default Value
Power On Sequence	A4h/A1h
S/W Reset	A4h/A1h
H/W Reset	A4h/A1h

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9.2.24 VAPVANEN (D2h): Enable VAP/VAN signal output

D2H	VAPVANEN (Enable VAP/VAN signal output)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VAPVANEN	0	↑	1	-	1	1	0	1	0	0	1	0	(D2h)
Parameter	1	↑	1	-	0	1	0	0	1	1	0	0	
Description	Enable VAP/VAN signal output												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

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9.2.25 CMD2EN (DFh): Command 2 Enable

DFH	CMD2EN (Command 2 Enable)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CMD2EN	0	↑	1	-	1	1	0	1	1	1	1	1	(DFh)
1st Parameter	1	↑	1	-	0	1	0	1	1	0	1	0	(5Ah)
2nd Parameter	1	↑	1	-	0	1	1	0	1	0	0	1	(69h)
3rd Parameter	1	↑	1	-	0	0	0	0	0	0	1	0	(02h)
4th Parameter	1	↑	1	-	0	0	0	0	0	0	0	EN	
Description	**EN:** "0": Commands in Command table 2 cannot be executed when EXTC level is "Low". "1": Commands in command table 2 can be executed when EXTC level is "Low".												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	5Ah/69h/02h/00h
S/W Reset	5Ah/69h/02h/00h
H/W Reset	5Ah/69h/02h/00h

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9.2.26 PVGAMCTRL (E0h): Positive Voltage Gamma Control

E0H	PVGAMCTRL (Positive Voltage Gamma Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PVGAMCTRL	0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)
1st Parameter	1	↑	1	-	V63P3	V63P2	V63P1	V63P0	V0P3	V0P2	V0P1	V0P0	
2nd Parameter	1	↑	1	-	0	0	V1P5	V1P4	V1P3	V1P2	V1P1	V1P0	
3rd Parameter	1	↑	1	-	0	0	V2P5	V2P4	V2P3	V2P2	V2P1	V2P0	
4th Parameter	1	↑	1	-	0	0	0	V4P4	V4P3	V4P2	V4P1	V4P0	
5th Parameter	1	↑	1	-	0	0	0	V6P4	V6P3	V6P2	V6P1	V6P0	
6th Parameter	1	↑	1	-	0	0	J0P1	J0P0	V13P3	V13P2	V13P1	V13P0	
7th Parameter	1	↑	1	-	0	V20P6	V20P5	V20P4	V20P3	V20P2	V20P1	V20P0	
8th Parameter	1	↑	1	-	0	V36P2	V36P1	V36P0	0	V27P2	V27P1	V27P0	
9th Parameter	1	↑	1	-	0	V43P6	V43P5	V43P4	V43P3	V43P2	V43P1	V43P0	
10th Parameter	1	↑	1	-	0	0	J1P1	J1P0	V50P3	V50P2	V50P1	V50P0	
11th Parameter	1	↑	1	-	0	0	0	V57P4	V57P3	V57P2	V57P1	V57P0	
12th Parameter	1	↑	1	-	0	0	0	V59P4	V59P3	V59P2	V59P1	V59P0	
13th Parameter	1	↑	1	-	0	0	V61P5	V61P4	V61P3	V61P2	V61P1	V61P0	
14th Parameter	1	↑	1	-	0	0	V62P5	V62P4	V62P3	V62P2	V62P1	V62P0	

Description

Please refer to 8.19.

Default value:

	Value(hex)
VP0[3:0]	0
VP1[5:0]	2C
VP2[5:0]	2E
VP4[4:0]	15
VP6[4:0]	10
VP13[3:0]	9
VP20[6:0]	48
VP27[2:0]	3
VP36[2:0]	3
VP43[6:0]	53
VP50[3:0]	B
VP57[4:0]	19
VP59[4:0]	18
VP61[5:0]	20
VP62[5:0]	25

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	VP63[3:0]	7
	JP0[1:0]	0
	JP1[1:0]	0

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Refer to description
S/W Reset	Refer to description
H/W Reset	Refer to description

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9.2.27 NVGAMCTRL (E1h): Negative Voltage Gamma Control

E1H	NVGAMCTRL (Negative Voltage Gamma Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVGAMCTRL	0	↑	1	-	1	1	1	0	0	0	0	1	(E1h)
1st Parameter	1	↑	1	-	V63N3	V63N2	V63N1	V63N0	V0N3	V0N2	V0N1	V0N0	
2nd Parameter	1	↑	1	-	0	0	V1N5	V1N4	V1N3	V1N2	V1N1	V1N0	
3rd Parameter	1	↑	1	-	0	0	V2N5	V2N4	V2N3	V2N2	V2N1	V2N0	
4th Parameter	1	↑	1	-	0	0	0	V4N4	V4N3	V4N2	V4N1	V4N0	
5th Parameter	1	↑	1	-	0	0	0	V6N4	V6N3	V6N2	V6N1	V6N0	
6th Parameter	1	↑	1	-	0	0	J0N1	J0N0	V13N3	V13N2	V13N1	V13N0	
7th Parameter	1	↑	1	-	0	V20N6	V20N5	V20N4	V20N3	V20N2	V20N1	V20N0	
8th Parameter	1	↑	1	-	0	V36N2	V36N1	V36N0	0	V27N2	V27N1	V27N0	
9th Parameter	1	↑	1	-	0	V43N6	V43N5	V43N4	V43N3	V43N2	V43N1	V43N0	
10th Parameter	1	↑	1	-	0	0	J1N1	J1N0	V50N3	V50N2	V50N1	V50N0	
11th Parameter	1	↑	1	-	0	0	0	V57N4	V57N3	V57N2	V57N1	V57N0	
12th Parameter	1	↑	1	-	0	0	0	V59N4	V59N3	V59N2	V59N1	V59N0	
13th Parameter	1	↑	1	-	0	0	V61N5	V61N4	V61N3	V61N2	V61N1	V61N0	
14th Parameter	1	↑	1	-	0	0	V62N5	V62N4	V62N3	V62N2	V62N1	V62N0	

Description

Please refer to 8.19.

Default value:

	Value(hex)
VN0[3:0]	0
VN1[5:0]	2C
VN2[5:0]	2E
VN4[4:0]	15
VN6[4:0]	10
VN13[3:0]	9
VN20[6:0]	48
VN27[2:0]	3
VN36[2:0]	3
VN43[6:0]	53
VN50[3:0]	B
VN57[4:0]	19
VN59[4:0]	18
VN61[5:0]	20
VN62[5:0]	25

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	VN63[3:0]	7
	JN0[1:0]	0
	JN1[1:0]	0

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Refer to description
S/W Reset	Refer to description
H/W Reset	Refer to description

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9.2.28 DGMLUTR (E2h): Digital Gamma Look-up Table for Red

E2H	DGMLUTR (Digital Gamma Look-up Table for Red)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DGMLUTR	0	↑	1	-	1	1	1	0	0	0	1	0	(E2h)
1st Parameter	1	↑	1	-	DGM_LUT_R00[7:0]								
2nd Parameter	1	↑	1	-	DGM_LUT_R01[7:0]								
⋮	1	↑	1	-	⋮								
31th Parameter	1	↑	1	-	DGM_LUT_R30[7:0]								
32th Parameter	1	↑	1	-	DGM_LUT_R31[7:0]								
⋮	1	↑	1	-	⋮								
63th Parameter	1	↑	1	-	DGM_LUT_R62[7:0]								
64th Parameter	1	↑	1	-	DGM_LUT_R63[7:0]								

Description

Please refer to 8.20.

Default value:

	Value(hex)
DGM_LUT_R00[7:0]	00h
DGM_LUT_R01[7:0]	04h
⋮	⋮
DGM_LUT_R30[7:0]	78h
DGM_LUT_R31[7:0]	7Ch
⋮	⋮
DGM_LUT_R62[7:0]	F8h
DGM_LUT_R63[7:0]	FCh

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Refer to description
S/W Reset	Refer to description

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		H/W Reset	Refer to description

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9.2.29 DGMLUTB (E3h): Digital Gamma Look-up Table for Blue

E3H	DGMLUTB (Digital Gamma Look-up Table for Blue)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DGMLUTB	0	↑	1	-	1	1	1	0	0	0	1	1	(E3h)
1st Parameter	1	↑	1	-	DGM_LUT_B00[7:0]								
2nd Parameter	1	↑	1	-	DGM_LUT_B01[7:0]								
⋮	1	↑	1	-	⋮								
31th Parameter	1	↑	1	-	DGM_LUT_B30[7:0]								
32th Parameter	1	↑	1	-	DGM_LUT_B31[7:0]								
⋮	1	↑	1	-	⋮								
63th Parameter	1	↑	1	-	DGM_LUT_B62[7:0]								
64th Parameter	1	↑	1	-	DGM_LUT_B63[7:0]								

Description

Please refer to 8.20.

Default value:

	Value(hex)
DGM_LUT_B00[7:0]	00h
DGM_LUT_B01[7:0]	04h
⋮	⋮
DGM_LUT_B30[7:0]	78h
DGM_LUT_B31[7:0]	7Ch
⋮	⋮
DGM_LUT_B62[7:0]	F8h
DGM_LUT_B63[7:0]	FCh

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Refer to description
S/W Reset	Refer to description

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		H/W Reset	Refer to description

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9.2.30 GATECTRL (E4h): Gate Control

E4H	GATECTRL (Gate Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GATECTRL	0	↑	1	-	1	1	1	0	0	1	0	0	(E4h)
1st Parameter	1	↑	1	-	0	0	NL5	NL4	NL3	NL2	NL1	NL0	
2nd Parameter	1	↑	1	-	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0	
3rd Parameter	1	↑	1	-	0	0	0	TMG	0	SM	0	GS	

Description

NL[5:0]: Set the number of gate line.

NL[5:0]	The number of gate line
0x00	8 gate line
0x01	16 gate line
0x02	24 gate line
⋮	⋮
0x27	320 gate line

SCN[5:0]: set the first scan line

SCN[5:0]	The first scan line
0x00	Gate 0
0x01	Gate 8
⋮	⋮
0x27	Gate 312

TMG: Gate mirror selection

TMG=”0”, local mirror as the number of gate line setting is not 320.

TMG=”1”, full mirror as the number of gate line setting is 320.

SM: Gate interlace mode selection

SM=”0”: Gate scan using interlace mode.

SM=”1”: Gate scan using non-interlace mode.

GS: Gate scan direction

GS=”0”: Gate scan direction is 0→319

GS=”1”: Gate scan direction is 319→0

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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Default	

Status	Default Value
Power On Sequence	27h/00h/10h
S/W Reset	27h/00h/10h
H/W Reset	27h/00h/10h

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9.2.31 SPI2EN (E7h): SPI2 Enable

E7H	SPI2EN (SPI2 Enable)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SPI2EN	0	↑	1	-	1	1	1	0	0	1	1	1	(E7h)
Parameter	1	↑	1	-	0	0	0	SPI2EN	0	0	0	SPIRD	

Description

SPI2EN: 2 data lane enable control.

"0": disable 2 data lane mode.

"1": enable 2 data lane mode

SPIRD: SPI read enable for command table 2

"0": commands in command table 2 can not be read in serial interface

"1": commands in command table 2 can be read in serial interface.

Note:

It needs one dummy clock if commands in command table 2 need to be read in serial interface.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

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9.2.32 PWCTRL2 (E8h): Power Control 2

E8H	PWCTRL2 (Power Control 2)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWCTRL2	0	↑	1	-	1	1	1	0	1	0	0	0	(E8h)
Parameter	1	↑	1	-	1	0	SBCLK1	SBCLK0	0	0	STP14CK1	STP14CK0	

Description

SBCLK[1:0]: Source booster clock selection

SBCLK[1:0]	
00h	SBCLK DIV 2
01h	SBCLK DIV 3
02h	SBCLK DIV 4
03h	SBCLK DIV 6

STP14CK[1:0]:STP14(AVDD/AVCL) booster clock selection

STP14CK[1:0]	
00h	BCLK DIV 2
01h	BCLK DIV 3
02h	BCLK DIV 4
03h	BCLK DIV 6

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	93h
S/W Reset	93h
H/W Reset	93h

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9.2.33 EQCTRL (E9h): Equalize time control

E9H	EQCTRL (Equalize time Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
EQCTRL	0	↑	1	-	1	1	1	0	1	0	0	1	(E9h)
1st Parameter	1	↑	1	-	0	0	0	SEQ4	SEQ3	SEQ2	SEQ1	SEQ0	
2nd Parameter	1	↑	1	-	0	0	0	SPRET4	SPRET3	SPRET2	SPRET1	SPRET0	
3rd Parameter	1	↑	1	-	0	0	0	0	GEQ3	GEQ2	GEQ1	GEQ0	

Description

SEQ[4:0]:Source Equalize Time

Source equalize time: SEQ[4:0]*400ns, SEQ[4:0]=0x01~0x1f

In 18bit RGB interface:

Source equalize time: SEQ[4:0]*4*1period of dotclk, SEQ[4:0]=0x01~0x1f

In 6bit RGB interface:

Source equalize time: SEQ[4:0]*4*3*1period of dotclk, SEQ[4:0]=0x01~0x1f

SPRET[4:0]: Source Pre-drive Time

Source pre-drive time: SPRET[4:0]*400ns, SPRET[4:0]=0x01~0x1f

In 18bit RGB interface:

Source equalize time: SPRET[4:0]*4*1period of dotclk, SPRET[4:0]=0x01~0x1f

In 6bit RGB interface:

Source equalize time: SPRET[4:0]*4*3*1period of dotclk, SPRET[4:0]=0x01~0x1f

GEQ[3:0]: Gate Equalize Time

Gate equalize time: GEQ[3:0]*400ns, GEQ[3:0]=0x00~0x0f

In 18bit RGB interface:

Gate equalize time: GEQ[3:0]*4*1period of dotclk, GEQ[3:0]=0x00~0x0f

In 6bit RGB interface:

Gate equalize time: GEQ[3:0]*4*3*1period of dotclk, GEQ[3:0]=0x00~0x0f

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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Default

Status	Default Value
Power On Sequence	11h/11h/08h
S/W Reset	11h/11h/08h
H/W Reset	11h/11h/08h

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9.2.34 PROMCTRL (ECh): Program Mode Control

ECH	PROMCTRL (Program Mode Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PROMCTRL	0	↑	1	-	1	1	1	0	1	1	0	0	(ECh)
Parameter	1	↑	1	-	0	0	0	0	0	0	0	1	
Description	When program mode enable, this command need be set.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

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9.2.35 PROMEN (FAh): Program Mode Enable

FAH	PROMEN (Program Mode Enable)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PROMEN	0	↑	1	-	1	1	1	1	1	0	1	0	(FAh)
1st Parameter	1	↑	1	-	0	1	0	1	1	0	1	0	(5Ah)
2nd Parameter	1	↑	1	-	0	1	1	0	1	0	0	1	(69h)
3rd Parameter	1	↑	1	-	1	1	1	0	1	1	1	0	(EEh)
4th Parameter	1	↑	1	-	0	0	0	0	0	PROMEN	0	0	
Description	**PROMEN:** "0": Program mode disable "1": Program mode enable												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

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9.2.36 NVMSET (FCh): NVM Setting

FCH	NVMSET (NVM Setting)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVMSET	0	↑	1	-	1	1	1	1	1	1	0	0	(FCh)
1st Parameter	1	↑	1	-	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	
2nd Parameter	1	↑	1	-	D7	D6	D5	D4	D3	D2	D1	D0	
Description	**ADD[7:0]:** NVM address setting **D[7:0]:** Data setting of NVM address												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h/00h
S/W Reset	00h/00h
H/W Reset	00h/00h

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9.2.37 PROMACT (FEh): Program action

FEH	PROMACT (Program action)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PROMACT	0	↑	1	-	1	1	1	1	1	1	1	0	(FEh)
1st Parameter	1	↑	1	-	0	0	1	0	1	0	0	1	(29h)
2nd Parameter	1	↑	1	-	1	0	1	0	0	1	0	1	(A5h)
Description	When program mode enable, this command need be set.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h/00h
S/W Reset	00h/00h
H/W Reset	00h/00h

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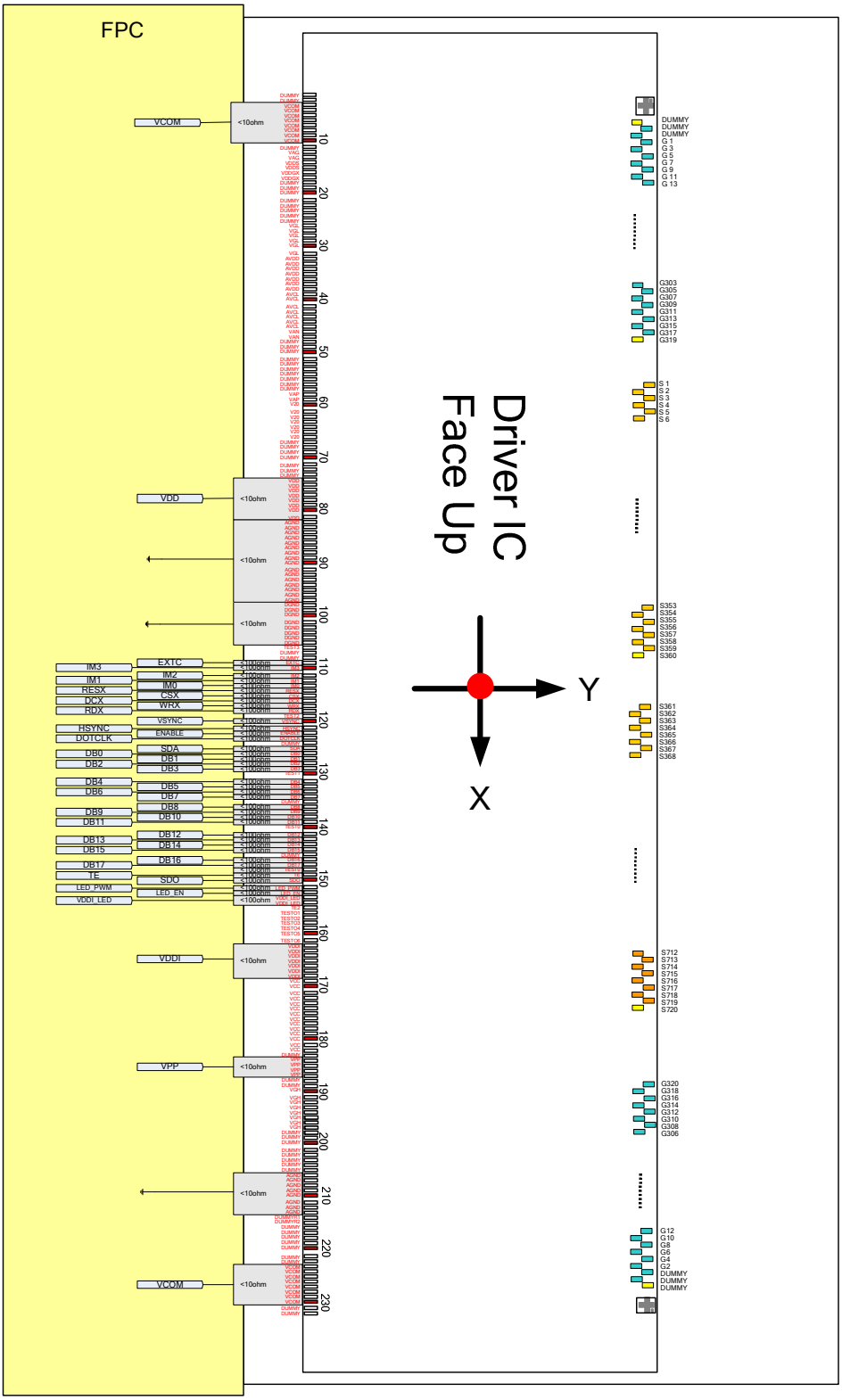
10 APPLICATION

10.1 Configuration of Power Supply Circuit



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10.2 Voltage Generation

The following is the ST7789VW analog voltage pattern diagram:

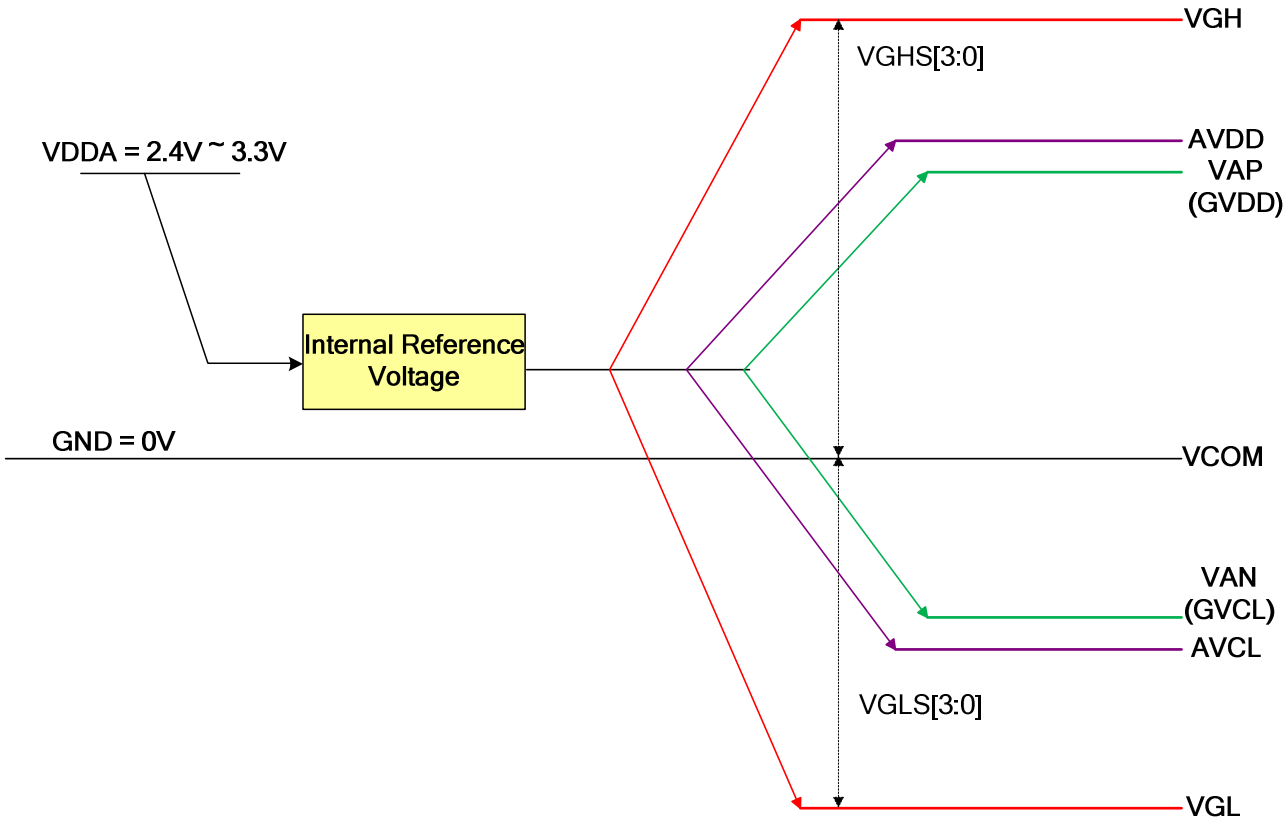

Figure 38 Power Booster Level

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10.3 Relationship about source voltage

The relationship about source voltage is shown as below:

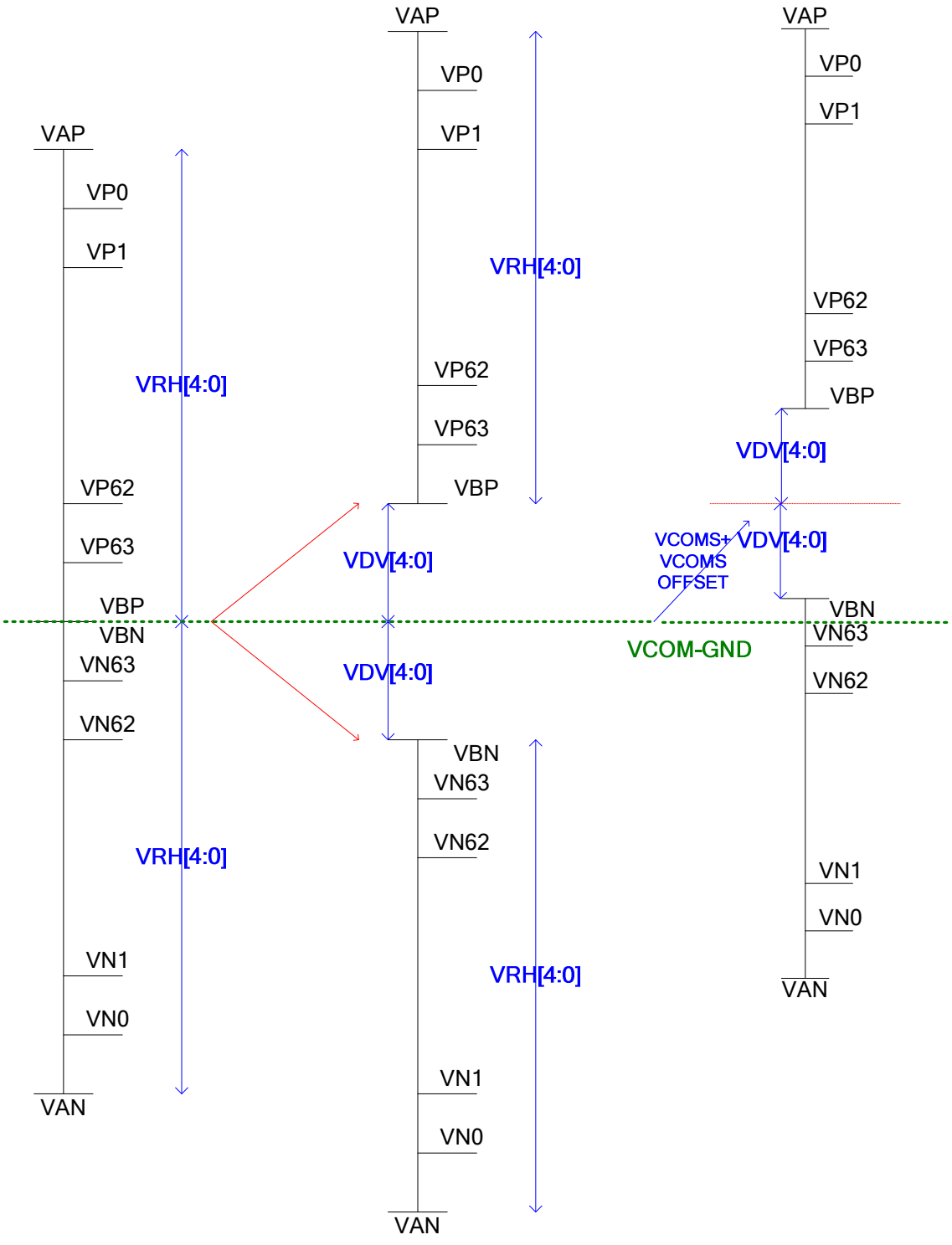

Figure 39 Relationship about source voltage

Note: if VDV=0V, VBP=VBN=VCOM+VCOM OFFSET.

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10.4 Applied Voltage to the TFT panel

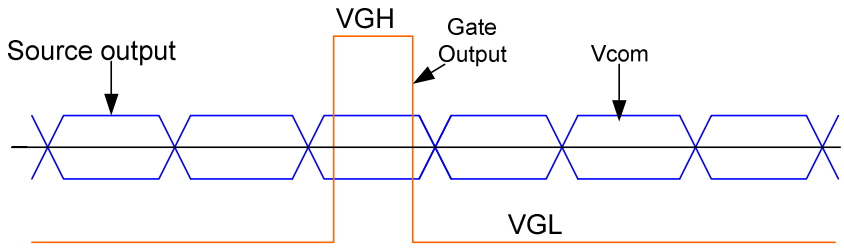

Figure 40 Voltage Output to TFT LCD Panel

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11 REVISION HISTORY

Version	Date	Description
V1.0	2017/09	First issue

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