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## 1. General description

Planar passivated sensitive gate four quadrant triac in a SOT404 (D2PAK) surface-mountable plastic package intended for use in general purpose bidirectional switching and phase control applications. This sensitive gate "series E" triac is intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

## 2. Features and benefits

- Direct triggering from low power drivers and logic ICs
- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Sensitive gate
- Surface-mountable package
- Triggering in all four quadrants

## 3. Applications

- General purpose motor control
- General purpose switching

## 4. Quick reference data

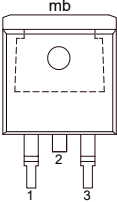
Table 1. Quick reference data

| Symbol                        | Parameter                            | Conditions                                                                                                                          | Min | Typ | Max | Unit               |
|-------------------------------|--------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|--------------------|
| $V_{DRM}$                     | repetitive peak off-state voltage    |                                                                                                                                     | -   | -   | 600 | V                  |
| $I_{T(RMS)}$                  | RMS on-state current                 | full sine wave; $T_{mb} \leq 99\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a> | -   | -   | 12  | A                  |
| $I_{TSM}$                     | non-repetitive peak on-state current | full sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 20\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a> | -   | -   | 95  | A                  |
|                               |                                      | full sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 16.7\text{ ms}$                                                 | -   | -   | 105 | A                  |
| $T_j$                         | junction temperature                 |                                                                                                                                     | -   | -   | 125 | $^{\circ}\text{C}$ |
| <b>Static characteristics</b> |                                      |                                                                                                                                     |     |     |     |                    |
| $I_{GT}$                      | gate trigger current                 | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G+; $T_j = 25\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 7</a>                    | -   | 2.5 | 10  | mA                 |
|                               |                                      | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G-; $T_j = 25\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 7</a>                    | -   | 4   | 10  | mA                 |
|                               |                                      | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G-; $T_j = 25\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 7</a>                    | -   | 5   | 10  | mA                 |

| Symbol                         | Parameter                         | Conditions                                                                                                                              | Min | Typ | Max  | Unit             |
|--------------------------------|-----------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|-----|-----|------|------------------|
|                                |                                   | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G+;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>                       | -   | 11  | 25   | mA               |
| $I_H$                          | holding current                   | $V_D = 12\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 9</a>                                                         | -   | 4   | 30   | mA               |
| $V_T$                          | on-state voltage                  | $I_T = 15\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 10</a>                                                        | -   | 1.4 | 1.65 | V                |
| <b>Dynamic characteristics</b> |                                   |                                                                                                                                         |     |     |      |                  |
| $dV_D/dt$                      | rate of rise of off-state voltage | $V_{DM} = 402\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit | -   | 50  | -    | V/ $\mu\text{s}$ |

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description                    | Simplified outline                                                                                          | Graphic symbol                                                                                |
|-----|--------|--------------------------------|-------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------|
| 1   | T1     | main terminal 1                | <br><b>D2PAK (SOT404)</b> | <br>sym051 |
| 2   | T2     | main terminal 2                |                                                                                                             |                                                                                               |
| 3   | G      | gate                           |                                                                                                             |                                                                                               |
| mb  | T2     | mounting base; main terminal 2 |                                                                                                             |                                                                                               |

6. Ordering information

Table 3. Ordering information

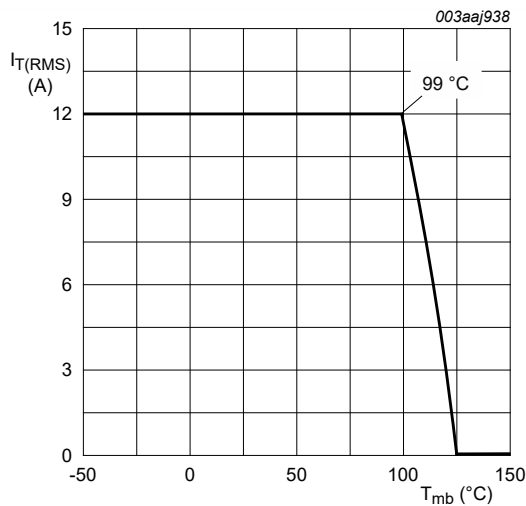
| Type number | Package |                                                                                  |         |
|-------------|---------|----------------------------------------------------------------------------------|---------|
|             | Name    | Description                                                                      | Version |
| BT138B-600E | D2PAK   | plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) | SOT404  |

## 7. Limiting values

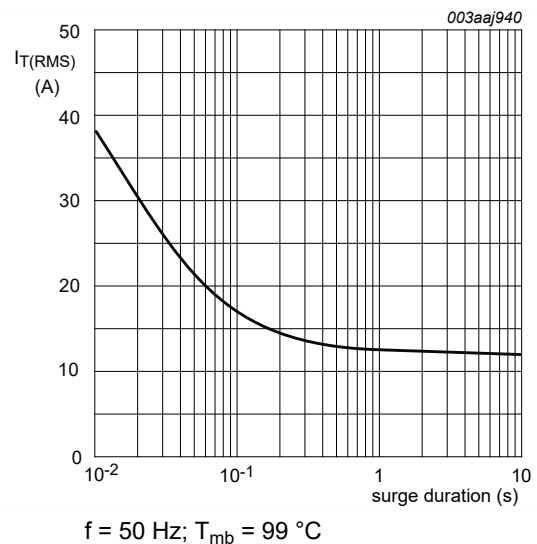
**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol              | Parameter                            | Conditions                                                                                                                                          | Min | Max | Unit                   |
|---------------------|--------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|------------------------|
| $V_{\text{DRM}}$    | repetitive peak off-state voltage    |                                                                                                                                                     | -   | 600 | V                      |
| $I_{\text{T(RMS)}}$ | RMS on-state current                 | full sine wave; $T_{\text{mb}} \leq 99\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>          | -   | 12  | A                      |
| $I_{\text{TSM}}$    | non-repetitive peak on-state current | full sine wave; $T_{\text{j(init)}} = 25\text{ }^{\circ}\text{C}$ ; $t_{\text{p}} = 20\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a> | -   | 95  | A                      |
|                     |                                      | full sine wave; $T_{\text{j(init)}} = 25\text{ }^{\circ}\text{C}$ ; $t_{\text{p}} = 16.7\text{ ms}$                                                 | -   | 105 | A                      |
| $I^2t$              | $I^2t$ for fusing                    | $t_{\text{p}} = 10\text{ ms}$ ; sine-wave pulse                                                                                                     | -   | 45  | $\text{A}^2\text{s}$   |
| $di_{\text{T}}/dt$  | rate of rise of on-state current     | $I_{\text{G}} = 50\text{ mA}$                                                                                                                       | -   | 50  | $\text{A}/\mu\text{s}$ |
| $I_{\text{GM}}$     | peak gate current                    |                                                                                                                                                     | -   | 2   | A                      |
| $P_{\text{GM}}$     | peak gate power                      |                                                                                                                                                     | -   | 5   | W                      |
| $P_{\text{G(AV)}}$  | average gate power                   | over any 20 ms period                                                                                                                               | -   | 0.5 | W                      |
| $T_{\text{stg}}$    | storage temperature                  |                                                                                                                                                     | -40 | 150 | $^{\circ}\text{C}$     |
| $T_{\text{j}}$      | junction temperature                 |                                                                                                                                                     | -   | 125 | $^{\circ}\text{C}$     |



**Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values**



**Fig. 2. RMS on-state current as a function of surge duration; maximum values**

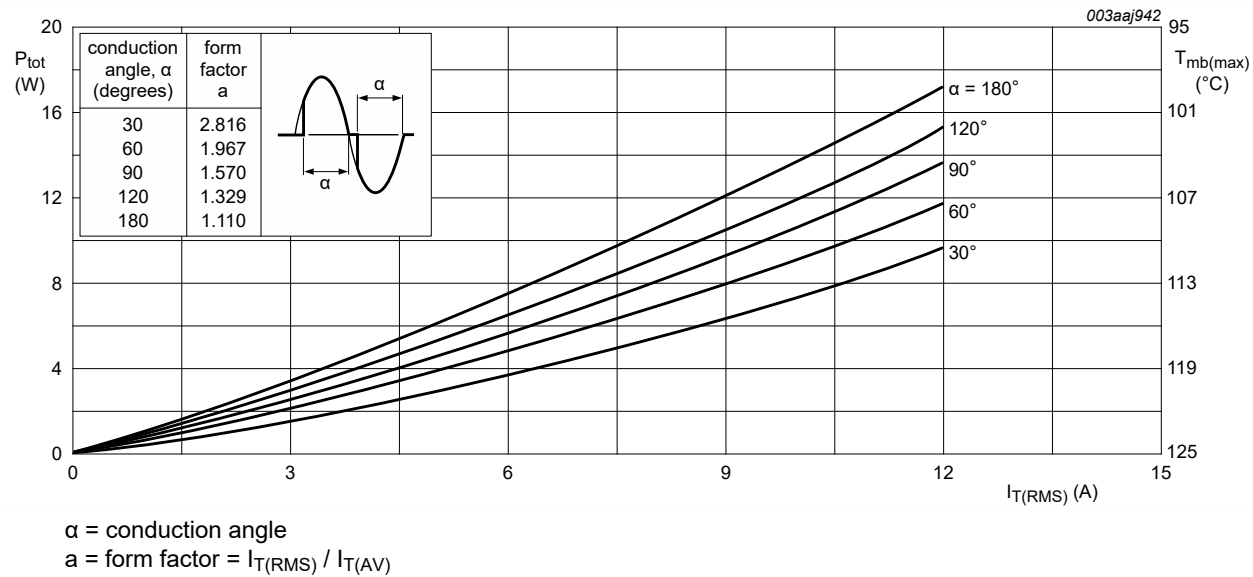


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

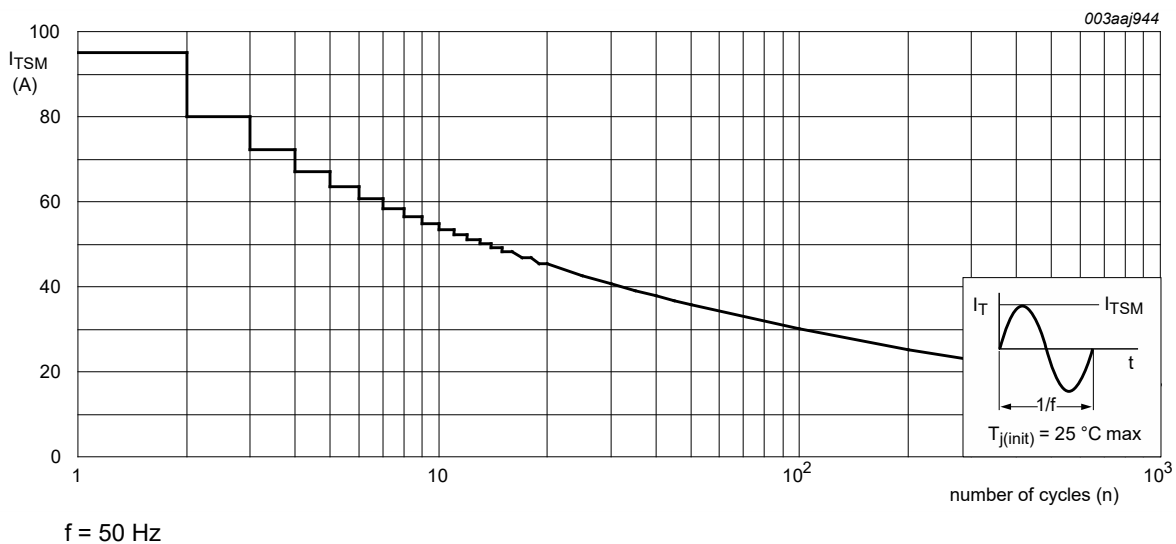
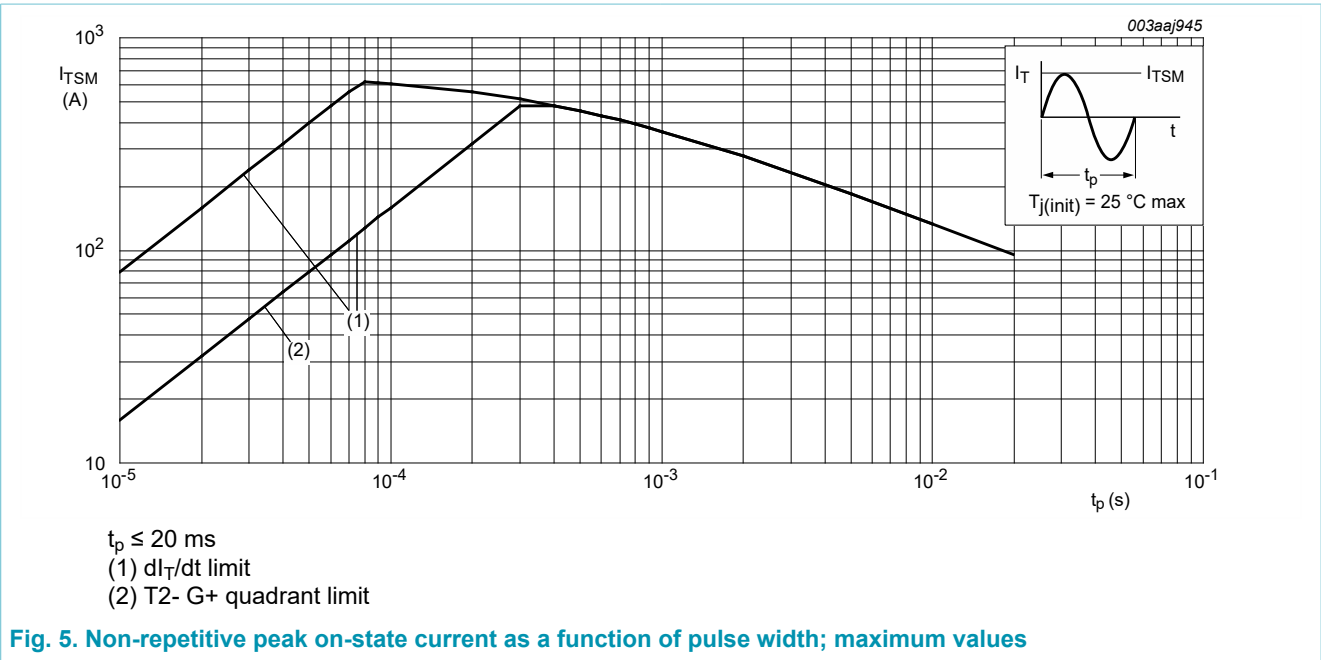


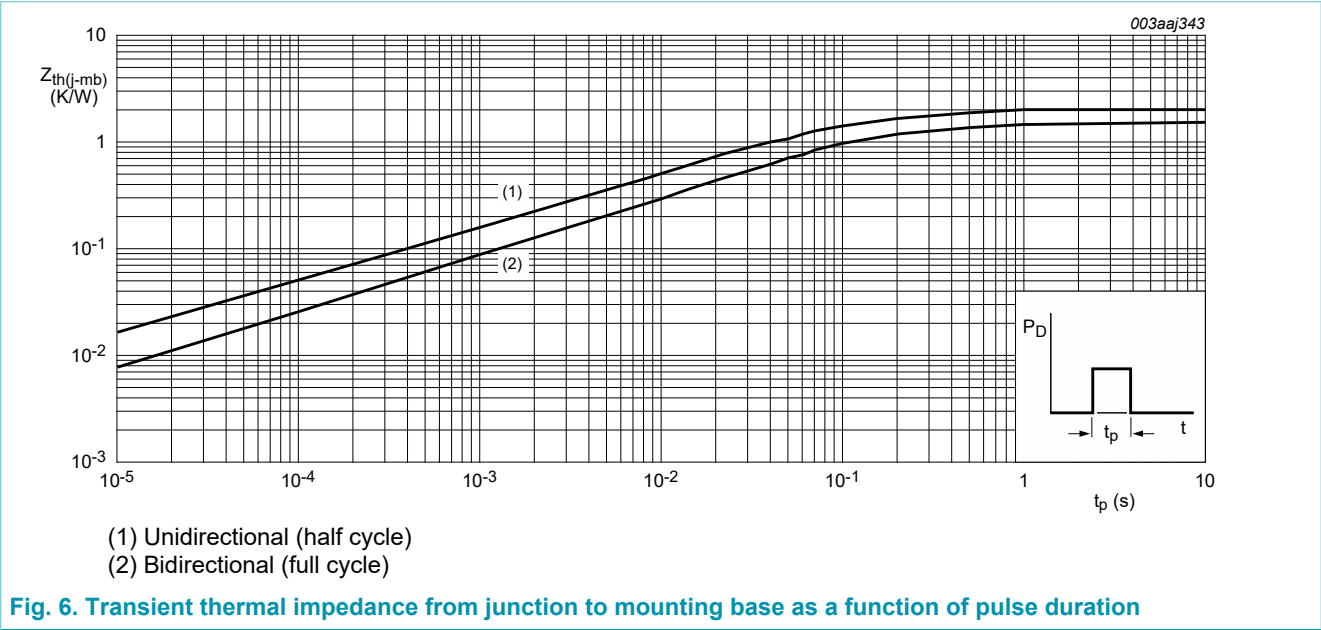
Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



8. Thermal characteristics

Table 5. Thermal characteristics

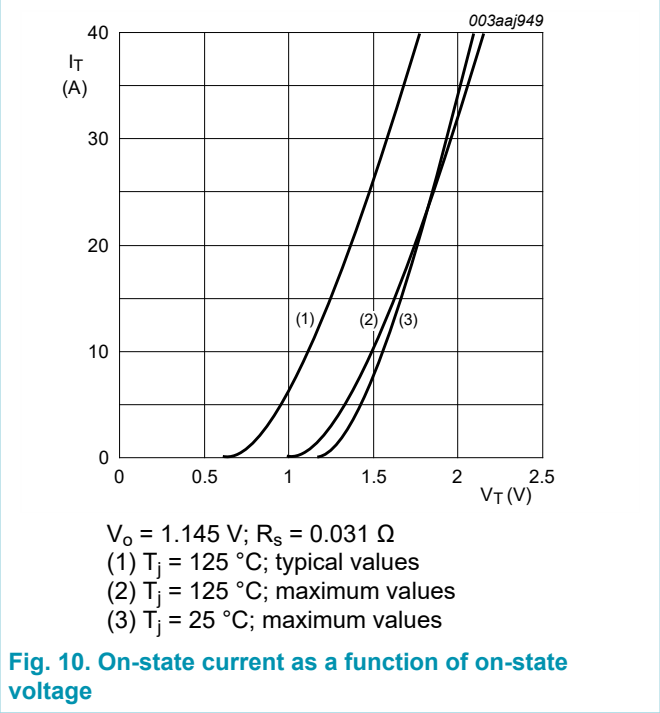
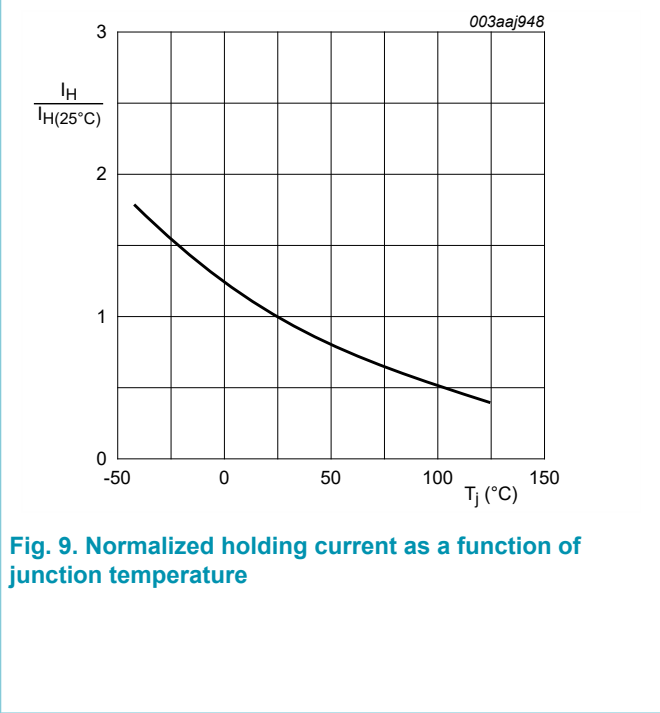
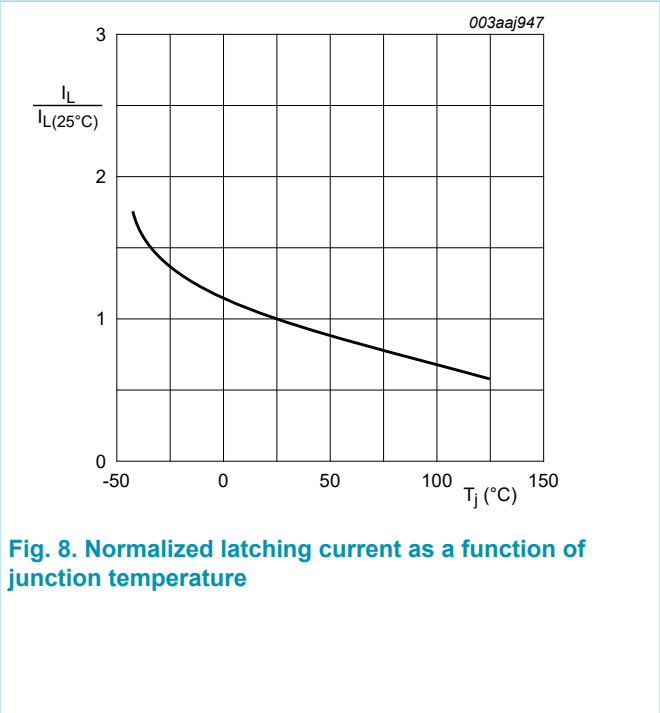
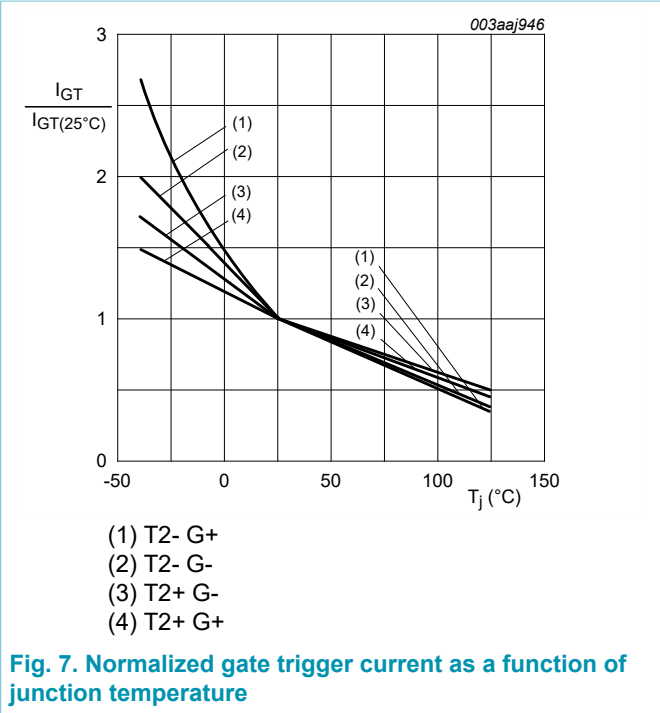
| Symbol         | Parameter                                            | Conditions                   |  | Min | Typ | Max | Unit |
|----------------|------------------------------------------------------|------------------------------|--|-----|-----|-----|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base    | full cycle; Fig. 6           |  | -   | -   | 1.5 | K/W  |
|                |                                                      | half cycle; Fig. 6           |  | -   | -   | 2   | K/W  |
| $R_{th(j-a)}$  | thermal resistance from junction to ambient free air | minimum footprint: FR4 board |  | -   | 55  | -   | K/W  |



## 9. Characteristics

Table 6. Characteristics

| Symbol                         | Parameter                         | Conditions                                                                                                                              |  | Min  | Typ | Max  | Unit             |
|--------------------------------|-----------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|--|------|-----|------|------------------|
| <b>Static characteristics</b>  |                                   |                                                                                                                                         |  |      |     |      |                  |
| $I_{GT}$                       | gate trigger current              | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G+;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>                       |  | -    | 2.5 | 10   | mA               |
|                                |                                   | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G-;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>                       |  | -    | 4   | 10   | mA               |
|                                |                                   | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G-;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>                       |  | -    | 5   | 10   | mA               |
|                                |                                   | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G+;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>                       |  | -    | 11  | 25   | mA               |
| $I_L$                          | latching current                  | $V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2+ G+;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>                       |  | -    | 3.2 | 30   | mA               |
|                                |                                   | $V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2+ G-;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>                       |  | -    | 16  | 40   | mA               |
|                                |                                   | $V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2- G-;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>                       |  | -    | 4   | 30   | mA               |
|                                |                                   | $V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2- G+;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>                       |  | -    | 5.5 | 40   | mA               |
| $I_H$                          | holding current                   | $V_D = 12\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 9</a>                                                         |  | -    | 4   | 30   | mA               |
| $V_T$                          | on-state voltage                  | $I_T = 15\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 10</a>                                                        |  | -    | 1.4 | 1.65 | V                |
| $V_{GT}$                       | gate trigger voltage              | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ;<br><a href="#">Fig. 11</a>                              |  | -    | 0.7 | 1    | V                |
|                                |                                   | $V_D = 400\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 125\text{ }^\circ\text{C}$ ;<br><a href="#">Fig. 11</a>                            |  | 0.25 | 0.4 | -    | V                |
| $I_D$                          | off-state current                 | $V_D = 600\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$                                                                                |  | -    | 0.1 | 0.5  | mA               |
| <b>Dynamic characteristics</b> |                                   |                                                                                                                                         |  |      |     |      |                  |
| $dV_D/dt$                      | rate of rise of off-state voltage | $V_{DM} = 402\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit |  | -    | 50  | -    | V/ $\mu\text{s}$ |



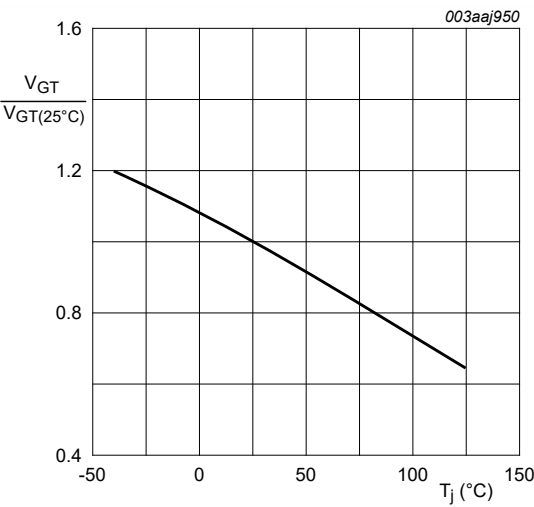


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

10. Package outline

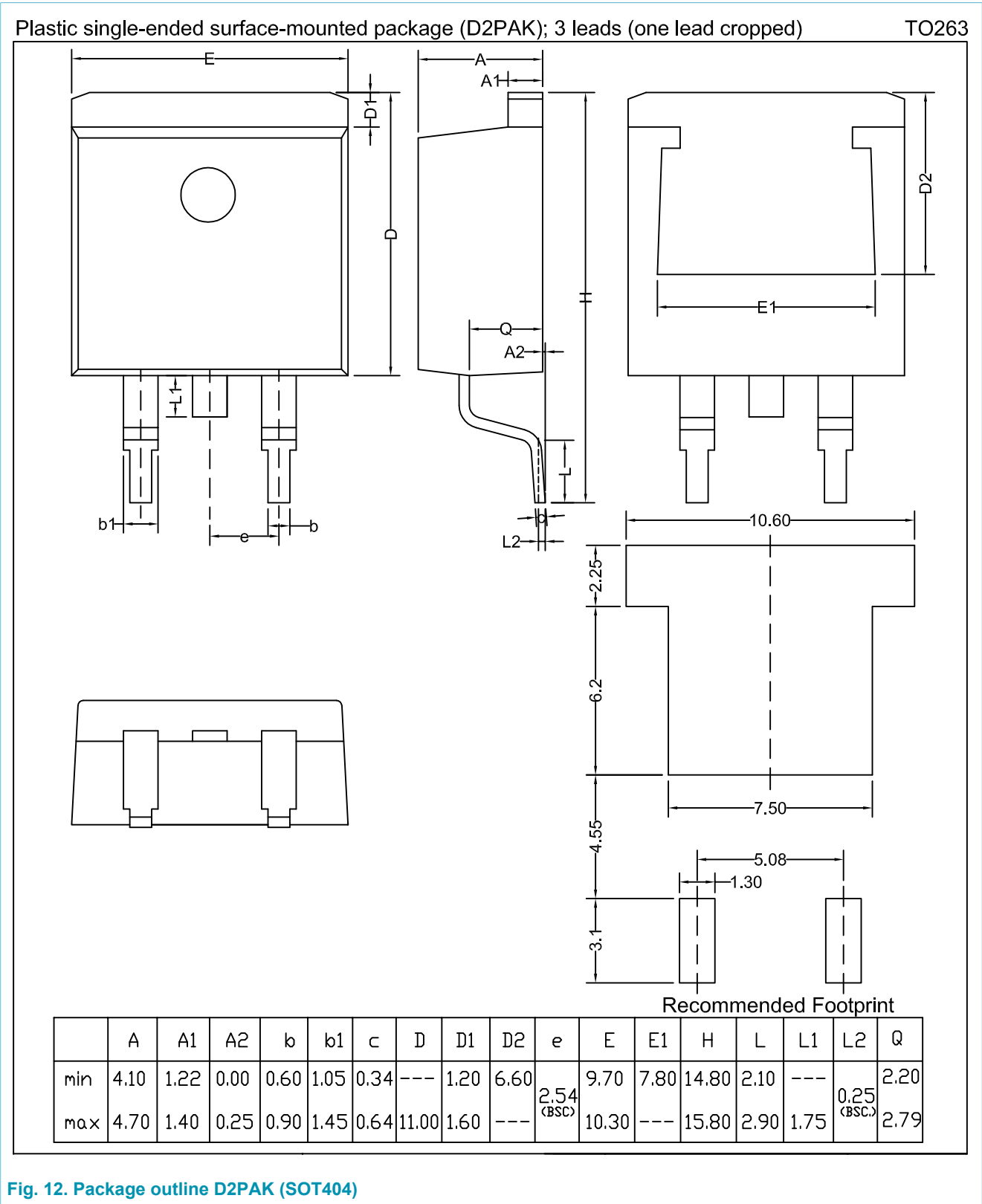


Fig. 12. Package outline D2PAK (SOT404)

## 11. Legal information

### Data sheet status

| Document status [1][2]         | Product status [3] | Definition                                                                            |
|--------------------------------|--------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
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- [1] Please consult the most recently issued document before initiating or completing a design.
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