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## Description

The AP22811 is a single channel current-limit integrated high-side power switch optimized for Universal Serial Bus (USB) and other hot-swap applications. The family of devices complies with USB standards and is available with both polarities of Enable input.

The device has fast short-circuit response time for improved overall system robustness, and has an integrated output discharge function to ensure completely controlled discharging of the output voltage capacitor. They provide a complete protection solution for applications subject to heavy capacitive loads and the prospect of short circuit, and offer reverse current blocking, overcurrent, overtemperature and short-circuit protection, as well as controlled rise time and undervoltage lockout functionality. A 6ms deglitch capability on the open-drain Flag output prevents false overcurrent reporting and does not require any external components.

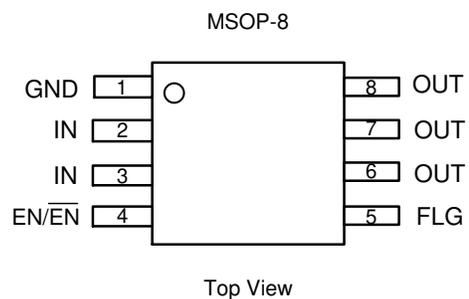
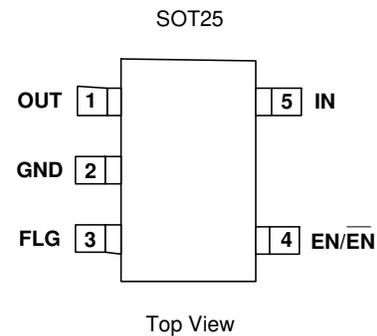
The AP22811 is available in standard Green SOT25 and MSOP-8 packages with RoHS compliance.

## Features

- Input Voltage Range: 2.7V to 5.5V
- 50mΩ On-Resistance
- Built-in Soft-Start with 0.6ms Typical Rise Time
- Fault Report (FLG) with Blanking Time (6ms typ)
- ESD Protection: 2kV HBM, 200V MM
- Active Low (B) or Active High (A) Enable
- Protection
  - Overcurrent with Auto Recovery
  - Short Circuit with Auto Recovery
  - Overtemperature with Auto Recovery
- Output Reverse Current/Voltage Protection
- Thermally Efficient Low Profile Package
- UL Recognized, File Number E322375
- IEC60950-1 CB Scheme Certified
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](mailto:contact@diodes.com) or your local Diodes representative. <https://www.diodes.com/quality/product-definitions/>**

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.  
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.  
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

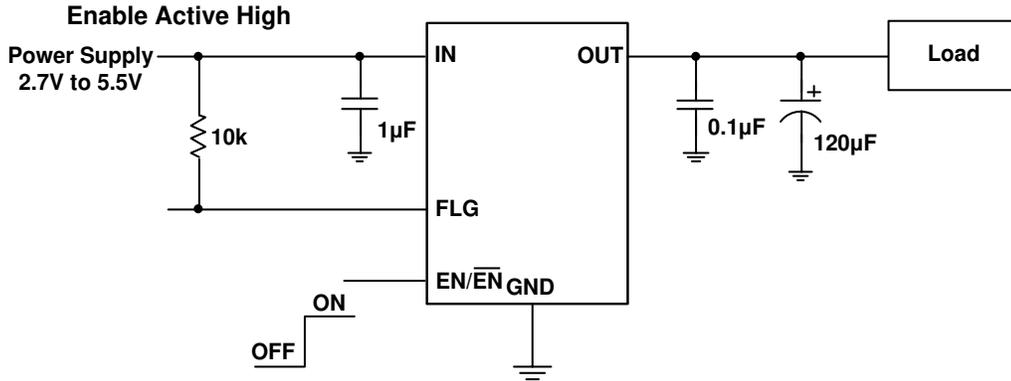
## Pin Assignments



## Applications

- Integrated load switches in Ultrabook PC's
- Power up/down sequencing in Ultrabook PC's
- Notebooks
- Netbooks
- Set-top boxes
- SSD (solid state drives)
- Consumer electronics
- Tablet PCs
- Telecom systems

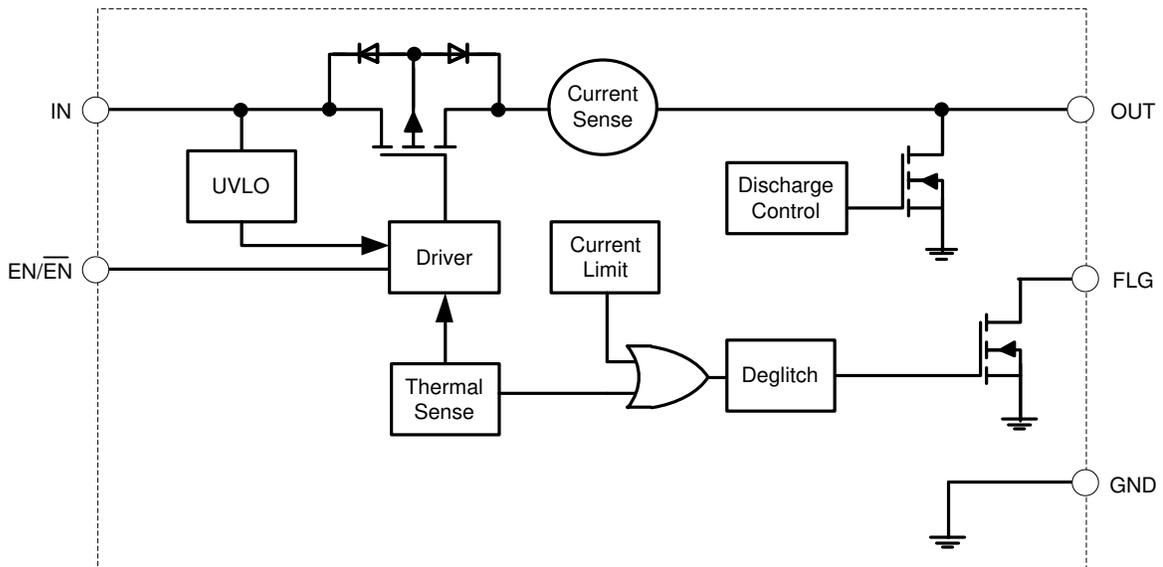
**Typical Applications Circuit**



**Pin Descriptions**

| Pin Number |         | Pin Name | Function   |
|------------|---------|----------|--|
| SOT25      | MSOP-8  |          |  |
| 1          | 6, 7, 8 | OUT      | Voltage Output Pin, connect a 0.1µF bypass capacitor and a high-value capacitor to GND, close to IC. (At least 10µF in USB application.) |
| 2          | 1       | GND      | Ground Pin of the Circuitry  |
| 3          | 5       | FLG      | Overcurrent and Overtemperature Fault Report; Open-Drain flag is active low when triggered.  |
| 4          | 4       | EN/EN    | Enable Input   |
|            |         |          | AP22811A: Active High<br>AP22811B: Active Low  |
| 5          | 2, 3    | IN       | Voltage Input Pin, connect a 1µF low ESR capacitor to GND, close to IC.  |

**Functional Block Diagram**



### Absolute Maximum Ratings (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.) (Note 4)

| Symbol                 | Parameter                               | Ratings                    | Unit             |                    |
|------------------------|---|----------------------------|------------------|--------------------|
| ESD HBM                | Human Body ESD Protection               | 2000                       | V                |                    |
| ESD MM                 | Machine Model ESD Protection            | 200                        | V                |                    |
| $V_{IN}$               | Input Voltage                           | -0.3 to 6.0                | V                |                    |
| $V_{OUT}$              | Output Voltage                          | -0.3 to ( $V_{IN} + 0.3$ ) | V                |                    |
| $V_{EN/\overline{EN}}$ | Enable Voltage                          | -0.3 to ( $V_{IN} + 0.3$ ) | V                |                    |
| $I_L$                  | Load Current                            | Internal Limited           | A                |                    |
| $T_{J(max)}$           | Maximum Junction Temperature            | +150                       | $^\circ\text{C}$ |                    |
| $T_{ST}$               | Storage Temperature                     | -65 to +150                | $^\circ\text{C}$ |                    |
| $R_{\theta JA}$        | Thermal Resistance, Junction to Ambient | SOT25 (Note 6)             | 123              | $^\circ\text{C/W}$ |
|                        |   | MSOP-8 (Note 5)            | 165              |                    |
| $R_{\theta JC}$        | Thermal Resistance, Junction to Case    | SOT25 (Note 6)             | 33               |                    |
|                        |   | MSOP-8 (Note 5)            | 33               |                    |

- Notes:
- Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.
  - Test condition for MSOP-8: device mounted on 1" x 1 1/2" x 2" FR-4 substrate PC board, 2oz copper with minimum recommended pad layout.
  - $R_{\theta JA}$  and  $R_{\theta JC}$  are measured at  $T_A = +25^\circ\text{C}$  on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

### Recommended Operating Conditions (Note 7)

| Symbol    | Parameter                                    | Min | Max      | Unit             |
|-----------|--|-----|----------|------------------|
| $V_{IN}$  | Input Voltage                                | 2.7 | 5.5      | V                |
| $I_{OUT}$ | Output Current                               | 0   | 2        | A                |
| $V_{IL}$  | EN/ $\overline{EN}$ Input Logic Low Voltage  | 0   | 0.5      | V                |
| $V_{IH}$  | EN/ $\overline{EN}$ Input Logic High Voltage | 1.5 | $V_{IN}$ | V                |
| $T_A$     | Operating Ambient Temperature                | -40 | +85      | $^\circ\text{C}$ |

- Note:
- Refer to the typical application circuit.

**Electrical Characteristics** ( $V_{IN} = 5V$  @  $T_A = +25^\circ C$ ,  $C_{IN} = 1\mu F$ ,  $C_L = 100nF$ , unless otherwise specified.)

| Symbol                      | Parameter  | Test Conditions   | Min | Typ  | Max | Unit       |
|-----------------------------|--|---|-----|------|-----|------------|
| $V_{UVLO}$                  | Input UVLO   | $V_{IN}$ Rising   | 1.6 | 2.0  | 2.4 | V          |
| $\Delta V_{UVLO}$           | Input UVLO Hysteresis                                  | $V_{IN}$ Decreasing   | —   | 180  | —   | mV         |
| $I_{SHDN}$                  | Input Shutdown Current                                 | Disabled, OUT = Open  | —   | 0.1  | 1   | $\mu A$    |
| $I_Q$                       | Input Quiescent Current                                | Enabled, OUT = Open   | —   | 80   | —   | $\mu A$    |
| $I_{LEAK}$                  | Input Leakage Current                                  | Disabled, OUT Grounded  | —   | 0.1  | 1   | $\mu A$    |
| $I_{REV}$                   | Reverse Leakage Current                                | Disabled, $V_{IN} = 0V$ , $V_{OUT} = 5V$ , $I_{REV}$ at $V_{IN}$          | —   | 0.01 | 1   | $\mu A$    |
| $R_{DS(ON)}$                | Switch On-Resistance                                   | $V_{IN} = 5V$ , $I_{OUT} = 1A$ $T_A = +25^\circ C$                        | —   | 50   | 65  | m $\Omega$ |
|                             |  | $V_{IN} = 3.3V$ , $I_{OUT} = 1A$ $T_A = +25^\circ C$                      | —   | 60   | 90  |            |
| $I_{LIMIT}$                 | Over Load Current Limit                                | $V_{IN} = 5V$ , $V_{OUT} = 4.5V$  | 2.2 | 2.7  | 3.2 | A          |
| $I_{SHORT}$                 | Short-Circuit Current Limit                            | Enabled, Output short to ground   | —   | 0.3  | —   | A          |
| $V_{IL}$                    | EN/ $\overline{EN}$ Input Logic Low Voltage            | $V_{IN} = 2.7V$ to $5.5V$   | —   | —    | 0.5 | V          |
| $V_{IH}$                    | EN/ $\overline{EN}$ Input Logic High Voltage           | $V_{IN} = 2.7V$ to $5.5V$   | 1.5 | —    | —   | V          |
| $I_{LEAK-EN/\overline{EN}}$ | EN/ $\overline{EN}$ Input Leakage                      | $V_{IN} = 5V$ , $V_{EN/\overline{EN}} = 0V$ and $5.5V$                    | —   | 0.01 | 1   | $\mu A$    |
| $I_{LEAK-O}$                | Output Leakage Current                                 | Disabled, $V_{OUT} = 0V$  | —   | 0.5  | 1   | $\mu A$    |
| $t_{D(ON)}$                 | Output Turn-On Delay Time                              | $C_L = 4.7\mu F$ , $R_{LOAD} = 10\Omega$ @ $V_{IN} = 3.3V$ Figure 1       | —   | 1.7  | —   | ms         |
| $t_R$                       | Output Turn-On Rise Time                               | $C_L = 4.7\mu F$ , $R_{LOAD} = 10\Omega$ @ $V_{IN} = 3.3V$ Figure 1       | 1.0 | 2.1  | 3.5 | ms         |
| $t_{D(OFF)}$                | Output Turn-Off Delay Time                             | $C_L = 4.7\mu F$ , $R_{LOAD} = 10\Omega$ @ $V_{IN} = 3.3V$ Figure 1       | —   | 20   | —   | $\mu s$    |
| $t_F$                       | Output Turn-Off Fall Time                              | $C_L = 4.7\mu F$ , $R_{LOAD} = 100\Omega$ @ $V_{IN} = 3.3V$ Figure 1      | —   | 0.65 | —   | ms         |
| $R_{FLG}$                   | FLG Output FET On-Resistance                           | $I_{FLG} = 10mA$  | —   | 40   | 60  | $\Omega$   |
| $I_{FOH}$                   | FLG Off Current  | $V_{FLG} = 5V$  | —   | 0.01 | 1   | $\mu A$    |
| $t_{BLANK}$                 | FLG Blanking Time                                      | Assertion or deassertion due to overcurrent and overtemperature condition | 2   | 6    | 13  | ms         |
| $t_{DIS}$                   | Discharge Time   | $C_L = 1\mu F$ , $V_{IN} = 5V$ , disabled to $V_{OUT} < 0.5V$             | —   | 0.4  | —   | ms         |
| $R_{DIS}$                   | Discharge Resistance                                   | $V_{IN} = 5V$ , Disabled, $I_{OUT} = 1mA$                                 | —   | 90   | 130 | $\Omega$   |
| $T_{SHDN}$                  | Thermal Shutdown Threshold                             | Enabled   | —   | +140 | —   | $^\circ C$ |
| $T_{HYS}$                   | Thermal Shutdown Hysteresis                            | —   | —   | +35  | —   | $^\circ C$ |
| $V_{RVP}$                   | Reverse-Voltage Comparator Trip Point                  | $V_{OUT} - V_{IN}$  | 25  | 50   | 75  | mV         |
| $I_{ROCP}$                  | Reverse Current Limit                                  | $V_{OUT} - V_{IN} = 100mV$  | —   | 400  | —   | mA         |
| $t_{TRIG}$                  | Time from Reverse-Voltage Condition to MOSFET Turn off | $V_{IN}$  | 2   | 6    | 13  | ms         |

**Performance Characteristics**

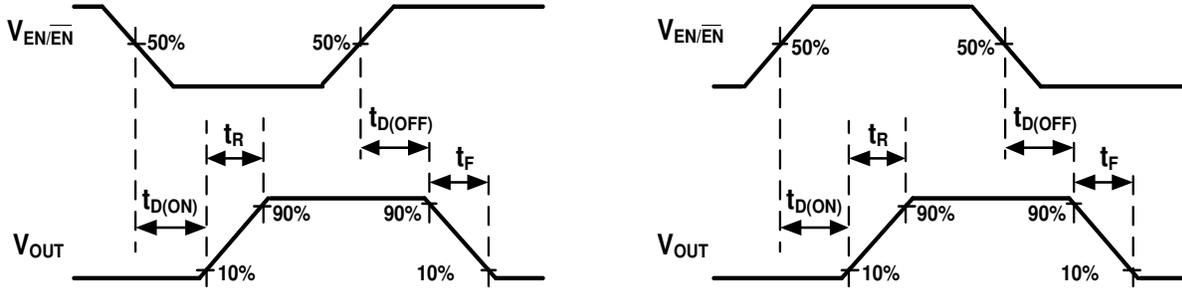
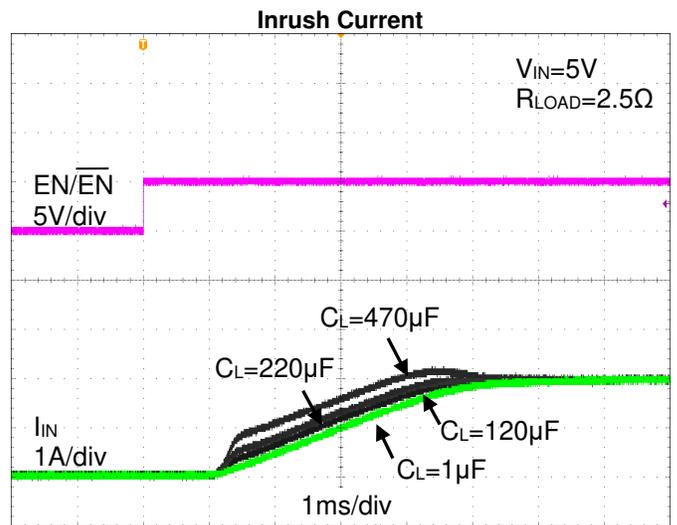
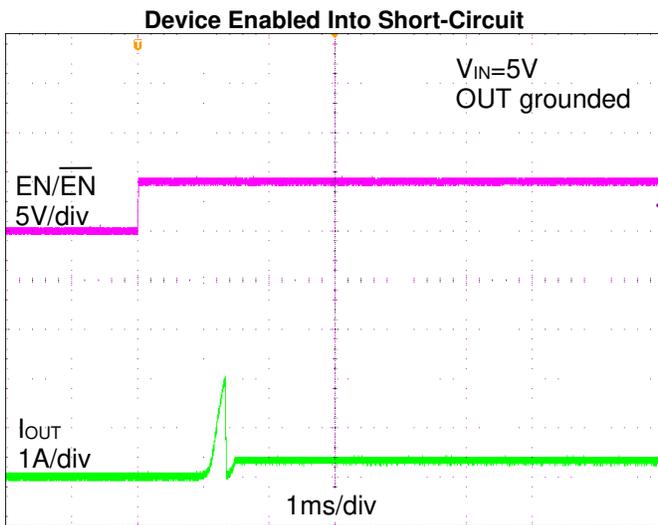
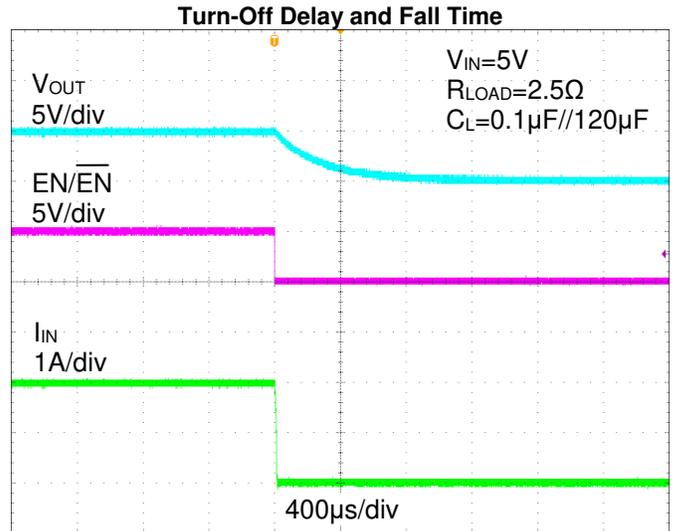
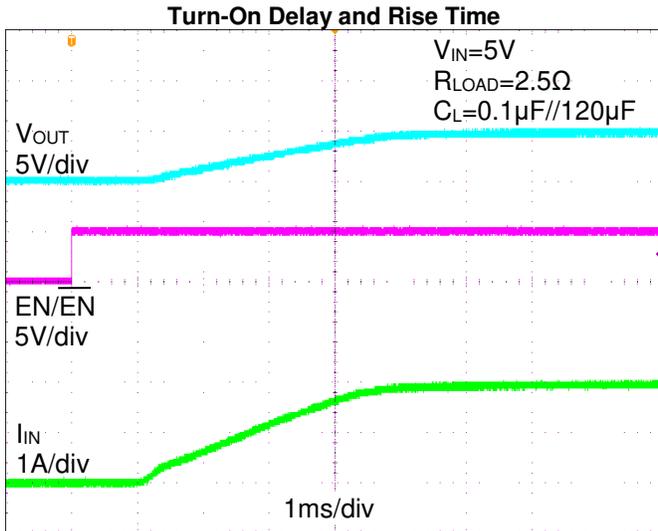
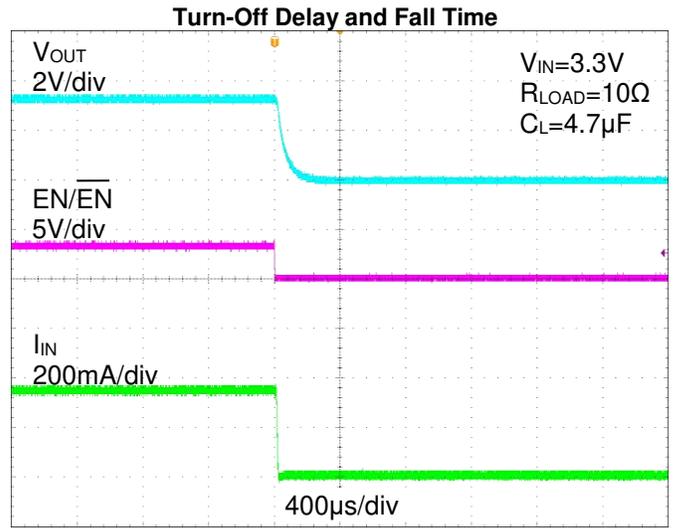
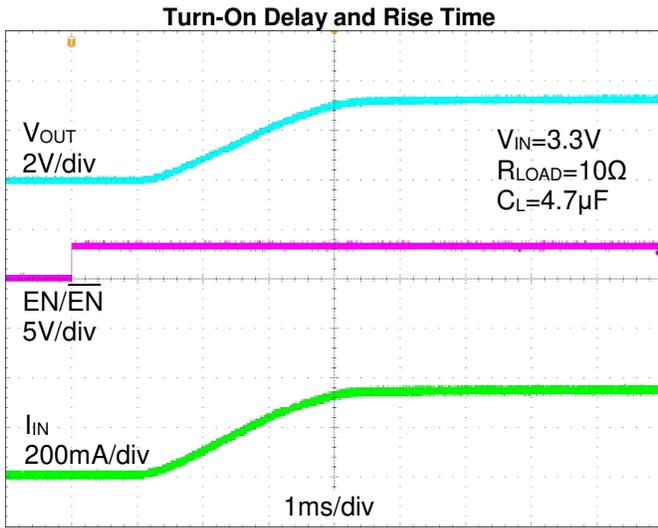


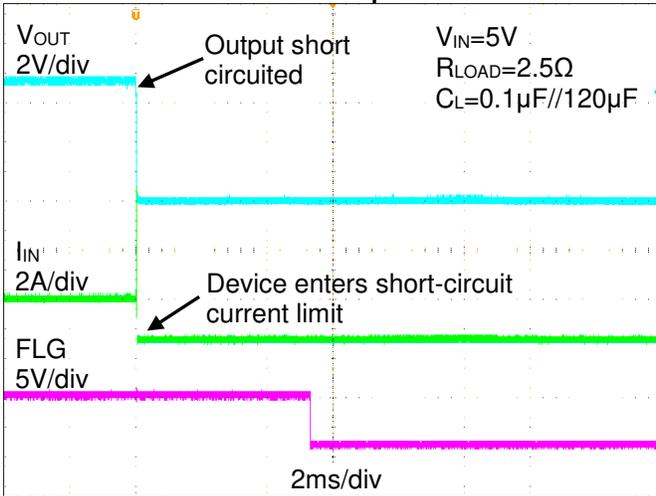
Figure 1. Voltage Waveforms: AP22811B (Active Low, Left), AP22811A (Active High, Right)

**Performance Characteristics** (continued) ( $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$ ,  $C_{IN} = 1\mu\text{F}$ ,  $C_L = 0.1\mu\text{F}$ , unless otherwise specified.)

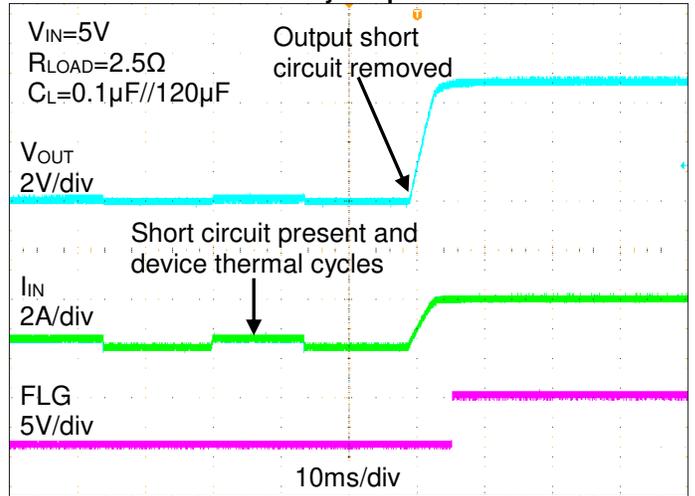


**Performance Characteristics** (continued) ( $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$ ,  $C_{IN} = 1\mu\text{F}$ ,  $C_L = 0.1\mu\text{F}$ , unless otherwise specified.)

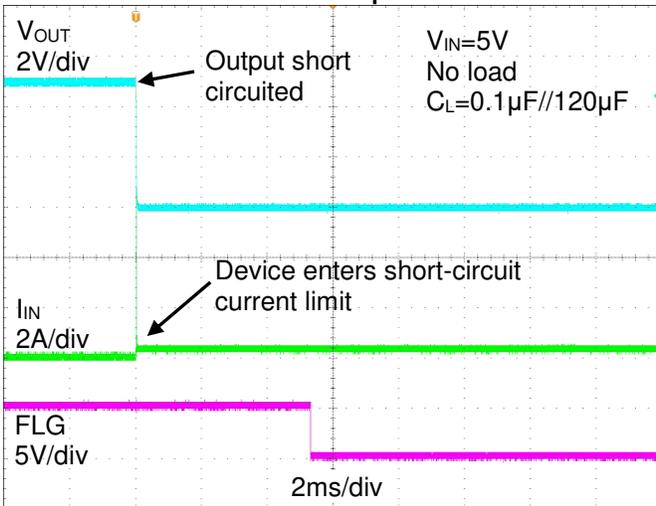
**Full-Load to Short-Circuit Transient Response**



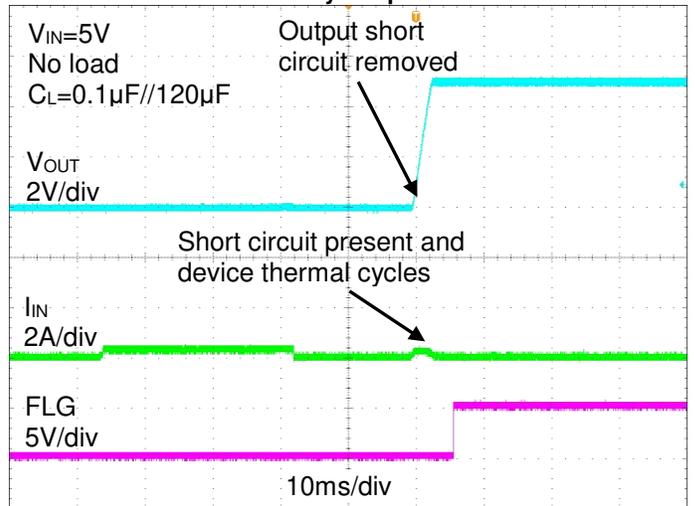
**Short-Circuit to Full-Load Recovery Response**



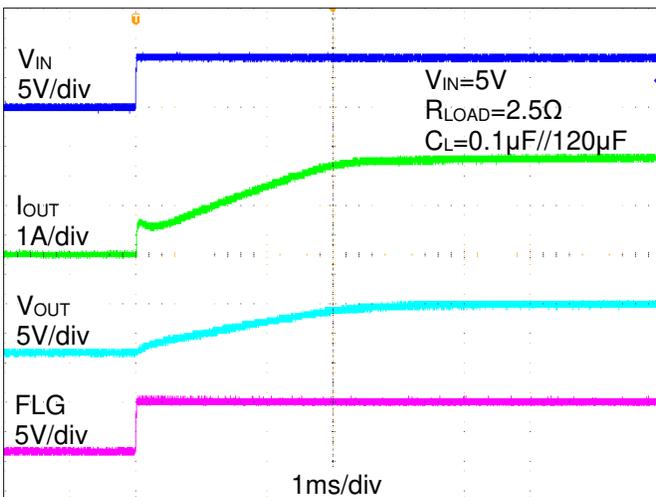
**No-Load to Short-Circuit Transient Response**



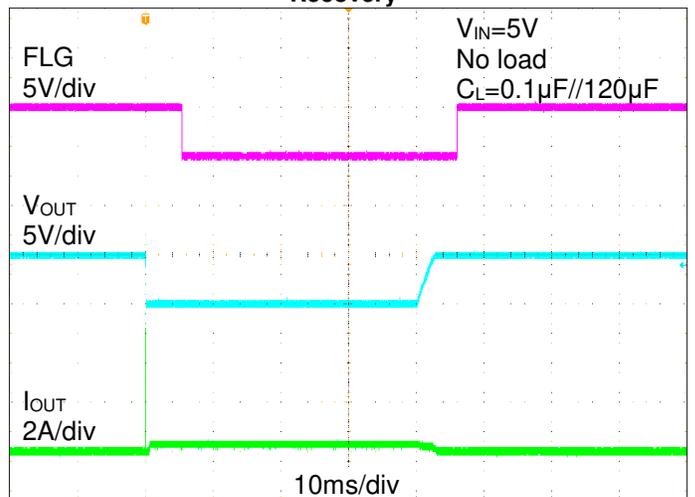
**Short-Circuit to No-Load Recovery Response**



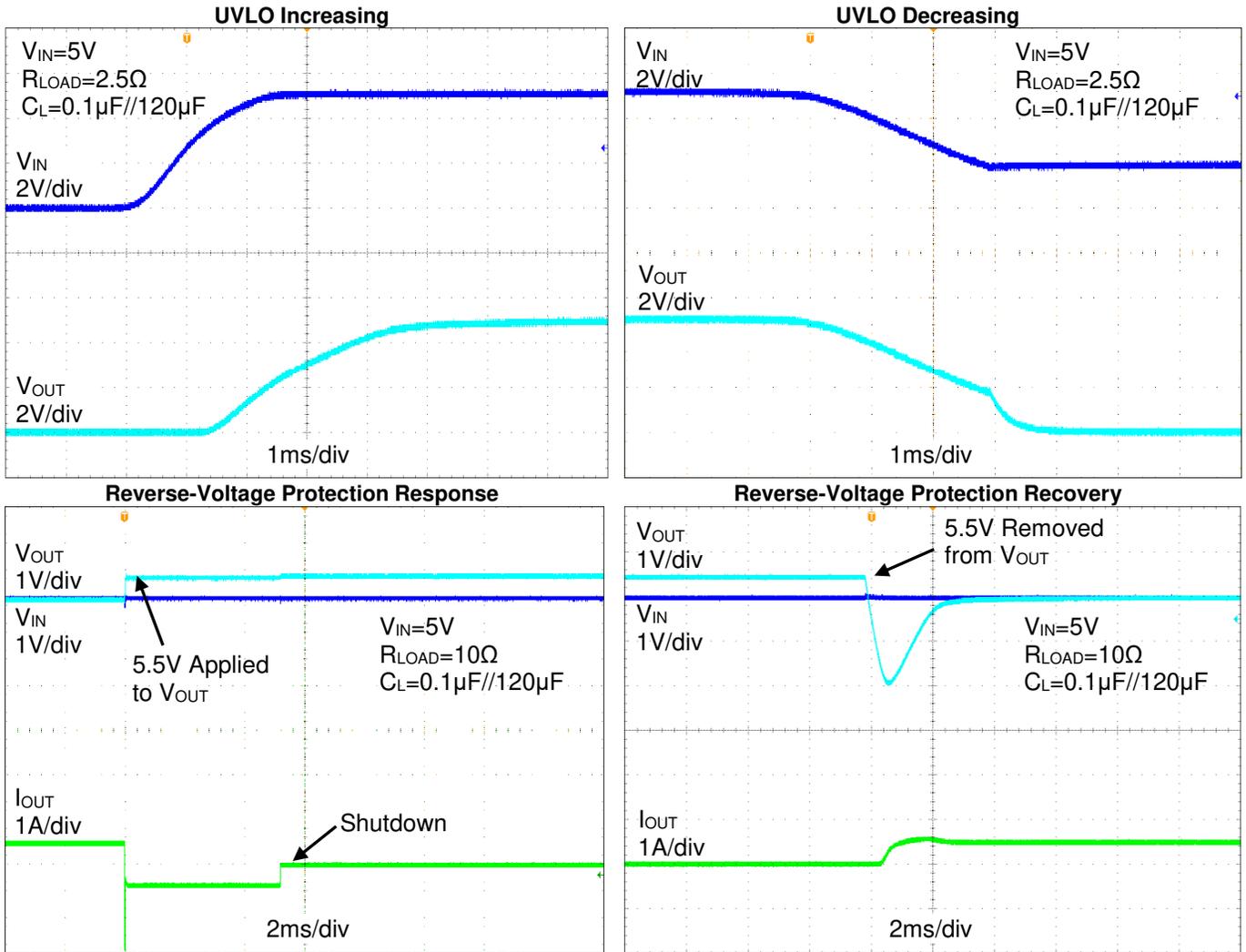
**Power ON**



**Short-Circuit with Blanking Time and Recovery**

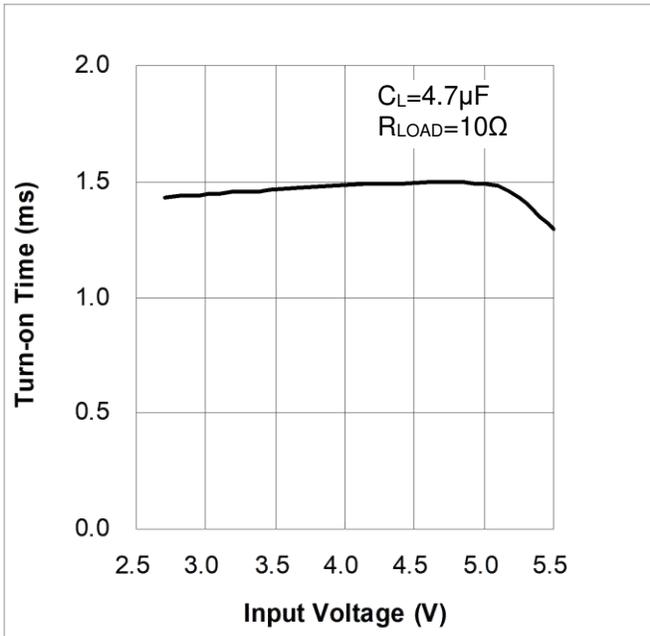


**Performance Characteristics** (continued) ( $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$ ,  $C_{IN} = 1\mu\text{F}$ ,  $C_L = 0.1\mu\text{F}$ , unless otherwise specified.)

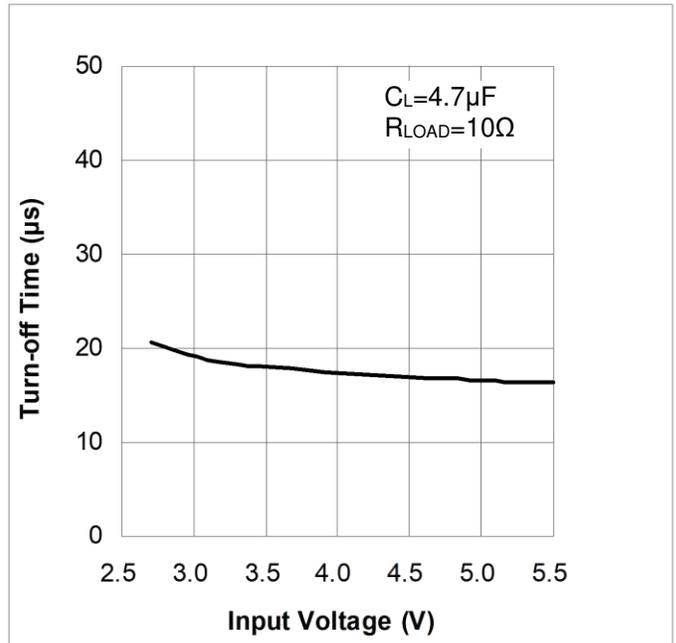


**Performance Characteristics** (continued) ( $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$ ,  $C_{IN} = 1\mu\text{F}$ ,  $C_L = 0.1\mu\text{F}$ , unless otherwise specified.)

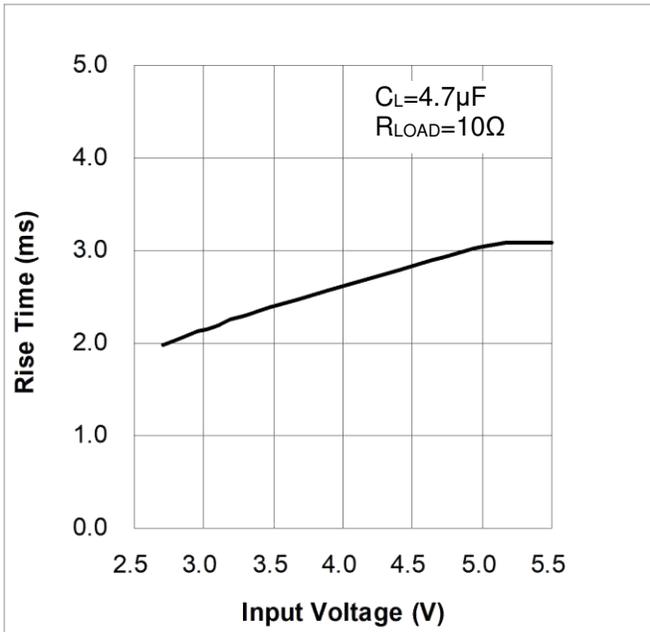
**Turn-on Time vs. Input Voltage**



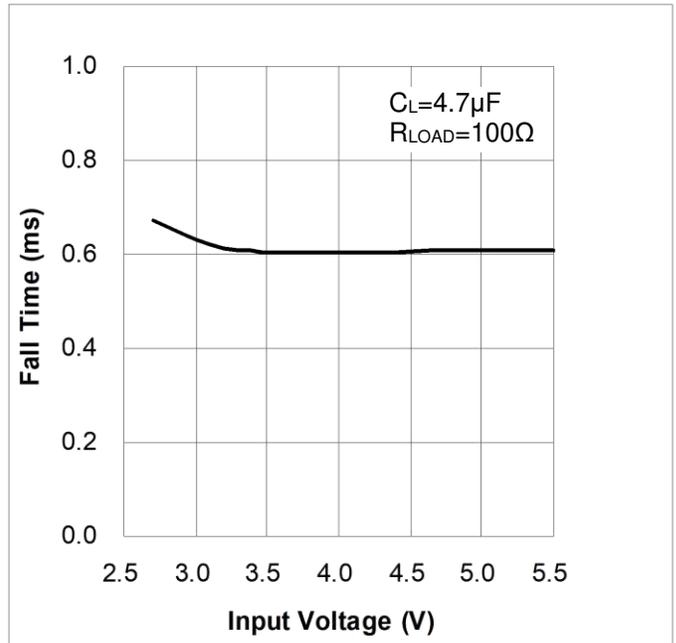
**Turn-off Time vs. Input Voltage**



**Rise Time vs. Input Voltage**

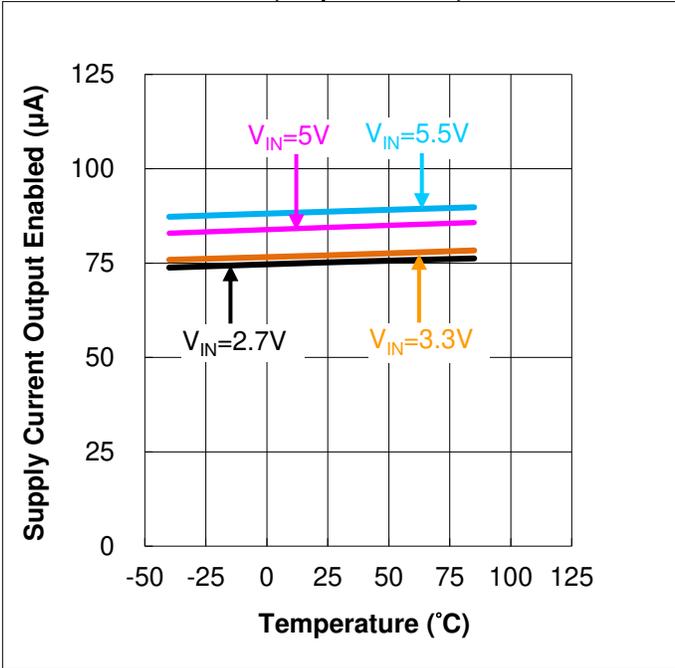


**Fall Time vs. Input Voltage**

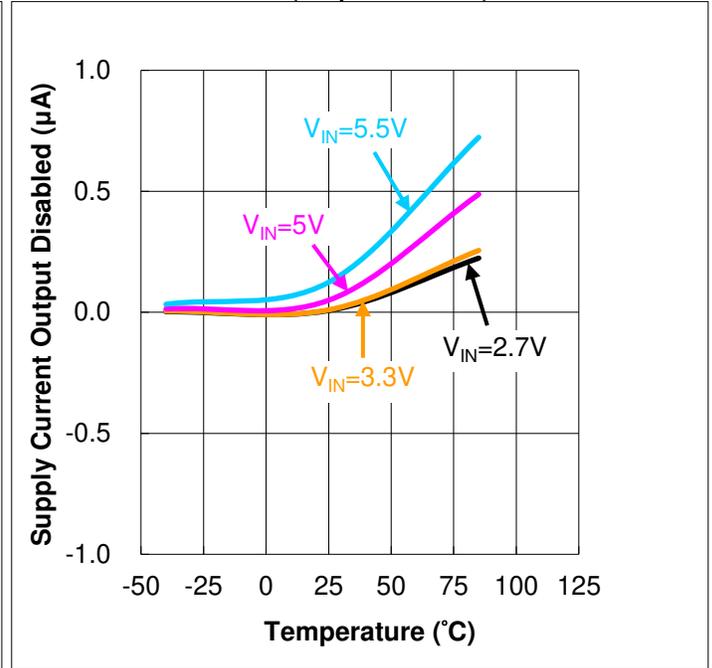


**Performance Characteristics** (continued) ( $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$ ,  $C_{IN} = 1\mu\text{F}$ ,  $C_L = 0.1\mu\text{F}$ , unless otherwise specified.)

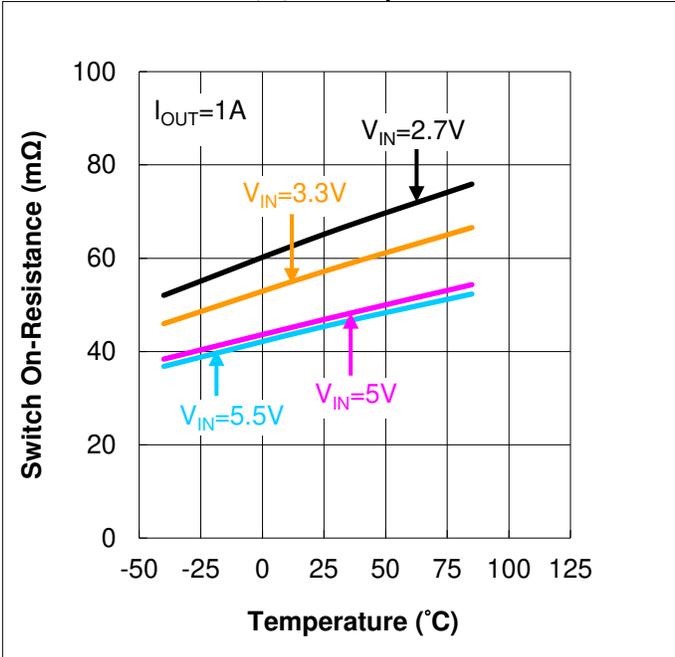
**Supply Current vs. Temperature (Output Enabled)**



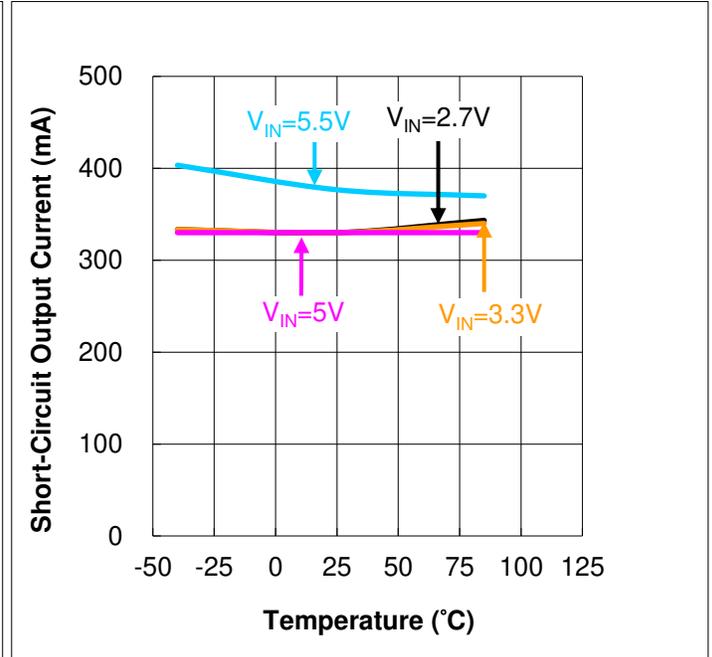
**Supply Current vs. Temperature (Output Disabled)**



**$R_{DS(ON)}$  vs. Temperature**

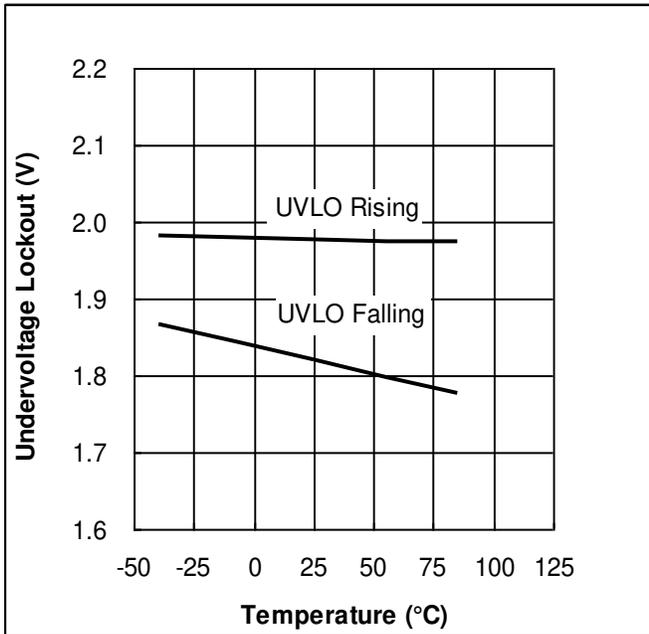


**Short-Circuit Output Current vs. Temperature**

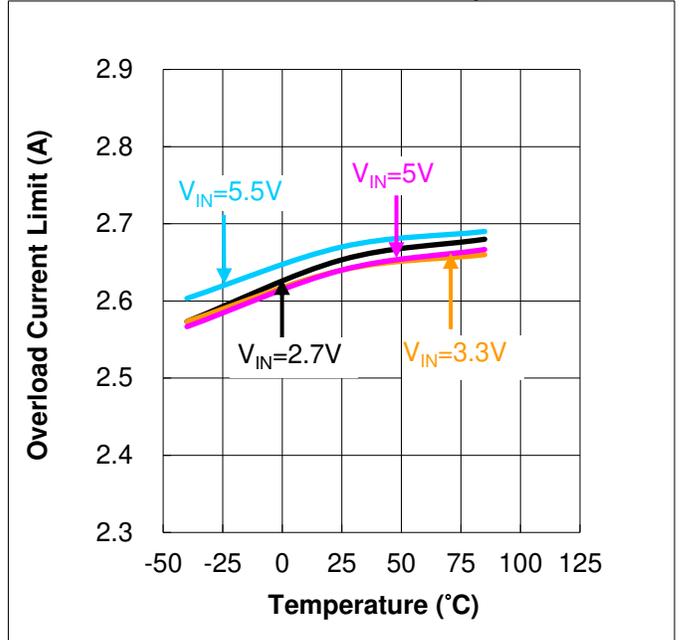


**Performance Characteristics** (continued) ( $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$ ,  $C_{IN} = 1\mu\text{F}$ ,  $C_L = 0.1\mu\text{F}$ , unless otherwise specified.)

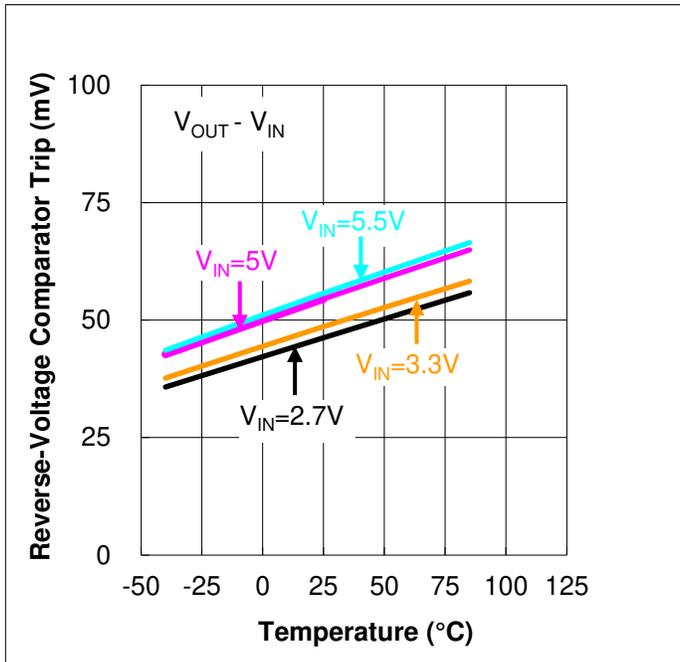
**Undervoltage Lockout vs. Temperature**



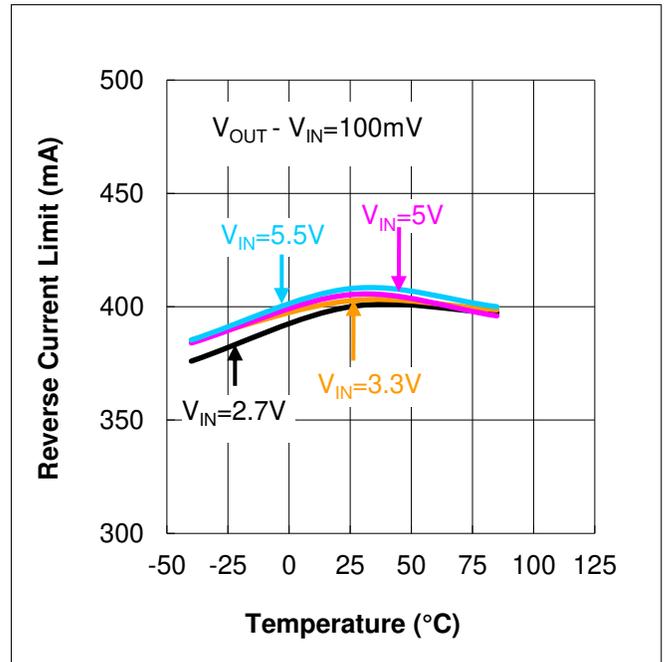
**Overload Current Limit vs. Temperature**



**Reverse-Voltage Comparator Trip vs. Temperature**



**Reverse Current Limit vs. Temperature**



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## Application Information

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### Input and Output Capacitors

It is needed to place a 1 $\mu$ F X7R or X5R ceramic bypass capacitor between IN and GND, close to the device. Placing a high-value capacitor (10 $\mu$ F or 47 $\mu$ F) close to input pin is also recommended when the output transient load is heavy. This precaution reduces power-supply transients that may cause ringing on the input.

Connect a minimum 100 $\mu$ F low ESR electrolytic or tantalum capacitor (or 10 $\mu$ F MLCC) between OUT and GND is also needed for hot-plug applications. It's a must to bypass the output with a 0.1 $\mu$ F ceramic capacitor which improves the immunity of the device to short-circuit transients. The Bulky 100 $\mu$ F or larger capacitors help to reduce output droop voltage when a device is plugged in. When abnormal short-circuit condition happens, these capacitors can also reduce output negative voltage due to parasitic inductive effect and avoid device damage.

Please note without the bypass capacitors, an output short may cause ringing on the input; if the voltage is over the maximum voltage rating, it will destroy the internal control circuitry even the duration is short.

### FLG Response

When an overcurrent or overtemperature shutdown condition is encountered, the FLG open-drain output goes active low after a nominal 6ms deglitch timeout. The FLG output remains low until both overcurrent and overtemperature conditions are removed. Connecting a heavy capacitive load to the output of the device can cause a momentary overcurrent condition, which does not trigger the FLG due to the 6ms deglitch timeout. The AP22811 is designed to eliminate false overcurrent reporting without the need of external components to remove unwanted pulses.

However, it is to be noted that, when the FLG pin is not supplied via the same  $V_{IN}$  voltage source of the AP22811 but other external power source, it is strongly required that the AP22811 must be sure to reach a stable operating voltage condition before the other power source applied to FLG pin.

### Overcurrent and Short-Circuit Protection

An internal sensing FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault stays long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted to GND before the device is enabled or before  $V_{IN}$  has been applied. The AP22811 senses the short circuit and immediately clamps output current to a certain safe level.

In the second condition, an output short or an overload occurs while the device is enabled. At the instance the overload occurs, higher current may flow for a very short period of time before the current limit function can react. After the current limit function has tripped, the device switches into current limiting mode and the current is clamped at  $I_{LIMIT}$ , or  $I_{SHORT}$ .

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold ( $I_{TRIG}$ ) is reached or until the thermal limit of the device is exceeded. The AP22811 is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its current limiting mode and is set at  $I_{LIMIT}$ .

### Thermal Protection

Thermal protection prevents the IC from damage when heavy-overload or short-circuit faults are present for extended periods of time. The AP22811 implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. Once the die temperature rises to approximately +140°C due to excessive power dissipation in an overcurrent or short-circuit condition, the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit, allowing the device to cool down approximately +35°C before the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The FLG open-drain output is asserted when an overtemperature shutdown or overcurrent occurs with 6ms deglitch.

### ON/OFF Input Operator

The EN/ $\overline{EN}$  input allows the output current to be switched on and off using a GPIO compatible input. The high signal (switch on) should be at least 1.5V, and the low signal (switch off) no higher than 0.65V. This pin should NOT be left floating. It is advisable to hold the EN/ $\overline{EN}$  signal low when applying or removing power.

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## Application Information (continued)

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### Undervoltage Lockout (UVLO)

Undervoltage lockout function (UVLO) keeps the internal power switch from being turned on until the power supply has reached at least 2V, even if the switch is enabled. Whenever the input voltage falls below approximately 2V, the power switch is quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed.

### Discharge Function

The discharge function of the device is active when enable is disabled or de-asserted. The discharge function with the nMOS power switch implementation is activated and offers a resistive discharge path for the external storage capacitor. This is designed for discharging any residue of the output voltage when either no external output resistance or load resistance is present at the output.

### Output Reverse-Voltage/Current Protection

The output reverse-voltage protection turns off the MOSFET switch whenever the output voltage is higher than the input voltage by 50mV for 6ms, and the MOSFET switch will turn on when output reverse-voltage/current conditions are removed.

### Power Dissipation and Junction Temperature

The low on-resistance of the internal MOSFET allows the small surface-mount packages to pass large current. Using the maximum operating ambient temperature ( $T_A$ ) and  $R_{DS(ON)}$ , the power dissipation can be calculated by:

$$P_D = R_{DS(ON)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

$T_A$  = Ambient temperature °C

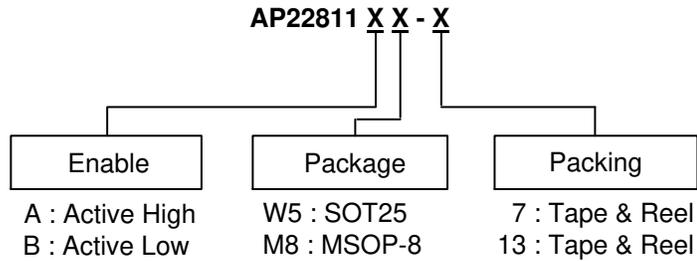
$R_{\theta JA}$  = Thermal resistance

$P_D$  = Total power dissipation

### Board Layout Instruction

Placing input and output capacitors, 1 $\mu$ F and 0.1 $\mu$ F+100 $\mu$ F respectively, close and next to the device pins must be implemented to minimize the effects of parasitic inductance. For best performance, all trace lengths should be kept as short as possible. The input and output PCB traces should be as wide as possible. Use a ground plane to enhance the power dissipation capability of the device.

## Ordering Information

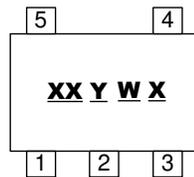


| Part Number   | Part Number Suffix | Package Code | Package | Packing |                 |
|---------------|--------------------|--------------|---------|---------|-----------------|
|               |                    |              |         | Qty.    | Carrier         |
| AP22811AW5-7  | -7                 | W5           | SOT25   | 3000    | 7" Tape & Reel  |
| AP22811BW5-7  | -7                 | W5           | SOT25   | 3000    | 7" Tape & Reel  |
| AP22811AM8-13 | -13                | M8           | MSOP-8  | 2500    | 13" Tape & Reel |
| AP22811BM8-13 | -13                | M8           | MSOP-8  | 2500    | 13" Tape & Reel |

## Marking Information

(1) SOT25

( Top View )

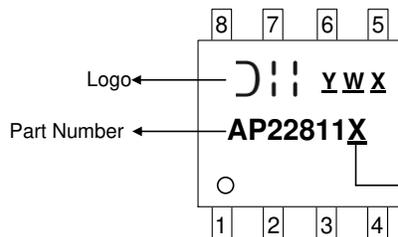


XX : Identification Code  
 Y : Year 0 to 9 (ex: 3 = 2023)  
 W : Week : A to Z : week 1 to 26;  
       a to z : week 27 to 52; z represents week 52 and 53  
 X : Internal Code

| Part Number  | Package | Identification Code |
|--------------|---------|---------------------|
| AP22811AW5-7 | SOT25   | 5Y                  |
| AP22811BW5-7 | SOT25   | 5Z                  |

(2) MSOP-8

( Top view )

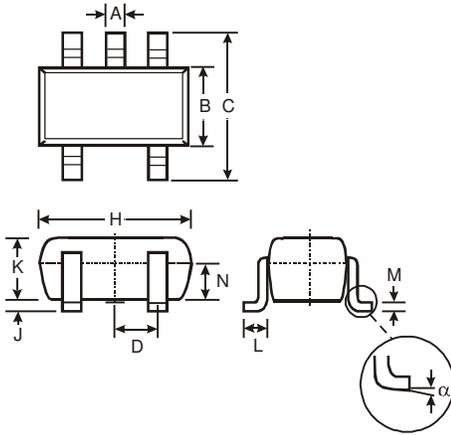


Y : Year : 0 to 9 (ex: 3 = 2023)  
 W : Week : A to Z : week 1 to 26;  
       a to z : week 27 to 52; z represents week 52 and 53  
 X : Internal Code  
 A : Active High  
 B : Active Low

**Package Outline Dimensions**

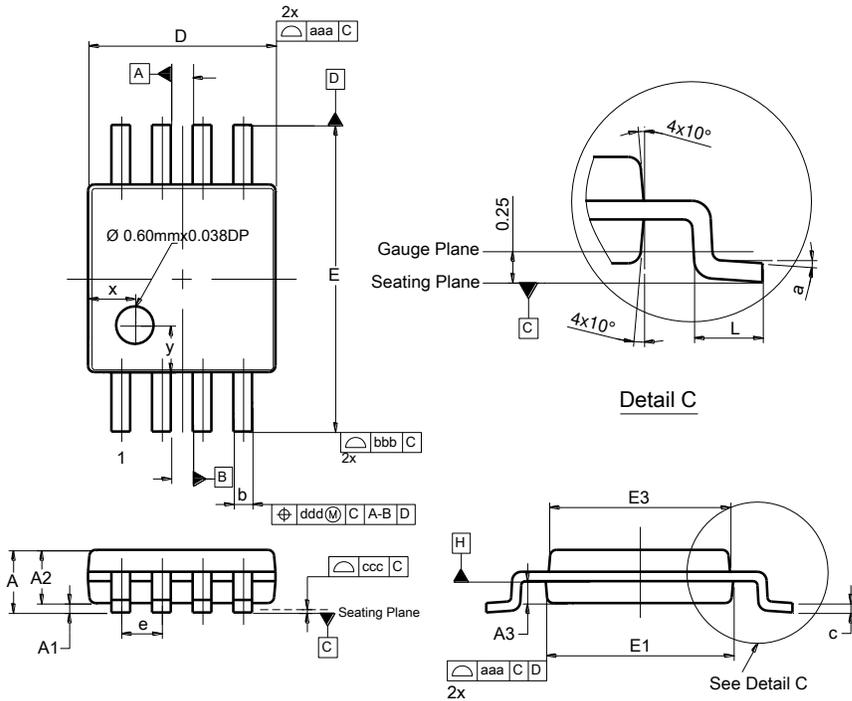
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

(1) SOT25



| SOT25                |       |      |      |
|----------------------|-------|------|------|
| Dim                  | Min   | Max  | Typ  |
| A                    | 0.35  | 0.50 | 0.38 |
| B                    | 1.50  | 1.70 | 1.60 |
| C                    | 2.70  | 3.00 | 2.80 |
| D                    | -     | -    | 0.95 |
| H                    | 2.90  | 3.10 | 3.00 |
| J                    | 0.013 | 0.10 | 0.05 |
| K                    | 1.00  | 1.30 | 1.10 |
| L                    | 0.35  | 0.55 | 0.40 |
| M                    | 0.10  | 0.20 | 0.15 |
| N                    | 0.70  | 0.80 | 0.75 |
| α                    | 0°    | 8°   | -    |
| All Dimensions in mm |       |      |      |

(2) MSOP-8

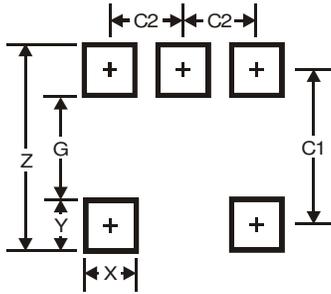


| MSOP-8               |      |      |       |
|----------------------|------|------|-------|
| Dim                  | Min  | Max  | Typ   |
| A                    | --   | 1.10 | --    |
| A1                   | 0.05 | 0.15 | 0.10  |
| A2                   | 0.75 | 0.95 | 0.86  |
| A3                   | 0.29 | 0.49 | 0.39  |
| b                    | 0.22 | 0.38 | 0.30  |
| c                    | 0.08 | 0.23 | 0.15  |
| D                    | 2.90 | 3.10 | 3.00  |
| E                    | 4.70 | 5.10 | 4.90  |
| E1                   | 2.90 | 3.10 | 3.00  |
| E3                   | 2.85 | 3.05 | 2.95  |
| e                    | --   | --   | 0.65  |
| L                    | 0.40 | 0.80 | 0.60  |
| a                    | 0°   | 8°   | 4°    |
| x                    | --   | --   | 0.750 |
| y                    | --   | --   | 0.750 |
| aaa                  | 0.20 |      |       |
| bbb                  | 0.25 |      |       |
| ccc                  | 0.10 |      |       |
| ddd                  | 0.13 |      |       |
| All Dimensions in mm |      |      |       |

**Suggested Pad Layout**

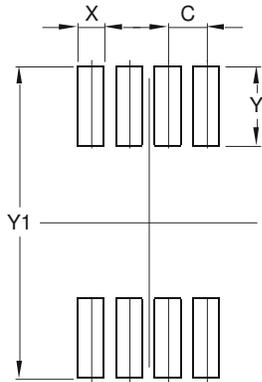
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

(1) SOT25



| Dimensions | Value (in mm) |
|------------|---------------|
| Z          | 3.20          |
| G          | 1.60          |
| X          | 0.55          |
| Y          | 0.80          |
| C1         | 2.40          |
| C2         | 0.95          |

(2) MSOP-8



| Dimensions | Value (in mm) |
|------------|---------------|
| C          | 0.650         |
| X          | 0.450         |
| Y          | 1.350         |
| Y1         | 5.300         |

**Mechanical Data**

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 (E3)
- Weight: SOT25 – 0.015 grams (Approximate)  
MSOP-8 – 0.027 grams (Approximate)

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