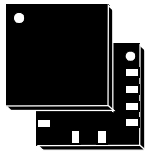
LSM303AGR

Ultra-compact high-performance eCompass module: ultra-low-power 3D accelerometer and 3D magnetometer

Datasheet - preliminary data



LGA-12 (2.0x2.0x1.0 mm)

Features

- 3 magnetic field channels and 3 acceleration channels
- ±50 gauss magnetic dynamic range
- ±2/±4/±8/±16 *g* selectable acceleration full scales
- 16-bit data output
- SPI / I^2C serial interfaces
- Analog supply voltage 1.71 V to 3.6 V
- Power-down mode / low-power mode
- Programmable interrupt generators for free-fall, motion detection and magnetic field detection
- Embedded self test
- Embedded temperature sensor
- Embedded FIFO
- ECOPACK®, RoHS and “Green” compliant

Applications

- Tilt-compensated compasses
- Map rotation
- Position detection
- Motion-activated functions
- Free-fall detection
- Click/double-click recognition
- Pedometers
- Intelligent power saving for handheld devices
- Display orientation
- Gaming and virtual reality input devices
- Impact recognition and logging
- Vibration monitoring and compensation

Description

The LSM303AGR is an ultra-low-power high-performance system-in-package featuring a 3D digital linear acceleration sensor and a 3D digital magnetic sensor.

The LSM303AGR has linear acceleration full scales of ±2*g*/±4*g*/±8*g*/±16*g* and a magnetic field dynamic range of ±50 gauss.

The LSM303AGR includes an I^2C serial bus interface that supports standard, fast mode, fast mode plus, and high-speed (100 kHz, 400 kHz, 1 MHz, and 3.4 MHz) and an SPI serial standard interface.

The system can be configured to generate an interrupt signal for free-fall, motion detection and magnetic field detection.

The magnetic and accelerometer blocks can be enabled or put into power-down mode separately.

The LSM303AGR is available in a plastic land grid array package (LGA) and is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Table 1. Device summary

Part number	Temp. range [°C]	Package	Packaging
LSM303AGR	-40 to +85	LGA-12	Tray
LSM303AGRTR	-40 to +85	LGA-12	Tape and reel

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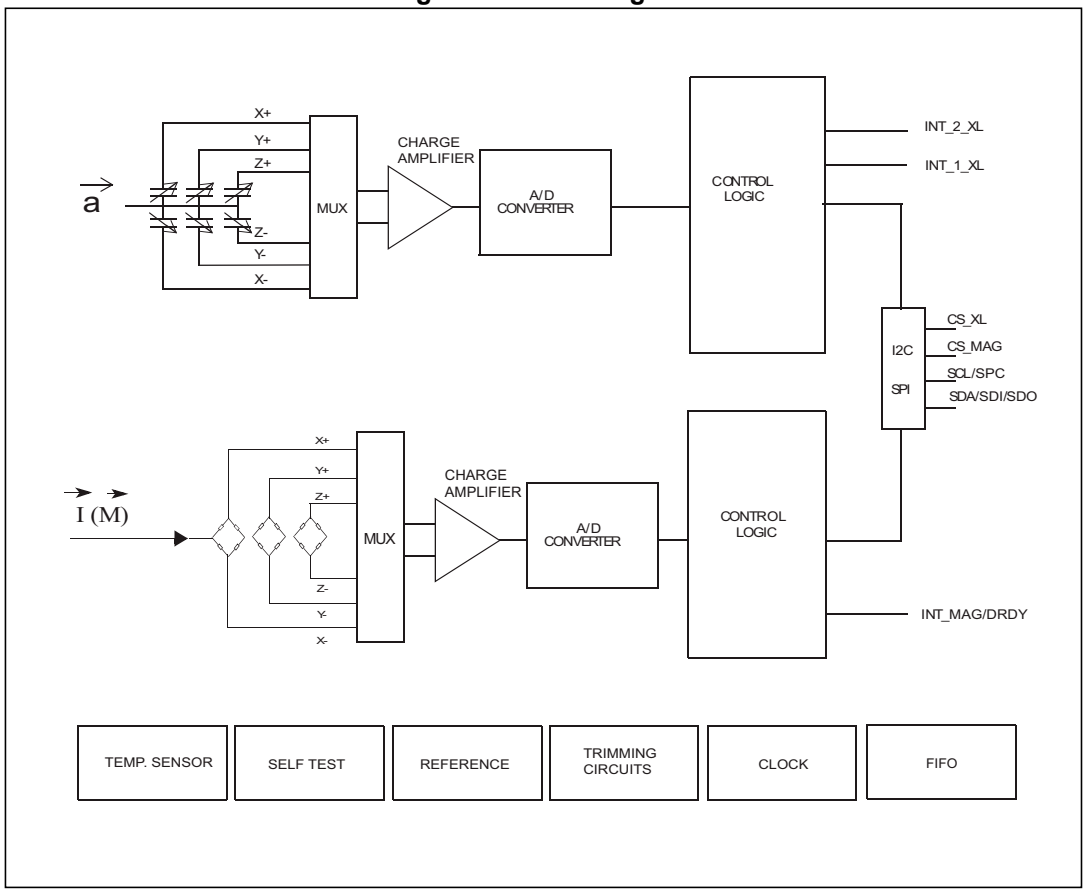
1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connections

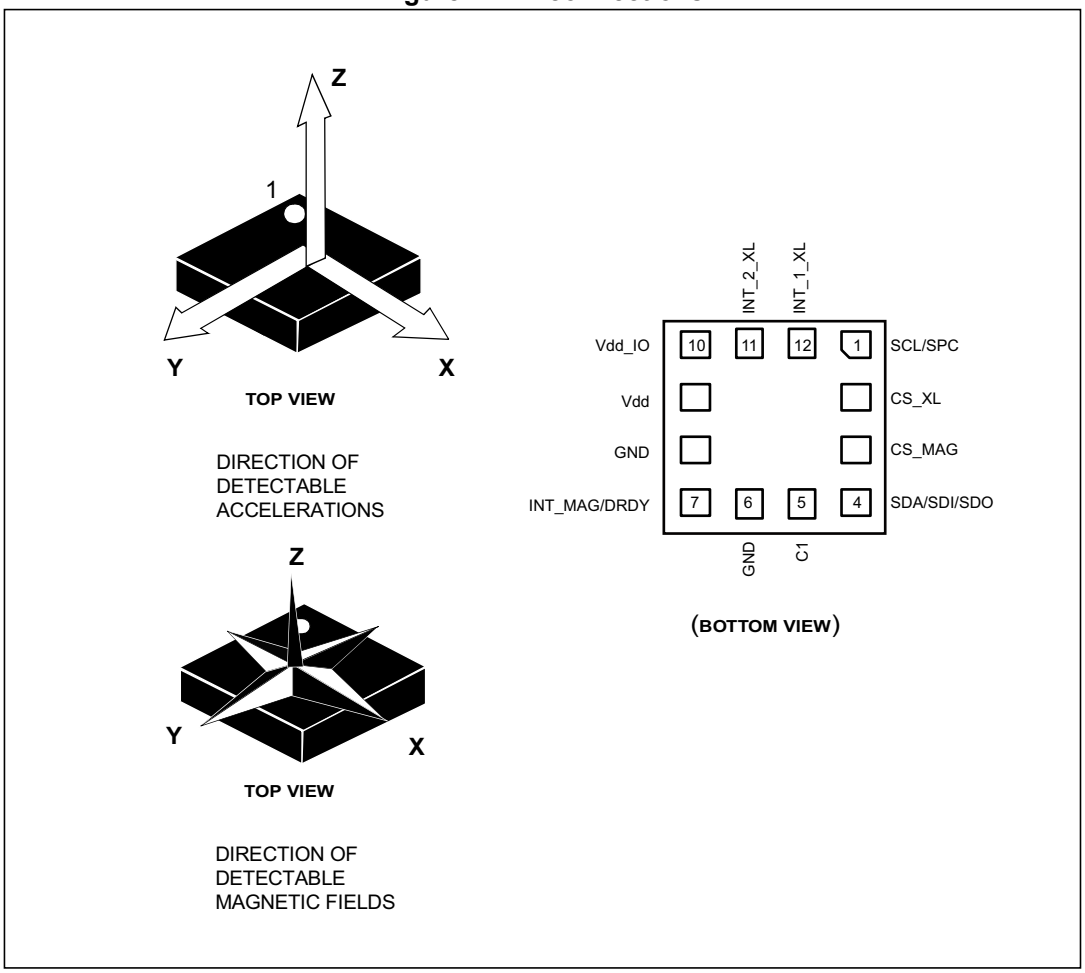


Table 2. Pin description

Pin#	Name	Function
1	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
2	CS_XL	Accelerometer: SPI enable I^2C/SPI mode selection 1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled
3	CS_MAG	Magnetometer: SPI enable I^2C/SPI mode selection 1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled
4	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
5	C1	Capacitor connection (C1 = 220 nF)
6	GND	Connected to GND
7	INT_MAG/DRDY	Magnetometer interrupt/data-ready signal
8	GND	0 V
9	Vdd	Power supply
10	Vdd_IO	Power supply for I/O pins
11	INT_2_XL	Accelerometer interrupt 2
12	INT_1_XL	Accelerometer interrupt 1

2 Module specifications

2.1 Sensor characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted[a].

Table 3. Sensor characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
LA_FS	Linear acceleration measurement range[2]			±2		*g*
				±4		
				±8		
				±16		
M_FS	Magnetic dynamic range			±49.152		gauss
LA_So	Linear acceleration sensitivity	FS = ±2 g and in normal mode		3.9		mg/LSB
		FS = ±2 g and in high-resolution mode		0.98		
		FS = ±2 g and in low-power mode		15.63		
		FS = ±4 g and in normal mode		7.82		
		FS = ±4 g and in high-resolution mode		1.95		
		FS = ±4 g and in low-power mode		31.26		
		FS = ±8 g and in normal mode		15.63		
		FS = ±8 g and in high-resolution mode		3.9		
		FS = ±8 g and in low-power mode		62.52		
		FS = ±16 g and in normal mode		46.9		
		FS = ±16 g and in high-resolution mode		11.72		
		FS = ±16 g and in low-power mode		187.58		
M_GN	Magnetic sensitivity			1.5		mgauss/ LSB
LA_TCSo	Linear acceleration sensitivity change vs. temperature[3]			0.01		%/°C
LA_TyOff	Typical zero-*g* level offset accuracy[4],[5]			±40		mg
M_TyOff	Magnetic sensor offset	With offset cancellation		0		gauss
		Without offset cancellation		±1		
LA_TCOff	Zero-*g* level change vs. temp.[3]	Max. delta from 25 °C		±0.5		mg/°C
LA_An	Linear acceleration RMS noise	ODR = 100 Hz, high-resolution mode, FS = ±2 *g*		3		mg (RMS)

a. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.71 V to 3.6 V.

Table 3. Sensor characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
M_R	Magnetic RMS noise(6)	High-performance mode		3		mgauss (RMS)
LA_ST	Linear acceleration self-test positive difference(7) (8) (9)	FS = ±2 *g*; normal mode	17		360	LSB
M_ST	Magnetic self-test(10)		15		500	mgauss
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Verified by wafer level test and measurement of initial offset and sensitivity.
3. Measurements are performed in a uniform temperature setup and they are based on characterization data in a limited number of samples, not measured during final test for production.
4. Typical zero-*g* level offset value after MSL3 preconditioning.
5. Offset can be eliminated by enabling the built-in high-pass filter.
6. With low-pass filter or offset cancellation enabled.
7. The sign of “Self-test output change” is defined by the ST bit in *CTRL_REG4_A (23h)*, for all axes.
8. “Self-test output change” is defined as the absolute value of:
   $OUTPUT[LSb]_{(Self\text{-}test\ enabled)}$ - $OUTPUT[LSb]_{(Self\text{-}test\ disabled)}$. 1LSb=4mg at 10bit representation, ±2 *g* full scale.
9. After enabling the ST bit, correct data is obtained after two samples (low-power mode / normal mode) or after eight samples (high-resolution mode).
10. Magnetic “self-test” is defined as: $OUTPUT[gauss]_{(Self\text{-}test\ enabled)}$ - $OUTPUT[gauss]_{(Self\text{-}test\ disabled)}$.

2.2 Temperature sensor characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted [b].

Table 4. Temperature sensor characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
TSDr	Temperature sensor output change vs. temp.			1		digit/°C(2)
TODR	Temperature refresh rate			ODR(3)		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. 8-bit resolution.
3. Refer to *Table 34*.

2.3 Electrical characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted.[b]

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
Vdd	Supply voltage		1.71		3.6	V
Vdd_IO	Module power supply for I/O(2)		1.71	1.8	Vdd+0.1	V
LA_Idd_NM	Accelerometer current consumption Magnetic sensor in power-down mode.	50 Hz ODR in normal mode		11		µA
		1 Hz ODR in normal mode		2		
		50 Hz ODR in low-power mode		6		
M_Idd_HR	Magnetic current consumption in high-resolution mode Accelerometer in power-down mode.	ODR = 20 Hz		200		µA
M_Idd_LP	Magnetic current consumption in low-power mode Accelerometer in power-down mode.	ODR = 20 Hz		50		µA
Idd_PD	Current consumption in power-down			1.5		µA
VIH	Digital high-level input voltage		0.8*Vdd_IO			V
VIL	Digital low-level input voltage				0.2*Vdd_IO	V
VOH	High-level output voltage	IOH = 4 mA	Vdd_IO - 0.2			V
VOL	Low-level output voltage	IOL = 4 mA			0.2	V
T_{OP}	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. It is possible to remove Vdd maintaining Vdd_IO without blocking the communication bus, in this condition the measurement chain is powered off.

b. The product is factory calibrated at 2.5 V.The operational power supply range is from 1.71 V to 3.6 V.

2.4 Communication interface characteristics

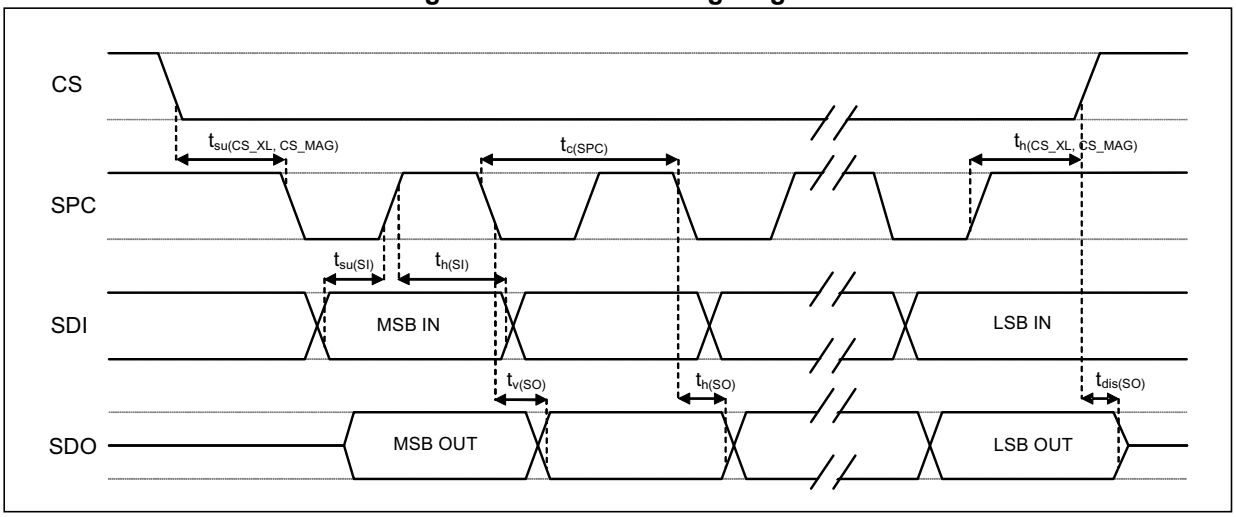
2.4.1 SPI - serial peripheral interface

Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value (1)		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS\_XL,\ CS\_MAG)}$	CS setup time	5		ns
$t_{h(CS\_XL,\ CS\_MAG)}$	CS hold time	20		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	5		
$t_{dis(SO)}$	SDO output disable time		50	

Figure 3. SPI slave timing diagram



Note: Values are guaranteed at 10 MHz clock frequency for SPI with 3 wires, based on characterization results, not tested in production.

Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

2.4.2 I²C - inter-IC control interface

Subject to general operating conditions for Vdd and Top.

Table 7. I²C slave timing values (standard and fast mode)

Symbol	Parameter	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	Low period of the SCL clock	4.7		1.3		µs
$t_{w(SCLH)}$	High period of the SCL clock	4.0		0.6		
$t_{su(SDA)}$	Data setup time	250		100		ns
$t_{h(SDA)}$	Data hold time	0	3.45	0	0.9	µs
$t_{h(ST)}$	START condition hold time	4		0.6		
$t_{su(SR)}$	Setup time for a repeated START condition	4.7		0.6		
$t_{su(SP)}$	Setup time for STOP condition	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

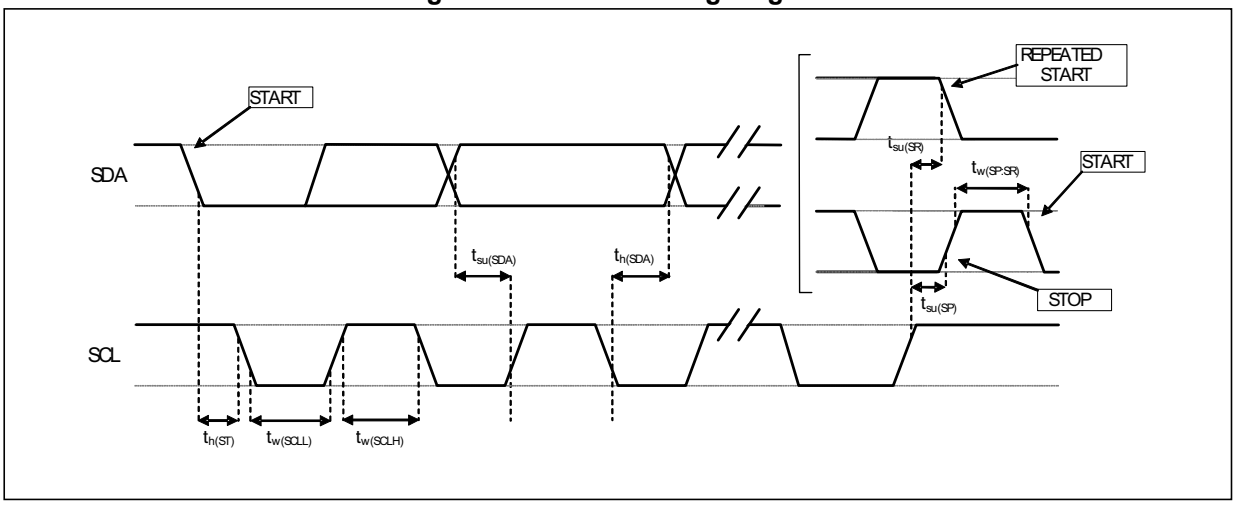
1. Data based on standard I²C protocol requirement, not tested in production.

Table 8. I²C slave timing values (fast mode plus and high speed)

Symbol	Parameter	I²C fast mode plus(1)		I²C high speed(1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	1	0	3.4	MHz
$t_{w(SCLL)}$	Low period of the SCL clock	0.5		0.16		µs
$t_{w(SCLH)}$	High period of the SCL clock	0.26		0.06		
$t_{su(SDA)}$	Data setup time	50		10		ns
$t_{h(SDA)}$	Data hold time	0		0	0.07	µs
$t_{h(ST)}$	START condition hold time	0.26		0.16		
$t_{su(SR)}$	Setup time for a repeated START condition	0.26		0.16		
$t_{su(SP)}$	Setup time for STOP condition	0.26		0.16		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	0.5				

1. Data based on standard I²C protocol requirement, not tested in production.

Figure 4. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 9. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin (CS_XL, CS_MAG, SCL/SPC, SDA/SDI/SDO)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 2.5 V)	3000 for 0.5 ms	*g*
		10000 for 0.1 ms	*g*
A_{UNP}	Acceleration (any axis, unpowered)	3000 for 0.5 ms	*g*
		10000 for 0.1 ms	*g*
M_{EF}	Maximum exposed field	10000	gauss
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection (HBM)	2	kV

Note: Supply voltage on any pin should never exceed 4.8 V

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

3 Terminology

3.1 Sensitivity

3.1.1 Linear acceleration sensor sensitivity

Sensitivity describes the gain of the sensor and can be determined by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

3.1.2 Magnetic sensor sensitivity

Sensitivity describes the ratio of the output digital data expressed in LSB units and the applied magnetic field expressed in mG (milligauss). It can be measured, for example, by applying a known magnetic field along one axis and measuring the digital output of the device.

3.2 Zero-*g* level

The zero-*g* level offset (LA_TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* on the X-axis and 0 *g* on the Y-axis whereas the Z-axis will measure 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from the ideal value in this case is called zero-*g* offset. Offset is to some extent a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little with temperature, see *Table 3* "Zero-*g* level change vs. temperature" (LA_TCOff). The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a population of sensors.

3.3 Zero-*gauss* level

Zero-*g*auss level offset (M_TyOff) describes the deviation of an actual output signal from the ideal output if no magnetic field is present.

3.4 Magnetic dynamic range

The magnetic dynamic range is defined as the magnetic field driven along one sensitive axis, giving the maximum digital output value.

4 Functionality

4.1 Magnetometer

4.1.1 Magnetometer power modes

The LSM303AGR magnetometer provides two different power modes: high-resolution and low-power modes.

The tables below summarize the selection of the low-pass filter and current consumption of the operating modes.

When the low-pass filter is enabled, the bandwidth is reduced while noise performance is improved without any increase in power consumption.

Table 10. Digital low-pass filter

CFG_REG_B_M [LPF]	(CFG_REG_A_M [LP = 0]) high-resolution mode		(CFG_REG_A_M [LP = 1]) low-power mode	
	BW [Hz]	Noise RMS [mg]	BW [Hz]	Noise RMS [mg]
0 (disable)	ODR/2	4	ODR/2	8.5
1 (enable)	ODR/4	3	ODR/4	6

Table 11. Current consumption of operating modes

ODR (Hz)	Current consumption (µA) (CFG_REG_A_M [LP] = 0) - high-resolution	Current consumption (µA) (CFG_REG_A_M [LP] = 1) - low-power
10	100	25
20	200	50
50	500	125
100	1000	250

The following table summarizes the turn-on time of the magnetometer in the two different power modes with the offset cancellation function enabled or disabled (see *Section 4.1.2: Magnetometer offset cancellation*).

Table 12. Operating mode and turn-on time

Operating mode	Turn-on time	
CFG_REG_A_M[LP]	CFG_REG_A_M[OFF_CANC = 0]	CFG_REG_A_M[OFF_CANC = 1]
0 (high-resolution)	9.4 ms	9.4 ms + 1/ODR
1 (low-power)	6.4 ms	6.4 ms + 1/ODR

4.1.2 Magnetometer offset cancellation

The offset cancellation is the result of performing a set and reset in the magnetic sensor.

The offset cancellation technique is defined as follows:

$$H_{out} = \frac{H_n - H_{n-1}}{2}$$

where H_n and H_{n-1} are two consecutive magnetic field measurements, one after a set pulse, the other after a reset pulse.

Considering a magnetic offset (H_{off}), the two magnetic field measurements are:

- Set: $H_n = H + H_{off}$
- Reset: $H_{n-1} = -H + H_{off}$

The offset is cancelled according the offset cancellation technique:

$$H_{out} = \frac{H_n - H_{n-1}}{2} = \frac{2H + H_{off} + -H_{off}}{2} = H$$

In the LSM303AGR the offset cancellation is enabled by setting the bit OFF_CANC = 1 in *CFG_REG_B_M (61h)*.

If the offset cancellation is disabled, a set of the magnetic sensor is performed anyway.

The set pulse frequency can be configured by setting the Set_FREQ bit in *CFG_REG_B_M (61h)*.

4.1.3 Magnetometer interrupt

In the LSM303AGR the magnetometer interrupt signal generation is based on the comparison between data and a programmable threshold.

To enable the interrupt function, in INT_CTRL_REG_M register (63h) the "IEN" bit must be set to '1'.

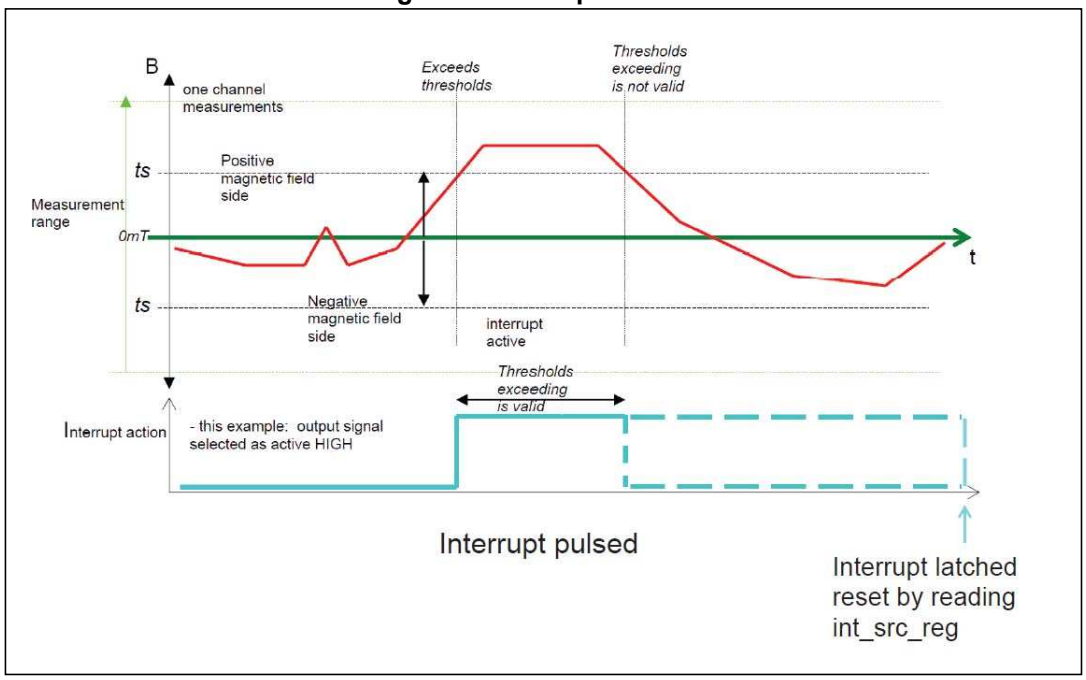
In the LSM303AGR the user can select the axis/axes in which the interrupt function can be enabled. In order to do this, the XIEN, YIEN, and ZIEN bits in *INT_CTRL_REG_M (63h)* need be set properly.

The threshold value can be programmed by setting the *INT_THS_L_REG_M (65h)* and *INT_THS_H_REG_M (66h)* registers.

The threshold is expressed in absolute value as a 15-bit unsigned number. The threshold has the same sensitivity as the magnetic data.

When magnetic data exceeds the positive or the negative threshold, the interrupt signal is generated and the information about the type of interrupt is stored in the *INT_SOURCE_REG_M (64h)* register. In particular, when magnetic data exceeds the positive threshold the P_TH_S_axis bit is set to '1', while if data exceeds the negative threshold the N_TH_S_axis bit is set to '1'. If magnetic data lay between the positive and the negative thresholds, no interrupt signal is released.

Figure 5. Interrupt function



Two different approaches for the interrupt function are available:

- Typical: comparison is between magnetic data read by the sensor and the programmable threshold;
- Advanced: comparison is made between magnetic data after hard-iron correction and the programmable threshold.

These approaches are configurable by setting the INT_on_DataOFF bit in *CFG_REG_B_M (61h)*.

If INT_on_DataOFF is set to '0' the typical approach is selected, otherwise if it is set to '1' the advanced approach is selected.

Two different interrupts are available:

- Pulsed interrupt signal: it goes high when the magnetic data exceed one of the two thresholds and goes low when the magnetic data are between the two thresholds. This kind of interrupt is selected by setting the IEL bit in *INT_CTRL_REG_M (63h)* to '0'.
- Latched interrupt signal: it goes high when the data exceed one of the two thresholds but is reset only once the source register is read and not when the magnetic data returns between the two thresholds. This kind of interrupt is selected by setting the IEL bit in *INT_CTRL_REG_M (63h)* to '1'.

The interrupt signal polarity can be set using the IEA bit in *INT_CTRL_REG_M (63h)*.

If IEA is set to '1' then the interrupt signal is active high, while if it is set to '0' the interrupt signal is active low.

In order to drive the interrupt signal from the DRDY pad, the INT_MAG_PIN bit in *CFG_REG_C_M (62h)* must be set to '1'.

4.1.4 Magnetometer hard-iron compensation

Hard-iron distortion occurs when a magnetic object is placed near the magnetometer and appears as a permanent bias in the sensor's outputs.

The hard-iron correction consists of compensating magnetic data from hard-iron distortion.

The operation is defined as follows:

$H_{out} = H_{read} – H_{HI}$

where:

- H_{read} is the generic uncompensated magnetic field data, as read by the sensor;
- H_{HI} is the hard-iron distortion field;
- H_{out} is the compensated magnetic data.

The computation of the hard-iron distortion field should be performed by an external processor. After the computation of the hard iron-distortion field has been performed, the measured magnetic data can be compensated.

The LSM303AGR offers the possibility of storing hard-iron data inside six dedicated registers from 45h to 4Ah.

Each register contains eight bits so that the hard-iron data can be expressed as a 16-bit two's complement number. The OFFSET_axis_REG_H registers contain the MSBs of the hard-iron data, while the OFFSET_axis_REG_L registers contain the LSBs.

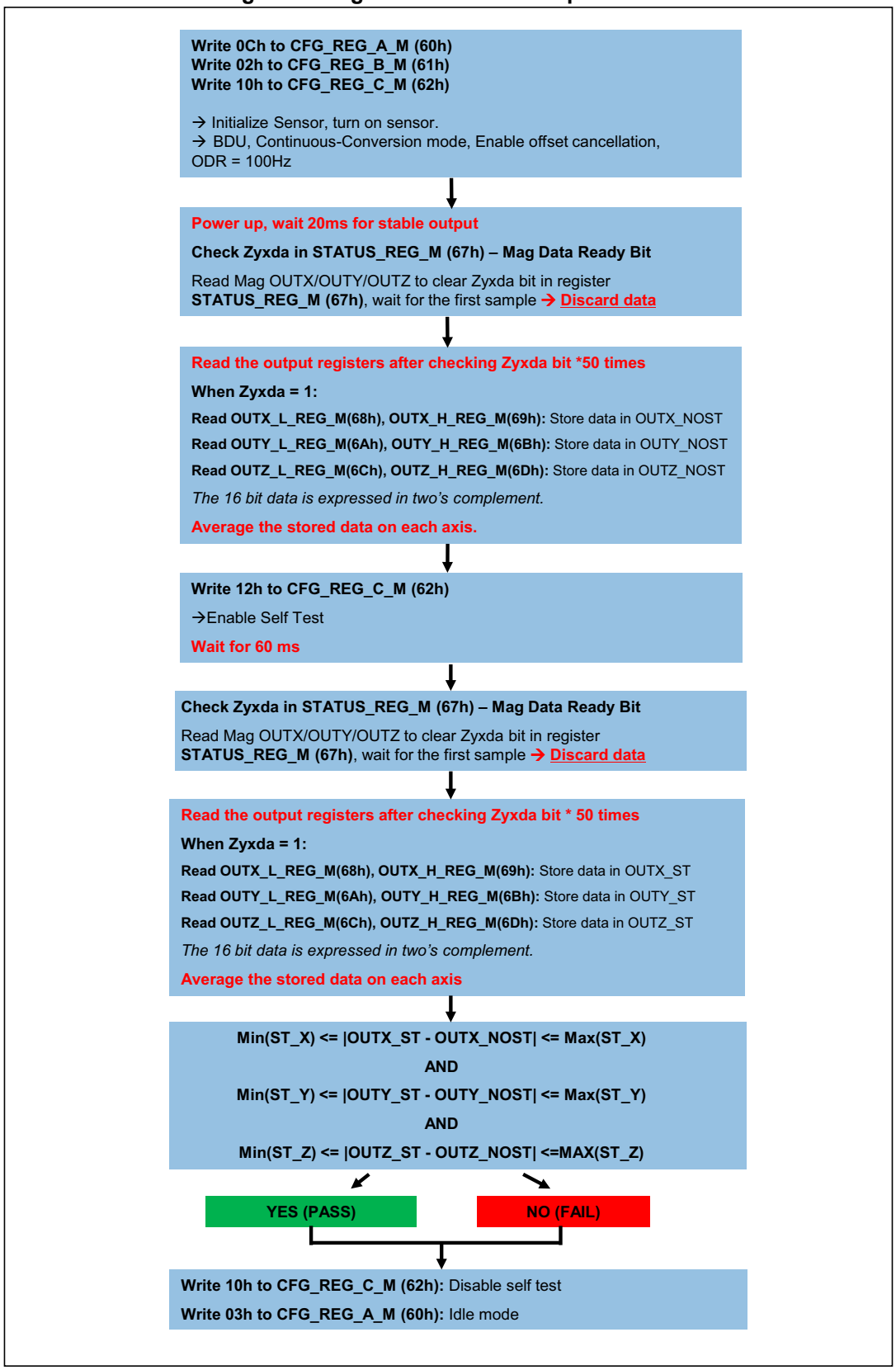
Hard-iron data have the same format and weight of the magnetic output data. The hard-iron values stored in dedicated registers are automatically subtracted from the output data.

4.1.5 Magnetometer self-test

The self-test function is available for the magnetic sensor. When the magnetic self-test is enabled, a current is forced into a coil inside the device. This current will generate a magnetic field that will produce a variation of the magnetometer output signals. If the output signals change within the amplitude limits specified in *Table 3*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

The self-test procedure is described in the following figure.

Figure 6. Magnetometer self-test procedure



4.2 Accelerometer

4.2.1 Accelerometer power modes

The LSM303AGR accelerometer provides three different linear acceleration operating modes: *high-resolution mode*, *normal mode* and *low-power mode*.

The table below summarizes how to select the different operating modes.

Table 13. Operating mode selection

Operating mode	CTRL_REG1_A[3] (LPen bit)	CTRL_REG4_A[3] (HR bit)	BW [Hz]	Turn-on time [ms]	So @ ±2 *g* [mg/digit]
Low-power mode (8-bit data output)	1	0	ODR/2	1	16
Normal mode (10-bit data output)	0	0	ODR/2	1.6	4
High-resolution mode (12-bit data output)	0	1	ODR/9	7/ODR	1
Not allowed	1	1	--	--	--

The turn-on time to transition to another operating mode is given in *Table 14*.

Table 14. Turn-on time for operating mode transition

Operating mode change	Turn-on time [ms]
12-bit mode to 8-bit mode	1/ODR
12-bit mode to 10-bit mode	1/ODR
10-bit mode to 8-bit mode	1/ODR
10-bit mode to 12-bit mode	7/ODR
8-bit mode to 10-bit mode	1/ODR
8-bit mode to 12-bit mode	7/ODR

Table 15. Current consumption of operating modes

Operating mode [Hz]	Low-power mode (8-bit data output) [µA]	Normal mode (10-bit data output) [µA]	High resolution (12-bit data output) [µA]
1	2	2	2
10	3	4	4
25	4	6	6
50	6	11	11
100	10	20	20
200	18	38	38
400	36	73	73

Table 15. Current consumption of operating modes (continued)

Operating mode [Hz]	Low-power mode (8-bit data output) [µA]	Normal mode (10-bit data output) [µA]	High resolution (12-bit data output) [µA]
1344	--	185	185
1620	100	--	--
5376	185	--	--

4.2.2 Accelerometer 6D / 4D orientation detection

The LSM303AGR includes 6D / 4D orientation detection which applies only to the accelerometer.

In this configuration the interrupt is generated when the device is stable in a known direction. In 4D configuration, detection of the position of the Z-axis is disabled.

4.2.3 Accelerometer activity/inactivity function

The Activity/Inactivity recognition function allows reducing the power consumption of the accelerometer block in order to supply other smart applications and is applicable only to the accelerometer block of the device.

When the Activity/Inactivity recognition function is activated, accelerometer is able to automatically go to 10 Hz sampling rate and to wake up as soon as the interrupt event has been detected, increasing the output data rate and bandwidth.

With this feature the system may be efficiently switched from/to low-power mode to full performance depending on user-selectable positioning and acceleration events, thus ensuring power saving and flexibility.

The Activity/Inactivity recognition function is activated by writing the desired threshold in the *Act_THS_A (3Eh)* register. The high-pass filter is automatically enabled.

Table 16. Activity/Inactivity function control registers

Register	LSB value
ACT_THS_A	Full scale / 128 [mg]
ACT_DUR_A	8/ODR [s]

When the acceleration becomes smaller than the threshold for at least the duration (8*ACT_DUR+1)/ODR, the ODR [3:0] bits of *CTRL_REG1_A (20h)* are bypassed (Inactivity) and internally set to 10 Hz (ODR [3:0] = 0010), but the content of the *CTRL_REG1_A (20h)*(ODR [3:0]) bits are left untouched.

When the acceleration becomes greater than the threshold (*Act_THS_A (3Eh)*), *CTRL_REG1_A (20h)* is restored immediately (Activity).

Once the Activity/Inactivity detection function is enabled, it will be applied to the INT_2 pin by setting the *CTRL_REG6_A (25h)* (P2_ACT) bit to ‘1’.

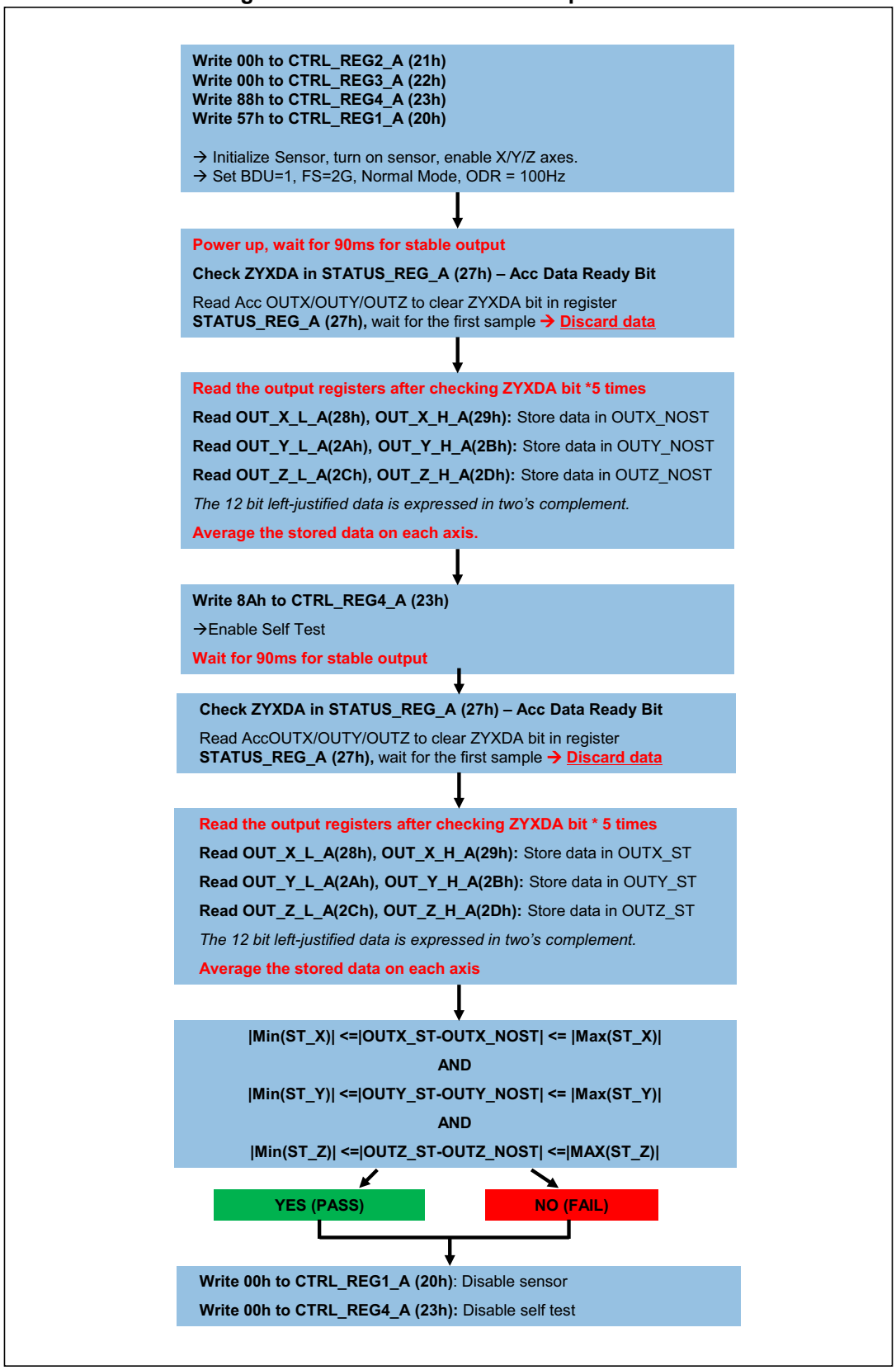
To disable the Activity/Inactivity detection function, set the content of the *Act_THS_A (3Eh)* register to 00h.

4.2.4 Accelerometer self-test

The self-test allows the user to check the sensor functionality without moving it. When the self-test is enabled, an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs will exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When the self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified inside *Table 3*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

The self-test procedure is described in the following figure.

Figure 7. Accelerometer self-test procedure



4.3 IC interface

The complete measurement chain is composed of a low-noise capacitive amplifier which converts the capacitive unbalancing of the MEMS sensor into an analog voltage using an analog-to-digital converter.

The acceleration and magnetic data may be accessed through an I^2C/SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller.

The LSM303AGR features a data-ready signal which indicates when new sets of measured acceleration and magnetic data are available, thus simplifying data synchronization in the digital system that uses the device.

4.4 FIFO

The FIFO buffer applies only to the accelerometer. The LSM303AGR embeds a 32-level FIFO for each of the three output channels, X, Y and Z. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO.

In order to enable the FIFO buffer, the FIFO_EN bit in *CTRL_REG5_A (24h)* must be set to '1'.

This buffer can work according to the following different modes: Bypass mode, FIFO mode, Stream mode and Stream-to-FIFO mode. Each mode is selected by the FM [1:0] bits in *FIFO_CTRL_REG_A (2Eh)*. Programmable FIFO watermark level, FIFO empty or FIFO overrun events can be enabled to generate dedicated interrupts on the INT_1_XL pin (configuration through *CTRL_REG3_A (22h)*).

In the *FIFO_SRC_REG_A (2Fh)* register the EMPTY bit is equal to '1' when all FIFO samples are ready and FIFO is empty.

In the *FIFO_SRC_REG_A (2Fh)* register the WTM bit goes to '1' if new data is written in the buffer and *FIFO_SRC_REG_A (2Fh)* (FSS [4:0]) is greater than or equal to *FIFO_CTRL_REG_A (2Eh)* (FTH [4:0]). *FIFO_SRC_REG_A (2Fh)* (WTM) goes to '0' if reading an X, Y, Z data slot from FIFO and *FIFO_SRC_REG_A (2Fh)* (FSS [4:0]) is less than or equal to *FIFO_CTRL_REG_A (2Eh)* (FTH [4:0]).

In the *FIFO_SRC_REG_A (2Fh)* register the OVRN_FIFO bit is equal to '1' if the FIFO slot is overwritten.

4.4.1 Bypass mode

In Bypass mode the FIFO is not operational and for this reason it remains empty. For each channel only the first address is used. The remaining FIFO levels are empty.

Bypass mode must be used in order to reset the FIFO buffer when a different mode is operating (i.e. FIFO mode).

4.4.2 FIFO mode

In FIFO mode, the buffer continues filling data from the X, Y and Z accelerometer channels until it is full (a set of 32 samples stored). When the FIFO is full, it stops collecting data from the input channels and the FIFO content remains unchanged.

An overrun interrupt can be enabled, I1_OVERRUN = '1' in the *CTRL_REG3_A (22h)* register, in order to be raised when the FIFO stops collecting data. When the overrun interrupt occurs, the first data has been overwritten and the FIFO stops collecting data from the input channels.

After the last read it is necessary to exit Bypass mode in order to reset the FIFO content. After this reset command, it is possible to restart FIFO mode just by selecting the FIFO mode configuration (FM[1:0] bits) in register *FIFO_CTRL_REG_A (2Eh)*.

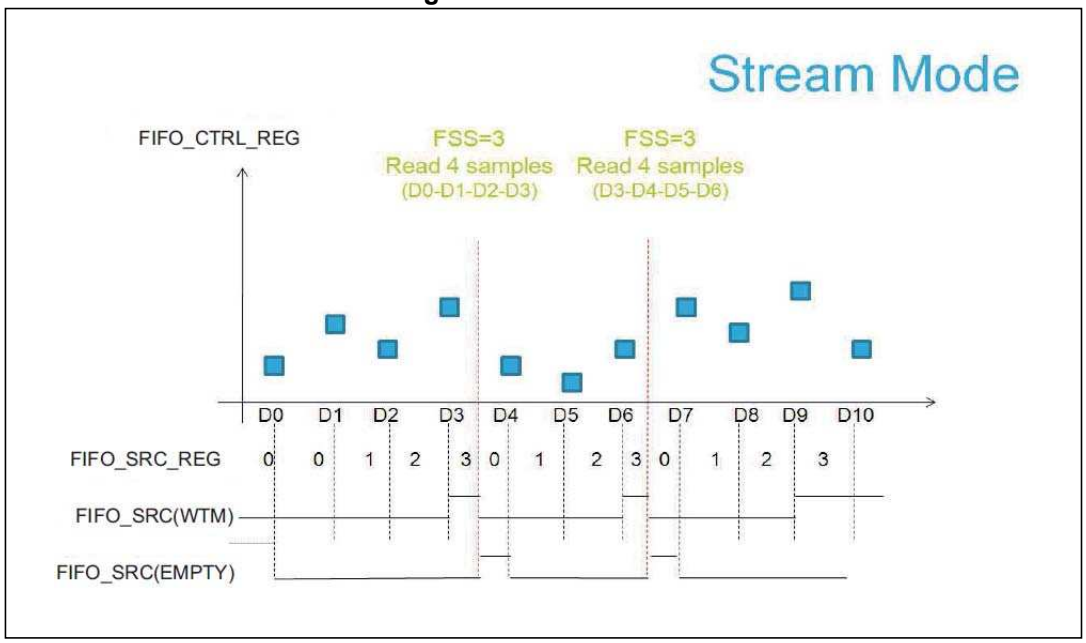
4.4.3 Stream mode

In Stream mode the FIFO continues filling data from the X, Y, and Z accelerometer channels until the buffer is full (a set of 32 samples stored) at which point the FIFO buffer index restarts from the beginning and older data is replaced by the current data. The oldest values continue to be overwritten until a read operation frees the FIFO slots.

An overrun interrupt can be enabled, I_XL_OVERRUN = '1' in the *CTRL_REG3_A (22h)* register, in order to read the entire contents of the FIFO at once. If, in the application, it is mandatory not to lose data and it is not possible to read at least one sample for each axis within one ODR period, a watermark interrupt can be enabled in order to read partially the FIFO and leave memory slots free for incoming data.

Setting the FTH [4:0] bit in the *FIFO_CTRL_REG_A (2Eh)* register to an N value, the number of X, Y and Z data samples that should be read at the rise of the watermark interrupt is up to (N+1).

Figure 8. Stream mode



4.4.4 Stream-to-FIFO mode

In Stream-to-FIFO mode, data from the X, Y and Z accelerometer channels are collected in a combination of Stream mode and FIFO mode. The FIFO buffer starts operating in Stream mode and switches to FIFO mode when the selected interrupt occurs.

When an interrupt event is configured on the INT_1_XL pin, the FIFO operates in Stream mode if the INT_1_XL pin value is equal to ‘0’ and it operates in FIFO mode if the INT_1_XL pin value is equal to ‘1’. Switching modes is dynamically performed according to the INT_1_XL pin value.

Stream-to-FIFO can be used in order to analyze the sampling history that generates an interrupt. The standard operation is to read the contents of FIFO when the FIFO mode is triggered and the FIFO buffer is full and stopped.

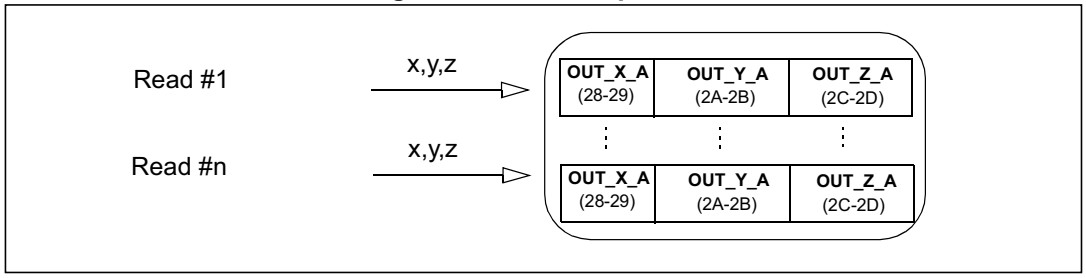
4.4.5 Retrieving data from FIFO

FIFO data is read from the *OUT_X_L_A (28h), OUT_X_H_A (29h)*, *OUT_Y_L_A (2Ah), OUT_Y_H_A (2Bh)*, and *OUT_Z_L_A (2Ch), OUT_Z_H_A (2Dh)* registers. A read operation using a serial interface of the *OUT_X_L_A (28h), OUT_X_H_A (29h)*, *OUT_Y_L_A (2Ah), OUT_Y_H_A (2Bh)* or *OUT_Z_L_A (2Ch), OUT_Z_H_A (2Dh)* output registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest X, Y and Z data are placed in the *OUT_X_L_A (28h), OUT_X_H_A (29h)*, *OUT_Y_L_A (2Ah), OUT_Y_H_A (2Bh)* and *OUT_Z_L_A (2Ch), OUT_Z_H_A (2Dh)* registers and both single read and read_burst operations can be used.

4.4.6 FIFO multiple read (burst)

Starting from Addr 28h multiple reads can be performed. Once the read reaches Addr 2Dh, the system automatically restarts from Addr 28h.

Figure 9. FIFO multiple read



4.5 Temperature sensor

The LSM303AGR is supplied with an internal temperature sensor. Temperature data can be enabled by setting the TEMP_EN[1:0] bits to '1' in the *TEMP_CFG_REG_A (1Fh)* register.

To retrieve the temperature sensor data the BDU bit in *CTRL_REG4_A (23h)* must be set to '1'.

Both the *OUT_TEMP_L_A (0Ch), OUT_TEMP_H_A (0Dh)* registers must be read.

Temperature data is stored inside OUT_TEMP_H as two's complement data in 8-bit format left-justified.

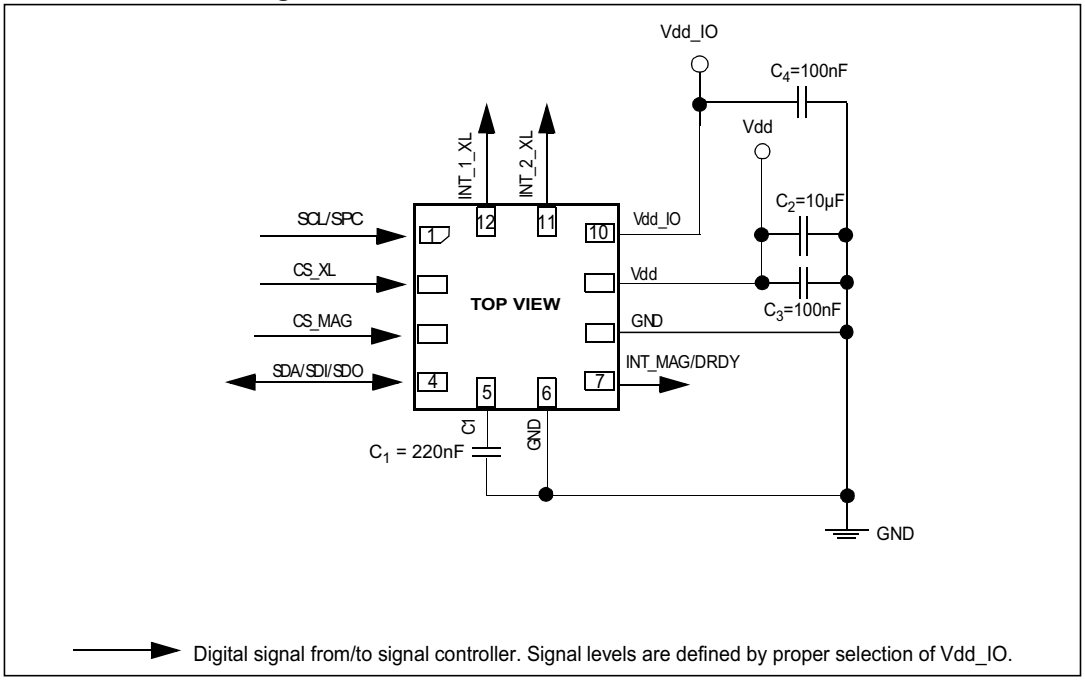
4.6 Factory calibration

The IC interface is factory calibrated for sensitivity (LA_So, M_GN), Zero-*g* level (LA_TyOff) and Zero-*gauss* level (M_TyOff).

The trim values are stored inside the device in nonvolatile memory. Anytime the device is turned on, the trim parameters are downloaded into the registers to be used during active operation. This allows using the device without further calibration.

5 Application hints

Figure 10. LSM303AGR electrical connections



The device core is supplied through the Vdd line while the I/O pads are supplied through the Vdd_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF aluminum) should be placed as near as possible to pin 9 of the device (common design practice).

It is possible to remove Vdd, maintaining Vdd_IO, without blocking the communication bus, in this condition the measurement chain is powered off.

The following recommendations apply to capacitor C1:

- It must be connected as close as possible to pins 5 and 6 since very high current pulses flow from C1 to pin 5 and 6. This avoid problems caused by inductive effects due to the length of the copper strips.
- It is highly recommended to use low ESR (max 200 mOhm)

The functionality of the device and the measured acceleration data are selectable and accessible through the I^2C or SPI interfaces. When using the I^2C, CS must be tied high (i.e. connected to Vdd_IO).

The functions, the threshold and the timing of the three interrupt pins (INT_1_XL, INT_2_XL, and INT_MAG) can be completely programmed by the user through the I^2C/SPI interface.

5.1 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standards.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com.

5.2 High-current wiring effects

High current in wiring and printed circuit traces can be culprits in causing errors in magnetic field measurements for compassing.

Conductor-generated magnetic fields will add to the Earth's magnetic field, leading to errors in compass heading computation.

Keep currents higher than 10 mA a few millimeters away from the sensor IC.

6 Digital interfaces

The registers embedded inside the LSM303AGR may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW-configured to operate in 3-wire interface mode.

The serial interfaces are mapped onto the same pads. To select/exploit the I^2C interface, the CS line must be tied high (i.e. connected to Vdd_IO).

Table 17. Serial interface pin description

Pin name	Pin description
CS_XL, CS_MAG	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)

6.1 I^2C serial interface

The LSM303AGR I^2C is a bus slave. The I^2C is employed to write data into registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 18. I^2C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd_IO through an external pull-up resistor. When the bus is free, both the lines are high.

The I^2C interface is compliant with fast mode (400 kHz) I^2C standards as well as with the normal mode.

6.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a high-to-low transition on the data line while the SCL line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the high period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LSM303AGR behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted: the 7 LSb represent the actual register address while the MSB enables address auto increment. If the MSb of the SUB field is ‘1’, the SUB (register address) is automatically increased to allow multiple data read/writes.

The slave address is completed with a Read/Write bit. If the bit was ‘1’ (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is ‘0’ (Write) the master will transmit to the slave with direction unchanged. *Table 23* explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

Table 19. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 20. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 21. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 22. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit

(MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left high by the slave. The master can then abort the transfer. A low-to-high transition on the SDA line while the SCL line is high is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In the presented communication format MAK is Master acknowledge and NMAK is No Master Acknowledge.

Default address:

The accelerometer sensor slave address is 0011001b while magnetic sensor slave address is 0011110b.

The slave addresses are completed with a Read/Write bit. If the bit was '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes. If the bit is '0' (Write) the master will transmit to the slave with direction unchanged. *Table 23* and *Table 24* explain how the SAD+Read/Write bit patterns are composed, listing all the possible configurations.

Linear acceleration sensor: the default (factory setting) 7-bit slave address is 0011001b.

Table 23. SAD + Read/Write patterns

Command	SAD[6:0]	R/W	SAD + R/W
Read	0011001	1	00110011 (33h)
Write	0011001	0	00110010 (32h)

Magnetic field sensor: the default (factory setting) 7-bit slave address is 0011110b.

Table 24. SAD + Read/Write patterns

Command	SAD[6:0]	R/W	SAD + R/W
Read	0011110	1	00111101 (3Dh)
Write	0011110	0	00111100 (3Ch)

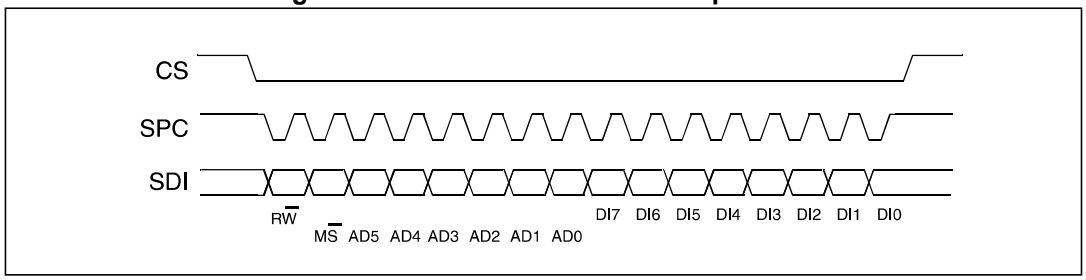
6.2 SPI bus interface

The LSM303AGR SPI is a bus slave. The SPI allows writing and reading the registers of the device.

The serial interface interacts with the application using 3 wires: **CS_XL** or **CS_MAG, SPC**, **SDI/O**.

6.2.1 Accelerometer SPI write

Figure 11. Accelerometer SPI write protocol



The SPI Write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: WRITE bit. The value is 0.

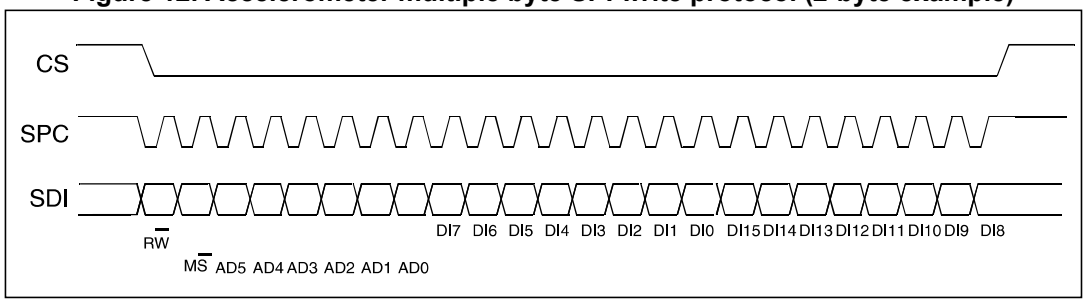
bit 1: MS bit. When O do not increment address, when 1 increment address in multiple writing.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15. data 01(7:0) {write mode). This is the data that is written inside the device (MSb first).

bit 16-...: data DI(...-8). Further data in multiple byte writes.

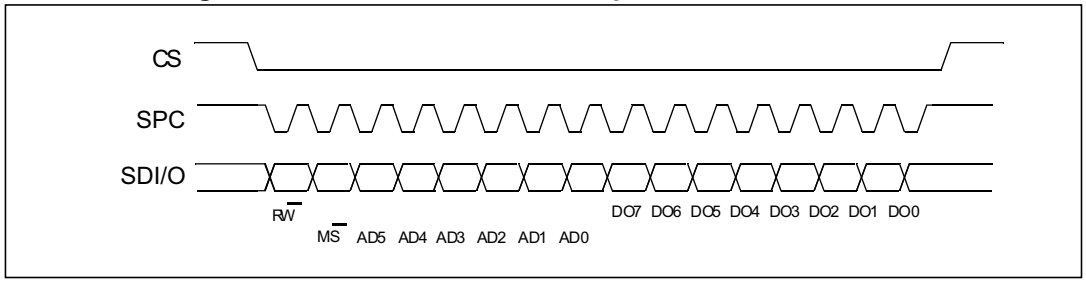
Figure 12. Accelerometer multiple byte SPI write protocol (2-byte example)



6.2.2 Accelerometer SPI read in 3-wire mode

3-wire mode is entered by setting the *CTRL_REG4_A (23h)* (SPI_ENABLE) bit equal '1' (SPI serial interface read enable).

Figure 13. Accelerometer SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: MS bit. When 0, does not increment the address; when 1, increments the address in multiple reads.

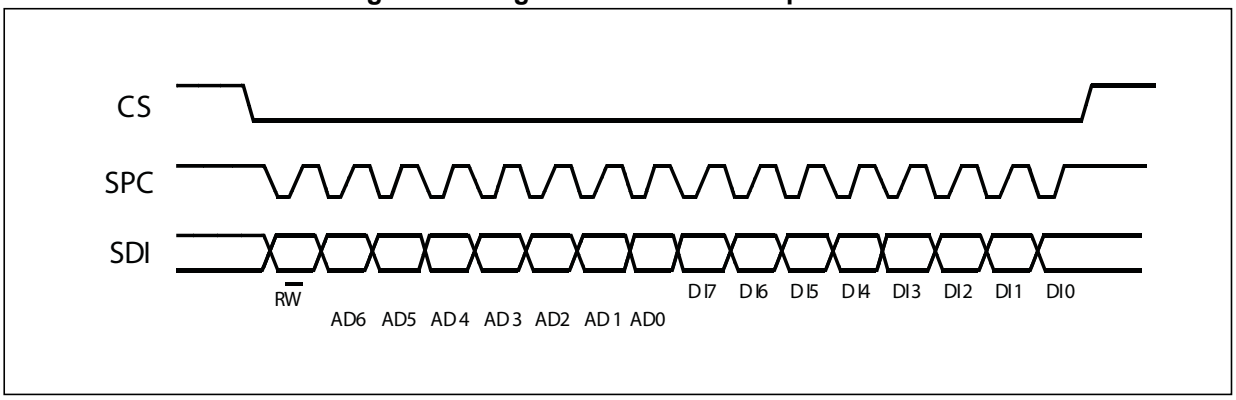
bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

6.2.3 Magnetometer SPI write

Figure 14. Magnetometer SPI write protocol



The SPI write command is performed with 16 clock pulses. The multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

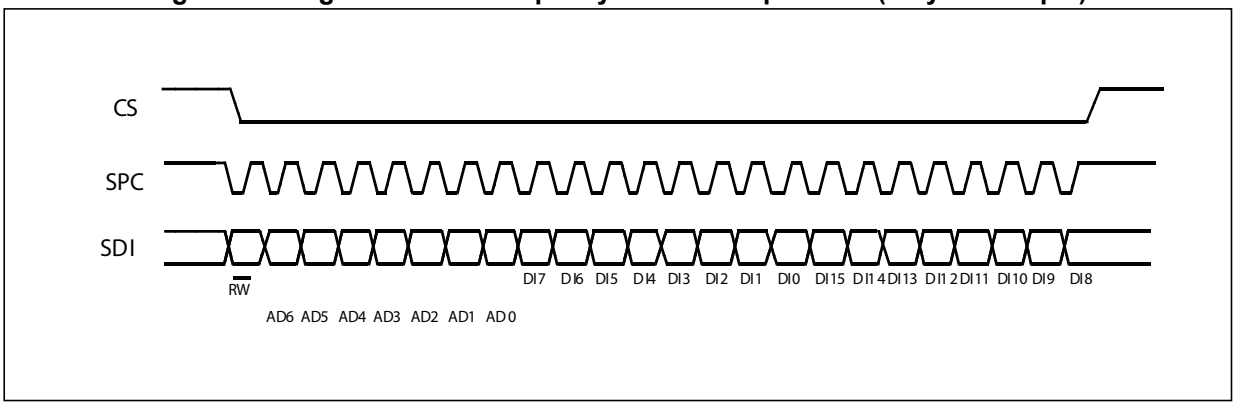
bit 0: WRITE bit. The value is 0.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

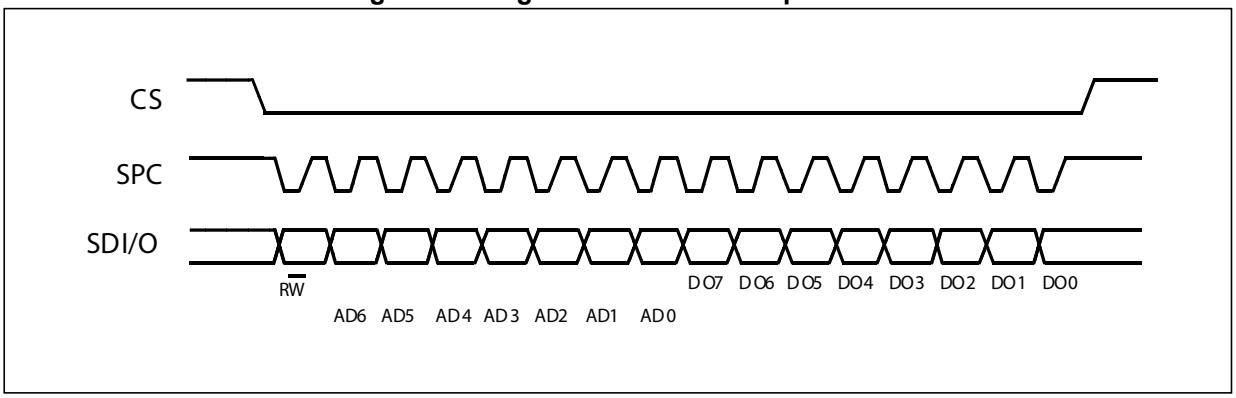
bit 16-... : data DI(...-8). Further data in multiple byte writes.

Figure 15. Magnetometer multiple byte SPI write protocol (2-byte example)



6.2.4 Magnetometer SPI read

Figure 16. Magnetometer SPI read protocol



The SPI read command is performed with 16 clock pulses:

bit 0: WRITE bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is available in 3-wire mode.

7 Register mapping

The table given below provides a list of the 8-bit registers embedded in the device and the corresponding addresses. Registers 00h through 3Fh are dedicated to the accelerometer while registers 40h through 6Fh are dedicated to the magnetometer.

Table 25. Register address map

Name	Type(1)	Register address		Default	Comment
		Hex	Binary		
Reserved		00 - 06			Reserved
STATUS_REG_AUX_A	R	07	000 0111		
Reserved	R	08-0B			Reserved
OUT_TEMP_L_A	R	0C	000 1100	Output	Output registers
OUT_TEMP_H_A	R	0D	000 1101	Output	
INT_COUNTER_REG_A	R	0E	000 1110		
WHO_AM_I_A	R	0F	000 1111	00110011	Dummy register
Reserved		10 - 1E			Reserved
TEMP_CFG_REG_A	R/W	1F	001 1111	00000000	
CTRL_REG1_A	R/W	20	010 0000	00000111	Accelerometer control registers
CTRL_REG2_A	R/W	21	010 0001	00000000	
CTRL_REG3_A	R/W	22	010 0010	00000000	
CTRL_REG4_A	R/W	23	010 0011	00000000	
CTRL_REG5_A	R/W	24	010 0100	00000000	
CTRL_REG6_A	R/W	25	010 0101	00000000	
REFERENCE/DATACAPTURE_A	R/W	26	010 0110	00000000	
STATUS_REG_A	R	27	010 0111	00000000	Accelerometer status register
OUT_X_L_A	R	28	010 1000	Output	Accelerometer output registers
OUT_X_H_A	R	29	010 1001	Output	
OUT_Y_L_A	R	2A	010 1010	Output	
OUT_Y_H_A	R	2B	010 1011	Output	
OUT_Z_L_A	R	2C	010 1100	Output	
OUT_Z_H_A	R	2D	010 1101	Output	
FIFO_CTRL_REG_A	R/W	2E	010 1110	00000000	FIFO registers
FIFO_SRC_REG_A	R	2F	010 1111	0010000	

Table 25. Register address map (continued)

Name	Type(1)	Register address		Default	Comment
		Hex	Binary		
INT1_CFG_A	R/W	30	011 0000	00000000	Interrupt 1 registers
INT1_SRC_A	R	31	011 0001	00000000	
INT1_THS_A	R/W	32	011 0010	00000000	
INT1_DURATION_A	R/W	33	011 0011	00000000	
INT2_CFG_A	R/W	34	011 0100	00000000	Interrupt 2 registers
INT2_SRC_A	R	35	011 0101	00000000	
INT2_THS_A	R/W	36	011 0110	00000000	
INT2_DURATION_A	R/W	37	011 0111	00000000	
CLICK_CFG_A	R/W	38	011 1000	00000000	
CLICK_SRC_A	R	39	011 1001	00000000	
CLICK_THS_A	R/W	3A	011 1010	00000000	
TIME_LIMIT_A	R/W	3B	011 1011	00000000	
TIME_LATENCY_A	R/W	3C	011 1100	00000000	
TIME_WINDOW_A	R/W	3D	011 1101	00000000	
Act_THS_A	R/W	3E	011 1110	00000000	
Act_DUR_A	R/W	3F	011 1111	00000000	
RESERVED		40-44			
OFFSET_X_REG_L_M	R/W	45	01000101	00000000	Magnetometer hard-iron registers
OFFSET_X_REG_H_M	R/W	46	01000110	00000000	
OFFSET_Y_REG_L_M	R/W	47	01000111	00000000	
OFFSET_Y_REG_H_M	R/W	48	01001000	00000000	
OFFSET_Z_REG_L_M	R/W	49	01001001	00000000	
OFFSET_Z_REG_H_M	R/W	4A	01001010	00000000	
RESERVED		4B-4C			
WHO_AM_I_M	R	4F	01001111	01000000	
RESERVED		50-5F			
CFG_REG_A_M	R/W	60	01100000	00000011	Magnetometer configuration registers
CFG_REG_B_M	R/W	61	01100001	00000000	
CFG_REG_C_M	R/W	62	01100010	00000000	
INT_CRTL_REG_M	R/W	63	01100011	11100000	Magnetometer interrupt configuration registers
INT_SOURCE_REG_M	R	64	01100100		
INT_THS_L_REG_M	R/W	65	01100101	00000000	
INT_THS_H_REG_M	R/W	66	01100110	00000000	

Table 25. Register address map (continued)

Name	Type(1)	Register address		Default	Comment
		Hex	Binary		
STATUS_REG_M	R	67	01100111		
OUTX_L_REG_M	R	68	01101000	output	Magnetometer output registers
OUTX_H_REG_M	R	69	01101001	output	
OUTY_L_REG_M	R	6A	01101010	output	
OUTY_H_REG_M	R	6B	01101010	output	
OUTZ_L_REG_M	R	6C	01101100	output	
OUTZ_H_REG_M	R	6D	01101101	output	
RESERVED		6E-6F			

1. R = read-only register, R/W = readable/writable register

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

8 Register description

8.1 STATUS_REG_AUX_A (07h)

Table 26. STATUS_REG_AUX register

--	TOR	--	--	--	TDA	--	--

Table 27. STATUS_REG_AUX description

TOR	Temperature data overrun. Default value: 0 (0: no overrun has occurred; 1: new temperature data has overwritten the previous data)
TDA	Temperature new data available. Default value: 0 (0: new temperature data is not yet available; 1: new temperature data is available)

8.2 OUT_TEMP_L_A (0Ch), OUT_TEMP_H_A (0Dh)

Temperature sensor data. Refer to *Section 4.5: Temperature sensor* for details on how to enable and read the temperature sensor output data.

8.3 INT_COUNTER_REG_A (0Eh)

Table 28. INT_COUNTER_REG register

IC7	IC6	IC5	IC4	IC3	IC2	IC1	IC0

8.4 WHO_AM_I_A (0Fh)

Table 29. WHO_AM_I register

0	0	1	1	0	0	1	1

Device identification register.

8.5 TEMP_CFG_REG_A (1Fh)

Table 30. TEMP_CFG_REG register

TEMP_EN1	TEMP_EN0	0	0	0	0	0	0

Table 31. TEMP_CFG_REG description

TEMP_EN[1:0]	Temperature sensor (T) enable. Default value: 00 (00: T disabled; 11: T enabled)

8.6 CTRL_REG1_A (20h)

Table 32. CTRL_REG1 register

ODR3	ODR2	ODR1	ODR0	LPen	Zen	Yen	Xen

Table 33. CTRL_REG1 description

ODR[3:0]	Data rate selection. Default value: 0000 (0000: power-down mode; others: refer to *Table 34*)
LPen	Low-power mode enable. Default value: 0 (0: normal mode, 1: low-power mode) (Refer to *Section 4.2.1: Accelerometer power modes*)
Zen	Z-axis enable. Default value: 1 (0: Z-axis disabled; 1: Z-axis enabled)
Yen	Y-axis enable. Default value: 1 (0: Y-axis disabled; 1: Y-axis enabled)
Xen	X-axis enable. Default value: 1 (0: X-axis disabled; 1: X-axis enabled)

ODR[3:0] is used to set the power mode and ODR selection. The following table indicates the frequency of each combination of ODR[3:0].

Table 34. Data rate configuration

ODR3	ODR2	ODR1	ODR0	Power mode selection
0	0	0	0	Power-down mode
0	0	0	1	HR / Normal / Low-power mode (1 Hz)
0	0	1	0	HR / Normal / Low-power mode (10 Hz)
0	0	1	1	HR / Normal / Low-power mode (25 Hz)
0	1	0	0	HR / Normal / Low-power mode (50 Hz)
0	1	0	1	HR / Normal / Low-power mode (100 Hz)
0	1	1	0	HR / Normal / Low-power mode (200 Hz)
0	1	1	1	HR/ Normal / Low-power mode (400 Hz)
1	0	0	0	Low-power mode (1.620 kHz)
1	0	0	1	HR/ Normal (1.344 kHz); Low-power mode (5.376 kHz)

8.7 CTRL_REG2_A (21h)

Table 35. CTRL_REG2 register

HPM1	HPM0	HPCF2	HPCF1	FDS	HPCLICK	HPIS2	HPIS1

Table 36. CTRL_REG2 description

HPM[1:0]	High-pass filter mode selection. Default value: 00 Refer to *Table 37* for filter mode configuration
HPCF[2:1]	High-pass filter cutoff frequency selection
FDS	Filtered data selection. Default value: 0 (0: internal filter bypassed; 1: data from internal filter sent to output register and FIFO)
HPCLICK	High-pass filter enable for CLICK function. (0: filter bypassed; 1: filter enabled)
HPIS2	High-pass filter enable for AOI function on Interrupt 2. (0: filter bypassed; 1: filter enabled)
HPIS1	High-pass filter enable for AOI function on Interrupt 1. (0: filter bypassed; 1: filter enabled)

Table 37. High-pass filter mode configuration

HPM1	HPM0	High-pass filter mode
0	0	Normal mode (reset by reading the *REFERENCE/DATACAPTURE_A (26h)* register)
0	1	Reference signal for filtering
1	0	Normal mode
1	1	Autoreset on interrupt event

8.8 CTRL_REG3_A (22h)

Table 38. CTRL_REG3 register

I1_CLICK	I1_AOI1	I1_AOI2	I1_DRDY1	I1_DRDY2	I1_WTM	I1_OVERRUN	--

Table 39. CTRL_REG3 description

I1_CLICK	CLICK interrupt on INT1 pin. Default value 0. (0: disable; 1: enable)
I1_AOI1	AOI1 interrupt on INT1 pin. Default value 0. (0: disable; 1: enable)
I1_AOI2	AOI2 interrupt on INT1 pin. Default value 0. (0: disable; 1: enable)
I1_DRDY1	DRDY1 interrupt on INT1 pin. Default value 0. (0: disable; 1: enable)
I1_DRDY2	DRDY2 interrupt on INT1 pin. Default value 0. (0: disable; 1: enable)
I1_WTM	FIFO watermark interrupt on INT1 pin. Default value 0. (0: disable; 1: enable)
I1_OVERRUN	FIFO overrun interrupt on INT1 pin. Default value 0. (0: disable; 1: enable)

8.9 CTRL_REG4_A (23h)

Table 40. CTRL_REG4 register

BDU	BLE(1)	FS1	FS0	HR	ST1	ST0	SPI_ ENABLE

1. The BLE function can be activated only in high-resolution mode

Table 41. CTRL_REG4 description

BDU	Block data update. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB have been read)
BLE	Big/Little Endian data selection. Default value: 0 (0: data LSb at lower address; 1: data MSb at lower address) The BLE function can be activated only in high-resolution mode
FS[1:0]	Full-scale selection. Default value: 00 (00: ±2*g*; 01: ±4*g*; 10: ±8*g*; 11: ±16*g*)
HR	Operating mode selection (refer to *Section 4.2.1: Accelerometer power modes*)
ST[1:0]	Self-test enable. Default value: 00 (00: self-test disabled; other: see *Table 42*)
SPI_ENABLE	3-wire SPI interface enable. Default: 0 (0: SPI 3-wire disabled; 1: SPI 3-wire enabled)

Table 42. Self-test mode configuration

ST1	ST0	Self-test mode
0	0	Normal mode
0	1	Self test 0
1	0	Self test 1
1	1	--

8.10 CTRL_REG5_A (24h)

Table 43. CTRL_REG5_A register

BOOT	FIFO_EN	--	--	LIR_INT1	D4D_INT1	LIR_INT2	D4D_INT2

Table 44. CTRL_REG5_A description

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
FIFO_EN	FIFO enable. Default value: 0 (0: FIFO disabled; 1: FIFO enabled)
LIR_INT1	Latch interrupt request on *INT1_SRC_A (31h)*, with *INT1_SRC_A (31h)* register cleared by reading *INT1_SRC_A (31h)* itself. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched)
D4D_INT1	4D enable: 4D detection is enabled on INT1 pin when 6D bit on *INT1_CFG_A (30h)* is set to 1.
LIR_INT2	Latch interrupt request on *INT2_SRC_A (35h)* register, with *INT2_SRC_A (35h)* register cleared by reading *INT2_SRC_A (35h)* itself. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched)
D4D_INT2	4D enable: 4D detection is enabled on INT2 pin when 6D bit on *INT2_CFG_A (34h)* is set to 1.

8.11 CTRL_REG6_A (25h)

Table 45. CTRL_REG6_A register

I2_CLICKen	I2_INT1	I2_INT2	BOOT_I2	P2_ACT	- -	H_LACTIVE	-

Table 46. CTRL_REG6_A description

I2_CLICKen	Click interrupt on INT2 pin. Default value: 0 (0: disabled; 1: enabled)
I2_INT1	Interrupt 1 function enable on INT2 pin. Default value: 0 (0: function disabled; 1: function enabled)
I2_INT2	Interrupt 2 function enable on INT2 pin. Default value: 0 (0: function disabled; 1: function enabled)
BOOT_I2	Boot on INT2 pin enable. Default value: 0 (0: disabled; 1:enabled)
P2_ACT	Activity interrupt enable on INT2 pin. Default value: 0. (0: disabled; 1:enabled)
H_LACTIVE	interrupt active. Default value: 0. (0: interrupt active-high; 1: interrupt active-low)

8.12 REFERENCE/DATACAPTURE_A (26h)

Table 47. REFERENCE/DATACAPTURE_A register

Ref7	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1	Ref0

Table 48. REFERENCE/DATACAPTURE_A description

Ref [7:0]	Reference value for interrupt generation. Default value: 0

8.13 STATUS_REG_A (27h)

Table 49. STATUS_REG_A register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

Table 50. STATUS_REG_A description

ZYXOR	X-, Y- and Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous set)
ZOR	Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data)
YOR	Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data)
XOR	X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data)
ZYXDA	X-, Y- and Z-axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z-axis new data available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YDA	Y-axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available; 1: new data for the Y-axis is available)

8.14 OUT_X_L_A (28h), OUT_X_H_A (29h)

X-axis acceleration data. The value is expressed as two's complement left-justified.
Please refer to *Section 4.2.1: Accelerometer power modes*.

8.15 OUT_Y_L_A (2Ah), OUT_Y_H_A (2Bh)

Y-axis acceleration data. The value is expressed as two's complement left-justified.
Please refer to *Section 4.2.1: Accelerometer power modes*.

8.16 OUT_Z_L_A (2Ch), OUT_Z_H_A (2Dh)

Z-axis acceleration data. The value is expressed as two's complement left-justified.
Please refer to *Section 4.2.1: Accelerometer power modes*.

8.17 FIFO_CTRL_REG_A (2Eh)

Table 51. FIFO_CTRL_REG_A register

FM1	FM0	TR	FTH4	FTH3	FTH2	FTH1	FTH0

Table 52. FIFO_CTRL_REG_A description

FM[1:0]	FIFO mode selection. Default value: 00 (see *Table 53*)
TR	Trigger selection. Default value: 0 0: trigger event allows triggering signal on INT1 1: trigger event allows triggering signal on INT2
FTH[4:0]	Default value: 00000

Table 53. FIFO mode configuration

FM1	FM0	FIFO mode
0	0	Bypass mode
0	1	FIFO mode
1	0	Stream mode
1	1	Stream-to-FIFO mode

8.18 FIFO_SRC_REG_A (2Fh)

Table 54. FIFO_SRC_REG_A register

WTM	OVRN_FIFO	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0

Table 55. FIFO_SRC_REG_A description

WTM	WTM bit is set high when FIFO content exceeds watermark level.
OVRN_FIFO	OVRN bit is set high when FIFO buffer is full; this means that the FIFO buffer contains 32 unread samples. At the following ODR a new sample set replaces the oldest FIFO value. The OVRN bit is set to 0 when the first sample set has been read.
EMPTY	EMPTY flag is set high when all FIFO samples have been read and FIFO is empty.
FSS [4:0]	FSS [4:0] field always contains the current number of unread samples stored in the FIFO buffer. When FIFO is enabled, this value increases at ODR frequency until the buffer is full, whereas, it decreases every time one sample set is retrieved from FIFO.

8.19 INT1_CFG_A (30h)

Table 56. INT1_CFG_A register

AOI	6D	ZHIE/ ZUPE	ZLIE/ ZDOWNE	YHIE/ YUPE	YLIE/ YDOWNE	XHIE/ XUPE	XLIE/ XDOWNE

Table 57. INT1_CFG_A description

AOI	And/Or combination of interrupt events. Default value: 0. Refer to *Table 58.*
6D	6-direction detection function enabled. Default value: 0. Refer to *Table 58.*
ZHIE/ ZUPE	Enable interrupt generation on Z high event or on direction recognition. Default value: 0 (0: disable interrupt request;1: enable interrupt request)
ZLIE/ ZDOWNE	Enable interrupt generation on Z low event or on direction recognition. Default value: 0 (0: disable interrupt request;1: enable interrupt request)
YHIE/ YUPE	Enable interrupt generation on Y high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
YLIE/ YDOWNE	Enable interrupt generation on Y low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
XHIE/ XUPE	Enable interrupt generation on X high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
XLIE/ XDOWNE	Enable interrupt generation on X low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)

The content of this register is loaded at boot.

A write operation to this address is possible only after system boot.

Table 58. Interrupt mode

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6-direction movement recognition
1	0	AND combination of interrupt events
1	1	6-direction position recognition

The difference between AOI-6D = ‘01’ and AOI-6D = ‘11’.

AOI-6D = ‘01’ is movement recognition. An interrupt is generated when the orientation moves from an unknown zone to a known zone. The interrupt signal remains for a duration ODR.

AOI-6D = ‘11’ is direction recognition. An interrupt is generated when the orientation is inside a known zone. The interrupt signal remains while the orientation is inside the zone.

8.20 INT1_SRC_A (31h)

Table 59. INT1_SRC_A register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 60. INT1_SRC_A description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

Interrupt 1 source register. Read-only register.

Reading at this address clears the *INT1_SRC_A (31h)* IA bit (and the interrupt signal on the INT1 pin) and allows the refresh of data in the *INT1_SRC_A (31h)* register if the latched option was chosen.

8.21 INT1_THS_A (32h)

Table 61. INT1_THS_A register

0	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 62. INT1_THS_A description

THS[6:0]	Interrupt 1 threshold. Default value: 000 0000 1 LSb = 16 mg @ FS = 2 *g* 1 LSb = 32 mg @ FS = 4 *g* 1 LSb = 62 mg @ FS = 8 *g* 1 LSb = 186 mg @ FS = 16 *g*

8.22 INT1_DURATION_A (33h)

Table 63. INT1_DURATION_A register

0	D6	D5	D4	D3	D2	D1	D0

Table 64. INT1_DURATION_A description

D[6:0]	Duration value. Default value: 000 0000 1 LSb = 1/ODR

The **D[6:0]** bits set the minimum duration of the Interrupt 2 event to be recognized. Duration steps and maximum values depend on the ODR chosen.

Duration time is measured in N/ODR, where N is the content of the duration register.

8.23 INT2_CFG_A (34h)

Table 65. INT2_CFG_A register

AOI	6D	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE

Table 66. INT2_CFG_A description

AOI	AND/OR combination of interrupt events. Default value: 0 (see *Table 67*)
6D	6-direction detection function enabled. Default value: 0. Refer to *Table 67.*
ZHIE	Enable interrupt generation on Z high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)

Table 66. INT2_CFG_A description (continued)

ZLIE	Enable interrupt generation on Z low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)
YHIE	Enable interrupt generation on Y high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YLIE	Enable interrupt generation on Y low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)
XHIE	Enable interrupt generation on X high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XLIE	Enable interrupt generation on X low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)

The content of this register is loaded at boot.

A write operation to this address is possible only after system boot.

Table 67. Interrupt mode

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6-direction movement recognition
1	0	AND combination of interrupt events
1	1	6-direction position recognition

The difference between AOI-6D = ‘01’ and AOI-6D = ‘11’.

AOI-6D = ‘01’ is movement recognition. An interrupt is generated when the orientation moves from an unknown zone to a known zone. The interrupt signal remains for a duration ODR.

AOI-6D = ‘11’ is direction recognition. An interrupt is generated when the orientation is inside a known zone. The interrupt signal remains while the orientation is inside the zone.

8.24 INT2_SRC_A (35h)

Table 68. INT2_SRC_A register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 69. INT2_SRC_A description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

Interrupt 2 source register. Read-only register.

Reading at this address clears the *INT2_SRC_A (35h)* IA bit (and the interrupt signal on the INT2 pin) and allows the refresh of data in the *INT2_SRC_A (35h)* register if the latched option was chosen.

8.25 INT2_THS_A (36h)

Table 70. INT2_THS_A register

0	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 71. INT2_THS_A description

THS[6:0]	Interrupt 2 threshold. Default value: 000 0000 1 LSb = 16 m*g* @ FS = 2 *g* 1 LSb = 32 m*g* @ FS = 4 *g* 1 LSb = 62 m*g* @ FS = 8 *g* 1 LSb = 186 m*g* @ FS = 16 *g*

8.26 INT2_DURATION_A (37h)

Table 72. INT2_DURATION_A register

0	D6	D5	D4	D3	D2	D1	D0

Table 73. INT2_DURATION_A description

D[6:0]	Duration value. Default value: 000 0000 1 LSb = 1/ODR(1)

1. Duration time is measured in N/ODR, where N is the content of the duration register.

The **D[6:0]** bits set the minimum duration of the Interrupt 2 event to be recognized. Duration time steps and maximum values depend on the ODR chosen.

8.27 CLICK_CFG_A (38h)

Table 74. CLICK_CFG_A register

--	--	ZD	ZS	YD	YS	XD	XS

Table 75. CLICK_CFG_A description

ZD	Enable interrupt double-click on Z-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
ZS	Enable interrupt single-click on Z-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YD	Enable interrupt double-click on Y-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YS	Enable interrupt single-click on Y-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XD	Enable interrupt double-click on X-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XS	Enable interrupt single-click on X-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)

8.28 CLICK_SRC_A (39h)

Table 76. CLICK_SRC_A register

	IA	DClick	SClick	Sign	Z	Y	X

Table 77. CLICK_SRC_A description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
DClick	Double-click enable. Default value: 0 (0: double-click detection disabled, 1: double-click detection enabled)
SClick	Single-click enable. Default value: 0 (0: single-click detection disabled, 1: single-click detection enabled)
Sign	Click sign. 0: positive detection, 1: negative detection
Z	Z click detection. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
Y	Y click detection. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
X	X click detection. Default value: 0 (0: no interrupt, 1: X high event has occurred)

8.29 CLICK_THS_A (3Ah)

Table 78. CLICK_THS_A register

-	Ths6	Ths5	Ths4	Ths3	Ths2	Ths1	Ths0

Table 79. CLICK_SRC_A description

Ths[6:0]	Click threshold. Default value: 000 0000

8.30 TIME_LIMIT_A (3Bh)

Table 80. TIME_LIMIT_A register

-	TLI6	TLI5	TLI4	TLI3	TLI2	TLI1	TLI0

Table 81. TIME_LIMIT_A description

TLI[6:0]	Click time limit. Default value: 000 0000

8.31 TIME_LATENCY_A (3Ch)

Table 82. TIME_LATENCY_A register

TLA7	TLA6	TLA5	TLA4	TLA3	TLA2	TLA1	TLA0

Table 83. TIME_LATENCY_A description

TLA[7:0]	Click time latency. Default value: 0000 0000

8.32 TIME_WINDOW_A (3Dh)

Table 84. TIME_WINDOW_A register

TW7	TW6	TW5	TW4	TW3	TW2	TW1	TW0

Table 85. TIME_WINDOW_A description

TW[7:0]	Click time window

8.33 Act_THS_A (3Eh)

Table 86. Act_THS_A register

--	Acth6	Acth5	Acth4	Acth3	Acth2	Acth1	Acth0

Table 87. Act_THS_A description

Acth[6:0]	Sleep-to-wake, return-to-sleep activation threshold in low-power mode 1 LSb = 16 m*g* @ FS = 2 *g* 1 LSb = 32 m*g* @ FS = 4 *g* 1 LSb = 62 m*g* @ FS = 8 *g* 1 LSb = 186 m*g* @ FS = 16 *g*

8.34 Act_DUR_A (3Fh)

Table 88. Act_DUR_A register

ActD7	ActD6	ActD5	ActD4	ActD3	ActD2	ActD1	ActD0

Table 89. Act_DUR_A description

ActD[7:0]	Sleep-to-wake, return-to-sleep duration 1 LSb = (8*1[LSb]+1)/ODR

8.35 OFFSET_X_REG_L_M (45h) and OFFSET_X_REG_H_M (46h)

These registers comprise a 16-bit register and represent X hard-iron offset in order to compensate environmental effects (data in two's complement). These values act on the magnetic output data value in order to delete the environmental offset.

8.36 OFFSET_Y_REG_L_M (47h) and OFFSET_Y_REG_H_M (48h)

These registers comprise a 16-bit register and represent Y hard-iron offset in order to compensate environmental effects (data in two's complement). These values act on the magnetic output data value in order to delete the environmental offset.

8.37 OFFSET_Z_REG_L_M (49h) and OFFSET_Z_REG_H_M (4Ah)

These registers comprise a 16-bit register and represent Z hard-iron offset in order to compensate environmental effects (data in two's complement). These values act on the magnetic output data value in order to delete the environmental offset.

8.38 WHO_AM_I_M (4Fh)

The identification register is used to identify the device (read-only register).

0	1	0	0	0	0	0	0

8.39 CFG_REG_A_M (60h)

The configuration register is used to configure the output data rate and the measurement configuration.

Table 90. CFG_REG_A_M register

0	0	SOFT_RST	LP	ODR1	ODR0	MD1	MD0

Table 91. CFG_REG_A_M register description

SOFT_RST	When this bit is set, the configuration registers and user registers are reset. Flash registers keep their values.
LP	Low-power mode enable. Default: 0 0: high-resolution mode 1: low-power mode enabled
ODR[1:0]	Output data rate configuration (see *Table 92: Output data rate configuration*)
MD[1:0]	Mode select bit. These bits select the mode of operation of the device (see *Table 93: System mode*)

Table 92. Output data rate configuration

ODR1	ODR0	ODR (Hz)
0	0	10 (default)
0	1	20
1	0	20
1	1	100

Table 93. System mode

MD1	MD0	Mode
0	0	Continuous mode. In continuous mode the device continuously performs measurements and places the result in the data register. The data-ready signal is generated when a new data set is ready to be read. This signal can be available on the external pin by setting the INT_MAG bit in *CFG_REG_C_M (62h)*.
0	1	Single mode. When single mode is selected, the device performs a single measurement, sets DRDY high and returns to idle mode. Mode register return to idle mode bit values.
1	0	Idle mode. Device is placed in idle mode. I^2C and SPI active.
1	1	Idle mode. Device is placed in idle mode. I^2C and SPI active.

8.40 CFG_REG_B_M (61h)

Table 94. CFG_REG_B_M register

0	0	0	0	INT_on_ DataOFF	Set_FREQ	OFF_CANC	LPF

Table 95. CFG_REG_B_M register description

INT_on_ DataOFF	If ‘1’, the interrupt block recognition checks data after the hard-iron correction to discover the interrrupt.
Set_FREQ	Selects the frequency of the set pulse. 0: set pulse is released every 63 ODR; 1: set pulse is release only at power-on after PD condition.
OFF_CANC	Enables offset cancellation.
LPF	Low-pass filter enable (see *Table 96*) 0: digital filter disabled; 1: digital filter enabled

Table 96. Digital low-pass filter

CFG_REG_B[LPF]	BW [Hz]
0 (disable)	ODR/2
1 (enable)	ODR/4

8.41 CFG_REG_C_M (62h)

Table 97. CFG_REG_C_M register

0	INT_MAG_PIN	I2C_DIS	BDU	BLE	0(1)	Self_test	INT_MAG

1. This bit must be set to '0' for the correct operation of the device.

Table 98. CFG_REG_C_M register description

INT_MAG_PIN	If '1', the INTERRUPT signal (INT bit inside *INT_SOURCE_REG_M (64h)*) is driven on INT_MAG_PIN
I2C_DIS	If '1', the I^2C interface is inhibited. Only the SPI interface can be used.
BDU	If enabled, reading of incorrect data is avoided when the user reads asynchronously. In fact if the read request arrives during an update of the output data, a latch is possible, reading incoherent high and low parts of the same register. Only one part is updated and the other one remains old.
BLE	If '1', an inversion of the low and high parts of the data occurs.
Self_test	If '1', the self-test is enabled.
INT_MAG	If '1', the DRDY pin is configured as a digital output.

8.42 INT_CTRL_REG_M (63h)

The interrupt control register is used to enable and to configure the interrupt recognition.

Table 99. INT_CRTL_REG_M register

XIEN	YIEN	ZIEN	0(1)	0(1)	IEA	IEL	IEN

1. This bit must be set to '0' for the correct operation of the device.

Table 100. INT_CTRL_REG_M register description

XIEN	Enables the interrupt recognition for the X-axis. Default: 0 1: enabled; 0: disabled.
YIEN	Enables the interrupt recognition for the Y-axis. Default: 0 1: enabled; 0: disabled.
ZIEN	Enables the interrupt recognition for the Z-axis. Default: 0 1: enabled; 0: disabled.
IEA	Controls the polarity of the INT bit (*INT_SOURCE_REG_M (64h)*) when an interrupt occurs. Default: 0 If IEA = 0, then INT = 0 signals an interrupt If IEA = 1, then INT = 1 signals an interrupt
IEL	Controls whether the INT bit (*INT_SOURCE_REG_M (64h)*) is latched or pulsed. Default: 0 If IEL = 0, then INT is pulsed. If IEL = 1, then INT is latched. Once latched, INT remains in the same state until *INT_SOURCE_REG_M (64h)* is read.
IEN	Interrupt enable. When set, enables the interrupt generation. The INT bit is in *INT_SOURCE_REG_M (64h)*. Default: 0

8.43 INT_SOURCE_REG_M (64h)

When interrupt latched is selected, reading this register resets all the bits in this register.

Table 101. INT_SOURCE_REG_M register

P_TH_S_X	P_TH_S_Y	P_TH_S_Z	N_TH_S_X	N_TH_S_Y	N_TH_S_Z	MROI	INT

Table 102. INT_SOURCE_REG_M register description

P_TH_S_X	X-axis value exceeds the threshold positive side
P_TH_S_Y	Y-axis value exceeds the threshold positive side
P_TH_S_Z	Z-axis value exceeds the threshold positive side
N_TH_S_X	X-axis value exceeds the threshold negative side
N_TH_S_Y	Y-axis value exceeds the threshold negative side
N_TH_S_Z	Z-axis value exceeds the threshold negative side
MROI	MROI flag generation is alway enabled.This flag is reset by reading *INT_SOURCE_REG_M (64h)*.
INT	This bit signals when the interrupt event occurs.

8.44 INT_THS_L_REG_M (65h)

This register contains the least significant bits of the threshold value chosen for the interrupt.

Table 103. INT_THS_L_REG_M register

TH7	THS6	TH5	TH4	TH3	TH2	TH1	TH0

Table 104. INT_THS_L_REG_M register description

TH[7:0]	Threshold value for the interrupt.

8.45 INT_THS_H_REG_M (66h)

This register contains the most significant bits of the threshold value chosen for the interrupt.

Table 105. INT_THS_H_REG_M register

TH7	THS6	TH5	TH4	TH3	TH2	TH1	TH0

Table 106. INT_THS_H_REG_M register description

TH[7:0]	Threshold value for the interrupt.

These registers set the threshold value for the output to generate the interrupt (INT bit in *INT_SOURCE_REG_M (64h)*). This threshold is common to all three (axes) output values and is unsigned unipolar. The threshold value is correlated to the current gain and it is unsigned because the threshold is considered as an absolute value, but crossing the threshold is detected for both positive and negative sides.

8.46 STATUS_REG_M (67h)

The status register is an 8-bit read-only register. This register is used to indicate device status. SR0 through SR7 indicate bit locations, with SR denoting the bits that are in the status register. SR7 denotes the first bit of the data stream.

Table 107. STATUS_REG_M register

Zyxor	zor	yor	xor	Zyxda	zda	yda	xda

Table 108. STATUS_REG_M register description

Zyxor	X-, Y- and Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous set).
zor	Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data).
yor	Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data).
xor	X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data).
Zyxda	X-, Y- and Z-axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available).
zda	Z-axis new data available. Default value: 0 (0: a new data for the Z-axis is not yet available; 1: a new data for the Z-axis is available)
yda	Y-axis new data available. Default value: 0 (0: a new data for the Y-axis is not yet available; 1: a new data for the Y-axis is available)
xda	X-axis new data available. Default value: 0 (0: a new data for the X-axis is not yet available; 1: a new data for the X-axis is available)

8.47 OUTX_L_REG_M, OUTX_H_REG_M (68h - 69h)

The data output X registers are two 8-bit registers, data output ch1 MSB register (69h) and output X LSB register (68h).

The output data represents the raw magnetic data only if OFFSET_X_REG is equal to zero, otherwise hard-iron calibration is included.

Table 109. OUTX_L_REG_M register

0	0	0	0	0	0	0	0

Table 110. OUTX_H_REG_M register

0	0	0	0	0	0	0	0

The value of the magnetic field is expressed in two’s complement. This register contains the X component of the magnetic data.

8.48 OUTY_L_REG_M, OUTY_H_REG_M (6Ah - 6Bh)

The data output Y registers are two 8-bit registers, data output ch1 MSB register (6Bh) and output Y LSB register (6Ah).

The output data represents the raw magnetic data only if OFFSET_Y_REG is equal to zero, otherwise hard-iron calibration is included.

Table 111. OUTY_L_REG_M register

0	0	0	0	0	0	0	0

Table 112. OUTY_H_REG_M register

0	0	0	0	0	0	0	0

The value of the magnetic field is expressed in two’s complement. This register contains the Y component of the magnetic data.

8.49 OUTZ_L_REG_M, OUTZ_H_REG_M (6Ch - 6Dh)

The data output Zregisters are two 8-bit registers, data output ch1 MSB register (6Bh) and output Z LSB register (6Ah).

The output data represents the raw magnetic data only if OFFSET_Z_REG is equal to zero, otherwise hard-iron calibration is included.

Table 113. OUTZ_L_REG_M register

0	0	0	0	0	0	0	0

Table 114. OUTZ_H_REG_M register

0	0	0	0	0	0	0	0

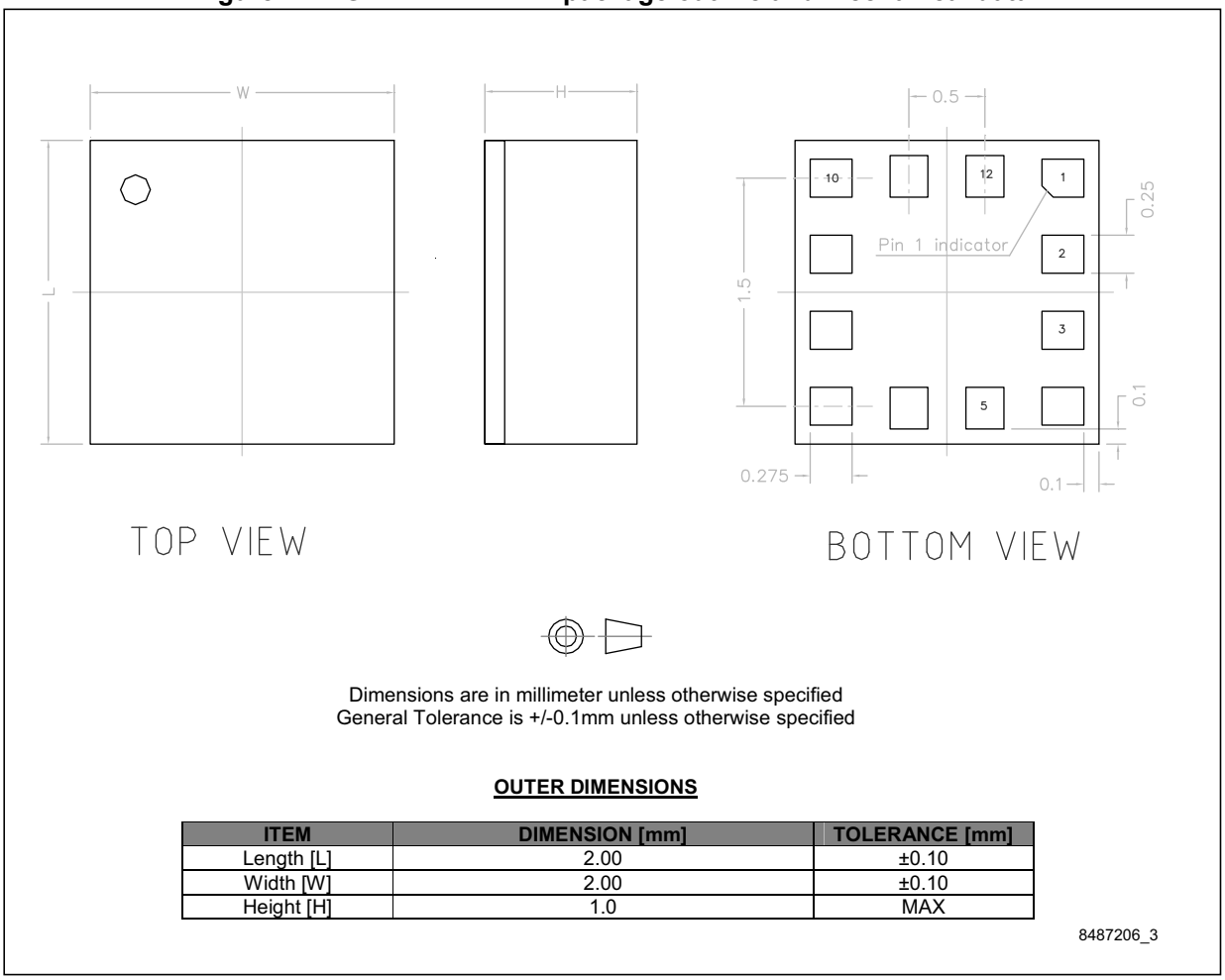
The value of the magnetic field is expressed in two’s complement. This register contains the Z component of the magnetic data.

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

9.1 LGA-12 package information

Figure 17. LGA-12 2x2x1 mm package outline and mechanical data



OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	2.00	±0.10
Width [W]	2.00	±0.10
Height [H]	1.0	MAX

8487206_3

10 Revision history

Table 115. Document revision history

Date	Revision	Changes
12-May-2015	1	Initial release
10-Jun-2015	2	Updated *Description* to include fast mode plus and high speed I^2C interface Added *Table 8: I^2C slave timing values (fast mode plus and high speed)*
26-Aug-2015	3	Added footnote *3* to *Table 3: Sensor characteristics* Added values for M_ST in *Table 3: Sensor characteristics* Updated *Figure 17: LGA-12 2x2x1 mm package outline and mechanical data*
06-Oct-2015	4	Updated *Table 3: Sensor characteristics* Added *Section 4.1.5: Magnetometer self-test* and updated *Section 4.2.4: Accelerometer self-test*
18-Nov-2015	5	Initial public release