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Allwinner H6 V200 User Manual

Revision 1.1

Oct.17, 2017

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Revision History

Revision	Date	Description
1.0	Sep. 05,2017	Initial Release Version
1.1	Oct. 17,2017	1、Update the feature of VE Decoder in chapter 2.2.6.1. 2、Modify the Task Status Register in chapter 3.14.5.5. 3、Add the comment of key address in chapter 3.14.3.4.

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Chapter 1 About This Documentation

1.1. Purpose

This documentation provides an overall description of the Allwinner's H6 V200 application processor, which describes the overview, features, logical structures, functions and register listings of each module. The documentation is intended to provide guidance to programmers writing code for H6 V200 processor. This documentation assumes that the reader has a background in computer engineering and/or software engineering, with the goal to aid anyone in understanding and potentially modifying the Allwinner provided code.

1.2. Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
 **WARNING**	A warning means that injury or death is possible if the instructions are not obeyed.
 **CAUTION**	A caution means that damage to equipment is possible.
 **NOTE**	Provides additional information to emphasize or supplement important points of the main text.

1.3. Notes

1.3.1. Register Attributes

The register attributes that may be found in this document are defined as follows.

Symbol	Description
R	Read Only
R/W	Read/Write
R/WAC	Read/Write-Automatic-Clear,clear the bit automatically when the operation of complete. Writing 0 has no effect

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R/WC	Read/Write-Clear
R/W0C	Read/Write 0 to Clear, Writing 1 has non-effect
R/W1C	Read/Write 1 to Clear, Writing 0 has non-effect
R/W1S	Read/Write 1 to Set, Writing 0 has non-effect
W	Write Only

1.3.2. Reset Value Conventions

In the register definition tables:
If other column value in a bit or multiple bits row is "/", that this bit or these multiple bits are unused.
If the default value of a bit or multiple bits is "UDF", that the default value is undefined.

1.3.3. Numerical System

The expressions of data capacity, frequency, and data rate are described as follows.

Type	Symbol	Value
Data capacity	1K	1024
	1M	1,048,576
	1G	1,073,741,824
Frequency,data rate	1k	1000
	1M	1,000,000
	1G	1,000,000,000

The expressions of addresses and data are described as follows.

Symbol	Example	Description
0x	0x0200,0x79	Address or data in hexadecimal
0b	0b010,0b00 000 111	Data or sequence in binary(register description is excluded.)
X	00X,XX1	In data expression,X indicates 0 or 1.For example, 00X indicates 000 or 001, XX1 indicates 001,011,101 or 111.

1.4. Acronyms and Abbreviations

The table below contains acronyms and abbreviations used in this documentation.

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AES	Advanced Encryption Standard
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
AHB	AMBA High-speed Bus
APB	Advanced Peripheral Bus
ARM	Advanced RISC Machine
ATE	The First Letter of Audio-Codec, TVE, EPHY
AVS	Audio Video Standard
BROM	Boot ROM
CIR	Consumer Infrared
CMOS	Complementary Metal-Oxide Semiconductor
CP15	Coprocessor 15
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CSI	Camera Serial Interface
CVBS	Composite Video Broadcast Signal
DES	Data Encryption Standard
DLL	Delay-Locked Loop
DMA	Direct Memory Access
DRC	Dynamic Range Compression
DVFS	Dynamic Voltage and Frequency Scaling
ECC	Error Correction Code
eFuse	Electrical Fuse, A one-time programmable memory
EHCI	Enhanced Host Controller Interface
eMMC	Embedded Multi-Media Card
ESD	Electrostatic Discharge
FBGA	Fine Ball Grid Array
FEL	Fireware Exchange Launch
FIFO	First In First Out
GIC	Generic Interrupt Controller
GMII	Gigabit Media Independent Interface
GPIO	General Purpose Input Output
GPU	Graphics Processing Unit
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
I2C	Inter Integrated Circuit
I2S	Inter IC Sound
JEDEC	Joint Electron Device Engineering Council
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group
LCD	Liquid-Crystal Display
LSB	Least Significant Bit
LVDS	Low Voltage Differential Signaling
MAC	Media Access Control
MII	Media Independent Interface

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MIPI	Mobile Industry Processor Interface
MLC	Multi-Level Cell
MMC	Multimedia Card
MPEG	Motion Pictures Expert Group
MPEG1	The First MPEG Compression Scheme Specification
MPEG4	The Most Current MPEG Compression Scheme Specification
MSB	Most Significant Bit
N/A	Not Application
NMI	Non Maskable Interrupt
NTSC	National Television Standards Committee
NVM	Non Volatile Storage Medium
OHCI	Open Host Controller Interface
OTP	One Time Programmable
OWA	One Wire Audio
PAL	Phase Alternating Line
PCM	Pulse Code Modulation
PHY	Physical Layer Controller
PID	Packet Identifier
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
R	Read only/non-Write
RGB	Read Green Blue
RMII	Reduced Media Independent Interface
ROM	Read Only Memory
RTC	Real Time Clock
R/W	Read/Write
R/WAC	Read/Write-Automatic-Clear,clear the bit automatically when the operation of complete.Writing 0 has no effect
R/WC	Read/Write-Clear
R/W0C	Read/Write 0 to Clear, Writing 1 has non-effect
R/W1C	Read/Write 1 to Clear, Writing 0 has non-effect
R/W1S	Read/Write 1 to Set, Writing 0 has non-effect
SDIO	Secure Digital Input Output
SDRAM	Sychronous Dynamic Random Access Memory
SLC	Single-Level Cell
SOC	System On Chip
SPI	Serial Peripheral Interface
S/PDIF	Sony/Philips Digital Interface Format
SRAM	Static Random Access Memory
TDES	Triple Data Encryption Standard
TWI	Two Wire Interface
UART	Universal Asynchronous Receiver Transmitter
UDF	Undefined
USB OTG	Universal Serial Bus On The Go

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UTMI	USB2.0 Transceiver Macrocell Interface

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Chapter 2 Overview

This part describes the overview for H6 V200 processor.

- Processor Overview
- Processor Features
- System Block Diagram

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2.1. Processor Overview

The Allwinner H6 V200 is a highly cost-efficient quad-core OTT Box processor, which is a part of growing home entertainment products that offer high-performance processing with a high degree of functional integration.

The H6 V200 processor has some very exciting features, for example:

- **CPU**: Quad-core ARM Cortex™-A53 Processor, a power-efficient ARM v8 architecture, it has 64 and 32bit execution states for scalable high performance ,which includes a NEON multimedia processing engine.
- **Graphics**: Mali-T720 Multi-Core, proven Midgard architecture with two shade cores, provides users with superior experience in video playback and mainstream game; OpenGL ES3.1and OpenCL1.2 standards are supported.
- **Video Engine**: H6 V200 provides multi-format high-definition video encoder/decoder with dedicated hardware, including H.265 decoder by 4K@60fps , H.264 decoder by 4K@30fps, H.263 decoder by 1080p@60fps, VP9 decoder by 4K@30fps, MPEG1/2/4 decoder by 1080p@60fps, VC1/VP8/AVS/AVS+ jizhun decoder by 1080p@60fps, H.264 encoder by 1080p@60fps.
- **Display Subsystem**: Supports Allwinner's SmartColor 3.0 for excellent display experience, and three display interfaces including RGB LCD display for LCD, HDMI2.0a output and TVOUT(Controlled by ATE) for TV.
- **Audio Subsystem**: Supports popular digital audio interfaces such as I2S/PCM,OWA,DMIC and Audio Hub, and supports I2S/PCM for connecting to an external audio codec. To reduce total system cost and enhance high integration, the H6 V200 also integrates an audio codec(Controlled by ATE) in processor.
- **Memory Controller**: The processor supports many types of external memory devices, including DDR4/DDR3/ DDR3L/LPDDR2/LPDDR3, NAND Flash with full disk encryption ,Nor Flash, SD/SDIO/MMC including eMMC up to rev5.1.
- **Security System**: The processor delivers hardware security features that enable trustzone security system, Digital Rights Management(DRM) , information encryption/decryption, secure boot and secure efuse.
- **Interfaces**: The processor has a broad range of hardware interfaces such as parallel CMOS sensor interface, 10/100/1000Mbps EMAC with EPHY(Controlled by ATE), USB OTG v2.0 operating at high speed(480Mbps) with PHY, USB3.0/2.0 Host with PHY, and a variety of other popular interfaces(SPI,UART,PCIe,One Wire,CIR,TSC,TWI,SCR).

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2.2. Processor Features

2.2.1. CPU Architecture

- Quad-core ARM Cortex™-A53 Processor
- Power-efficient ARM v8 architecture
- 64 and 32bit execution states for scalable high performance
- Trustzone technology supported
- 3~10x better software encryption performance
- Supports NEON Advanced SIMD(Single Instruction Multiple Data)instruction for acceleration of media and signal processing functions
- Supports Large Physical Address Extensions(LPAE)
- VFPv4 Floating Point Unit
- 32KB L1 Instruction cache and 32KB L1 Data cache per core
- 512KB L2 cache shared

2.2.2. GPU Architecture

- Mali-T720 Multi-Core, proven Midgard architecture with two shade cores
- Supports OpenGL ES 3.1/3.0/2.0/1.1, OpenCL 1.2/1.1, DirectX 11 FL9_3, and Renderscript/Filterscript
- Supports Transaction Elimination, saving external bandwidth and energy
- Supports ASTC, best-in-class compression, reduced size and improved quality
- Supports FAST(4x)FSAA, IO Coherency

2.2.3. Memory Subsystem

2.2.3.1. Boot ROM

- On chip ROM
- Supports system boot from the following devices:
  - NAND Flash
  - SD card
  - eMMC
  - SPI Nor Flash
- Supports secure boot and normal boot
- Supports one key USB mass production upgrade
- Supports system code download through USB OTG and card
- Supports boot media priority sequence through boot select pin and efuse

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2.2.3.2. SDRAM

- Compatible with JEDEC standard DDR4/DDR3/DDR3L/LPDDR2/LPDDR3 SDRAM
- Supports clock frequency up to 933MHz(DDR4)
- 32-bit bus width
- Up to 2GB address space
- Supports 2 chip selects
- 18 address signal lines and 3 bank signal lines
- Random read or write operation is supported

2.2.3.3. NAND Flash

- Up to 8-bit data bus width
- Up to 80-bit ECC per 1024 bytes
- Supports 2CE/2RB
- Supports 1024, 2048, 4096, 8192, 16384, 32768 bytes size per page
- Supports SLC/MLC/TLC flash and EF-NAND memory
- Supports SDR, ONFI DDR and Toggle DDR NAND
- Supports full disk encryption(FDE) function
- Embedded DMA to do data transfer
- Supports data transfer together with normal DMA

2.2.3.4. SMHC

- Up to 3 SD/MMC host controller(SMHC) interfaces
- SMHC0 controls the device that comply with the Secure Digital Memory(SD3.0)
  - 4-bit bus width
  - SDR mode 50MHz@3.3V IO pad
- SMHC1 controls the devices that comply with the Secure Digital Input/Output(SDIO3.0)
  - 4-bit bus width
  - SDR mode 50MHz@3.3V IO pad
  - SDR mode 150MHz@1.8V IO pad
  - DDR mode 50MHz@1.8V IO pad
- SMHC2 controls the devices that comply with the MultiMediaCard(MMC5.1)
  - 8-bit bus width
  - SDR mode 150MHz@1.8V IO pad
  - DDR mode 100MHz@1.8V IO pad
  - DDR mode 50MHz@3.3V IO pad
- SMHC2 supports full disk encryption(FDE) function
- Supports hardware CRC generation and error detection
- Supports block size of 1 to 65535 bytes

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2.2.4. System Peripheral

2.2.4.1. Timer

- The timer module implements the timing and counting functions, which includes Timer0 and Timer1,Watchdog, AVS and 64-bit counter
- Timer0 and Timer1 for system scheduler counting
  - Configurable 8 prescale factor
  - Programmable 32-bit down timer
  - Supports two working modes: continue mode and single count mode
  - Generates an interrupt when the count is decreased to 0
- 1 Watchdog for transimitting a reset signal to reset the entire system after an exception occurs in the system
  - Supports 12 initial values to configure
  - Supports the generation of timeout interrupts
  - Supports the generation of reset signal
  - Supports watchdog restart the timing
- 2 AVS counters(AVS0 and AVS1) for synchronizing video and audio in the player
  - Programmable 33-bit up timer
  - Initial value can be updated anytime
  - 12-bit frequency divider factor
  - Supports Pause/Start function
- One 64-bit Counter to count timing for GPU
  - Supports clear zero function
  - Performs latch operation once before getting the current counter value

2.2.4.2. GIC

- Supports 16 Software Generated Interrupts(SGIs), 16 Private Peripheral Interrupts(PPIs) and 147 Shared Peripheral Interrupts(SPIs)
- Enabling, disabling, and generating processor interrupts from hardware interrupt
- Software-generated Interrupts (SGIs)
- Interrupt masking and prioritization
- Uniprocessor and multiprocessor environments
- The ARM architecture Security Extensions
- The ARM architecture Virtualization Extensions
- Wakeup events in power-management environments

2.2.4.3. DMA

- Up to 16-channel DMA
- Interrupt generated for each DMA channel
- Transfers data width of 8/16/32/64-bit
- Supports linear and IO address modes

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- Supports data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory, peripheral-to-peripheral
- Supports transfer with linked list
- DRQ response includes wait mode and handshake mode
- DMA channel supports pause function

2.2.4.4. CCU

- 11 PLLs
- Supports an external 32.768kHz crystal oscillator ,an external 24MHz DCXO and an internal RC16MHz oscillator
- Supports clock configuration and clock generated for corresponding modules
- Supports software-controlled clock gating and software-controlled reset for corresponding modules

2.2.4.5. IOMMU

- Supports virtual address to physical address mapping by hardware implementation
- Supports DE0/2, VE_R, VE, CSI, VP9 parallel address mapping
- Supports DE0/2, VE_R, VE, CSI, VP9 bypass function independently
- Supports DE0/2,VE_R,VE,CSI,VP9 prefetch independently
- Supports DE0/2,VE_R,VE,CSI,VP9 Interrupt handing mechanism independently
- Supports level1 and level2 TLB for special using, and level2 TLB for sharing
- Supports TLB Fully cleared and Partially disabled
- Supports trigger PTW behavior when TLB miss
- Supports checking the permission
- Performance: Average (L1+L2)TLB Hit rate: up to 99.9%, Average Latency: 5±1cycle

2.2.4.6. PWM

- Supports outputting two kinds of waveform: continuous waveform and pulse waveform
- 0% to 100% adjustable duty cycle
- Up to 24MHz output frequency
- The minimum resolution is 1/65536

2.2.4.7. Thermal Sensor

- Temperature Accuracy : ±3℃ from 0℃ to +100℃, ±5℃ from -20℃ to +125℃
- Power supply voltage:1.8V
- Averaging filter for thermal sensor reading
- Supports over-temperature protection interrupt and over-temperature alarm interrupt
- Supports 2 sensors:sensor0 for CPU,sensor1 for GPU

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2.2.4.8. Message Box

- Provides interrupt communication mechanism for on-chip processor
- Two users for Message Box: user0 for CPUS, user1 for CPUX
- Each of Queue has a 4x32-bits FIFO for eight Message Queues
- Each of Queue could be configured as transmitter or receiver

2.2.4.9. Spinlock

- 32 spinlocks
- Two kinds of status of lock register: TAKEN and NOT TAKEN
- Lock time of the processor is predictable(less than 200 cycles)

2.2.4.10. Crypto Engine(CE)

- Supports Symmetrical algorithm: AES,DES,TDES,XTS
  - Supports ECB,CBC,CTS,CTR,CFB,OFB,CBC-MAC mode for AES
  - Supports 128/192/256-bit key for AES
  - Supports ECB,CBC,CTR,CBC-MAC mode for DES/TDES
  - Supports 256/512-bit key for XTS
- Supports Hash algorithm: MD5,SHA,HMAC
  - Supports SHA1,SHA224,SHA384,SHA512 for SHA
  - Supports HMAC-SHA1,HMAC-SHA256 for HMAC
  - MD5,SHA,HMAC are padded using hardware. If not last package, input should align with 512 bits
- Supports Asymmetrical algorithm: RSA, ECC
  - RSA supports 512/1024/2048/4096-bit width
  - ECC Supports 160/224/256/384/521-bit width
- Supports 160-bit hardware PRNG with 175-bit seed
- Supports 256-bit hardware TRNG
- Internal Embedded DMA to do data transfer
- Supports secure and non-secure interfaces respectively
- Supports task chain mode for each request. Task or task chain are executed at request order
- 8 scatter group(sg) are supported for both input and output data
- DMA has multiple channel, each corresponding to one suit of algorithms

2.2.4.11. Embedded Crypto Engine(EMCE)

- Connects directly to SMHC or NDFC for disc encryption application
- Supports AES algorithm
- Supports 128-bit, 192-bit and 256-bit key size for AES
- Supports ECB, CBC,XTS modes

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2.2.4.12. Security ID(SID)

- Supports 4K-bit EFUSE for chip ID and security application

2.2.4.13. CPU Configuration

- Capable of CPU reset, including core reset, debug circuit reset, etc
- Capable of other CPU-related control, including interface control, CP15 control, and power control, etc
- Capable of checking CPU status, including idle status, SMP status, and interrupt status, etc

2.2.5. Display Subsystem

2.2.5.1. DE3.0

- Output size up to 4096x4096
- Supports four alpha blending channels for main display, two channels for aux display
- Supports four overlay layers in each channel, and has an independent scaler
- Supports potter-duff compatible blending operation
- Supports input format semi-planar of YUV422/YUV420/YUV411/P010/P210 and planar of YUV422/YUV420/YUV411, ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/RGB565
- Supports Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-side Half 3D format data
- Supports 10-bit processing path for HDR video
- Supports HDR-to-SDR and HLG-to-HDR conversion for HDR video and SDR-to-HDR conversion for SDR UI
- Supports SmartColor 3.0 for excellent display experience
  - Supports high quality video scaler with edge pattern detection
  - Adaptive detail/edge enhancement
  - Adaptive color enhancement
  - Adaptive contrast enhancement and fresh tone rectify
  - Adaptive de-noising with image quality assessment and block detector function
- Supports 3-D de-interlacer with low angle interpolation
- Supports writeback for high efficient dual display and miracast

2.2.5.2. Display Output

- Supports HDMI2.0a output
  - Up to 4K@60fps resolution
  - Compatible with HDCP 2.2 for HDMI
  - Integrated CEC hardware
  - Supports HDMI and LCD display output at the same time
  - Supports HDMI 3D display
  - Supports 8/10-bit color depth
  - Supports HDCP1.4

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  - Supports output format: RGB, YUV444, YUV422, YUV420
  - Supports HDR
- Supports TV Encoder
  - System resources is controlled by ATE
  - Supports CCIR656 and Serial YUV interface
  - 1 CVBS out, supports NTSC and PAL
  - Plug status auto detecting
- Supports RGB LCD interface with DE/SYNC mode
  - Up to 1920x1080@60fps resolution
  - 18-bit data bus
  - Supports RGB666/RGB656 dither function

2.2.6. Video Engine

2.2.6.1. Video Decoder

- Supports multi-format video playback, including:
  - H.265 Main10/L5.1: 4K@60fps
  - H.264 BP/MP/HP Level4.2: 4K@30fps
  - H.263 BP: 1080p@60fps
  - MPEG1 MP/HL: 1080p@60fps
  - MPEG2 MP/HL: 1080p@60fps
  - MPEG4 SP/ASP L5: 1080p@60fps
  - Sorenson Spark: 1080p@60fps
  - VP8 N/A: 1080p@60fps
  - VP9:Profile 0/2 4K@30fps
  - VC1 SP/MP/AP: 1080p@60fps
  - AVS-P2/AVS-P16(AVS+) jizhun : 1080p@60fps
  - Xvid N/A: 1080p@60fps
- Supports 1080p blu-ray 3D
- Supports 3D size:3840x1080,1920x2160
- Supports decoding output format: T32 x 32, YV12, NV12, NV21, and HEVC also supports afbc

2.2.6.2. Video Encoder

- Supports H.264 BP/MP/HP video encoder up to 1080p@60fps
- Supports JPEG@4080x4080 video encoder
- Supports input picture size up to 4800x4800
- Supports input format: tiled (128x32)/YU12/YV12/NU12/NV12/ARGB/YUYV
- Supports Alpha blending
- Supports thumb generation
- Supports 4x2 scaling ratio: from 1/16 to 64 arbitrary non-integer ratio
- Supports rotated input

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2.2.7. Image Subsystem

2.2.7.1. CSI

- Support 8/10bit digital camera interface
- Support BT656 interface
- Support ITU-R BT.656 time-multiplexed format
- Maximum still capture resolution for parallel interface to 5M
- Maximum video capture resolution for parallel interface to 1080p@30fps
- Maximum pixel clock for parallel to 148.5MHz

2.2.8. Audio Subsystem

2.2.8.1. Audio Hub

- Concurrent switching between audio clients
  - The audio clients are I2S/PCM, DAM and APBIF
  - A TX client can talk to multiple RX clients simultaneously
  - A RX client can only talk to one TX clients
- Scalable MxN crossbar switch, where
  - M is the number of TX clients
  - N is the number of RX clients
- Supports three 64x32bit TX streams FIFO and three 128x32bit RX streams FIFO for APB DMA operations
- Supports two DAM(Digital Audio Mixer) interface, one I2S/PCM interface for HDMI ,one I2S/PCM interface for Audio Codec

2.2.8.2. I2S/PCM

- Up to 4 I2S/PCM controllers
- One controller for HDMI, one controller for Audio Codec,others for digital audio mixer application
- Compliant with standard Philips Inter-IC sound (I2S) bus specification
- Compliant with Left-justified, Right-justified, PCM mode, and TDM (Time Division Multiplexing) format
- Supports full-duplex synchronous work mode
- Supports Master/Slave mode
- Supports clock up to 24.576MHz
- Supports adjustable audio sample resolution from 8-bit to 32-bit
- Supports 8-bit u-law and 8-bit A-law companded sample
- One 128 depth x 32-bit width TXFIFO for data transmit, one 64 depth x 32-bit width RXFIFO for data receive
- Supports programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Programmable FIFO thresholds

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2.2.8.3. One Wire Audio(OWA)

- IEC-60958 transmitter and receiver functionality
- Compatible with S/PDIF interface
- Supports channel status insertion for the transmitter
- Supports channel status capture on the receiver
- Hardware Parity generation on the transmitter
- Hardware Parity checking on the receiver
- One 128 x 24 bits TX FIFO and one 64 x 24 bits RXFIFO for audio data transfer
- Programmable FIFO thresholds
- Supports 16-bit,20-bit and 24-bit data formats

2.2.8.4. DMIC

- Up to 8 channels
- Supports maximum 8 digital microphones
- Supports sample rate from 8 kHz to 48 kHz

2.2.8.5. Audio Codec

- System resources are controlled by ATE
- Two audio digital-to-analog(DAC) channels
  - 100dB SNR@A-weight
  - Supports DAC Sample Rates from 8kHz to 192kHz
- Supports analog/digital volume control
- Two differential microphone inputs
- One lineout output with voltage ramp
- Two audio analog-to-digital(ADC) channels
  - 92dB SNR@A-weight
  - Supports ADC Sample Rates from 8kHz to 48kHz
- Supports Automatic Gain Control(AGC) adjusting the ADC recording output

2.2.9. Security Processing

- Full Disk Encryption(FDE), supports AES-ECB/CBC
- 4K bits Efuse(OTP)
- Protection for JTAG and other debugging port
- HDCP 2.2/1.4 protection for HDMI outputs
- Trusted execution environment(TEE)
- Digital rights management(DRM)
- Mainstream advanced CA
- Secure boot
- Secure Storage

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- Secure upgrade
- Transparent RAM scrambling
- Hardware TRNG

2.2.10. External Peripherals

2.2.10.1. USB

- One USB 2.0 OTG
  - Complies with USB2.0 Specification
  - Supports High-Speed (HS,480 Mbps),Full-Speed(FS,12 Mbps) and Low-Speed(LS,1.5 Mbps) in host mode
  - Supports High-Speed (HS,480 Mbps),Full-Speed(FS,12 Mbps) in device mode
  - Complies with Enhanced Host Controller Interface(EHCI)Specification, Version 1.0, and the Open Host Controller Interface(OHCI) Specification, Version 1.0a for host mode
  - Up to 8 User-Configurable Endpoints for Bulk, Isochronous and Interrupt bi-directional transfers (Endpoint1, Endpoint2, Endpoint3, Endpoint4)
  - Supports (4KB+64Bytes) FIFO for EPs(including EP0)
  - Supports point-to-point and point-to-multipoint transfer in both host and peripheral mode
- One USB 2.0 Host
  - Supports High-Speed (HS,480 Mbps),Full-Speed(FS,12 Mbps) and Low-Speed(LS,1.5 Mbps) device
  - Compatible with Enhanced Host Controller Interface(EHCI)Specification, Version 1.0, and the Open Host Controller Interface(OHCI) Specification, Version 1.0a.
- One USB 3.0 Host
  - Supports Super-Speed(SS,5 Gbps),High-Speed (HS,480 Mbps),Full-Speed(FS,12 Mbps) and Low-Speed(LS,1.5 Mbps) in host mode
  - USB3.0 PIPE3 PHY interface
  - USB 2.0 UTMI+(L3) PHY interface
  - Simultaneous IN and OUT transfer support in superspeed mode

2.2.10.2. UART

- Up to 5 UART controllers
- Two of 5 UART controllers support 2-wire while others support 4-wire
- Compatible with industry-standard 16550 UARTs
- 256-Bytes Transmit and Receive data FIFOs
- Capable of speed up to 5Mbps
- Supports 5-8 data bits and 1/1.5/2 stop bits
- Supports Even, Odd or No Parity
- Supports DMA controller interface
- Supports Software/ Hardware Flow Control
- Supports IrDA 1.0 SIR
- Supports RS-485/9-bit mode

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2.2.10.3. SPI

- Up to 2 SPI controllers
- Full-duplex synchronous serial interface
- 5 clock sources
- Master/Slave configurable
- Four chip selects to support multiple peripherals
- 8-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable
- Interrupt or DMA support
- Support 3-Wire/4-Wire SPI
- Support programmable serial data frame length: 0bit to 32bits
- Support Standard SPI,Dual-Output/Dual-Input SPI, Quad-Output/Quad-Input SPI

2.2.10.4. TWI

- Up to 4 TWI(Two Wire Interface) controllers
- Software-programmable for slave or master
- Supports repeated START signal
- Multi-master systems supported
- Allows 10-bit addressing with TWI bus
- Performs arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Supports speed up to 400 Kbit/s (‘fast mode’)
- Allows operation from a wide range of input clock frequency

2.2.10.5. TSC

- Up to 4 TS controllers
- Supports SPI/SSI interface,interface timing parameters are configurable
- 32 channels PID filter for each TSF
- Multiple transport stream packet (188, 192, 204) format support
- Hardware packet synchronous byte error detecting
- Hardware PCR packet detecting
- 64x16-bits FIFO for TSG, 64x32-bits FIFO for TSF
- Configurable SPI transport stream generator for streams in DRAM memory
- Supports DVB-CSA V1.1, DVB-CSA V2.1 Descrambler

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2.2.10.6. SCR

- Up to 2 SCR(Smart Card Reader) controllers
- Supports APB slave interface for easy integration with AMBA-based host systems
- Supports the ISO/IEC 7816-3:1997(E) and EMV2000 (4.0) Specifications
- Supports adjustable clock rate and bit rate
- Configurable automatic byte repetition
- Supports asynchronous half-duplex character transmission and block transmission
- Supports synchronous and any other non-ISO 7816 and non-EMV cards
- Performs functions needed for complete smart card sessions, including:
  - Card activation and deactivation
  - Cold/warm reset
  - Answer to Reset (ATR) response reception
  - Data transfers to and from the card

2.2.10.7. EMAC

- Compliant with the IEEE 802.3-2002 standard
- Supports 10/100/1000-Mbps data transfer rates
- Supports RMII/RGMII PHY interface
- Supports a variety of flexible address filtering modes
- Supports full and half duplex operations
- Programmable frame length to support Standard or Jumbo Ethernet frames with size up to 16KB
- Supports linked-list descriptor list structure
- 4KB TXFIFO for transmission packets and 16KB RXFIFO for reception packets

2.2.10.8. EPHY

- System resources are controlled by ATE
- Fully IEEE 802.3 10/100 Base-TX compliant and supports EEE
- Auto negotiation and parallel detection capability for automatic speed and duplex selection
- Programmable loopback mode for diagnostic
- Supports WOL (Wake-On-Lan) functionality
- Design for Testability with extensive testability feature and 95% fault coverage
- Power consumption (100Base-TX) less than 140mW

2.2.10.9. PCIe

- Complies with PCI Express Base 2.0 Specification
- Embedded PCI Express PHY,supports x1 Gen2(5.0 Gbps) lane
- Only supports Root Complex(RC) mode
- Maximum payload size: 256 bytes
- Supports 2 Inbound windows and 2 Outbound windows

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2.2.10.10. CIR Transmitter

- Supports arbitrary wave generator
- Configurable carrier frequency
- 128 bytes FIFO for data buffer
- Interrupt and DMA supported

2.2.10.11. CIR Receiver

- Flexible receiver for consumer IR remote control
- Programmable FIFO thresholds
- 64x8 bits FIFO for data buffer
- Sample clock up to 1MHz

2.2.10.12. One Wire

- Hardware implement of 1-wire protocol
- Supports master function
- Supports simple mode and standard mode

2.2.11. Package

- FBGA 451 balls, 0.65mm ball pitch, 15mm x 15mm

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2.3. System Block Diagram

Figure 2-1 shows the block diagram of H6 V200 processor.

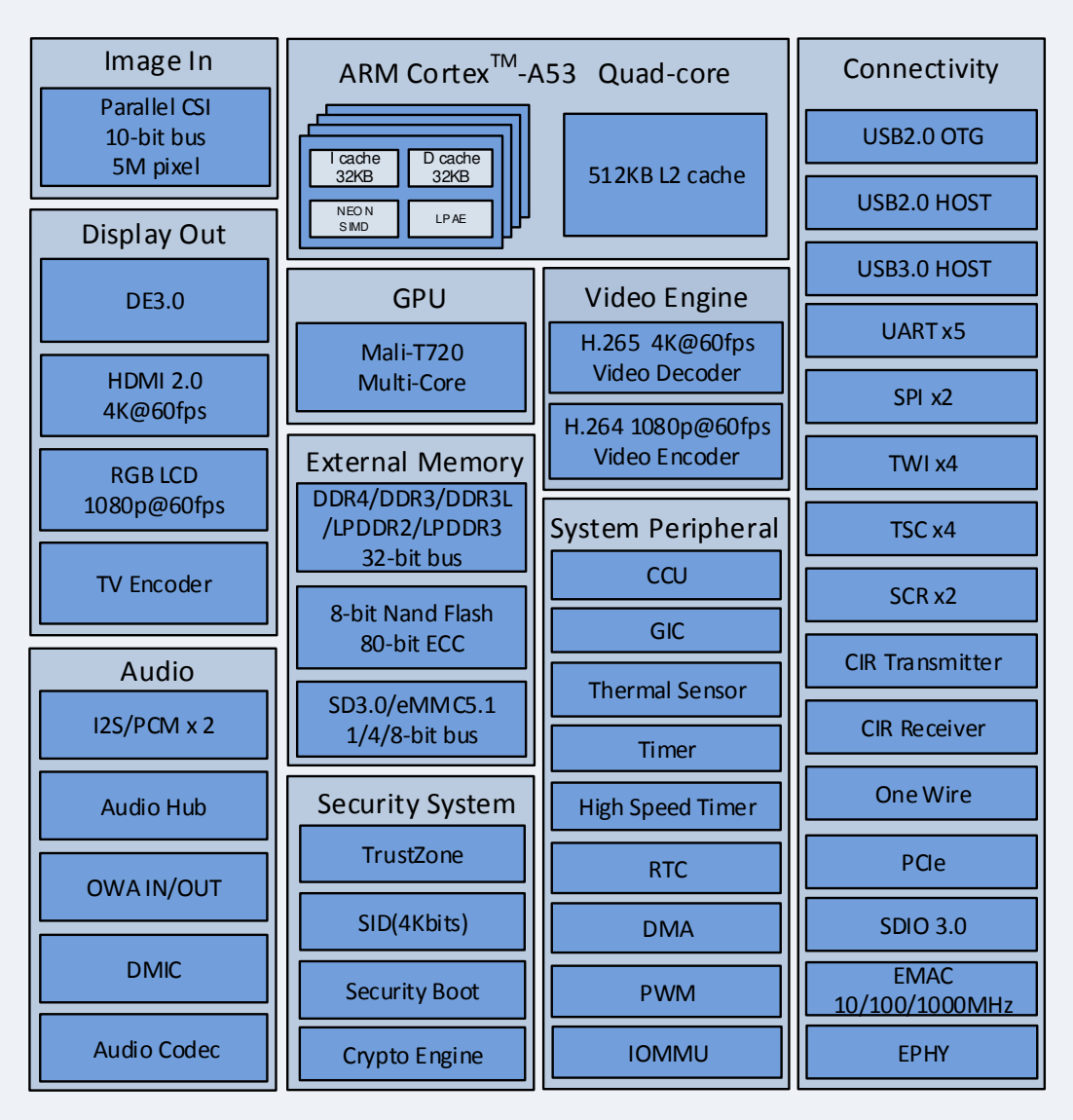


Figure 2-1. H6 V200 Block Diagram

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Chapter 3 System

The chapter describes the H6 V200 system from following sections:

- Memory Mapping
- Boot System
- CCU
- CPUX Configuration
- IOMMU
- System Configuration
- Timer
- High Speed Timer
- PWM
- DMA
- GIC
- Message Box
- Spinlock
- Crypto Engine
- Embedded Crypto Engine
- Security ID
- Thermal Sensor Controller
- RTC
- PSI
- ATE Controller
- Port Controller(CPUX-PORT)
- Port Controller(CPUS-PORT)

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3.1. Memory Mapping

Module	Address(It is for Cluster CPU)	Size(Bytes)
N-BROM	0x0000 0000—0x0000 9FFF	40K
S-BROM	0x0000 0000—0x0000 FFFF	64K
SRAM A1	0x0002 0000---0x0002 7FFF	32K
SRAM C	0x0002 8000---0x0004 5FFF	120K
SRAM A2	0x0010 0000---0x0010 3FFF	16K
	0x0010 4000---0x0011 7FFF	80K
DE	0x0100 0000---0x013F FFFF	4M
DI0	0x0142 0000---0x0143 FFFF	128K
GPU	0x0180 0000---0x0183 FFFF	256K
CE_NS	0x0190 4000---0x0190 47FF	2K
CE_S	0x0190 4800---0x0190 4FFF	2K
EMCE	0x0190 5000---0x0190 5FFF	4K
CE_KEY_SRAM	0x0190 8000---0x0190 8FFF	4K
VE SRAM	0x01A0 0000---0x01BF FFFF	2M
VP9	0x01C0 0000---0x01C0 0FFF	4K
VE	0x01C0 E000---0x01C0 FFFF	8K
SYS_CFG	0x0300 0000---0x0300 0FFF	4K
CCU	0x0300 1000---0x0300 1FFF	4K
DMAC	0x0300 2000---0x0300 2FFF	4K
MSGBOX	0x0300 3000---0x0300 3FFF	4K
SPINLOCK	0x0300 4000---0x0300 4FFF	4K
HSTIMER	0x0300 5000---0x0300 5FFF	4K
SID	0x0300 6000---0x0300 6FFF	4K
TIMER	0x0300 9000---0x0300 93FF	1K
PWM	0x0300 A000---0x0300 A3FF	1K
GPIO	0x0300 B000---0x0300 B3FF	1K
PSI	0x0300 C000---0x0300 C3FF	1K
DCU	0x0301 0000---0x0301 FFFF	64K
GIC	0x0302 0000---0x0302 FFFF	64K
IOMMU	0x030F 0000---0x030F FFFF	64K
DRAM_CTRL	0x0400 2000---0x0400 5FFF	16K
NAND0	0x0401 1000---0x0401 1FFF	4K
SMHC0	0x0402 0000---0x0402 0FFF	4K
SMHC1	0x0402 1000---0x0402 1FFF	4K
SMHC2	0x0402 2000---0x0402 2FFF	4K
UART0	0x0500 0000---0x0500 03FF	1K
UART1	0x0500 0400---0x0500 07FF	1K
UART2	0x0500 0800---0x0500 0BFF	1K

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UART3	0x0500 0C00---0x0500 0FFF	1K
TWI0	0x0500 2000---0x0500 23FF	1K
TWI1	0x0500 2400---0x0500 27FF	1K
TWI2	0x0500 2800---0x0500 2BFF	1K
TWI3	0x0500 2C00---0x0500 2FFF	1K
SCR0	0x0500 5000---0x0500 53FF	1K
SCR1	0x0500 5400---0x0500 57FF	1K
SPI0	0x0501 0000---0x0501 0FFF	4K
SPI1	0x0501 1000---0x0501 1FFF	4K
EMAC	0x0502 0000---0x0502 FFFF	64K
TS0	0x0506 0000---0x0506 0FFF	4K
THS	0x0507 0400---0x0507 07FF	1K
CIR_TX	0x0507 1000---0x0507 13FF	1K
I2S/PCM3	0x0508 F000---0x0508 FFFF	4K
I2S/PCM0	0x0509 0000---0x0509 0FFF	4K
I2S/PCM1	0x0509 1000---0x0509 1FFF	4K
I2S/PCM2	0x0509 2000---0x0509 2FFF	4K
OWA	0x0509 3000---0x0509 33FF	1K
DMIC	0x0509 5000---0x0509 53FF	1K
Audio HUB	0x0509 7000---0x0509 7FFF	4K
USB0(USB2.0_OTG)	0x0510 0000---0x051F FFFF	1M
USB1(USB3.0_HOST)	0x0520 0000---0x052F FFFF	1M
USB3(USB2.0_HOST)	0x0531 1000---0x0531 1FFF	4K
PCIe	0x0540 0000---0x054F FFFF	1M
HDMI_TX0(1.4/2.0)	0x0600 0000---0x060F FFFF	1M
DISP_IF_TOP	0x0651 0000---0x0651 0FFF	4K
TCON_LCD	0x0651 1000---0x0651 1FFF	4K
TCON_TV	0x0651 5000---0x0651 5FFF	4K
CSI_SRAM	0x0660 0000---0x0661 FFFF	128K
CSI	0x0662 0000---0x0663 FFFF	128K
RTC	0x0700 0000---0x0700 03FF	1K
R_CPUS_CFG	0x0700 0400---0x0700 0BFF	2K
R_PRCM	0x0701 0000---0x0701 03FF	1K
R_TIMER	0x0702 0000---0x0702 03FF	1K
R_WDOG	0x0702 0400---0x0702 07FF	1K
R_TWDOG	0x0702 0800---0x0702 0BFF	1K
R_PWM	0x0702 0C00---0x0702 0FFF	1K
R_INTC	0x0702 1000---0x0702 13FF	1K
R_GPIO	0x0702 2000---0x0702 23FF	1K
R_CIR_RX	0x0704 0000---0x0704 03FF	1K
R_OWC	0x0704 0400---0x0704 07FF	1K
R_UART	0x0708 0000---0x0708 03FF	1K
R_TWI	0x0708 1400---0x0708 17FF	1K
CPU_SYS_CFG	0x0810 0000---0x0810 03FF	1K

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CNT_R	0x0811 0000---0x0811 0FFF	4K
CNT_C	0x0812 0000---0x0812 0FFF	4K
C0_CPUX_CFG	0x0901 0000---0x0901 0FFF	4K
C0_CPUX_MBIST	0x0902 0000---0x0902 0FFF	4K
DRAM SPACE	0x4000 0000---0xFFFF FFFF	3G

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3.2. Boot System

3.2.1. Overview

The H6 V200 system has several ways to boot. It has an integrated the on-chip Boot ROM (BROM) which could be considered the primary program-loader. On startup, H6 V200 starts to fetch the first instruction from address 0x0, where is the BROM located at.

The Boot system is split up into two parts :FEL and Media Boot. The task of FEL is to write the external data to the local NVM,the task of the Media Boot is to loaded from NVM an effective and legitimate BOOT0 up and running.

The Boot System includes the following features:

- Supports CPU0 Boot Process and NON_CPU0 Boot Process
- Supports Super Standby Wakeup Process
- Supports Hotplug Process
- Supports Mandatory Upgrade Process through SDC0 and USB
- Supports GPIO Pin or eFuse to select the kind of boot media to boot
- Supports Normal Boot and Secure Boot
- Supports loads only certified firmware for Secure Boot
- Ensures that the Secure Boot is a trusted environment

3.2.2. Operations and Functional Descriptions

3.2.2.1. BROM System Security Setting

If the H6 V200 has implemented the ARM TrustZone technology,when the Secure Enable Bit is enabled,the H6 V200 will enable the the ARM TrustZone technology.

So the BROM is divided into Normal BROM and Secure BROM. The Secure BROM protects against the potential threat of attackers modifying areas of code or data in programmable memory .

On startup,the H6 V200 will read the Secure Enable Bit,if the bit is 0,then mapping Normal Brom code to address 0x0, or mapping Secure Brom code to address 0x0.

3.2.2.2. Boot Select Description

The BROM system supports the following boot media:

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- SD/MMC
- NAND FLASH
- SPI NOR FLASH

There are two ways of Boot Select:GPIO Pin Select and eFuse Select. The BROM will read the state of BOOT_MODE , according to the state of BOOT_MODE to decide whether GPIO pin or eFuse to select the kind of boot media to boot. The BOOT_MODE is actually a bit in the SID. Table 3-1 shows BOOT_MODE Setting.

Table 3-1.BOOT_MODE Setting

BOOT_MODE[0]	Boot Select Type
0	GPIO Pin Select
1	eFuse Select

If the state of the BOOT_MODE is 0,that is to choose the GPIO Pin ,which has two pins to select which boot media to boot.Table 3-2 shows GPIO Pin Boot Select Setting.

Table 3-2. GPIO Pin Boot Select Setting

Pin_Boot_Select[0]	Boot media
0	SMHC0->NAND FLASH->SMHC2->SPI_NOR
1	SMHC0->SMHC2->NAND FLASH->SPI_NOR

If the state of the BOOT_MODE is 1,that is to choose the eFuse .eFuse select has 12 bits,so each of the 3 bits is divided into a group of the Boot Select ,so it has four groups of boot_select .Table 3-3 shows eFuse Boot Select Configure.

Table 3-3. eFuse Boot Select Configure

eFuse_Boot_Select_Cfg[11:0]	Description
eFuse_Boot_Select[2:0]	eFuse_Boot_Select_1
eFuse_Boot_Select[5:3]	eFuse_Boot_Select_2
eFuse_Boot_Select[8:6]	eFuse_Boot_Select_3
eFuse_Boot_Select[11:9]	eFuse_Boot_Select_4

Table 3-4 describes each group of the eFuse Boot select settings. The first group to the third group are the same settings,but the fourth group need to be careful.If eFuse_Boot_Select_4 is set to 111,that means the way of the *Try*.The way of *Try* is followed by SMHC0,SMHC2,NAND FLASH,SPI NOR FLASH.

Table 3-4. eFuse Boot Select Setting

eFuse_Boot_Select_n	Boot media
000	Try
001	NAND
010	SMHC2
011	SPI NOR FLASH

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100	Reserved
101	Reserved
110	Reserved
111	The next group of the eFuse_Boot_Select,when the n is equal to 4,it will be a way of *Try*.

3.2.2.3. BROM System Description

3.2.2.3.1. Normal BROM Process

In Normal boot mode,the system boot will start from CPU0 or NON_CPU0, BROM will read CPU ID number to distinguish CPU0 or NON_CPU0,then BROM will read the **Hotplug Flag Regsiter** and the **Supper Standby Flag Regsiter** ,according to the flag whether to go through the appropriate process.Finally,BROM will read the state of the FEL Pin,if the FEL Pin signal is detected to pull to high level, then the system will jump to the Try Media Boot process,or jump to the mandatory upgrade process. Figure 3-1 shows the Normal BROM Process.

 **NOTE**

NON_CPU0 means the CPU core n(n>0).

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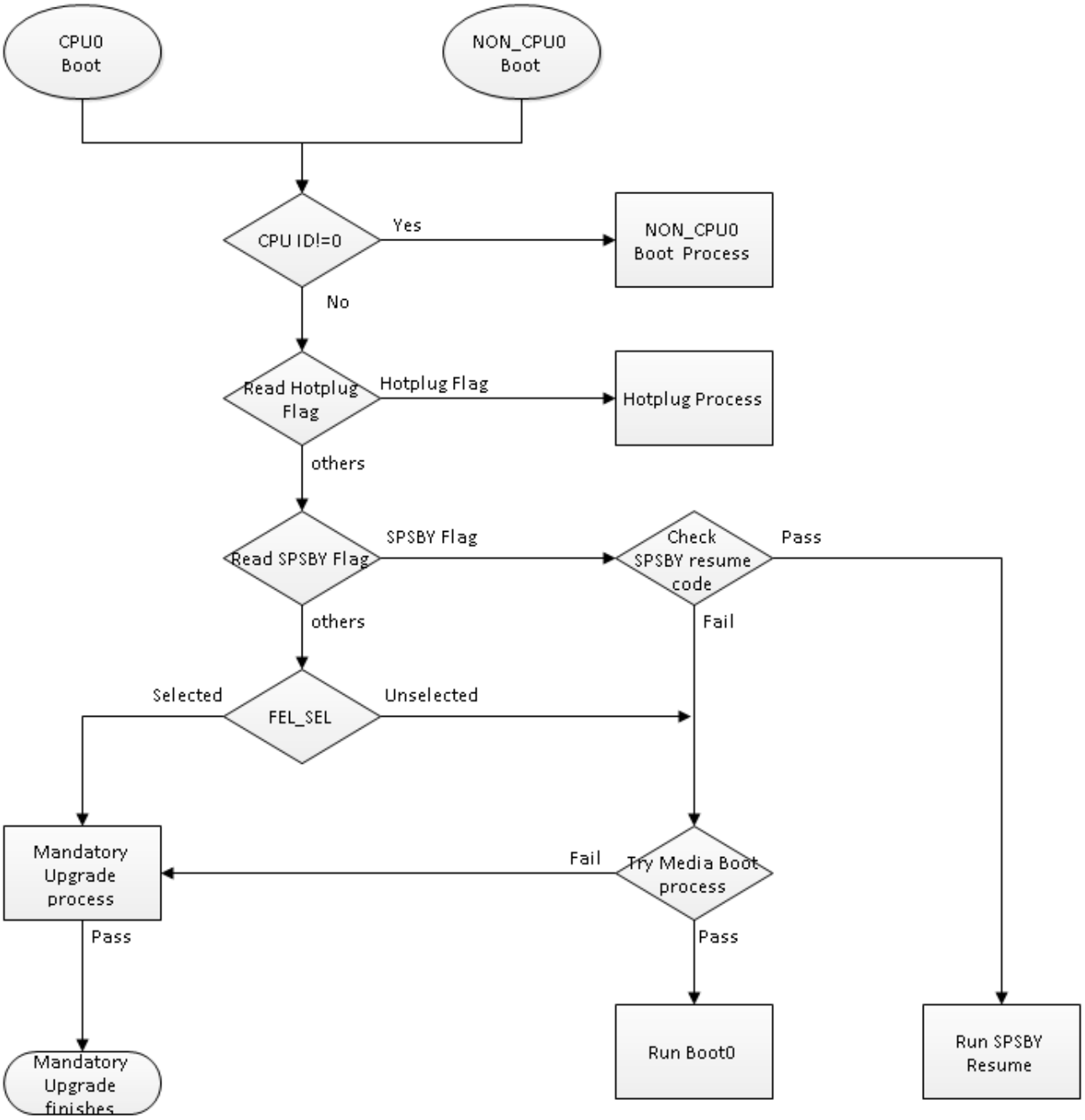


Figure 3-1. Normal Mode Boot Process

3.2.2.3.2. Secure BROM Process

In Security Boot mode, after the fast boot process finishes, the system will go to run Security BROM software. Figure 3-2 shows the Secure BROM Process.

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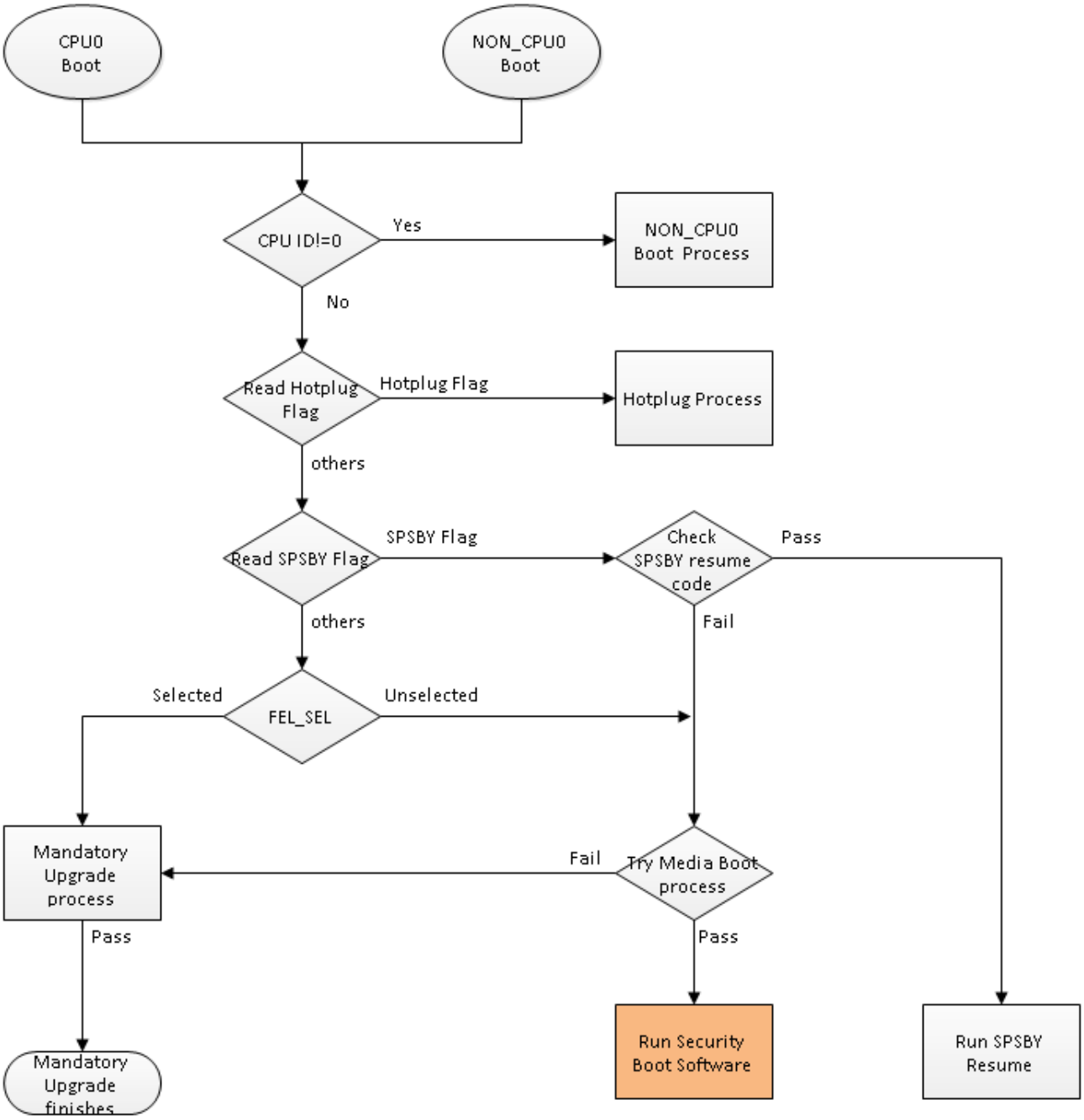


Figure 3-2. Security Mode Boot Process

The Secure BROM includes the following features:

- Supports X509 certificate
- Supports cryptographic algorithms: AES128,SHA256,RSA2048,DES
- Supports OTP/eFuse

Before runing Security Boot software ,the software must check whether it has been modified or replaced,so the system will check verify the integrity of the certificate,because the certificate has been using the RSA algorithm signature.The system also uses the Crypto Engine (CE) hardware module to accelerate the speed of encryption and decryption.Accordding to using standard cryptography to ensure that the firmware images can be trusted,so the Secure BROM ensure the system security state is as expected.

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3.2.2.3.3. NON_CPU0 Boot Process

If CPU ID is greater than 0,the system boot from boot from NON_CPU0,BROM will read the Soft Entry Address Register,then jump the Soft Entry Address,and run NON_CPU0 boot code. Figure 3-3 shows the NON_CPU0 Boot Process.

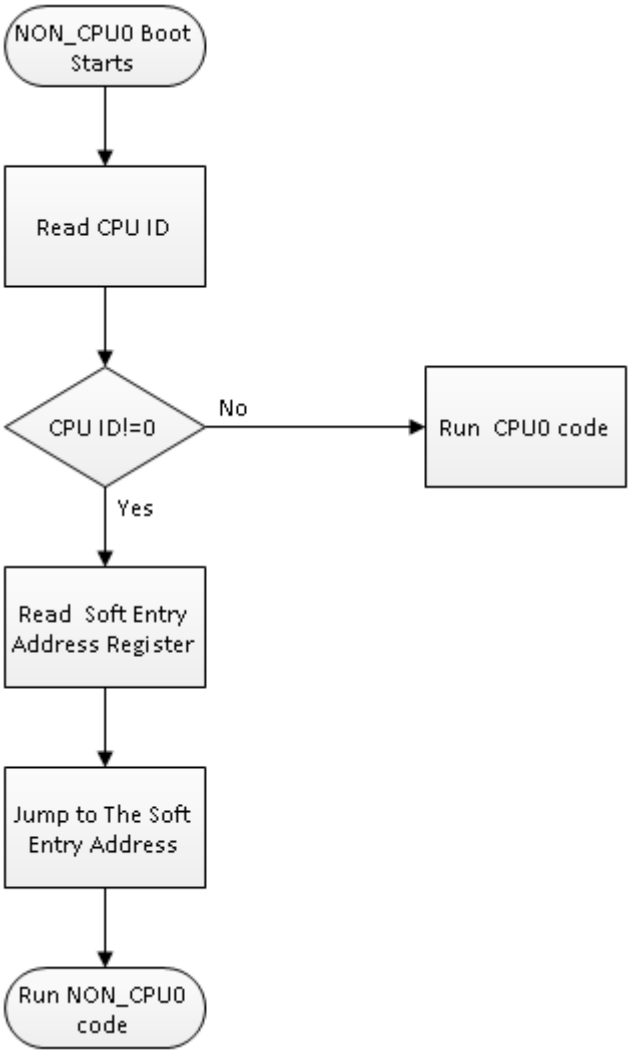


Figure 3-3. CPU-0+ Boot Process

NOTE

The Soft Entry Address Register is 0x070001BC.

3.2.2.4. CPU0 Hot Plug Process

The Hot Plug flag determines whether the system will do hotplug boot. If CPU Hotplug Flag value is equal to

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0×FA50392F, then read the Soft Entry Register and the system will jump to the Soft Entry Address. Figure 3-4 shows the CPU0 Hotplug Process.

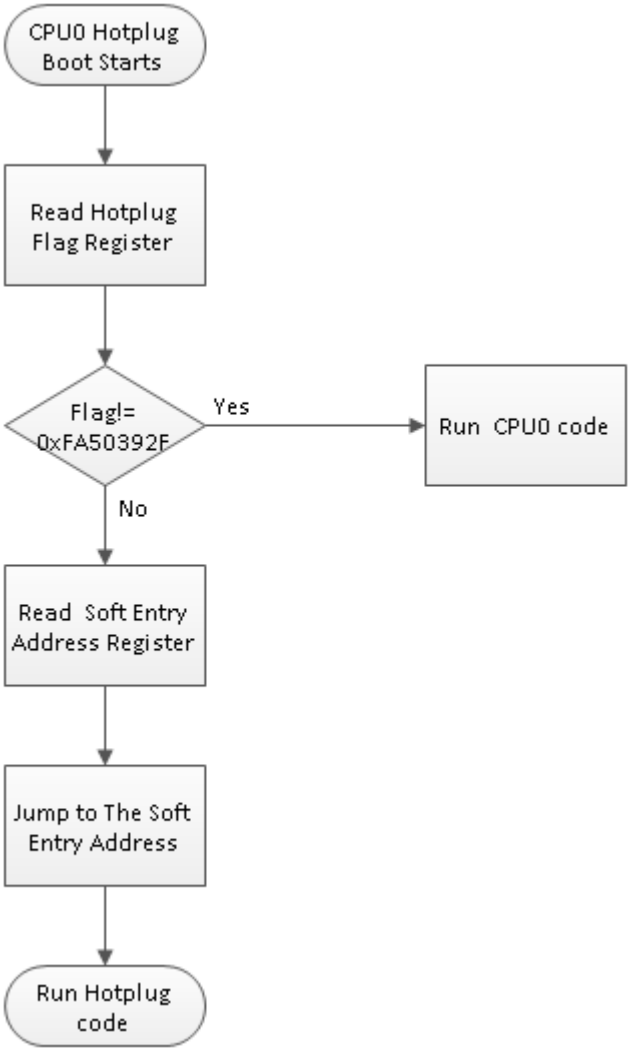


Figure 3-4. CPU0 Hot Plug Process

NOTE

The Hotplug Flag Register is 0x070001B8. The Soft Entry Address Register is 0x070001BC.

3.2.2.5. Super Standby Wakeup Process

Super Standby(SPSBY) wakeup will be started by CPUS, and will be carried on by CPU0 after the CPU0 released. If the SPSBY register value is checked to be the SPSBY flag, then the system will go to SPSBY wakeup process.Figure 3-5 shows the SPSBY Wakeup Process.

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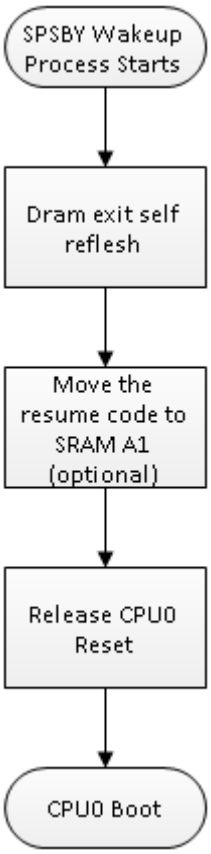


Figure 3-5. SPSBY Wakeup Process

During the SPSBY wakeup, the system will first check the SPSBY resume code pointed by SPSBY resume code pointer.If it is right, then the system will run SPSBY wakeup, otherwise the system will jump to the Try Media Boot process.Figure 3-6 shows the SPSBY Resume Code Check Process.

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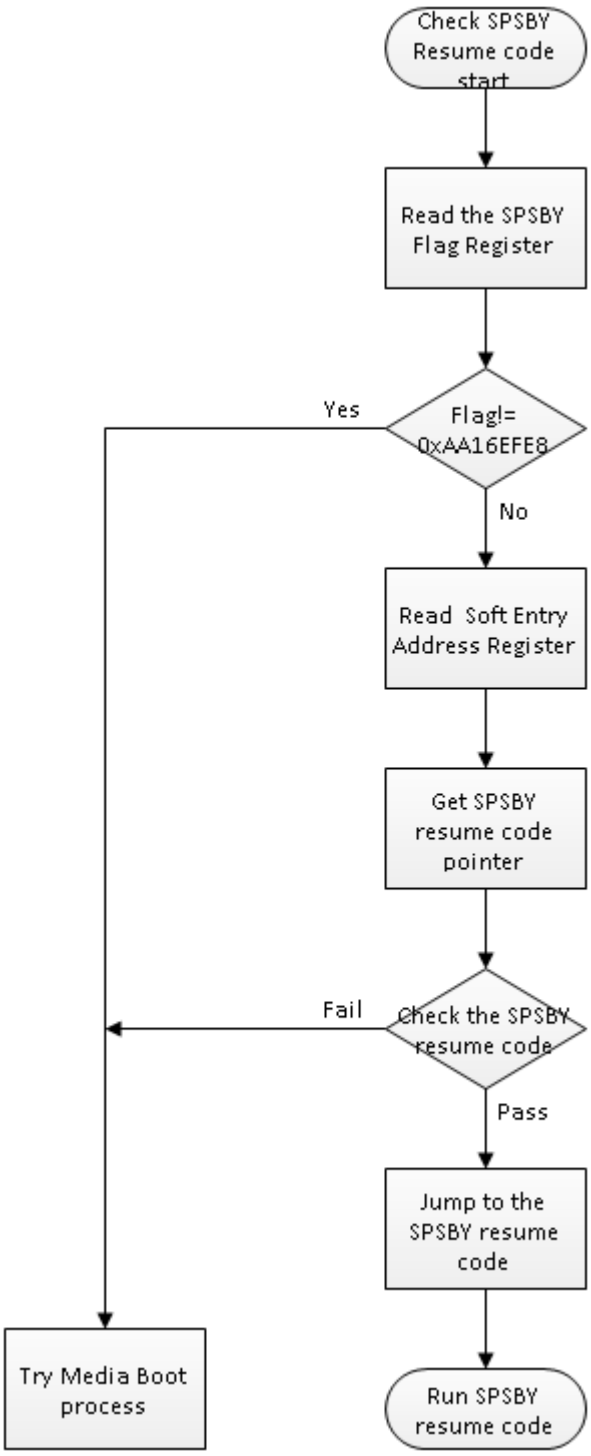


Figure 3-6. SPSBY Resume Code Check Process

3.2.2.6. Mandatory Upgrade Process

If the FEL Pin signal is detected to pull low, then the system will jump to mandatory upgrade process. Figure 3-7 shows the mandatory upgrade process.

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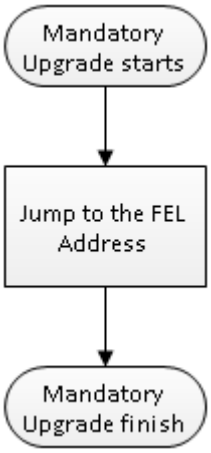


Figure 3-7. Mandatory Upgrade Process

NOTE

The FEL address of the Normal BROM is 0x20. The FEL address of the Secure BROM is 0x64.

3.2.2.7. FEL Process

When the system chooses to enter Mandatory Upgrade Process,then jump to the FEL Process.Figure 3-8 shows the FEL process.

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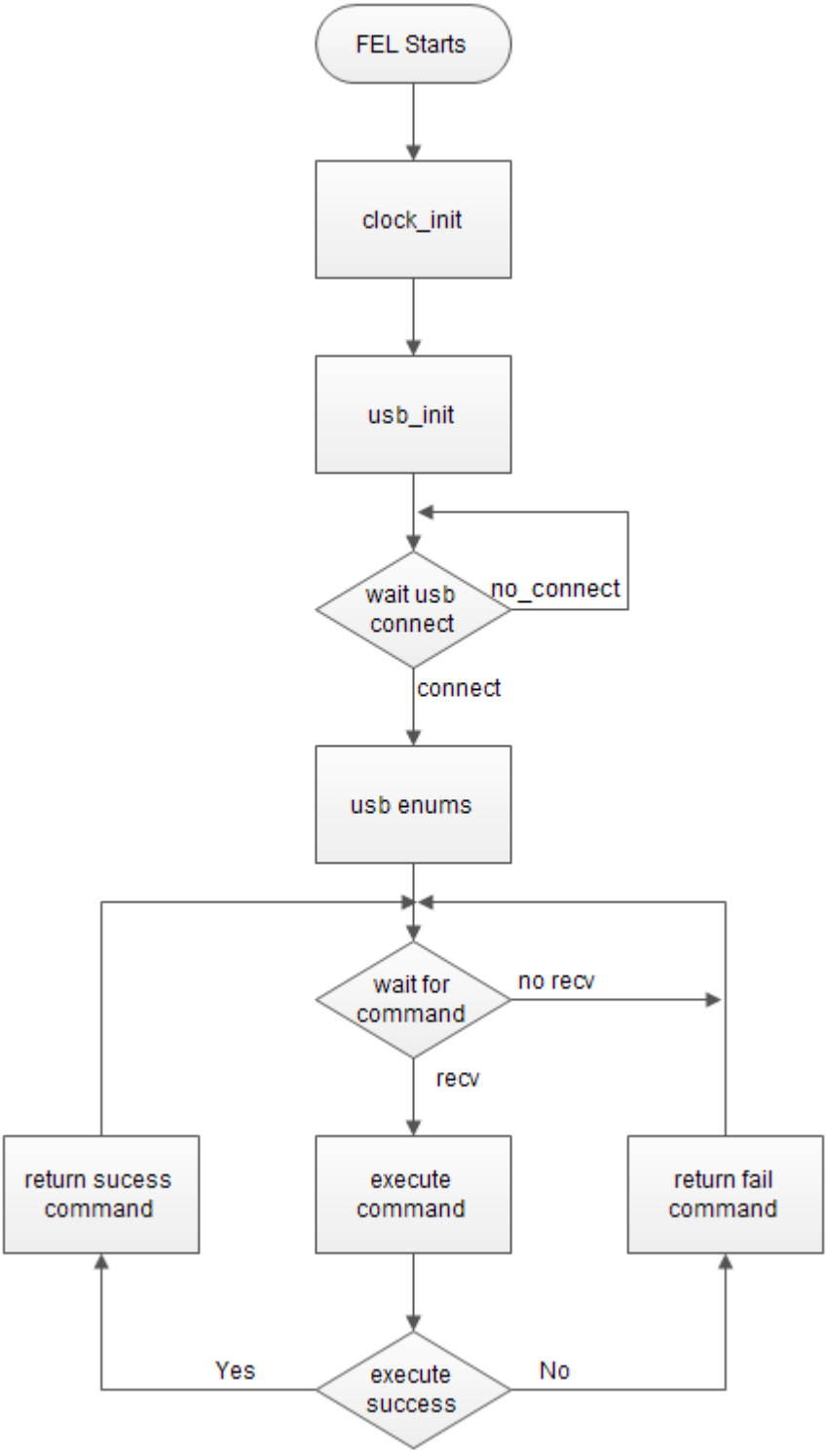


Figure 3-8. USB FEL Process

3.2.2.8. Normal Try Media Boot Process

If the FEL Pin signal is detected to pulled to high level, then the system will jump to the Try Media Boot process.

Try Media Boot Process will read the state of BOOT_MODE register,according to the state of BOOT_MODE, GPIO pin or Efuse is descided to select which boot media to boot.Figure 3-9 shows Normal BROM GPIO Pin Boot Select Process.

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NOTE

SMHC0 is external SD/TF card. SMHC2 is external eMMC.

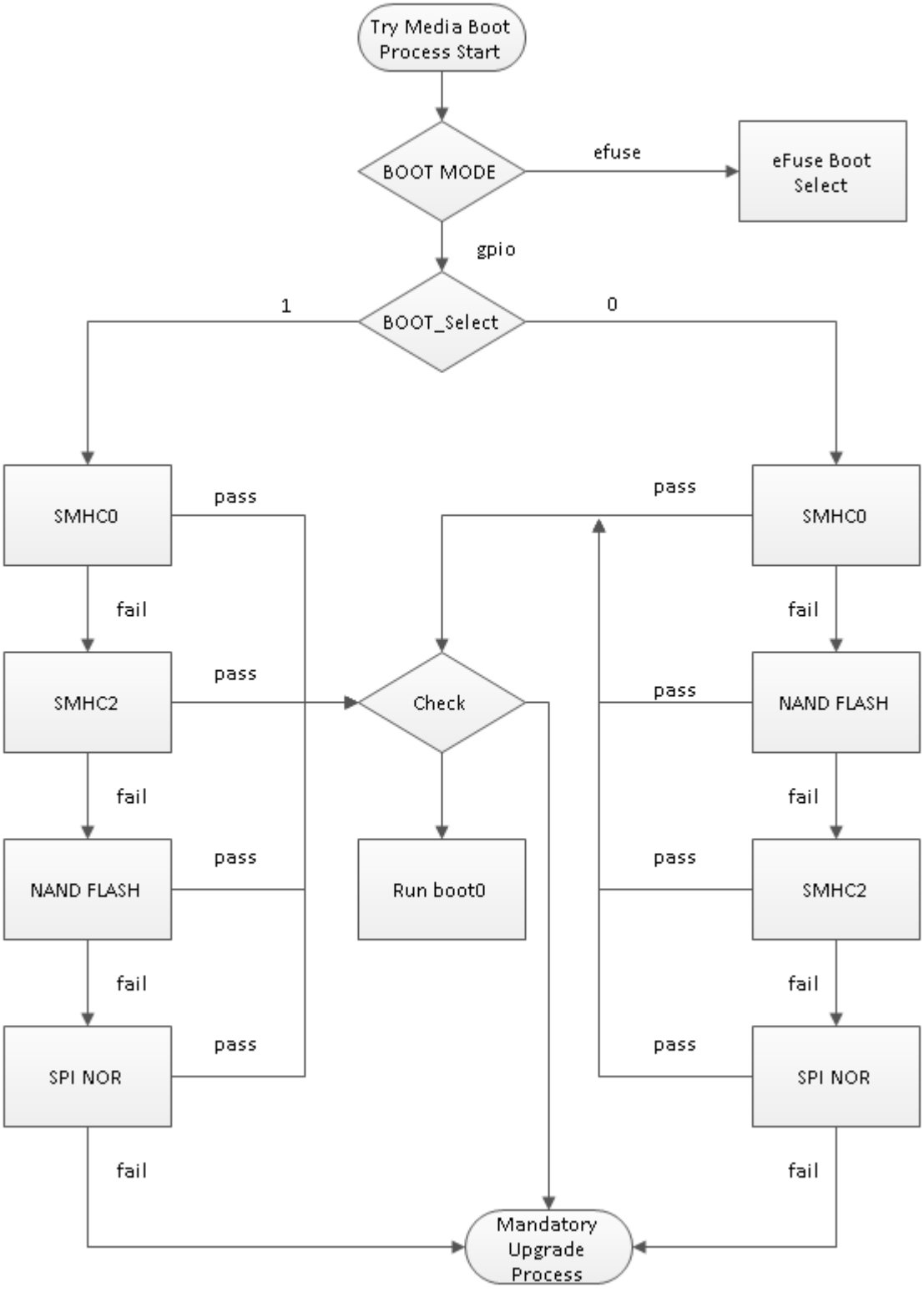


Figure 3-9. GPIO Pin Boot Select Process

Figure 3-10 shows Normal BROM eFuse Boot Select Process.

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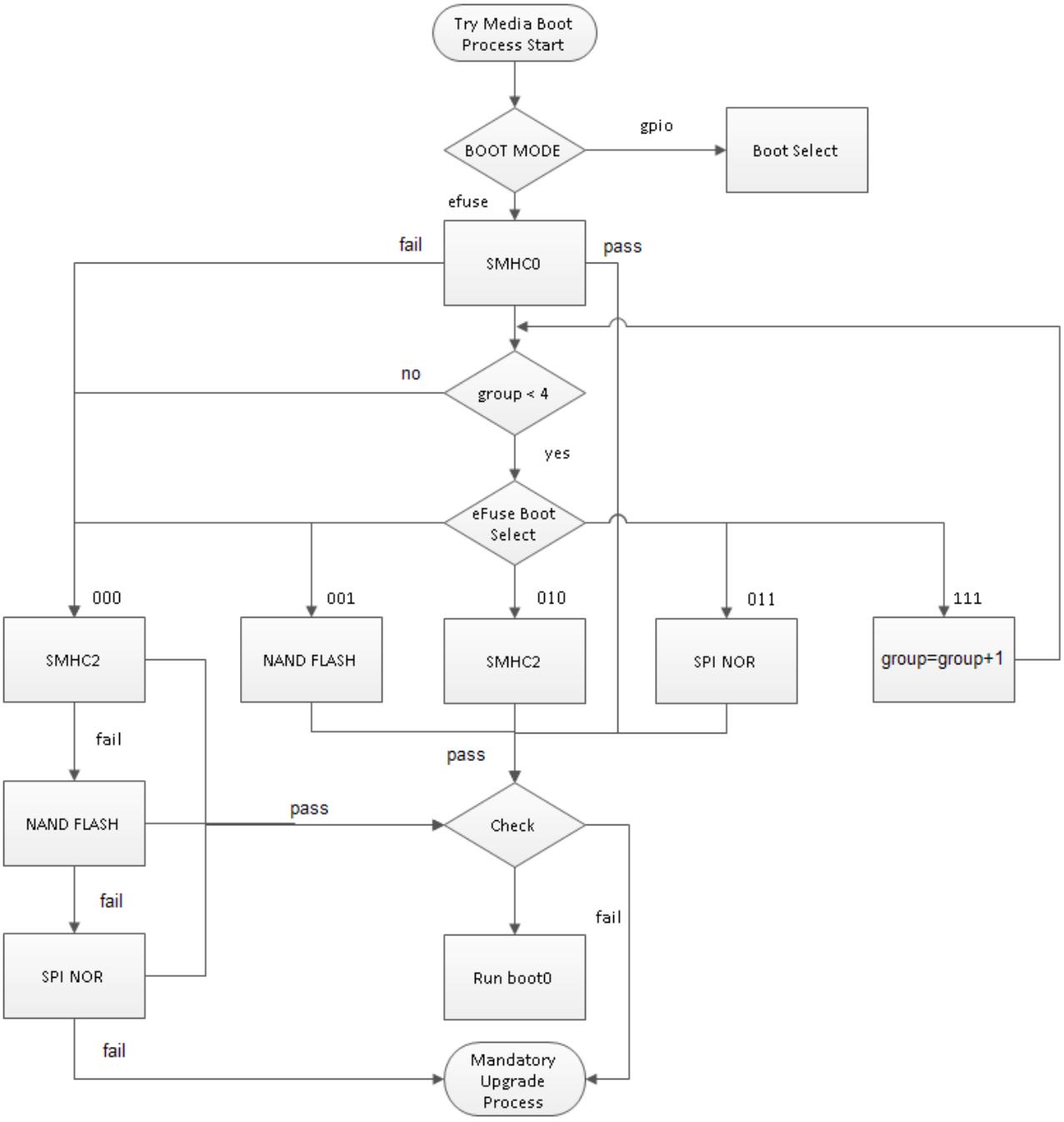


Figure 3-10. eFuse Boot Select Process

3.2.2.9. Secure Try Media Boot Process

For Secure Try Media Boot Process,the system will verify the integrity of the certificate. Figure 3-11 shows Secure BROM GPIO Pin Boot Select Process.

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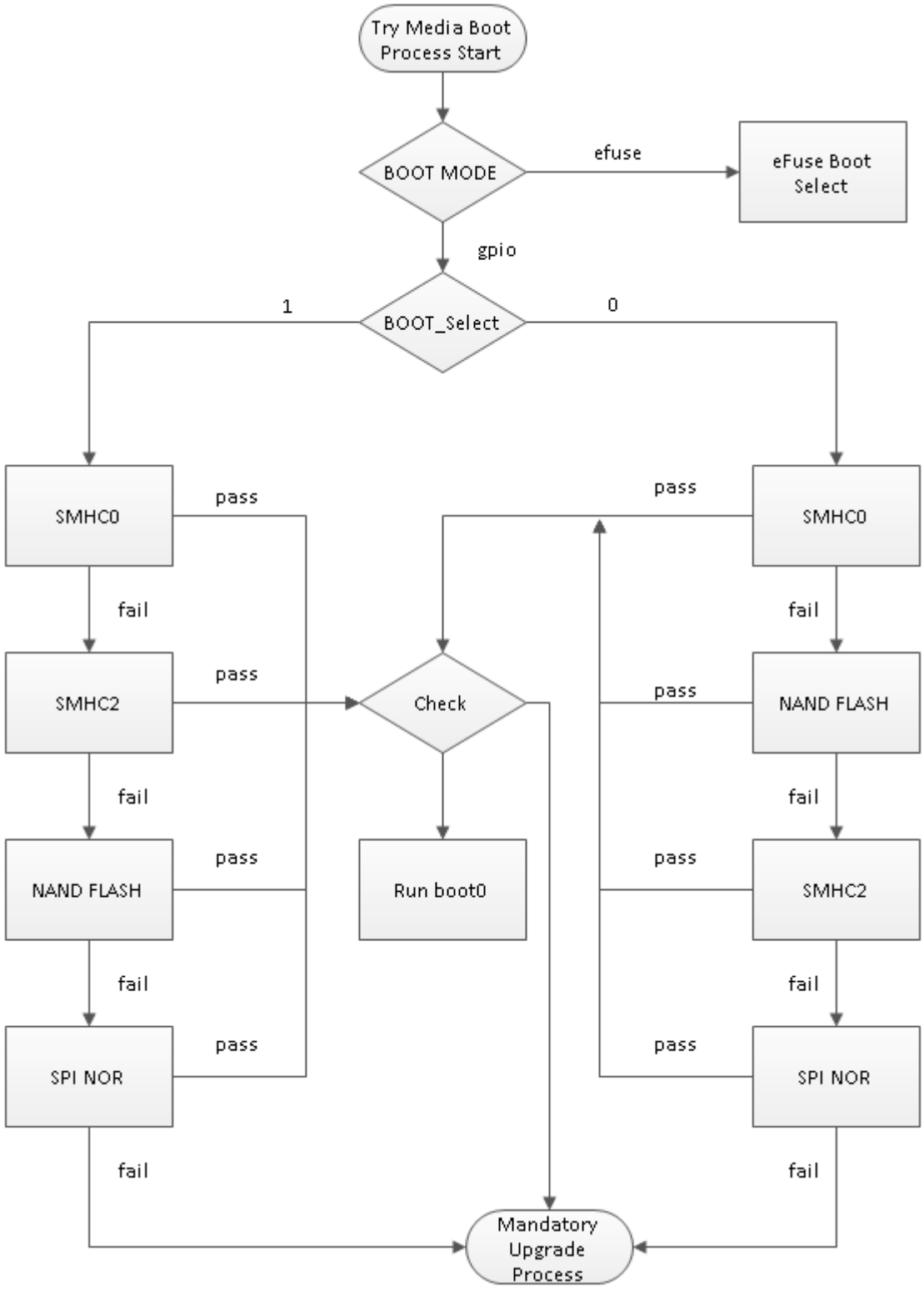


Figure 3-11. Secure BROM GPIO Pin Boot Select Process

Figure 3-12 shows Secure BROM eFuse Boot Select Process.

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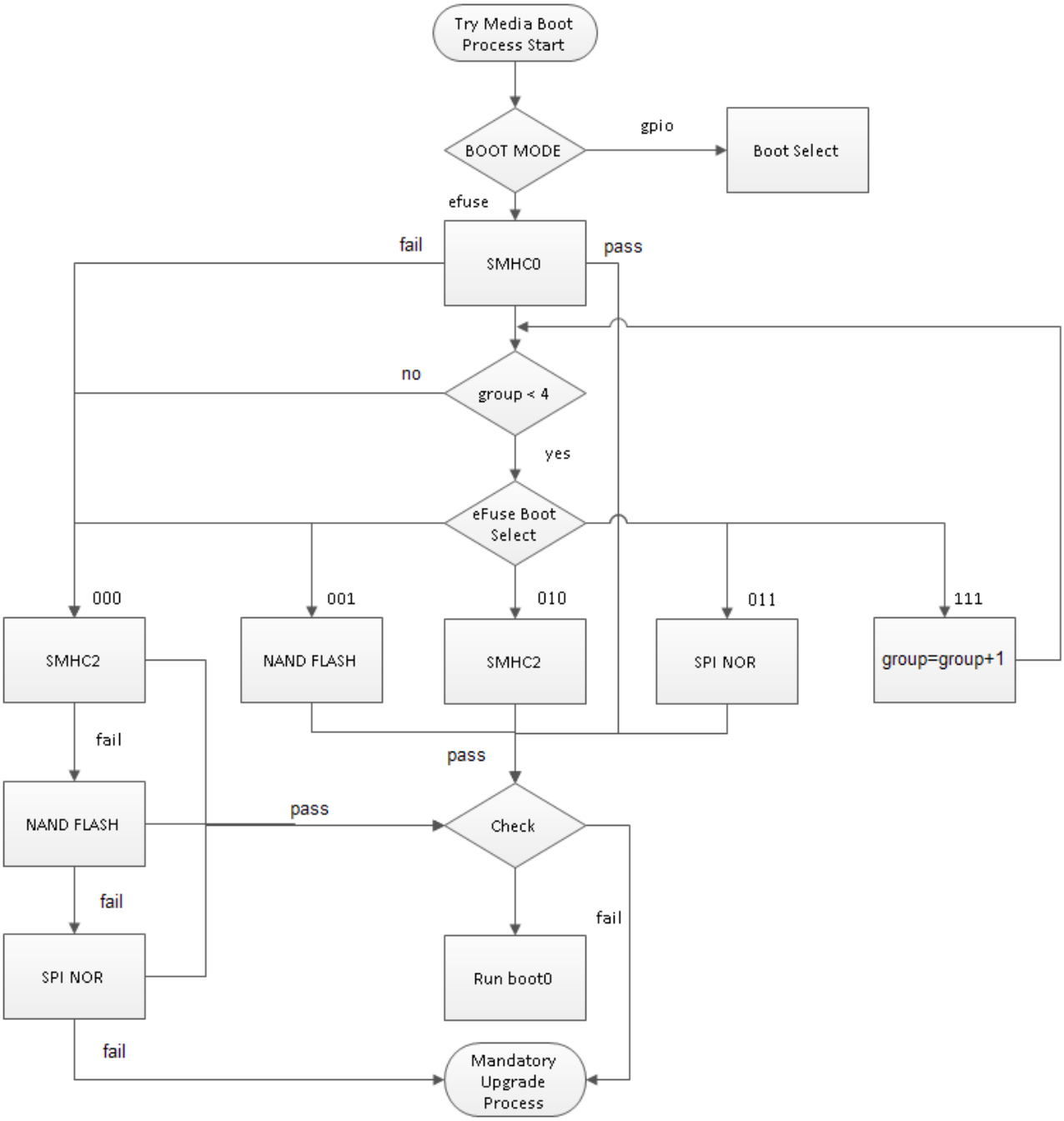


Figure 3-12. Secure BROM eFuse Boot Select Process

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3.3. CCU

3.3.1. Overview

The CCU controls the PLLs configuration and most of the clock generation, division, distribution, synchronization and gating. CCU input signals include the external clock for the reference frequency (24MHz). The outputs from CCU are mostly clocks to other blocks in the system.

Features:

- 11 PLLs
- Bus Source and Divisions
- Clock Output Control
- PLL Bias Control
- PLL Tunning Control
- PLL Pattern Control
- Configuring Modules Clock
- Bus Clock Gating
- Bus Software Reset
- PLL Lock Control

3.3.2. Operations and Functional Descriptions

3.3.2.1. System Bus Tree

Figure 3-13 shows a block diagram of the System Bus Tree.

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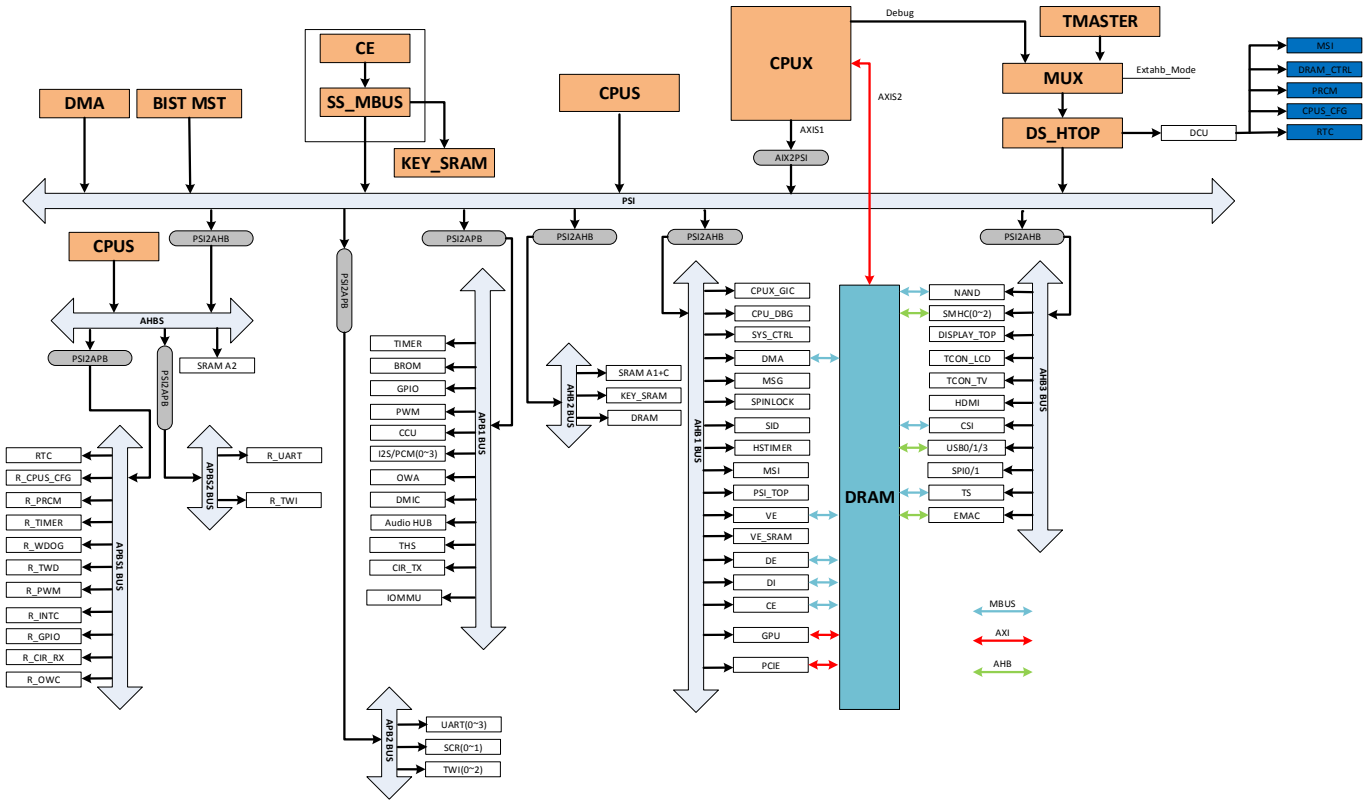


Figure 3-13. System Bus Tree

3.3.2.2. Bus Clock Tree

Figure 3-14 shows a block diagram of the Bus Clock Tree.

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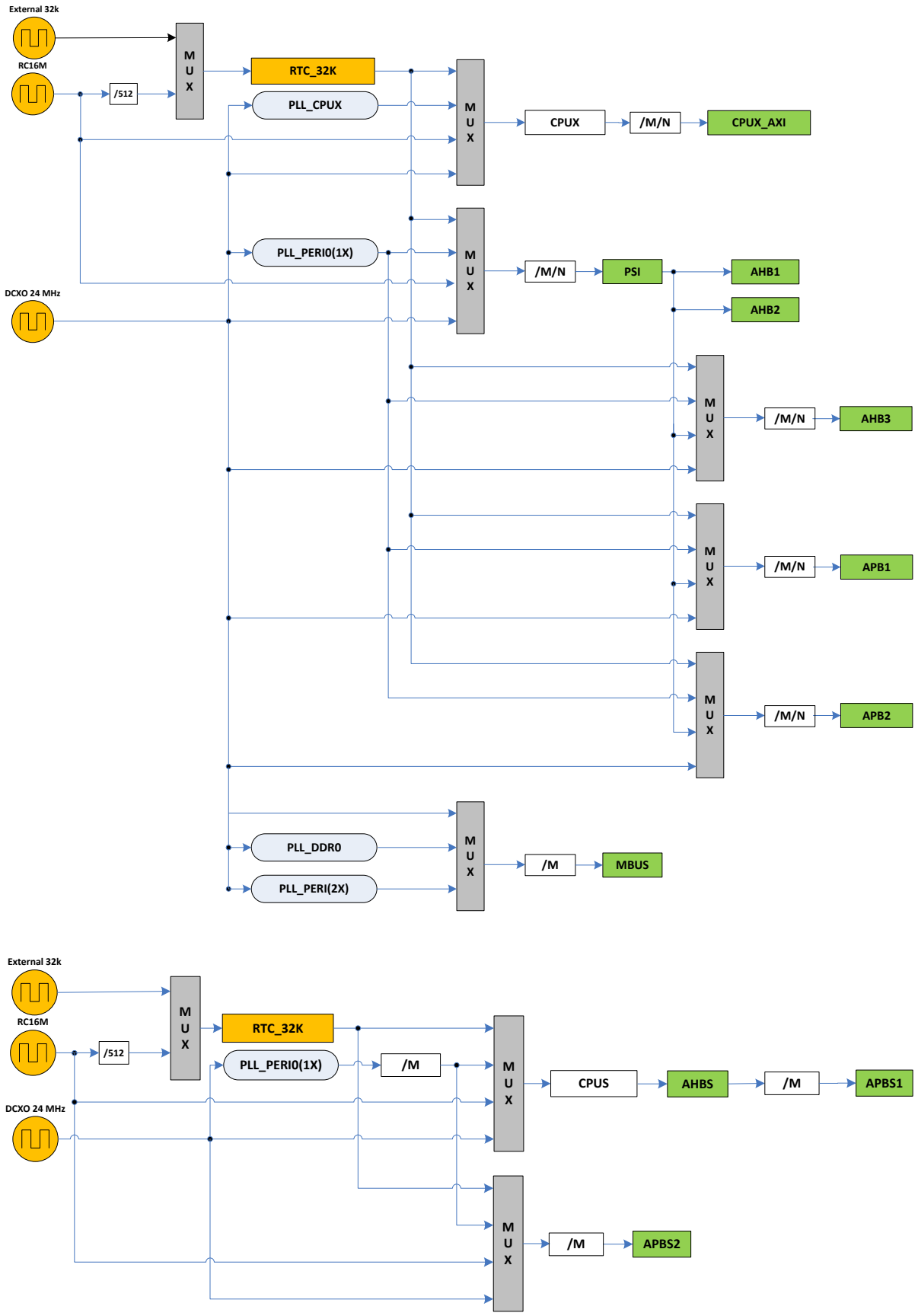


Figure 3-14. Bus Clock Tree

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3.3.2.3. Module Clock Tree

Figure 3-15 shows a block diagram of the Module Clock Tree.

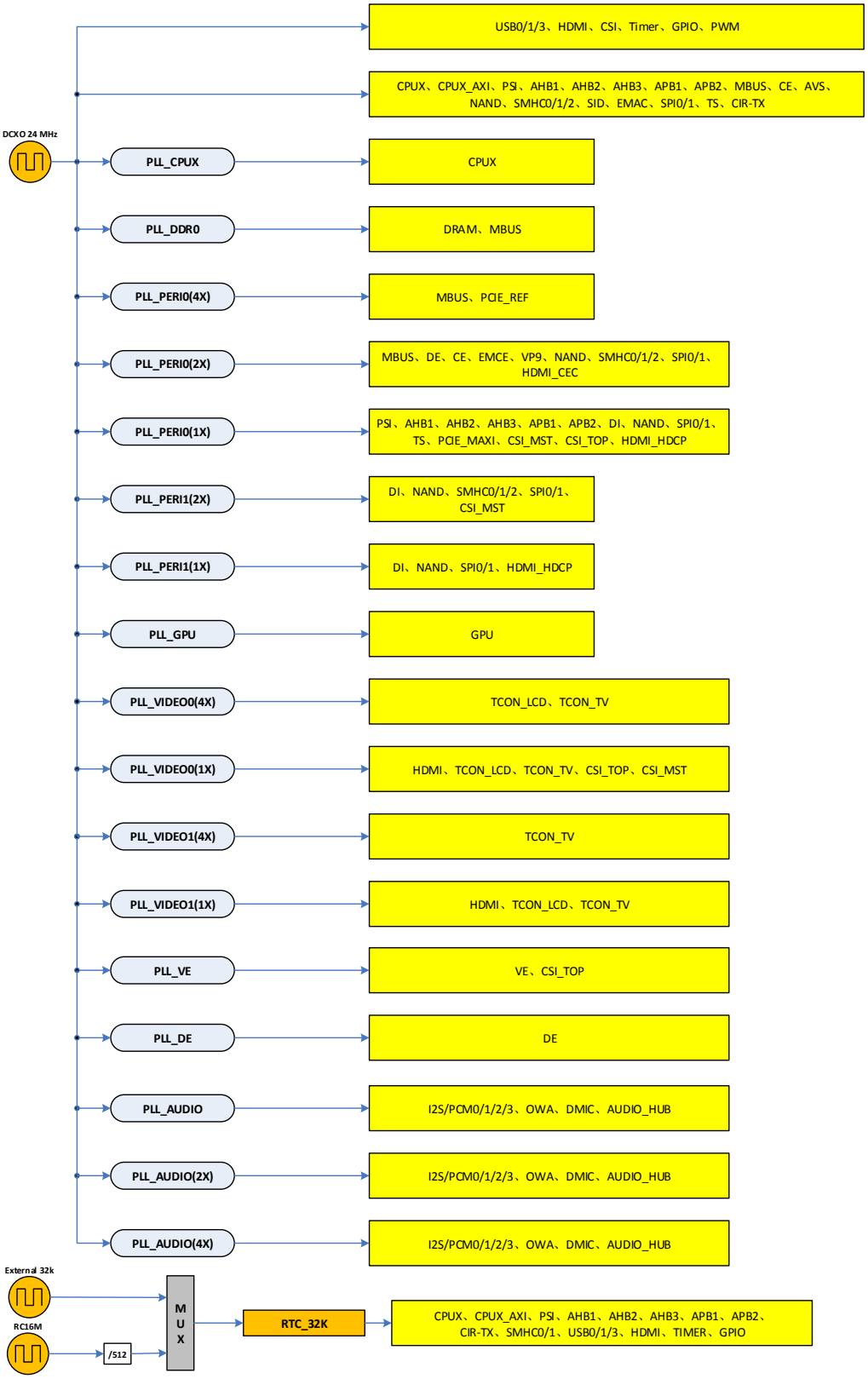


Figure 3-15. Module Clock Tree

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3.3.2.4. PLL Clock Frequency

Table 3-5. PLL Clock Frequency

PLLs	Stable Oparating Frequency	Actual Oparating Frequency	Spread Spectrum	Linear FM	Rate Control	Pk-Pk	Duty	Lock Time
PLL_CPUX	288MHz~5.0GHz (24*N)	288MHz~2.0GHz	No	No	No	< 200ps	Yes	1.5ms
PLL_DDR0	180MHz~3.0GHz (24*N/M0/M1)	192MHz~2.0GHz	Yes	No	No	200MHz~800MHz(< 200ps) 800MHz~1.3GHz(< 140ps) 1.3GHz~2.0GHz(< 100ps)	Yes	2ms
PLL_PERI0(4X)	180MHz~3.0GHz (24*N/M0/M1)	2.4GHz	No	No	No	< 200ps	Yes	500us
PLL_PERI1(4X)	180MHz~3.0GHz (24*N/M0/M1)	2.4GHz	Yes	No	No	< 200ps	Yes	500us
PLL_GPU	180MHz~3GHz (24*N/M0/M1)	168MHz~800MHz	Yes	No	No	< 200ps	Yes	500us
PLL_VIDEO0(4X)	180MHz~3.0GHz (24*N/M)	192MHz~1200MHz	Yes	No	No	< 200ps	Yes	500us
PLL_VIDEO1(4X)	180MHz~3.0GHz (24*N/M)	192MHz~1200MHz	Yes	No	No	< 200ps	Yes	500us
PLL_VE	180MHz~3.0GHz (24*N/M0/M1)	192MHz~800MHz	Yes	No	No	< 200ps	Yes	500us
PLL_DE	180MHz~3.0GHz (24*N/M0/M1)	192MHz~600MHz	Yes	No	No	< 200ps	Yes	500us
PLL_HSIC	180MHz~3.0GHz (24*N/M0/M1)	480MHz	Yes	No	No	< 200ps	Yes	500us
PLL_AUDIO	24.576MHz 22.5792MHz (24*N/div1/div2)	24.576MHz 22.5792MHz (24.576*8)M (22.5792*8)M	Yes	No	No	< 200ps	Yes(M0=2)	500us

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3.3.2.5. Typical Applications

PLL Applications: use the available clock sources to generate clock roots to various parts of the chip. In practical application, other PLLs do not support dynamic frequency scaling except for PLL_CPUX.

Table 3-6. PLLs Typical Applications

PLLs	Typical Applications	Dynamic Frequency Scaling(DFS)
PLL_CPUX	CPUX	Support
PLL_DDR0	MBUS,DRAM	Not Support
PLL_PERI0(4X)	MBUS,PCIE	Not Support
PLL_PERI0(2X)	MBUS, DE,G2D,CE,NAND0/1,SMHC0/1/2,SPI0/1	Not Support
PLL_PERI0(1X)	PSI,AHB1,AHB2,AHB3,APB1,APB2, DI,NAND,SPI0/1 ,TS,CSI_MST,CSI_TOP	Not Support
PLL_PERI1(2X)	DI,NAND,SMHC0/1/2,SPI0/1,CSI_MST	Not Support
PLL_PERI1(1X)	DI,NAND ,SPI0/1,HDMI_HDCP	Not Support
PLL_GPU	GPU	Support
PLL_VIDEO0(4X)	TCON_LCD,TCON_TV	Not Support
PLL_VIDEO0(1X)	TCON_LCD,TCON_TV, HDMI, CSI_TOP,CSI_MST	Not Support
PLL_VIDEO1(4X)	TCON_TV	Not Support
PLL_VIDEO1(1X)	TCON_TV,TCON_LCD,HDMI	Not Support
PLL_VE	VE,CSI_TOP	Not Support
PLL_DE	DE	Not Support
PLL_AUDIO	I2S/PCM0,I2S/PCM1,I2S/PCM2,I2S/PCM3,OWA,DMIC, AUDIO_CODEC	Not Support

NOTE

All module clocks do not support DFS unless other noted. Because when switching module clock source or adjusting division-ratio, the burr or transient instability may be generated, which will hang dead the module.

3.3.3. Programming Guildlines

3.3.3.1. PLL

(1) In practical application, other PLLs do not support dynamic frequency scaling except for PLL_CPUX and PLL_GPU.

(2) The user guide of PLL Lock(using PLL_CPUX as an example)

(a).PLL_CPUX from close to open:

- Write 0 to the bit29 of **PLL_CPUX_CTRL_REG**.
- Configure the parameters **(N,K,M,P)** of **PLL_CPUX_CTRL_REG**.

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- Write 1 to the **Enable** bit of CPU PLL**PLL_CPUX_CTRL_REG**.
- Write 1 to the bit29 of **PLL_CPUX_CTRL_REG**.
- Read the bit28 of **PLL_CPUX_CTRL_REG**, when it is 1, then CPUX PLL is locked.
- Delay 20us.

(b).PLL_CPUX frequency conversion:

- Write 0 to the bit29 of **PLL_CPUX_CTRL_REG**.
- Configure the parameters **(N,K,M,P)** of **PLL_CPUX_CTRL_REG**.
- Write 1 to the bit29 of **PLL_CPUX_CTRL_REG**.
- Read the bit28 of **PLL_CPUX_CTRL_REG**, when it is 1, then CPUX PLL is locked.
- Delay 20us.

(c).PLL_CPU from open to close:

- Write 0 to the **Enable** bit of **PLL_CPUX_CTRL_REG**.
- Write 0 to the bit29 of **PLL_CPUX_CTRL_REG**.

3.3.3.2. BUS

(1) When setting the BUS clock , you should set the division factor firstly, and after the division factor becomes valid, switch the clock source. The clock source will be switched after at least three clock cycles.
(2) The BUS clock should not be dynamically changed in most applications.

3.3.3.3. Clock Switch

Make sure that the clock source output is valid before the clock source switch, and then set a proper divide ratio; after the division factor becomes valid, switch the clock source.

3.3.3.4. Gating and Reset

Make sure that the reset signal has been released before the release of module clock gating.

3.3.4. Register List

Module Name	Base Address
CCU	0x0300 1000

Register Name	Offset	Description
PLL_CPUX_CTRL_REG	0x0000	PLL_CPUX Control Register
PLL_DDR0_CTRL_REG	0x0010	PLL_DDR0 Control Register
PLL_PERI0_CTRL_REG	0x0020	PLL_PERI0 Control Register
PLL_PERI1_CTRL_REG	0x0028	PLL_PERI1 Control Register
PLL_GPU_CTRL_REG	0x0030	PLL_GPU Control Register

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PLL_VIDEO0_CTRL_REG	0x0040	PLL_VIDEO0 Control Register
PLL_VIDEO1_CTRL_REG	0x0048	PLL_VIDEO1 Control Register
PLL_VE_CTRL_REG	0x0058	PLL_VE Control Register
PLL_DE_CTRL_REG	0x0060	PLL_DE Control Register
PLL_HSIC_CTRL_REG	0x0070	PLL_HSIC Control Register
PLL_AUDIO_CTRL_REG	0x0078	PLL_AUDIO Control Register
PLL_DDR0_PAT_REG	0x0110	PLL_DDR0 Pattern Register
PLL_PERI1_PAT0_REG	0x0128	PLL_PERI1 Pattern0 Register
PLL_PERI1_PAT1_REG	0x012C	PLL_PERI1 Pattern1 Register
PLL_GPU_PAT0_REG	0x0130	PLL_GPU Pattern0 Register
PLL_GPU_PAT1_REG	0x0134	PLL_GPU Pattern1 Register
PLL_VIDEO0_PAT0_REG	0x0140	PLL_VIDEO0 Pattern0 Register
PLL_VIDEO0_PAT1_REG	0x0144	PLL_VIDEO0 Pattern1 Register
PLL_VIDEO1_PAT0_REG	0x0148	PLL_VIDEO1 Pattern0 Register
PLL_VIDEO1_PAT1_REG	0x014C	PLL_VIDEO1 Pattern1 Register
PLL_VE_PAT0_REG	0x0158	PLL_VE Pattern0 Register
PLL_VE_PAT1_REG	0x015C	PLL_VE Pattern1 Register
PLL_DE_PAT0_REG	0x0160	PLL_DE Pattern0 Register
PLL_DE_PAT1_REG	0x0164	PLL_DE Pattern1 Register
PLL_HSIC_PAT0_REG	0x0170	PLL_HSIC Pattern0 Register
PLL_HSIC_PAT1_REG	0x0174	PLL_HSIC Pattern1 Register
PLL_AUDIO_PAT0_REG	0x0178	PLL_AUDIO Pattern0 Register
PLL_AUDIO_ PAT1_REG	0x017C	PLL_AUDIO Pattern1 Register
PLL_CPUX_BIAS_REG	0x0300	PLL_CPUX Bias Register
PLL_DDR0_BIAS_REG	0x0310	PLL_DDR0 Bias Register
PLL_PERI0_BIAS_REG	0x0320	PLL_PERI0 Bias Register
PLL_PERI1_BIAS_REG	0x0328	PLL_PERI1 Bias Register
PLL_GPU_BIAS_REG	0x0330	PLL_GPU Bias Register
PLL_VIDEO0_BIAS_REG	0x0340	PLL_VIDEO0 Bias Register
PLL_VIDEO1_BIAS_REG	0x0348	PLL_VIDEO1 Bias Register
PLL_VE_BIAS_REG	0x0358	PLL_VE Bias Register
PLL_DE_BIAS_REG	0x0360	PLL_DE Bias Register
PLL_ISP_BIAS_REG	0x0368	PLL_ISP Bias Register
PLL_HSIC_BIAS_REG	0x0370	PLL_HSIC Bias Register
PLL_AUDIO_BIAS_REG	0x0378	PLL_AUDIO Bias Register
PLL_CPUX_TUN_REG	0x0400	PLL_CPUX Tunning Register
CPUX_AXI_CFG_REG	0x0500	CPUX_AXI Configuration Register
PSI_AHB1_AHB2_CFG_REG	0x0510	PSI_AHB1_AHB2 Configuration Register
AHB3_CFG_REG	0x051C	AHB3 Configuration Register
APB1_CFG_REG	0x0520	APB1 Configuration Register
APB2_CFG_REG	0x0524	APB2 Configuration Register
CCI400_CFG_REG	0x0530	CCI400 Configuration Register
MBUS_CFG_REG	0x0540	MBUS Configuration Register
DE_CLK_REG	0x0600	DE Clock Register

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DE_BGR_REG	0x060C	DE Bus Gating Reset Register
DI_CLK_REG	0x0620	DI Clock Register
DI_BGR_REG	0x062C	DI Bus Gating Reset Register
GPU_CLK_REG	0x0670	GPU Clock Register
GPU_BGR_REG	0x067C	GPU Bus Gating Reset Register
CE_CLK_REG	0x0680	CE Clock Register
CE_BGR_REG	0x068C	CE Bus Gating Reset Register
VE_CLK_REG	0x0690	VE Clock Register
VE_BGR_REG	0x069C	VE Bus Gating Reset Register
EMCE_CLK_REG	0x06B0	EMCE Clock Register
EMCE _BGR_REG	0x06BC	EMCE Bus Gating Reset Register
VP9_CLK_REG	0x06C0	VP9 Clock Register
VP9 _BGR_REG	0x06CC	VP9 Bus Gating Reset Register
DMA_BGR_REG	0x070C	DMA Bus Gating Reset Register
MSGBOX_BGR_REG	0x071C	MessageBox Bus Gating Reset Register
SPINLOCK_BGR_REG	0x072C	Spinlock Bus Gating Reset Register
HSTIMER_BGR_REG	0x073C	HSTimer Bus Gating Reset Register
AVS_CLK_REG	0x0740	AVS Clock Register
DBGSYS_BGR_REG	0x078C	DBGSYS Bus Gating Reset Register
PSI_BGR_REG	0x079C	PSI Bus Gating Reset Register
PWM_BGR_REG	0x07AC	PWM Bus Gating Reset Register
IOMMU_BGR_REG	0x07BC	IOMMU Bus Gating Reset Register
DRAM_CLK_REG	0x0800	DRAM Clock Register
MBUS_MST_CLK_GATING_REG	0x0804	MBUS Master Clock Gating Register
DRAM_BGR_REG	0x080C	DRAM Bus Gating Reset Register
NAND_0_CLK_REG	0x0810	NAND0 Clock Register
NAND_1_CLK_REG	0x0814	NAND1 Clock Register
NAND_BGR_REG	0x082C	NAND Bus Gating Reset Register
SMHC0_CLK_REG	0x0830	SMHC0 Clock Register
SMHC1_CLK_REG	0x0834	SMHC1 Clock Register
SMHC2_CLK_REG	0x0838	SMHC2 Clock Register
SMHC_BGR_REG	0x084C	SMHC Bus Gating Reset Register
UART_BGR_REG	0x090C	UART Bus Gating Reset Register
TWI_BGR_REG	0x091C	TWI Bus Gating Reset Register
SCR_BGR_REG	0x093C	SCR Bus Gating Reset Register
SPI0_CLK_REG	0x0940	SPI0 Clock Register
SPI1_CLK_REG	0x0944	SPI1 Clock Register
SPI_BGR_REG	0x096C	SPI Bus Gating Reset Register
EMAC_BGR_REG	0x097C	EMAC Bus Gating Reset Register
TS_CLK_REG	0x09B0	TS Clock Register
TS_BGR_REG	0x09BC	TS Bus Gating Reset Register
IRTX_CLK_REG	0x09C0	CIR-TX Clock Register
IRTX_BGR_REG	0x09CC	CIR-TX Bus Gating Reset Register
THS_BGR_REG	0x09FC	THS Bus Gating Reset Register

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I2S/PCM3_CLK_REG	0x0A0C	I2S/PCM3 Clock Register
I2S/PCM0_CLK_REG	0x0A10	I2S/PCM0 Clock Register
I2S/PCM1_CLK_REG	0x0A14	I2S/PCM1 Clock Register
I2S/PCM2_CLK_REG	0x0A18	I2S/PCM2 Clock Register
I2S/PCM_BGR_REG	0x0A1C	I2S/PCM Bus Gating Reset Register
OWA_CLK_REG	0x0A20	OWA Clock Register
OWA_BGR_REG	0x0A2C	OWA Bus Gating Reset Register
DMIC_CLK_REG	0x0A40	DMIC Clock Register
DMIC_BGR_REG	0x0A4C	DMIC Bus Gating Reset Register
AUDIO_HUB _CLK_REG	0x0A60	AUDIO_HUB Clock Register
AUDIO_HUB_BGR_REG	0x0A6C	AUDIO_HUB Bus Gating Reset Register
USB0_CLK_REG	0x0A70	USB0 Clock Register
USB1_CLK_REG	0x0A74	USB1 Clock Register
USB3_CLK_REG	0x0A7C	USB3 Clock Register
USB_CGR_REG	0x0A8C	USB Clock Gating Reset Register
PCIE_REF_CLK_REG	0x0AB0	PCIE REF Clock Register
PCIE_AXI_CLK_REG	0x0AB4	PCIE AXI Clock Register
PCIE_AUX_CLK_REG	0x0AB8	PCIE AUX Clock Register
PCIE_CGR_REG	0x0ABC	PCIE Clock Gating Reset Register
cHDMI_CLK_REG	0x0B00	HDMI Clock Register
HDMI_SLOW_CLK_REG	0x0B04	HDMI Slow Clock Register
HDMI_CEC_CLK_REG	0x0B10	HDMI CEC Clock Register
HDMI_BGR_REG	0x0B1C	HDMI Bus Gating Reset Register
DISPLAY_IF_TOP_BGR_REG	0x0B5C	DISPLAY_IF_TOP Bus Gating Reset Register
TCON_LCD_CLK_REG	0x0B60	TCON_LCD Clock Register
TCON_LCD_BGR_REG	0x0B7C	TCON_LCD Bus Gating Reset Register
TCON_TV_CLK_REG	0x0B80	TCON_TV Clock Register
TCON_TV_BGR_REG	0x0B9C	TCON_TV Bus Gating Reset Register
CSI_MISC_CLK_REG	0x0C00	CSI MISC Clock Register
CSI_TOP_CLK_REG	0x0C04	CSI TOP Clock Register
CSI_MST_CLK0_REG	0x0C08	CSI Master Clock0 Register
CSI_BGR_REG	0x0C2C	CSI Bus Gating Reset Register
HDMI_HDCP_CLK_REG	0x0C40	HDMI HDCP Clock Register
HDMI_HDCP _CLK_REG	0x0C4C	HDMI HDCP Clock Register
CCU_SEC_SWITCH_REG	0x0F00	CCU Security Switch Register
PLL_LOCK_DBG_CTRL_REG	0x0F04	PLL Lock Debug Control Register

3.3.5. Register Description

3.3.5.1. PLL_CPUX Control Register (Default Value: 0x0200_1000)

Offset: 0x0000			**Register Name: PLL_CPUX_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**

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31	R/W	0x0	PLL_ENABLE. 0: Disable. 1: Enable. The PLL_CPUX= 24MHz*N/P.  **NOTE** **The PLL_CPUX output clock must be in the range of 200MHz~3GHz.** **Its default value is 408MHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	/	/	/
26:24	R/W	0x2	PLL_LOCK_TIME. PLL Lock Time. This bit is a stepping range from a frequency to another frequency,it can adjust the speed of clock changing.
23:18	/	/	/
17:16	R/W	0x0	PLL_OUT_EXT_DIVP. PLL Output External Divider P. 00: 1 01: 2 10: 4 11: / When output clock is less than 288MHz,clock frequency is outputted by dividing P.
15:8	R/W	0x10	PLL_FACTOR_N PLL Factor N. N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N should be more than or equal to 11
7:2	/	/	/
1:0	R/W	0x0	PLL_FACTOR_M. PLL Factor M M = PLL_FACTOR_M + 1 PLL_FACTOR_M is from 0 to 3. M is only used for backdoor testing.

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3.3.5.2. PLL_DDR0 Control Register (Default Value: 0x0000_2301)

Offset: 0x0010			Register Name: PLL_DDR0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable. 1: Enable. The PLL_DDR0 = 24MHz*N/M0/M1. PLL_DDR0 is 432MHz by default.
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE. 0: Disable. 1: Enable.
23:16	/	/	/
15:8	R/W	0x23	PLL_FACTOR_N PLL Factor N. N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N should be more than or equal to 11.
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1. PLL Input Div M1. M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_M0. PLL Output Div M0. M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.3. PLL_PERI0 Control Register (Default Value: 0x0000_6300)

Offset: 0x0020			Register Name: PLL_PERI0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable. 1: Enable.

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			The PLL_PERI0(4X) = 24MHz*N/M0/M1. The PLL_PERI0(2X) = (24MHz*N/M0/M1)/2. The PLL_PERI0(1X) = (24MHz*N/M0/M1)/4. PLL_PERI0(4X) is 2.4GHz by default. PLL_PERI0(4X) output clock should be 2.4GHz. It is not suggested to change this parameter.
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:16	/	/	/
15:8	R/W	0x63	PLL_FACTOR_N PLL Factor N. N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N should be more than or equal to 11
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1. PLL Input Div M1. M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x0	PLL_OUTPUT_DIV_M0. PLL Output Div M0. M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.4. PLL_PERI1 Control Register (Default Value: 0x0000_6300)

Offset: 0x0028			**Register Name: PLL_PERI1_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable. 1: Enable. The PLL_PERI1(4X) = 24MHz*N/M0/M1. The PLL_PERI1(2X) = (24MHz*N/M0/M1)/2. The PLL_PERI1(1X) = (24MHz*N/M0/M1)/4. PLL_PERI1(4X) is 2.4GHz by default. PLL_PERI1(4X) output clock should be 2.4GHz. It is not suggested to change this parameter.
30	/	/	/

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29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE. 0: Disable. 1: Enable.
23:16	/	/	/
15:8	R/W	0x63	PLL_FACTOR_N PLL Factor N. N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N should be more than or equal to 11.
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1. PLL Input Div M1. M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x0	PLL_OUTPUT_DIV_M0. PLL Output Div M0. M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.5. PLL_GPU Control Register (Default Value: 0x0000_2301)

Offset: 0x0030			**Register Name: PLL_GPU_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable. 1: Enable. The PLL_GPU = 24MHz*N/M0/M1. PLL_GPU is 432MHz by default.
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)

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27:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE. 0: Disable. 1: Enable.
23:16	/	/	/
15:8	R/W	0x23	PLL_FACTOR_N PLL Factor N. N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N should be more than or equal to 11.
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1. PLL Input Div M1. M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_M0. PLL Output Div M0. M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.6. PLL_VIDEO0 Control Register (Default Value: 0x0000_6203)

Offset: 0x0040			**Register Name: PLL_VIDEO0_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable. 1: Enable. For application, PLL_VIDEO0(4X)= 24MHz*N/M. PLL_VIDEO0(1X)=24MHz*N/M/4. PLL_VIDEO0 is 1188MHz by default.
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE. 0: Disable. 1: Enable.
23:16	/	/	/

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15:8	R/W	0x62	PLL_FACTOR_N PLL Factor N. N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N should be more than or equal to 11
7:2	/	/	/
1	R/W	0x1	PLL_INPUT_DIV_M. PLL Input Div M. M1=PLL_INPUT_DIV_M + 1 PLL_INPUT_DIV_M is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_D. PLL Output Div D. (This factor is used for testing.) M0=PLL_OUTPUT_DIV_D + 1 PLL_OUTPUT_DIV_D is from 0 to 1. For test, PLL_VIDEO0(4X) =24MHz*N/M/D

3.3.5.7. PLL_VIDEO1 Control Register (Default Value: 0x0000_6203)

Offset: 0x0048			Register Name: PLL_VIDEO1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable. 1: Enable. For application, PLL_VIDEO1(4X)= 24MHz*N/M. PLL_VIDEO1(1X)=24MHz*N/M/4. PLL_VIDEO0 is 1188MHz by default.
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE. 0: Disable. 1: Enable.
23:16	/	/	/
15:8	R/W	0x62	PLL_FACTOR_N PLL Factor N. N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254.

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			In application, PLL_FACTOR_N should be more than or equal to 11
7:2	/	/	/
1	R/W	0x1	PLL_INPUT_DIV_M. PLL Input Div M. M1=PLL_INPUT_DIV_M + 1 PLL_INPUT_DIV_M is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_D. PLL Output Div D.(This factor is used for testing.) M0=PLL_OUTPUT_DIV_D + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1. For test, PLL_VIDEO1(4X) =24MHz*N/M/D

3.3.5.8. PLL_VE Control Register (Default Value: 0x0000_2301)

Offset: 0x0058			Register Name: PLL_VE_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable. 1: Enable. The PLL_VE = 24MHz*N/M0/M1. PLL_VE is 432MHz by default.
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE. 0: Disable. 1: Enable.
23:16	/	/	/
15:8	R/W	0x23	PLL_FACTOR_N PLL Factor N. N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N should be more than or equal to 11
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1. PLL Input Div M1. M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.

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0	R/W	0x1	PLL_OUTPUT_DIV_M0. PLL Output Div M0. M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.9. PLL_DE Control Register (Default Value: 0x0000_2301)

Offset: 0x0060			Register Name: PLL_DE_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable. 1: Enable. The PLL_DE = 24MHz*N/M0/M1. PLL_DE is 432MHz by default.
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE. 0: Disable. 1: Enable.
23:16	/	/	/
15:8	R/W	0x23	PLL_FACTOR_N PLL Factor N. N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N should be more than or equal to 11
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1. PLL Input Div M1. M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_M0. PLL Output Div M0. M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

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3.3.5.10. PLL_HSIC Control Register (Default Value: 0x0000_2701)

Offset: 0x0070			Register Name: PLL_HSIC_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable. 1: Enable. The PLL_HSIC = 24MHz*N/M0/M1. PLL_HSCI is 480MHz by default.
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE. 0: Disable. 1: Enable.
23:16	/	/	/
15:8	R/W	0x27	PLL_FACTOR_N PLL Factor N. N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N should be more than or equal to 11
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1. PLL Input Div M1. M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_M0. PLL Output Div M0. M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.11. PLL_AUDIO Control Register (Default Value: 0x0014_2A01)

Offset: 0x0078			Register Name: PLL_AUDIO_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

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31	R/W	0x0	PLL_ENABLE. 0: Disable. 1: Enable. This PLL is for Audio. The PLL_AUDIO = 24MHz*N/(Input_div+1)/(Output_div+1)/(P+1). PLL_AUDIO(4X) = 24MHz*N/(Input_div+1)/2 PLL_AUDIO is 24.5714 MHz by default.
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE. 0: Disable. 1: Enable.
23:22	/	/	/
21:16	R/W	0x14	PLL_POST_DIV_P. PLL Post-div P. P= PLL_POST_DIV_P +1 PLL_POST_DIV_P is from 0 to 63.
15:8	R/W	0x2A	PLL_FACTOR_N PLL Factor N. N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N should be more than or equal to 11
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1. PLL Input Div M1. M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_M0. PLL Output Div M0. M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.12. PLL_DDR0 Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: PLL_DDR0_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN.

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			Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: Triangular
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When PLL_INPUT_DIV_M1 is 1,this register is set to 1.
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.3.5.13. PLL_PERI1 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0128			**Register Name: PLL_PERI1_PAT0_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: Triangular
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When PLL_INPUT_DIV_M1 is 1,this register is set to 1.
18:17	R/W	0x0	FREQ. Frequency.

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			00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.3.5.14. PLL_PERI1 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x012C			Register Name: PLL_PERI1_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN.
23:21	/	/	/
20	R/W	0x0	FRAC_EN.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN.

3.3.5.15. PLL_GPU0 Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: PLL_GPU0_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: Triangular
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When PLL_INPUT_DIV_M1 is 1,this register is set to 1.
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz
16:0	R/W	0x0	WAVE_BOT.

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			Wave Bottom.

3.3.5.16. PLL_GPU Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: PLL_GPU_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN.
23:21	/	/	/
20	R/W	0x0	FRAC_EN.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN.

3.3.5.17. PLL_VIDEO0 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0140			Register Name: PLL_VIDEO0_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: Triangular
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz when PLL_INPUT_DIV_M1 is 1, this register is set to 1.
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

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3.3.5.18. PLL_VIDEO0 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0144			Register Name: PLL_VIDEO0_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN.
23:21	/	/	/
20	R/W	0x0	FRAC_EN.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN.

3.3.5.19. PLL_VIDEO1 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0148			Register Name: PLL_VIDEO1_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: Triangular
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz when PLL_INPUT_DIV_M1 is 1, this register is set to 1.
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.3.5.20. PLL_VIDEO1 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x014C			Register Name: PLL_VIDEO1_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:25	/	/	/
24	R/W	0x0	DITHER_EN.
23:21	/	/	/
20	R/W	0x0	FRAC_EN.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN.

3.3.5.21. PLL_VE Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0158			Register Name: PLL_VE_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular(1bit) 11: Triangular(nbit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz when PLL_INPUT_DIV_M1 is 1, this register is set to 1.
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.3.5.22. PLL_VE Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x015C			Register Name: PLL_VE_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN.
23:21	/	/	/
20	R/W	0x0	FRAC_EN.
19:17	/	/	/

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16:0	R/W	0x0	FRAC_IN.

3.3.5.23. PLL_DE Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: PLL_DE_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: Triangular
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz when PLL_INPUT_DIV_M1 is 1, this register is set to 1.
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.3.5.24. PLL_DE Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: PLL_DE_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN.
23:21	/	/	/
20	R/W	0x0	FRAC_EN.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN.

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3.3.5.25. PLL_HSIC Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0170			Register Name: PLL_HSIC_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: Triangular
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz when PLL_INPUT_DIV_M1 is 1, this register is set to 1.
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.3.5.26. PLL_HSIC Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0174			Register Name: PLL_HSIC_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN.
23:21	/	/	/
20	R/W	0x0	FRAC_EN.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN.

3.3.5.27. PLL_AUDIO Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0178			Register Name: PLL_AUDIO_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

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31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: Triangular
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz when PLL_INPUT_DIV_M1 is 1, this register is set to 1.
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.3.5.28. PLL_AUDIO Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x017C			Register Name: PLL_AUDIO_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN.
23:21	/	/	/
20	R/W	0x0	FRAC_EN.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN.

3.3.5.29. PLL_CPUX Bias Register (Default Value: 0x8003_0000)

Offset: 0x0300			Register Name: PLL_CPUX_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	VCO_RST. VCO reset in.
30:21	/	/	/
20:16	R/W	0x03	PLL_BIAS_CURRENT.

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			PLL current bias control [4:0], CPU_CP.
15:0	/	/	/

3.3.5.30. PLL_DDR0 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0310			Register Name: PLL_DDR0_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL. PLL bias control [4:0].
15:0	/	/	/

3.3.5.31. PLL_PERI0 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0320			Register Name: PLL_PERI0_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL. PLL bias control [4:0].
15:0	/	/	/

3.3.5.32. PLL_PERI1 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0328			Register Name: PLL_PERI1_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL. PLL bias control [4:0].
15:0	/	/	/

3.3.5.33. PLL_GPU Bias Register (Default Value: 0x0003_0000)

Offset: 0x0330			Register Name: PLL_GPU_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL. PLL bias control [4:0].
15:0	/	/	/

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3.3.5.34. PLL_VIDEO0 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0340			Register Name: PLL_VIDEO0_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL. PLL bias control [4:0].
15:0	/	/	/

3.3.5.35. PLL_VIDEO1 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0348			Register Name: PLL_VIDEO1_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL. PLL bias control [4:0].
15:0	/	/	/

3.3.5.36. PLL_VE Bias Register (Default Value: 0x0003_0000)

Offset: 0x0358			Register Name: PLL_VE_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL. PLL bias control [4:0].
15:0	/	/	/

3.3.5.37. PLL_DE Bias Register (Default Value: 0x0003_0000)

Offset: 0x0360			Register Name: PLL_DE_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL. PLL bias control [4:0].
15:0	/	/	/

3.3.5.38. PLL_HSIC Bias Register (Default Value: 0x0003_0000)

Offset: 0x0370			Register Name: PLL_HSIC_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/

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20:16	R/W	0x3	PLL_BIAS_CTRL. PLL bias control [4:0].
15:0	/	/	/

3.3.5.39. PLL_AUDIO Bias Register (Default Value: 0x0003_0000)

Offset: 0x0378			Register Name: PLL_AUDIO_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL. PLL bias control [4:0].
15:0	/	/	/

3.3.5.40. PLL_CPUX Tuning Register (Default Value: 0x4440_4000)

Offset: 0x0400			Register Name: PLL_CPUX_TUN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x4	VCO_RNG_CTRL. VCO range control [2:0].
27	/	/	/
26:24	R/W	0x4	KVCO_GAIN_CTRL. KVCO gain control [2:0].
23	/	/	/
22:16	R/W	0x40	CNT_INIT_CTRL. Counter initial control [6:0].
15	R/W	0x0	C_OD0. C-REG-OD0 for verify.
14:8	R/W	0x40	C_B_IN. C-B-IN [6:0] for verify.
7	R/W	0x0	C_OD1. C-REG-OD1 for verify.
6:0	R	0x0	C_B_OUT. C-B-OUT [6:0] for verify.

3.3.5.41. CPUX_AXI Configuration Register (Default Value: 0x0000_0001)

Offset: 0x0500			Register Name: CPUX_AXI_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select

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			00: OSC24M 01: CCU_32K 10: RC16M 11: PLL_CPUX CPUX Clock = Clock Source CPUX_AXI Clock = Clock Source/M CPUX _APB Clock = Clock Source/N
23:10	/	/	/
9:8	R/W	0x0	CPUX _APB_FACTOR_N. Factor N.(N = FACTOR_N +1) The range is from 1 to 4
7:2	/	/	/
1:0	R/W	0x1	FACTOR_ M Factor M.(M= FACTOR_M +1) The range is from 1 to 4

3.3.5.42. PSI_AHB1_AHB2 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0510			**Register Name: PSI_AHB1_AHB2_CFG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: CCU_32K 10: RC16M 11: PLL_PERI0(1X) PSI_AHB1_AHB2 CLK = Clock Source/M/N.
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N 00: 1 01: 2 10: 4 11: 8
7:2	/	/	/
1:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range is from 1 to 4

3.3.5.43. AHB3 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x051C	**Register Name: AHB3_CFG_REG**

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Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: CCU_32K 10: PSI 11: PLL_PERI0(1X) AHB3 CLK = Clock Source/M/N.
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N 00: 1 01: 2 10: 4 11: 8
7:2	/	/	/
1:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range is from 1 to 4

3.3.5.44. APB1 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x520			Register Name: APB1_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: CCU_32K 10: PSI 11: PLL_PERI0(1X) APB1 CLK = Clock Source/M/N.
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N 00: 1 01: 2 10: 4 11: 8
7:2	/	/	/
1:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range is from 1 to 4

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3.3.5.45. APB2 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x524			Register Name: APB2_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: CCU_32K 10: PSI 11: PLL_PERI0(1X) APB2 CLK = Clock Source/M/N.
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N 00: 1 01: 2 10: 4 11: 8
7:2	/	/	/
1:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range is from 1 to 4

3.3.5.46. MBUS Configuration Register (Default Value: 0xC000_0000)

Offset: 0x540			Register Name: MBUS_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	CLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON MBUS CLK = Clock Source/M.
30	R/W	0x1	MBUS_RST. MBUS Reset 0: Assert 1: De-assert
29:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERI0(2X)

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			10: PLL_DDR0 11: PLL_PERI0(4X)
23:3	/	/	/
2:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range is from 1 to 8

3.3.5.47. DE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0600			Register Name: DE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 0: PLL_DE 1: PLL_PERI0(2X)
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range is from 1 to 16

3.3.5.48. DE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x060C			Register Name: DE_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DE_RST. DE Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DE_GATING. Gating Clock For DE 0: Mask 1: Pass

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3.3.5.49. DI Clock Register (Default Value: 0x0000_0000)

Offset: 0x0620			Register Name: DI_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 0: PLL_PERI0(1X) 1: PLL_PERI1(1X)
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range is from 1 to 16

3.3.5.50. DI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x062C			Register Name: DI_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DI_RST. DI Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DI_GATING. Gating Clock For DI 0: Mask 1: Pass

3.3.5.51. GPU Clock Register (Default Value: 0x0000_0000)

Offset: 0x0670			Register Name: GPU_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.

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30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 0: PLL_GPU 1: /
23:3	/	/	/
2:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range is from 1 to 8

3.3.5.52. GPU Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x067C			Register Name: GPU_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	GPU_RST. GPU Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	GPU_GATING. Gating Clock For GPU 0: Mask 1: Pass

3.3.5.53. CE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0680			Register Name: CE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 0: OSC24M 1: PLL_PERI0(2X)
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N 00: 1 01: 2

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			10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range is from 1 to 16

3.3.5.54. CE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x068C			Register Name: CE_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	CE_RST. CE Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	CE_GATING. Gating Clock For CE 0: Mask 1: Pass

3.3.5.55. VE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0690			Register Name: VE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/Divider M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 0: PLL_VE 1: /
23:3	/	/	/
2:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range is from 1 to 8

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3.3.5.56. VE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x069C			Register Name: VE_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	VE_RST. VE Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	VE_GATING. Gating Clock For VE 0: Mask 1: Pass

3.3.5.57. EMCE Clock Register (Default Value: 0x0000_0000)

Offset: 0x06B0			Register Name: EMCE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 0: OSC24M 1: PLL_PERI0(2X)
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N 00: /1 01: /2 10: /4 11: /8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_ M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15

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3.3.5.58. EMCE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x06BC			Register Name: EMCE_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	EMCE_RST. EMCE Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	EMCE_GATING. Gating Clock For EMCE 0: Mask 1: Pass

3.3.5.59. VP9 Clock Register (Default Value: 0x0000_0000)

Offset: 0x06C0			Register Name: VP9_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/Divider M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 0: PLL_VE 1: PLL_PERI0(2X)
23:3	/	/	/
2:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 7.

3.3.5.60. VP9 Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x06CC			Register Name: VP9_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	VP9_RST. VP9 Reset. 0: Assert 1: De-assert

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15:1	/	/	/
0	R/W	0x0	VP9_GATING. Gating Clock For VP9 0: Mask 1: Pass

3.3.5.61. DMA Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x070C			Register Name: DMA_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DMA_RST. DMA Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DMA_GATING. Gating Clock For DMA 0: Mask 1: Pass

3.3.5.62. MSGBOX Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x071C			Register Name: MSGBOX_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	MSGBOX_RST. MSGBOX Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	MSGBOX_GATING. Gating Clock For MSGBOX 0: Mask 1: Pass

3.3.5.63. SPINLOCK Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x072C			Register Name: SPINLOCK_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	SPINLOCK_RST.

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			SPINLOCK Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	SPINLOCK_GATING. Gating Clock For SPINLOCK 0: Mask 1: Pass

3.3.5.64. HSTIMER Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x073C			Register Name: HSTIMER_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	HSTIMER_RST. HSTIMER Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	HSTIMER_GATING. Gating Clock For HSTIMER 0: Mask 1: Pass

3.3.5.65. AVS Clock Register (Default Value: 0x0000_0000)

Offset: 0x0740			Register Name: AVS_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = OSC24M.
30:0	/	/	/

3.3.5.66. DBGSYS Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x078C			Register Name: DBGSYS_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DBGSYS_RST. DBGSYS Reset.

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			0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DBGSYS_GATING. Gating Clock For DBGSYS 0: Mask 1: Pass

3.3.5.67. PSI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x079C			Register Name: PSI_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	PSI_RST. PSI Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	PSI_GATING. Gating Clock For PSI 0: Mask 1: Pass

3.3.5.68. PWM Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x07AC			Register Name: PWM_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	PWM_RST. PWM Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	PWM_GATING. Gating Clock For PWM 0: Mask 1: Pass

3.3.5.69. IOMMU Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x07BC			Register Name: IOMMU_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/

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0	R/W	0x0	IOMMU_GATING. Gating Clock For IOMMU 0: Mask 1: Pass

3.3.5.70. DRAM Clock Register (Default Value: 0x0100_0000)

Offset: 0x0800			Register Name: DRAM_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	MODULE_RST. Module Reset 0: Assert 1: De-assert SCLK = Clock Source/M.
29:28	/	/	/
27	R/WAC	0x0	SDRCLK_UPD. SDRCLK Configuration 0 update. 0:Invalid 1:Valid Setting this bit will validate Configuration 0. It will be auto cleared after the Configuration 0 is valid.
26	/	/	/
25:24	R/W	0x1	CLK_SRC_SEL. Clock Source Select 00: PLL_DDR0 Others: /
23:2	/	/	/
1:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range is from 1 to 4

3.3.5.71. MBUS Master Clock Gating Register (Default Value: 0x0000_0000)

Offset: 0x0804			Register Name: MBUS_MAT_CLK_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11	R/W	0x0	DI_MCLK_GATING. Gating MBUS Clock For DE_Interlace 0: Mask 1: Pass
10:9	/	/	/
8	R/W	0x0	CSI_MCLK_GATING.

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			Gating MBUS Clock For CSI 0: Mask 1: Pass
7:6	/	/	/
5	R/W	0x0	NAND_MCLK_GATING. Gating MBUS Clock For NAND 0: Mask 1: Pass
4	/	/	/
3	R/W	0x0	TS_MCLK_GATING. Gating MBUS Clock For TS 0: Mask 1: Pass
2	R/W	0x0	CE_MCLK_GATING. Gating MBUS Clock For CE 0: Mask 1: Pass
1	R/W	0x0	VE_MCLK_GATING. Gating MBUS Clock For VE 0: Mask 1: Pass
0	R/W	0x0	DMA_MCLK_GATING. Gating MBUS Clock For DMA 0: Mask 1: Pass

NOTE

DE MCLK is put in internal module for control.

3.3.5.72. DRAM Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x080C			Register Name: DRAM_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DRAM_RST. DRAM Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DRAM_GATING. Gating Clock For DRAM 0: Mask

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			1: Pass

3.3.5.73. NAND_0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0810			Register Name: NAND_0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: OSC24M 001: PLL_PERI0(1X) 010: PLL_PERI1(1X) 011: PLL_PERI0(2X) 100: PLL_PERI1(2X) 1XX:/
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15

3.3.5.74. NAND_1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0814			Register Name: NAND_1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL.

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			Clock Source Select 000: OSC24M 001: PLL_PERI0(1X) 010: PLL_PERI1(1X) 011: PLL_PERI0(2X) 100: PLL_PERI1(2X) 1XX:/
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15

3.3.5.75. NAND Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x082C			Register Name: NAND_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	NAND_RST. NAND Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	NAND_GATING. Gating Clock For NAND 0: Mask 1: Pass

3.3.5.76. SMHC0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0830			Register Name: SMHC0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.

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30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: OSC24M 001: PLL_PERI0(2X) 010: PLL_PERI1(2X) 011: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15

3.3.5.77. SMHC1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0834			Register Name: SMHC1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: OSC24M 001: PLL_PERI0(2X) 010: PLL_PERI1(2X) 011: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M

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			Factor M.(M= FACTOR_M +1) The range is from 1 to 16

3.3.5.78. SMHC2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0838			Register Name: SMHC2_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: OSC24M 001: PLL_PERI0(2X) 010: PLL_PERI1(2X) 011: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15

3.3.5.79. SMHC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x084C			Register Name: SMHC_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0x0	SMHC2_RST. SMHC2 Reset. 0: Assert 1: De-assert
17	R/W	0x0	SMHC1_RST. SMHC1 Reset. 0: Assert

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			1: De-assert
16	R/W	0x0	SMHC0_RST. SMHC0 Reset. 0: Assert 1: De-assert
15:3	/	/	/
2	R/W	0x0	SMHC2_GATING. Gating Clock For SMHC2 0: Mask 1: Pass
1	R/W	0x0	SMHC1_GATING. Gating Clock For SMHC1 0: Mask 1: Pass
0	R/W	0x0	SMHC0_GATING. Gating Clock For SMHC0 0: Mask 1: Pass

3.3.5.80. UART Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x090C			Register Name: UART_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	UART3_RST. UART3 Reset. 0: Assert 1: De-assert
18	R/W	0x0	UART2_RST. UART2 Reset. 0: Assert 1: De-assert
17	R/W	0x0	UART1_RST. UART1 Reset. 0: Assert 1: De-assert
16	R/W	0x0	UART0_RST. UART0 Reset. 0: Assert 1: De-assert
15:4	/	/	/
3	R/W	0x0	UART3_GATING. Gating Clock For UART3 0: Mask

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			1: Pass
2	R/W	0x0	UART2_GATING. Gating Clock For UART2 0: Mask 1: Pass
1	R/W	0x0	UART1_GATING. Gating Clock For UART1 0: Mask 1: Pass
0	R/W	0x0	UART0_GATING. Gating Clock For UART0 0: Mask 1: Pass

3.3.5.81. TWI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x091C			Register Name: TWI_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	TWI3_RST. TWI3 Reset. 0: Assert 1: De-assert
18	R/W	0x0	TWI2_RST. TWI2 Reset. 0: Assert 1: De-assert
17	R/W	0x0	TWI1_RST. TWI1 Reset. 0: Assert 1: De-assert
16	R/W	0x0	TWI0_RST. TWI0 Reset. 0: Assert 1: De-assert
15:4	/	/	/
3	R/W	0x0	TWI3_GATING. Gating Clock For TWI3 0: Mask 1: Pass
2	R/W	0x0	TWI2_GATING. Gating Clock For TWI2 0: Mask 1: Pass

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1	R/W	0x0	TWI1_GATING. Gating Clock For TWI1 0: Mask 1: Pass
0	R/W	0x0	TWI0_GATING. Gating Clock For TWI0 0: Mask 1: Pass

3.3.5.82. SCR Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x093C			Register Name: SCR_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	SCR1_RST. SCR1 Reset. 0: Assert 1: De-assert
16	R/W	0x0	SCR0_RST. SCR0 Reset. 0: Assert 1: De-assert
15:2	/	/	/
1	R/W	0x0	SCR1_GATING. Gating Clock For SCR1 0: Mask 1: Pass
0	R/W	0x0	SCR0_GATING. Gating Clock For SCR0 0: Mask 1: Pass

3.3.5.83. SPI0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0940			Register Name: SPI0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select

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			000: OSC24M 001: PLL_PERI0(1X) 010: PLL_PERI1(1X) 011: PLL_PERI0(2X) 100: PLL_PERI1(2X) 1XX:/
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15

3.3.5.84. SPI1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0944			Register Name: SPI1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: OSC24M 001: PLL_PERI0(1X) 010: PLL_PERI1(1X) 011: PLL_PERI0(2X) 100: PLL_PERI1(2X) 1XX:/
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/

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3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15

3.3.5.85. SPI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x096C			Register Name: SPI_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	SPI1_RST. SPI1 Reset. 0: Assert 1: De-assert
16	R/W	0x0	SPI0_RST. SPI0 Reset. 0: Assert 1: De-assert
15:2	/	/	/
1	R/W	0x0	SPI1_GATING. Gating Clock For SPI1 0: Mask 1: Pass
0	R/W	0x0	SPI0_GATING. Gating Clock For SPI0 0: Mask 1: Pass

3.3.5.86. EMAC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x097C			Register Name: EMAC_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	EMAC_RST. EMAC Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	EMAC_GATING. Gating Clock For EMAC 0: Mask 1: Pass

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3.3.5.87. TS Clock Register (Default Value: 0x0000_0000)

Offset: 0x09B0			Register Name: TS_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 0: OSC24M 1: PLL_PERI0(1X)
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15

3.3.5.88. TS Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x09BC			Register Name: TS_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	TS0_RST. TS0 Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	TS0_GATING. Gating Clock For TS0 0: Mask 1: Pass

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3.3.5.89. CIR-TX Clock Register (Default Value: 0x0000_0000)

Offset: 0x09C0			Register Name: CIRTX_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 0: CCU_32K 1: OSC24M
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15

3.3.5.90. CIR-TX Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x09CC			Register Name: CIRTX_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	CIRTX_RST. CIRTX Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	CIRTX_GATING. Gating Clock For CIRTX 0: Mask 1: Pass

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3.3.5.91. THS Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x09FC			Register Name: THS_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	THS_RST. THS Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	THS_GATING. Gating Clock For THS 0: Mask 1: Pass

3.3.5.92. I2S/PCM3 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A0C			Register Name: I2S/PCM3_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: PLL_AUDIO 01: PLL_AUDIO(2X) 10: PLL_AUDIO(4X) 11: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N 00: 1 01: 2 10: 4 11: 8
7:0	/	/	/

3.3.5.93. I2S/PCM0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A10			Register Name: I2S/PCM0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

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31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: PLL_AUDIO 01: PLL_AUDIO(2X) 10: PLL_AUDIO(4X) 11: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N 00: 1 01: 2 10: 4 11: 8
7:0	/	/	/

3.3.5.94. I2S/PCM1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A14			Register Name: I2S/PCM1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: PLL_AUDIO 01: PLL_AUDIO(2X) 10: PLL_AUDIO(4X) 11: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N 00: 1 01: 2 10: 4 11: 8

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7:0	/	/	/

3.3.5.95. I2S/PCM2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A18			Register Name: I2S/PCM2_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: PLL_AUDIO 01: PLL_AUDIO(2X) 10: PLL_AUDIO(4X) 11: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N 00: 1 01: 2 10: 4 11: 8
7:0	/	/	/

3.3.5.96. I2S/PCM Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A1C			Register Name: I2S/PCM_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	I2S/PCM3_RST. I2S/PCM3 Reset. 0: Assert 1: De-assert
18	R/W	0x0	I2S/PCM2_RST. I2S/PCM2 Reset. 0: Assert 1: De-assert
17	R/W	0x0	I2S/PCM1_RST. I2S/PCM1 Reset. 0: Assert

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			1: De-assert
16	R/W	0x0	I2S/PCM0_RST. I2S/PCM0 Reset. 0: Assert 1: De-assert
15:4	/	/	/
3	R/W	0x0	I2S/PCM3_GATING. Gating Clock For I2S/PCM3 0: Mask 1: Pass
2	R/W	0x0	I2S/PCM2_GATING. Gating Clock For I2S/PCM2 0: Mask 1: Pass
1	R/W	0x0	I2S/PCM1_GATING. Gating Clock For I2S/PCM1 0: Mask 1: Pass
0	R/W	0x0	I2S/PCM0_GATING. Gating Clock For I2S/PCM0 0: Mask 1: Pass

3.3.5.97. OWA Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A20			Register Name: OWA_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: PLL_AUDIO 01: PLL_AUDIO(2X) 10: PLL_AUDIO(4X) 11: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N 00: 1 01: 2

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			10: 4 11: 8
7:0	/	/	/

3.3.5.98. OWA Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A2C			Register Name: OWA_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	OWA_RST. OWA Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	OWA_GATING. Gating Clock For OWA 0: Mask 1: Pass

3.3.5.99. DMIC Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A40			Register Name: DMIC_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: PLL_AUDIO 01: PLL_AUDIO(2X) 10: PLL_AUDIO(4X) 11: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N 00: 1 01: 2 10: 4 11: 8
7:0	/	/	/

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3.3.5.100. DMIC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A4C			Register Name: DMIC_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DMIC_RST. DMIC Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DMIC_GATING. Gating Clock For DMIC 0: Mask 1: Pass

3.3.5.101. AUDIO_HUB Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A60			Register Name: AUDIO_HUB_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: PLL_AUDIO 01: PLL_AUDIO(2X) 10: PLL_AUDIO(4X) 11: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N 00: 1 01: 2 10: 4 11: 8
7:0	/	/	/

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3.3.5.102. AUDIO_HUB Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A6C			Register Name: AUDIO_HUB_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	AUDIO_HUB _RST. AUDIO_HUB Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	AUDIO_HUB _GATING. Gating Clock For AUDIO_HUB 0: Mask 1: Pass

3.3.5.103. USB0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A70			Register Name: USB0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING_OHCI0. Gating Special Clock For OHCI0 0: Clock is OFF 1: Clock is ON
30	R/W	0x0	USBPHY0_RST. USB PHY0 Reset 0: Assert 1: De-assert
29	R/W	0x0	SCLK_GATING_USBPHY0. Gating Special Clock For USBPHY0 0: Clock is OFF 1: Clock is ON SCLK is from OSC24M
28:26	/	/	/
25:24	R/W	0x0	OHCI0_12M_SRC_SEL OHCI0 12M Source Select 00: 12MHz divided from 48MHz 01: 12MHz divided from 24MHz 10: LOSC 11: /
23:0	/	/	/

3.3.5.104. USB1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A74	Register Name: USB1_CLK_REG

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Bit	Read/Write	Default/Hex	Description
31	/	/	/
30	R/W	0x0	USBPHY1_RST. USB PHY1 Reset 0: Assert 1: De-assert
29	R/W	0x0	SCLK_GATING_USBPHY1. Gating Special Clock For USBPHY1 0: Clock is OFF 1: Clock is ON
28:0	/	/	/

3.3.5.105. USB3 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A7C			Register Name: USB3_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING_OHCI3. Gating Special Clock For OHCI3 0: Clock is OFF 1: Clock is ON
30	R/W	0x0	USBPHY3_RST. USB PHY3 Reset 0: Assert 1: De-assert
29	R/W	0x0	SCLK_GATING_USBPHY3. Gating Special Clock For USBPHY3 0: Clock is OFF 1: Clock is ON SCLK is from OSC24M
28	R/W	0x0	USBHSIC_RST. USB HSIC Reset 0: Assert 1: De-assert
27	R/W	0x0	SCLK_GATING_12M_HSIC Gating Special 12M Clock For HSIC 0: Clock is OFF 1: Clock is ON SCLK is OSC24M/2
26	R/W	0x0	SCK_GATING_HSIC Gating Special Clock For HSIC 0: Clock is OFF 1: Clock is ON The special clock is from PLL_HSIC
25:24	R/W	0x0	OHCI3_12M_SRC_SEL

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			OHCI3 12M Source Select 00: 12M divided from 48MHz 01: 12M divided from 24MHz 10: LOSC 11: /
23:0	/	/	/

3.3.5.106. USB Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A8C			Register Name: USB_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	USBOTG_RST. USBOTG Reset. 0: Assert 1: De-assert
23	R/W	0x0	USBEHCI3_RST. USBEHCI3 Reset. 0: Assert 1: De-assert
22	/	/	/
21	R/W	0x0	USB3.0_HOST_RST. USB3.0_HOST. 0: Assert 1: De-assert
20	R/W	0x0	USBEHCI0_RST. USBEHCI0 Reset. 0: Assert 1: De-assert
19	R/W	0x0	USBOHCI3_RST. USBOHCI3 Reset. 0: Assert 1: De-assert
18:17	/	/	/
16	R/W	0x0	USBOHCI0_RST. USBOHCI0 Reset. 0: Assert 1: De-assert
15:9	/	/	/
8	R/W	0x0	USBOTG_GATING. Gating Clock For USBOTG 0: Mask 1: Pass
7	R/W	0x0	USBEHCI3_GATING.

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			Gating Clock For USBEHCI3 0: Mask 1: Pass
6	/	/	/
5	R/W	0x0	USB3.0_HOST_GATING. Gating Clock For USB3.0_HOST 0: Mask 1: Pass
4	R/W	0x0	USBEHCI0_GATING. Gating Clock For USBEHCI0 0: Mask 1: Pass
3	R/W	0x0	USBOHCI3_GATING. Gating Clock For USBOHCI3 0: Mask 1: Pass
2:1	/	/	/
0	R/W	0x0	USBOHCI0_GATING. Gating Clock For USBOHCI0 0: Mask 1: Pass

3.3.5.107. PCIE Ref Clock Register (Default Value: 0x0000_0000)

Offset: 0x0AB0			Register Name: PCIE_REF_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source. PLL_PERI0(4X) dividing frequency can get REFCLK_100M.
30	R/W	0x0	PAD_CLK_OUTPUT_GATING. Pad Clock Output Gating 0: Clock Output is OFF 1: Clock Output is ON
29:0	/	/	/

3.3.5.108. PCIE MAXI Clock Register (Default Value: 0x0000_0000)

Offset: 0x0AB4			Register Name: PCIE_MAXI_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING.

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			Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M. Clock Source is PLL_PERI0(1X).
30:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15

3.3.5.109. PCIE AUX Clock Register (Default Value: 0x0000_0000)

Offset: 0x0AB4			Register Name: PCIE_AUX_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M. Clock Source is OSC24M.
30:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 31

3.3.5.110. PCIE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0ABC			Register Name: PCIE_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	PCIE_POWERUP_RST. PCIE Power up Reset. 0: Assert 1: De-assert
16	R/W	0x0	PCIE_P_RST. PCIE P Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	PCIE _GATING. Gating Clock For PCIE 0: Mask 1: Pass

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3.3.5.111. HDMI Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B00			Register Name: HDMI_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: PLL_VIDEO0(1X) 01: PLL_VIDEO1(1X) 10: PLL_VIDEO1(4X) 11: /
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15

3.3.5.112. HDMI Slow Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B04			Register Name: HDMI_SLOW_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = OSC24M.
30:0	/	/	/

3.3.5.113. HDMI CEC Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B10			Register Name: HDMI_CEC_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = OSC24M.

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30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 0: CCU_32K 1: PLL_PERI0(2X)/36621 =32.769kHz
23:0	/	/	/

3.3.5.114. HDMI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0B1C			Register Name: HDMI_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	HDMI_SUB_RST. HDMI_SUB Reset. 0: Assert 1: De-assert
16	R/W	0x0	HDMI_MAIN_RST. HDMI_MAIN Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	HDMI_GATING. Gating Clock For HDMI 0: Mask 1: Pass

3.3.5.115. DISPLAY_IF_TOP Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0B5C			Register Name: DISPLAY_IF_TOP_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DISPLAY_IF_TOP_RST. DISPLAY_IF_TOP Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DISPLAY_IF_TOP_GATING. Gating Clock For DISPLAY_IF_TOP 0: Mask 1: Pass

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3.3.5.116. TCON LCD Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B60			Register Name: TCON_LCD_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL_VIDEO0(1X) 001: PLL_VIDEO0(4X) 010: PLL_VIDEO1(1X) Others:/
23:0	/	/	/

3.3.5.117. TCON LCD Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0B7C			Register Name: TCON_LCD_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	TCON_LCD_RST. TCON_LCD Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	TCON_LCD_GATING. Gating Clock For TCON_LCD 0: Mask 1: Pass

3.3.5.118. TCON TV Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B80			Register Name: TCON_TV_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:27	/	/	/

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26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL_VIDEO0(1X) 001: PLL_VIDEO0(4X) 010: PLL_VIDEO1(1X) 011: PLL_VIDEO1(4X) Others:/
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15

3.3.5.119. TCON TV Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0B9C			Register Name: TCON_TV_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	TCON_TV0_RST. TCON_TV0 Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	TCON_TV0_GATING. Gating Clock For TCON_TV0 0: Mask 1: Pass

3.3.5.120. CSI MISC Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C00			Register Name: CSI_MISC_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	CSI_CCI_CLK_GATING Gating CCI Special Clock,Clock source is OSC24M 0: Clock is OFF 1: Clock is ON

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3.3.5.121. CSI TOP Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C04			Register Name: CSI_TOP_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000:PLL_VIDEO0(1X) 001:/ 010:PLL_VE 011:PLL_PERI0(1X) Others:/
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15

3.3.5.122. CSI Master Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C08			Register Name: CSI0_MST_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MCLK0_GATING Gating CSI Master Clock0,this clock output to external device. 0: Clock is OFF 1: Clock is ON MCLK0 = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_VIDEO0(1X) 010: PLL_PERI0(1X) 011: PLL_PERI1(1X) Others:/
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1)

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			FACTOR_M is from 0 to 31

3.3.5.123. CSI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0C2C			Register Name: CSI_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	CSI_RST. CSI Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	CSI_GATING. Gating Clock For CSI 0: Mask 1: Pass

3.3.5.124. HDMI HDCP Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C40			Register Name: HDMI_HDCP_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: PLL_PERI0(1X) 01: PLL_PERI1(1X) Others:/
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15

3.3.5.125. HDMI HDCP Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0C4C			Register Name: HDMI_HDCP_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	HDMI_HDCP_RST.

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			HDMI_HDCP Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	HDMI_HDCP_GATING. Gating Clock For HDMI_HDCP 0: Mask 1: Pass

3.3.5.126. CCU Security Switch Register (Default Value: 0x0000_0000)

Offset: 0x0F00			Register Name: CCU_SEC_SWITCH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	MBUS_SEC. MBUS clock register security. 0: Secure 1: Non-secure
1	R/W	0x0	BUS_SEC. Bus relevant registers' security. 0: Secure 1: Non-secure
0	R/W	0x0	PLL_SEC. PLL relevant registers' security. 0: Secure 1: Non-secure

3.3.5.127. PLL Lock Debug Control Register (Default Value: 0x0000_0000)

Offset: 0x0F04			Register Name: PLL_LOCK_DBG_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DBG_EN Debug Enable 0: Disable 1: Enable
30:25	/	/	/
24:20	R/W	0x0	DBG_SEL Debug Select 00000: PLL_CPUX 00001: / 00010: PLL_DDR0 00011:/ 00100: PLL_PERI0(2X)

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			00101: PLL_PERI1(2X) 00110:PLL_GPU 00111:/ 01000: PLL_VIDEO0(4X) 01001: PLL_VIDEO1(4X) 01010: / 01011: PLL_VE 01100: PLL_DE 01101: / 01110: PLL_HSIC 01111: PLL_AUDIO Others: /
19	/	/	/
18:17	R/W	0x0	UNLOCK_LEVEL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
16	R/W	0x0	LOCK_LEVEL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
15:0	/	/	/

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3.4. CPUX Configuration

3.4.1. Overview

CPUX Configuration(CPUX_CFG) module is used to configure CLUSTER0 control, including power on,reset, cache, debug, and check the status of CPU. It will be used when you want to disable/enable the CPU, cluster switch, CPU status check, and debug, etc.

The CPUX_CFG module includes C0_CPUX_CFG and CPU_SUBSYS_CTRL.

The C0_CPUX_CFG module is used for configuring CLUSTER0, such as reset, control, cache, debug, CPU status.

The CPU_SUBSYS_CTRL module is used for the system resource control of CPU sub-system, such as CCI-400,GIC-400,JTAG.

Features:

- CPU Reset System:CORE reset,debug circuit reset and other reset function.
- CPU related control: interface control, CP15 control, power on and power down control.
- CPU status check: idle status, SMP status, interrupt status and so on.
- CPU debug related register for control and status.

3.4.2. Block Diagram

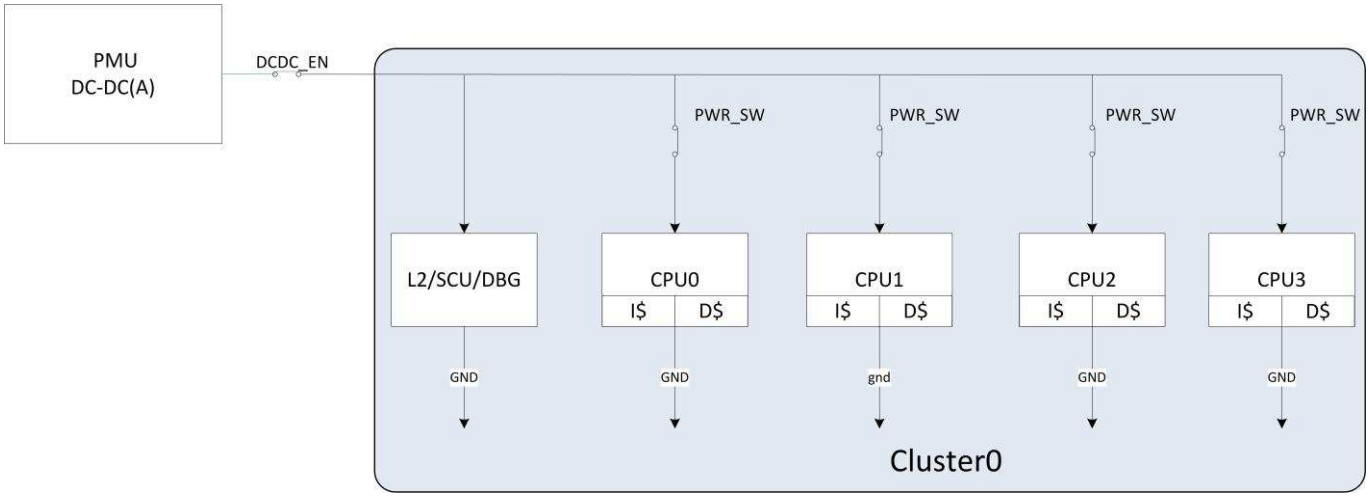


Figure 3-16. CPUX_CFG Block Diagram

The figure above lists the power domain of CLUSTER in default. All power switch of CPU core are default to power on.All CPU pwron_rst is de-assert, core reset of CPU0 de-assert,core reset of CPU [3:1] assert.

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Since each CPU core and its appended circuits have the same power domain, the processor and related L1 cache, neon and vfp should be taken as a whole core.

3.4.3. Operations and Functional Descriptions

3.4.3.1. Signal Description

For the detail of CPUX signal, please refer to ***ARM Cortex-A53 TRM***.

3.4.3.2. L2 Idle Mode

When the L2 of Cluster needs to enter WFI mode, firstly make sure the CPU0/1/2/3 of Cluster enter WFI mode, which can be checked through **Cluster CPU Status Register**, and then pull high the **ACINACTM** of Cluster by writing related register bit to 1, and then check whether L2 enters idle status by checking whether the **STANDBYWFIL2** is high. Remember to set the **ACINACTM** to low when exiting the L2 idle mode.

3.4.3.3. CPUX Reset System

The CPU reset includes **core reset**, **power-on reset** and **H_Reset**. And their scopes rank: **core reset** < **power-on Reset** < **H_Reset**. The description of all reset signal in CPUX Reset System is as follows.

Table 3-7. Reset Signal Description

Reset signal	Description
CORE_RST	This is the primary reset signal which resets the corresponding core logic that includes NEON and VFP, Debug, ETM, breakpoint and watchpoint logic. This maps to a warm reset that covers reset of the processor logic.
PWRON_RST	This power-on reset signal resets all the processor logic, including the Debug, ETM trace unit, breakpoint, watchpoint logic, and performance monitors logic. This maps to a cold reset that covers reset of the processor logic and the integrated debug functionality. This does not reset debug logic in the debug power domain. Including CORE_RST/ETM_RST/DBG_RST.
AXI2MBUS_RST	Reset the AXI2MBUS interface logic circuit.
L2_RST	This single, cluster-wide signal resets the L2 memory system and the logic in the SCU.
ETM_RST	Reset ETM debug logic circuit.
DBG_RST	Reset only the debug, and breakpoint and watchpoint logic in the processor power domain. It also resets the debug logic for each processor in the debug power domain.
SOC_DBG_RST	Reset all the debug logic including DBG_RST.
MBIST_RST	Resets all resettable registers in the cluster, for entry into, and exit from, MBIST mode.
H_RST	Including PWRON_RST/L2_RST/MBIST_RST/SOC_DBG_RST/C0_CPUX_CFG.
CPU_SUBSYS_RST	Including C0_H_RST/GIC-400/CPU_SUBSYS_CTRL.

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3.4.3.4. Operation Principle

The CPU-related operation needs proper configuration of CPUCFG related register, as well as related system control resource including BUS, clock ,reset and power control.

3.4.4. Cluster Configuration Register List

Module Name	Base Address
CPU_CFG	0x09010000

Register Name	Offset	Description
C0_RST_CTRL	0x0000	Cluster 0 Reset Control Register
/	/	/
C0_CTRL_REG0	0x0010	Cluster 0 Control Register0
C0_CTRL_REG1	0x0014	Cluster 0 Control Register1
C0_CTRL_REG2	0x0018	Cluster 0 Control Register2
/	/	/
CACHE_CFG_REG	0x0024	Cache Configuration Register
/	/	/
RVBARADDR0_L	0x0040	Reset Vector Base Address Register0_L
RVBARADDR0_H	0x0044	Reset Vector Base Address Register0_H
RVBARADDR1_L	0x0048	Reset Vector Base Address Register1_L
RVBARADDR1_H	0x004C	Reset Vector Base Address Register1_H
RVBARADDR2_L	0x0050	Reset Vector Base Address Register2_L
RVBARADDR2_H	0x0054	Reset Vector Base Address Register2_H
RVBARADDR3_L	0x0058	Reset Vector Base Address Register3_L
RVBARADDR3_H	0x005C	Reset Vector Base Address Register3_H
/	/	/
C0_CPU_STATUS	0x0080	Cluster 0 CPU Status Register
L2_STATUS_REG	0x0084	Cluster 0 L2 Status Register
/	/	/
DBG_REG0	0x00C0	Cluster 0 Debug Control Register0
DBG_REG1	0x00C4	Cluster 0 Debug Control Register1

3.4.5. Cluster Configuration Register Description

3.4.5.1. Cluster Reset Control Register(Default Value: 0x13FF_0101)

Offset: 0x0000	Register Name: C_RST_CTRL

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Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R/W	0x1	DDR_RST AXI2MBUS logic circuit Rest. 0: assert 1: de-assert
27:26	/	/	/
25	R/W	0x1	MBIST_RST CPUBIST Reset. The reset signal for test. 0: assert 1: de-assert
24	R/W	0x1	SOC_DBG_RST. Cluster SOC Debug Reset 0: assert 1: de-assert.
23:20	R/W	0xF	ETM_RST Cluster ETM Reset Assert. 0: assert 1: de-assert
19:16	R/W	0xF	DBG_RST Cluster Debug Reset Assert. 0: assert 1: de-assert
15:9	/	/	/
8	R/W	0x1	L2_RST. Cluster L2 Cache Reset 0: assert 1: de-assert.
7:4	/	/	/
3:0	R/W	0x1	CORE_RESET. Cluster CPU[3:0] Reset Assert. 0: assert 1: de-assert.

3.4.5.2. Cluster Control Register0(Default Value:0x8000_0000)

Offset: 0x0010			Register Name: C0_CTRL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	SYSBAR_DISABLE. Disable broadcasting of barriers onto system bus 0: Barriers are broadcast onto system bus,this requires an AMBA4 interconnect. 1: Barriers are not broadcast onto the system bus.This is compatible

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			with an AXI3 interconnect.
30	R/W	0x0	BROADCAST_INNER. Enable broadcasting of Inner Shareable transactions 0: Inner shareable transactions are not broadcasted externally. 1: Inner shareable transactions are broadcasted externally.
29	R/W	0x0	BROADCAST_OUTER. Enable broadcasting of outer shareable transactions 0: Outer Shareable transactions are not broadcasted externally. 0: Outer Shareable transactions are broadcasted externally.
28	R/W	0x0	BROADCAST_CACHE_MAINT Enable broadcasting of cache maintenance operations to downstream caches 0: Cache maintenance operations are not broadcasted to downstream caches. 1: Cache maintenance operations are broadcasted to downstream caches.
27:24	R/W	0x0	AA64nAA32 Register width state.Determines which execution state the processor boots into after a cold reset. 0: AArch32 1: AArch64 The processor should boot from BROM when in AArch32 state while it should boot from the RVBARADDR(Reset Vector Base Address) when in AArch64 state.
23:12	/	/	/
11:8	R/W	0x0	CP15S_DISABLE. Disable write access to some secure CP15 register.
7:5	/	/	/
4	R/W	0x0	L2_RST_DISABLE. Disable automatic L2 cache invalidate at reset. 0: L2 cache is reset by hardware. 1: L2 cache is not reset by hardware.
3:0	R/W	0x0	L1_RST_DISABLE. Disable automatic Cluster CPU[3:0] L1 cache invalidate at reset. 0: L1 cache is reset by hardware. 1: L1 cache is not reset by hardware.

3.4.5.3. Cluster Control Register1(Default Value:0x0000_0000)

Offset: 0x0014			**Register Name: C_CTRL_REG1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ACINACTM. Snoop interface is inactive and no longer accepting requests.

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			0: Snoop interface is active 1: Snoop interface is inactive

3.4.5.4. Cluster Control Register2(Default :0x0000_0010)

Offset: 0x0018			Register Name: C_CTRL_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	EVENTI Event input for processor wake-up from WFE state. This bit must remain HIGH for at least one clock cycle to be visible by the cores.
23:20	R/W	0x0	EXM_CLR[3:0] Clear the status of interface.
19:17	/	/	/
16	R/W	0x0	CLREXMONREQ Clearing of the external global exclusive monitor request. When this bit is asserted, it acts as a WFE wake-up event to all the cores in the MPCore device.
15:12	R/W	0x0	CRYPTODISABLE Disable the Cryptography Extensions.
11:9	/	/	/
8	R/W	0x0	L2FLUSHREQ L2 hardware flush request.
7:5	/	/	/
4	R/W	0x1	GICCDISABLE. Globally disables the CPU interface logic and routes the "External" signals directly to the processor: 0: Enable the GIC CPU interface logic. 1: Disable the GIC CPU interface logic.
3:0	/	/	/

3.4.5.5. Cache Configuration Register (Default Value: 0x0000_001A)

Offset: 0x0024			Register Name: CACHE_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:3	R/W	0x3	EMA Cache SRAM EMA control port
2:1	R/W	0x1	EMAW Cache SRAM EMAW control port
0	R/W	0x0	EMAS Cache SRAM EMAS control port

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3.4.5.6. Reset Vector Base Address Register0_L(Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: RVBARADDR0_L
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	R/W	0x0	RVBARDDR[31:2] Reset Vector Base Address[39:2] for executing in 64-bit state (AArch64)of CPU0.
1:0	/	/	/

3.4.5.7. Reset Vector Base Address Register0_H(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: RVBARADDR0_H
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	RVBARDDR[39:32] Reset Vector Base Address[39:2]for executing in 64-bit state (AArch64) of CPU0.

3.4.5.8. Reset Vector Base Address Register1_L(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: RVBARADDR1_L
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	R/W	0x0	RVBARDDR[31:2] Reset Vector Base Address[39:2] for executing in 64-bit state (AArch64)of CPU1.
1:0	/	/	/

3.4.5.9. Reset Vector Base Address Register1_H(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: RVBARADDR1_H
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	RVBARDDR[39:32] Reset Vector Base Address[39:2]for executing in 64-bit state (AArch64) of CPU1.

3.4.5.10. Reset Vector Base Address Register2_L(Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: RVBARADDR2_L
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	R/W	0x0	RVBARDDR[31:2]

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			Reset Vector Base Address[39:2] for executing in 64-bit state (AArch64)of CPU2.
1:0	/	/	/

3.4.5.11. Reset Vector Base Address Register2_H(Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: RVBARADDR2_H
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	RVBARDDR[39:32] Reset Vector Base Address[39:2]for executing in 64-bit state (AArch64) of CPU2.

3.4.5.12. Reset Vector Base Address Register3_L(Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: RVBARADDR3_L
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	R/W	0x0	RVBARDDR[31:2] Reset Vector Base Address[39:2] for executing in 64-bit state (AArch64)of CPU3.
1:0	/	/	/

3.4.5.13. Reset Vector Base Address Register3_H(Default Value: 0x0000_0000)

Offset: 0x005C			Register Name: RVBARADDR3_H
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	RVBARDDR[39:32] Reset Vector Base Address[39:2]for executing in 64-bit state (AArch64) of CPU3.

3.4.5.14. Cluster CPU Status Register(Default : 0x000E_0000)

Offset: 0x0080			Register Name: C_CPU_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R	0x0	SMP_AMP CPU[3:0] is in Symmetric Multiprocessing mode or Asymmetric Multiprocessing mode. 0: AMP mode 1: SMP mode

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23:20	/	/	/
19:16	R	0xE	STANDBYWFI. Indicates if Cluster CPU[3:0] is in WFI standby mode. 0: Processor not in WFI standby mode. 1: Processor in WFI standby mode
15:12	/	/	/
11:8	R	0x0	STANDBYWFE. Indicates if Cluster CPU[3:0] is in the WFE standby mode. 0: Processor not in WFE standby mode 1: Processor in WFE standby mode
7:1	/	/	/
0	R	0x0	STANDBYWFIL2. Indicates if the Cluster L2 memory system is in WFI standby mode. 0: Cluster L2 not in WFI standby mode 1: Cluster L2 in WFI standby mode

3.4.5.15. L2 Status Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: L2_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10	R	0x0	L2FLUSHDONE L2 hardware flush complete
9	R	0x0	EVENTO Event output. This bit is asserted HIGH for 3 clock cycles when any core in the cluster executes an SEV instruction.
8	R	0x0	CLREXMONACK Clearing of the external global exclusive monitor acknowledge.
7:0	/	/	/

3.4.5.16. Cluster 0 Debug Control Register0(Default Value:0x0000_000F)

Offset: 0x00C0			Register Name: DBG_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DBGL1RSTDISABLE Disable L1 data cache automatic invalidate on reset functionality. 0: Enable automatic invalidation of L1 data cache on reset 1: Disable automatic invalidation of L1 data cache on reset
15:12	/	/	/
11:8	R/W	0x0	DBGRESTART[3:0] External restart requests.
7:4	/	/	/

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3:0	R/W	0xF	C_DBGPWRDUP. Cluster Powered-up 0: Core is powered down 1: Core is powered up

3.4.5.17. Cluster 0 Debug Control Register1 (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: DBG_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:12	R/W	0x0	DBGRESTARTED[3:0] Handshake for DBGRESTART.
11:8	R	0x0	C_DBGRSTREQ. Warm reset request.
7:4	R	0x0	C_DBGNOPWRDWN. No power-down request. Debugger has requested that processor is not powered down. Debug no power down[3:0].
3:0	R	0x0	C_DBGPWRUPREQ. Power up request. Debug power up request[3:0] 0: Do not request that the core is powered up 1: Request that the core is powered up

3.4.6. CPU Subsystem Control Register List

Module Name	Base Address
CPU_SUBSYS_CTRL	0x08100000

Register Name	Offset	Description
GENER_CTRL_REG0	0x0000	General Control Register0
GENER_CTRL_REG1	0x0004	General Control Register1
GIC_JTAG_RST_CTRL	0x000C	GIC and Jtag Reset Control Register
C0_INT_EN	0x0010	Cluster0 Interrupt Enable Control Register
IRQ_FIQ_STATUS	0x0014	GIC IRQ/FIQ Status Register
GENER_CTRL_REG2	0x0018	General Control Register2

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3.4.7. CPU Subsystem Control Register Description

3.4.7.1. General Control Register0(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: GENER_CTRL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	GIC_CFGSDISABLE. Disables write access to some secure GIC registers.

3.4.7.2. General Control Register1(Default Value: 0x0000_000E)

Offset: 0x0004			Register Name: GENER_CTRL_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:4	R/W	0x0	QOSOVERRIDE. If HIGH, internally generated values override the **ARQOS** and **AWQOS** inputs. One bit exists for each slave interface.
3:2	R/W	0x3	ACCHANNELEN. If LOW, then AC requests are not issued on the corresponding slave interface. One bit exists for each slave interface.
1	R/W	0x1	CCI_CLK_ON. Set 1 means CCI Clock always on.
0	R/W	0x0	CCI_CLK_OFF. Set 1 means CCI Clock always off. **NOTE** **When CCI_CLK_OFF and CCI_CLK_ON are valid at the same time ,CCI_CLK_OFF has the higher priority than CCI_CLK_ON.**

3.4.7.3. GIC and Jtag Reset Control Register(Default Value: 0x0000_0F01)

Offset: 0x000C			Register Name: GIC_JTAG_RST_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:16	R/W	0x0	EXM_CLR[3:0] Clear the status of interface, for debug
15:12	/	/	/
11	R/W	0x1	CS_RST

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			CoreSight Reset. 0: assert 1: de-assert.
10	R/W	0x1	DAP_RST DAP Reset. 0: assert 1: de-assert.
9	R/W	0x1	PORTRST Jtag portrst. 0: assert 1: de-assert.
8	R/W	0x1	TRST. Jtag trst. 0: assert 1: de-assert.
7:1	/	/	/
0	R/W	0x1	GIC_RESET. Gic_reset_cpu_reg 0: assert 1: de-assert.

3.4.7.4. Cluster 0 Interrupt Enable Register(Default Value: 0x0000_FFFF)

Offset: 0x0010			Register Name: C0_INT_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFFFF	C0_GIC_EN Interrupt enable control register. Mask irq_out/firq_out to system domain.

3.4.7.5. GIC IRQ/FIQ Status Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: IRQ_FIQ_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0000	FIQ_OUT[15:0]
15:0	R/W	0x0000	IRQ_OUT[15:0]

3.4.7.6. General Control Register2(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: GENER_CTRL_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/

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16	R/W	0x0	CDBGRSTACK
15:1	/	/	/
0	R/W	0x0	C0_TSCLKCHANGE

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3.5. IOMMU

3.5.1. Overview

IOMMU(I/O Memory management unit) is designed for product specific memory requirements. It maps the virtual address(sent by peripheral access memory)to the physical address. IOMMU allows multiple ways to manage the location of physical address, and it can use physical address which has potentially conflict mapping for different processes to allocate memory space, and also allow application of non-continuous address mapping to continuous virtual address space.

Features:

- Supports virtual address to physical address mapping by hardware implementation
- Supports DE0/2, VE_R, VE, CSI, VP9 parallel address mapping
- Supports DE0/2, VE_R, VE, CSI, VP9 bypass function independently
- Supports DE0/2,VE_R,VE,CSI,VP9 prefetch independently
- Supports DE0/2,VE_R,VE,CSI,VP9 Interrupt handing mechanism independently
- Supports level1 and level2 TLB for special using, and level2 TLB for sharing
- Supports TLB Fully cleared and Partially disabled
- Supports trigger PTW behavior when TLB miss
- Supports checking the permission
- Performance: Average (L1+L2)TLB Hit rate: up to 99.9%, Average Latency: 5±1cycle

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3.5.2. Block Diagram

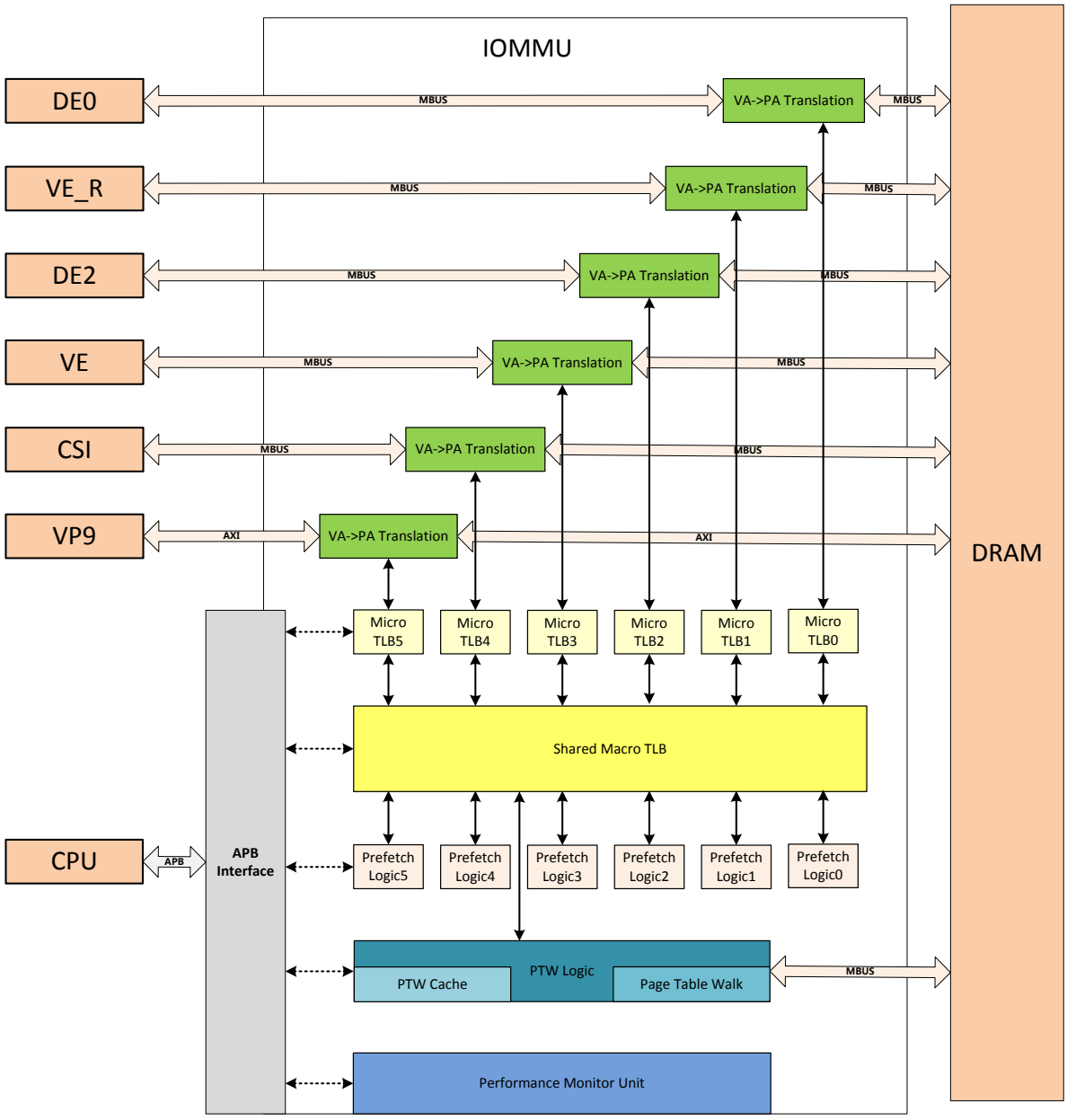


Figure 3-17. IOMMU Block Diagram

3.5.3. Operations and Functional Descriptions

3.5.3.1. Clock Sources

IOMMU contains two clock domains in the module. Address mapping generated by MBUS clock domain, and Register and interrupt processing generated by APB clock domain. The two domains are asynchronous, and they are from different clock sources.

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3.5.3.2. Operation Modes

3.5.3.2.1. Initialization

- Release the IOMMU reset signal by writing 1 to the IOMMU Reset Register bit[31];
- Write the base address of the first TLB to the IOMMU Translation Table Base Register;
- Set up the IOMMU Interrupt Enable Register;
- Enable the IOMMU by configuring the IOMMU Enable Register in the final.

3.5.3.2.2. Address Operates

In the process of address mapping, The peripheral virtual address VA[31:12] are retrieved in the Level1 TLB, when TLB hit, the mapping finished, or they are retrieved in the level2 TLB in the same way. If TLB hit, it will write the mapping to the Level1 TLB, and this shows Level1 TLB hit. If Level1 and level2 TLB retrieved miss, it will trigger the PTW. After opening peripheral bypass function, the corresponding register is IOMMU Bypass Register, IOMMU will not map the address for peripheral typed the address, and it will output the virtual address as physical address.The typical application is as follows.

- **Micro TLB hit**

a) The master device sends a transfer command, and also sends the address to the corresponding Micro TLB, and searches virtual address corresponding to the level2 page table;
b) If Micro TLB hit, it will return a corresponding physical addresses and the level2 page table of permission Index;
c) Address transform module converts the virtual address into physical address, and checks the permissions at the same time. If pass, transfer is completed.

- **Micro TLB miss, Macro TLB hit**

a) The master device send a transfer command, and also send the address to the corresponding Micro TLB, and searches virtual address corresponding to the level 2 page table;
b) If Micro TLB misses, then continue to search Macro TLB;
c) If Macro TLB misses, it will return the level2 page table to Micro TLB;
d) Micro receives the page table, and put it to Micro TLB(if this Micro TLB is full, there has replace activities), at the same time send page table entries to address translation module;
e) Address transform module converts the virtual address into physical address, and checks the permissions at the same time. If pass, transfer is completed.

- **Micro TLB miss, Micro TLB miss, PTW Cache hit**

a) The master device sends a transfer command, and also sends the address to the corresponding Micro TLB, and searches virtual address corresponding to the level 2 page table;
b) If Micro TLB misses, then continue to search Macro TLB;
c) If Macro TLB misses, theniw will send the request to the PTW to return the corresponding page table;
d) PTW first accesses PTW Cache, confirms the required level 1 page table to exist in the PTW Cache, sends the page table to PTW logic;
e) PTW logic returns the corresponding level2 page table from memory page table according to Level1 page table, checks the effectiveness, and sends to Macro TLB;
f) Macro TLB stores the level 2 page table (may happen replace activities), and will return the level 2 page table to Micro

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TLB;
g) Micro TLB receives the page table entries, puts in the Micro TLB (if this Micro TLB is full, there will happen replace activities), and sends page table entries to address translation module;
h) Address transform module converts the virtual address into physical address, and checks the permissions at the same time. If pass, transfer is completed.

- **Micro TLB miss, Micro TLB miss, PTW Cache miss**

a) The master device sends a transfer command, and also sends the address to the corresponding Micro TLB, and searches virtual address corresponding to the level2 page table;
b) If Micro TLB misses, then continue to search Macro TLB;
c) If Macro TLB misses, theniw will send the request to the PTW to return the corresponding page table;
d) PTW accesses PTW Cache, there is no needing Level1 page table;
e) PTW accesses memory, gets the corresponding Level1 page table and stores in the PTW Cache;
f) PTW logic returns the corresponding level2 page table from memory page table according to Level1 page table, checks the effectiveness, and sends to Macro TLB;
g) Macro TLB stores the level2 page table (may happen replace activities), and will return the level 2 page table to Micro TLB;
h) Micro TLB receives the page table entries, puts in the Micro TLB (if this Micro TLB is full, there will happen replace activities), and sends page table entries to address translation module;
i) Address transform module converts the virtual address into physical address, and checks the permissions at the same time. If pass, transfer is completed.

- **Permission error**

a) Permission check is always performs in the address conversion;
b) Once the permission check makes mistake, new access of the master suspends, before this visit continues;
c) Set the error status register;
d) Trigger interrupt.

- **Invalid Level1 page table**

a) Invalid Level1 page table checks when PTW logic reads the new level page table from memory;
b) The PTW read sequentially two page table entries from the memory (64-bit data, a complete cache line), and stores in the PTW cache;
c) If the current page table is detected invalid, then the error flag is set, and the interrupt is triggered, the cache line need to be invalidated.

NOTE

Invalid page table has two situations: the reading target page table from the memory is invalid; and the page table stored in PTW Cache with target page table is found to be invalid after using;
If a page table is invalid,then total cache line need to be invalidated, that is two page tables.

- **Invalid level2 page table**

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a) Invalid level2 page table checks when Macro TLB reads the new level page table from memory;
b) The Macro TLB read sequentially two page table entries from the memory (64-bit data, a complete cache line), and stores in the Macro TLB;
c) If the current page table is detected invalid, then the error flag is set, and the interrupt is triggered, the cache line need to be invalidated.

NOTE

Invalid page table has two situations: the reading target page table from the memory is invalid; and the page table stored in Macro TLB with target page table is found to be invalid after using;
If a page table is invalid,then total cache line need to be invalidated, that is two page tables.

Internal address switch process shows in Figure 3-18.

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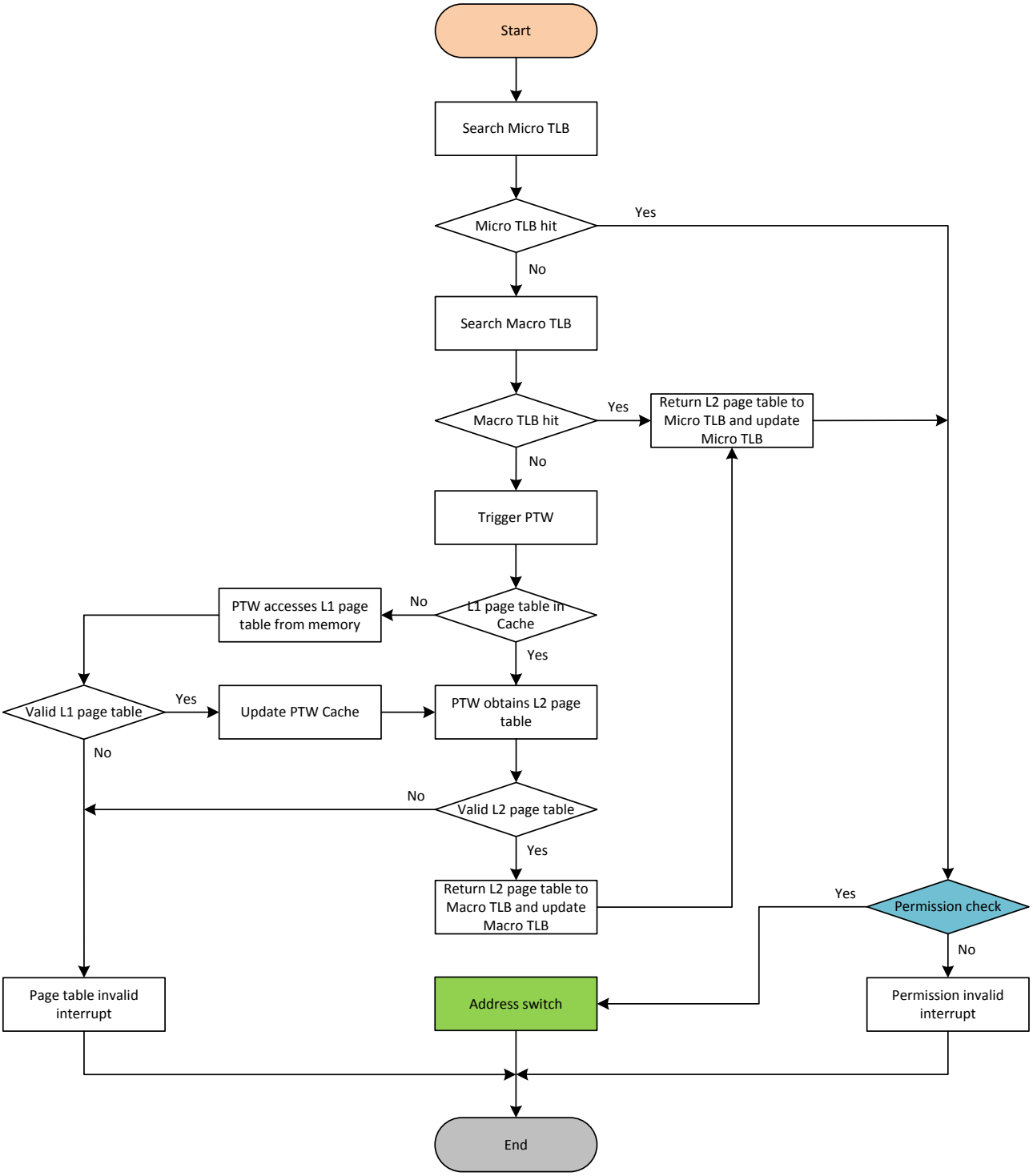


Figure 3-18. Internal Switch Process

3.5.3.2.3. VA-PA Mapping

IOMMU page table is defined as Level2 mapping, the first level is 1M address space mapping, the second level is 4K address space. This version does not support 1K, 16K and other page table size. IOMMU supports a page table only, its meaning is:

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a) All peripherals connected to IOMMU use the same virtual address space;
b) The virtual address space of the peripherals can overlap;
c) Different virtual addresses can map to the same physical address space;

Base address of the page table is defined by software, and need 16 KByte address alignment; Page table of the Level2 table item need 1 KByte address alignment. A complete VA-PA address translation process is shown in Figure 3-19.

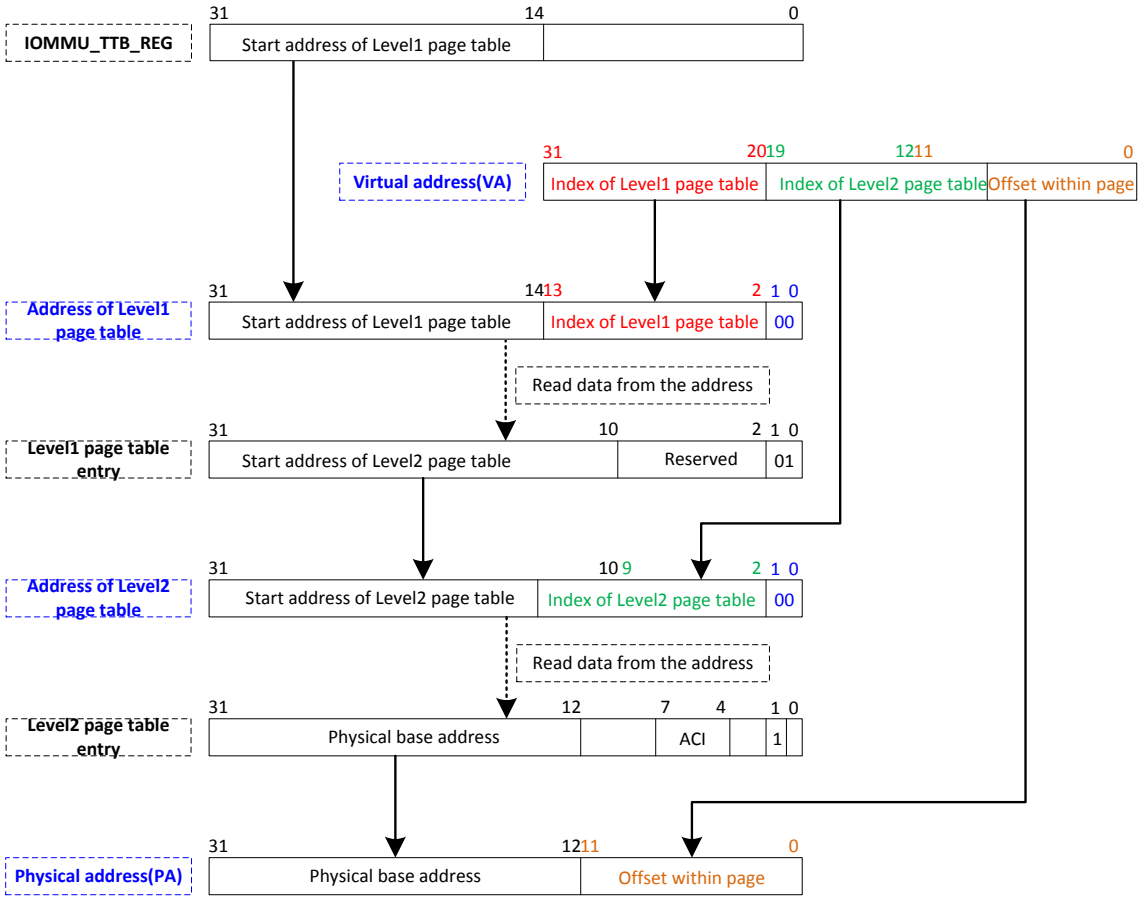


Figure 3-19. VA-PA Switch Process

3.5.3.2.4. Clear and Invalidate TLB

When more page table content refresh or table address changes, all VA-PA mapping which has been cached in TLB will no longer be valid , then you need configure **IOMMU TLB Flush Enable Register** to clear the TLB or PTW Cache. First suspend the TLB or Cache access, then configure the corresponding Flush bit of **IOMMU TLB Flush Enable Register** , after operation takes effect, related peripherals can continue to send new access memory operations.

When some page table is invalid or incorrect mapping, you can set the TLB Invalidation relevant register to invalidate TLB VA-PA mapping pairs. First, write target address to **IOMMU TLB Invalidation Address Register**;then, set configuration values to **IOMMU TLB Invalidation Address Mask Register** , the requirements are as follows:
a) The value of **IOMMU TLB Invalidation Address Mask Register** cannot be less than the IOMMU TLB Invalidation Address Register.
b) The higher bit of **IOMMU TLB Invalidation Address Mask Register** must be continuous 1, the lower bit must be

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continuous 0, for example ,0xfffff000, 0xffffe000, 0xffffc000, 0xffff8000, 0xffff0000 belongs to the legal value; and 0xffffd000, 0xffffb000, 0xfffa000, 0xffff9000, 0xffff7000 belongs to illegal values.

Finally, Configure **IOMMU TLB Invalidation Enable Register** to enable invalid operation. Among the method of invalid address is that target address AND mask address gets maximum valid bit and determines destination address range.The figure is as follows.

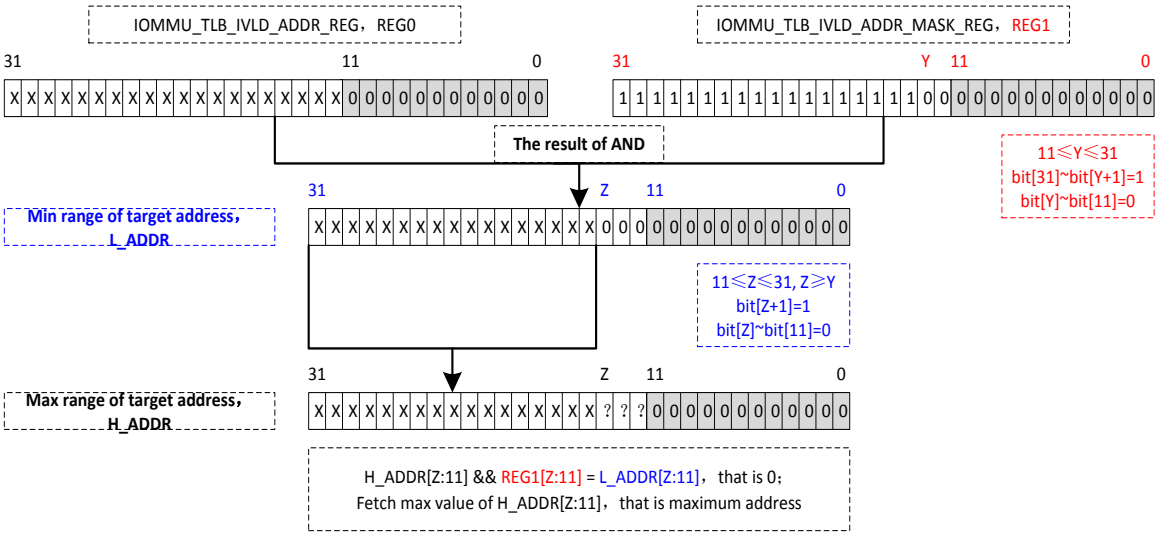


Figure 3-20. Invalid TLB Address Range

For example:

a) When the value of **IOMMU TLB Invalidation Address Mask Register** is 0xFFFFF000 by default,the result of AND is target address,that is ,invalid target address.

b) When the value of **IOMMU TLB Invalidation Address Mask Register** is 0xFFFF0000, the value of **IOMMU TLB Invalidation Address Register** is 0xEEEE1000, then target address range is from 0xEEEE0000 to 0xEEEEF000.

c) When the value of **IOMMU TLB Invalidation Address Mask Register** is 0xFFFFC000, the value of **IOMMU TLB Invalidation Address Register** is 0xEEEE8000, then target address range is from 0xEEEE8000 to 0xEEEEB000.

d) When the value of **IOMMU TLB Invalidation Address Mask Register** is 0xFFFF8000, the value of **IOMMU TLB Invalidation Address Register** is 0xEEEEC000, then target address range is from 0xEEEE8000 to 0xEEEEF000.

e) When the value of **IOMMU TLB Invalidation Address Mask Register** is 0xFFFFC000, the value of **IOMMU TLB Invalidation Address Register** is 0xEEEE0000, then target address range is from 0xEEEE0000 to 0xEEEE3000.

3.5.3.3. Page Table Format

3.5.3.3.1. Level1 Page Table

The format of Level1 page table is as follows.

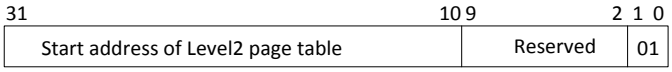


Figure 3-21. Level1 Page Table Format

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Bit[31:10]: Base address of Level2 page table;
Bit[9:2]: Reserved;
Bit[1:0]: 01 is valid page table;others are fault;

3.5.3.3.2. Level2 Page Table

The format of Level2 page table is as follows.

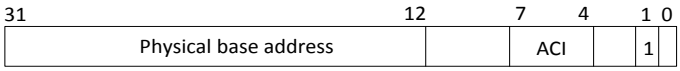


Figure 3-22. Level1 Page Table Format

Bit[31:12]: Physical address of 4K address;
Bit[11:8]: Reserved;
Bit[7:4]: ACI， permission control index; correspond to permission control bit of **IOMMU Domain Authority Control Register**;
Bit[3:2]: Reserved;
Bit[1]: 1 is valid page table; 0 is fault;
Bit[0]: Reserved

3.5.3.3.3. Permission Index

The read/write access control of series register such as **IOMMU Domain Authority Control Register** is as follows.

11	10	9	8	7	6	5	4	3	2	1	0
W	R	W	R	W	R	W	R	W	R	W	R

Figure 3-23. Read/Write Permission Control

Bit[1:0]/Bit[17:16]: Master0 read/write permission control;
Bit[3:2]/Bit[19:18]: Master1 read/write permission control;
Bit[5:4]/Bit[21:20]: Master2 read/write permission control;
Bit[7:6]/Bit[23:22]: Master3 read/write permission control;
Bit[9:8]/Bit[25:24]: Master4 read/write permission control;
Bit[11:10]/Bit[27:26]: Master5 read/write permission control;

The value of **IOMMU Domain Authority Control Register** is read-only by default. Other registers can configure through system requirement. In address switch process, the corresponding relation between ACI and Domain is as follows.

Table 3-8. Relation between ACI and Domain

ACI	Domain	Register
0	Domain 0	IOMMU Domain Authority Control Register 0
1	Domain 1	IOMMU Domain Authority Control Register 0

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2	Domain 2	IOMMU Domain Authority Control Register 1
3	Domain 3	IOMMU Domain Authority Control Register 1
4	Domain 4	IOMMU Domain Authority Control Register 2
5	Domain 5	IOMMU Domain Authority Control Register 2
6	Domain 6	IOMMU Domain Authority Control Register 3
7	Domain 7	IOMMU Domain Authority Control Register 3
8	Domain 8	IOMMU Domain Authority Control Register 4
9	Domain 9	IOMMU Domain Authority Control Register 4
10	Domain 10	IOMMU Domain Authority Control Register 5
11	Domain 11	IOMMU Domain Authority Control Register 5
12	Domain 12	IOMMU Domain Authority Control Register 6
13	Domain 13	IOMMU Domain Authority Control Register 6
14	Domain 14	IOMMU Domain Authority Control Register 7
15	Domain 15	IOMMU Domain Authority Control Register7

After enabled **IOMMU Domain Authority Overwrite Register**, the read/write control permission can override all **IOMMU Domain Authority Control Register**.

3.5.4. Programming Guidelines

3.5.4.1. IOMMU Reset

In order to shield the influence of IOMMU reset ,be sure IOMMU is never opened, or no unfinished bus operation, or DRAM and peripherals already open the corresponding switch before the IOMMU module software reset operation.

3.5.4.2. IOMMU Enable

Before opening the IOMMU address mapping function, Translation Table Base register should be correctly configured, or all the masters are in the bypass state, or all the masters do not send the bus command.

3.5.4.3. Configure TTB

Operating the register must close IOMMU address mapping function, namely IOMMU_ENABLE_REG [0] is 0; or Bypass function of all masters is set to 1, or no the state of transfer bus commands.

3.5.4.4. Clear TTB

In the Flush operation, all TLB/Cache access will be suspended; but the operation entered the TLB will continue to complete before the Flush starts.

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3.5.4.5. Read/Write VA Data

For virtual address, read and write the corresponding physical address data, be sure IOMMU module address mapping function is normal or not. First, make sure to read or write, and then configure the target virtual address or write data, then start to read or write function, after being finished, check if the results is as expected.

3.5.4.6. PMU Statistics

When PMU function is used for the first time, **Set IOMMU PMU Enable Register** can be enabled; when reading the relevant Register, **Clear IOMMU PMU Enable Register** need be enabled; when PMU function is used next time, **first IOMMU PMU Clear Register** is set, after counter is cleared, **Set IOMMU PMU Enable Register** can be enabled. Given a level2 page table administers continuous 4 KB address, if Micro TLB misses in continuous virtual address, there may need to return a level2 page table to hit from Macro TLB; but the hit number is not recorded in the Macro TLB hit and Micro TLB hit related register. So true hit rate calculation is as follows:

Hit Rate = N1/M1 + (1-N1/M1)*N2/M2

N1: Micro TLB hit number

M1: Micro TLB access number

N2: Macro TLB hit number

M2: Macro TLB access number

3.5.5. Register List

Module Name	Base Address
IOMMU	0x030F0000

Register Name	Offset	Description
IOMMU_RESET_REG	0x0010	IOMMU Reset Register
IOMMU_ENABLE_REG	0x0020	IOMMU Enable Register
IOMMU_BYPASS_REG	0x0030	IOMMU Bypass Register
IOMMU_AUTO_GATING_REG	0x0040	IOMMU Auto Gating Register
IOMMU_WBUF_CTRL_REG	0x0044	IOMMU Write Buffer Control Register
IOMMU_OOO_CTRL_REG	0x0048	IOMMU Out Of Order Control Register
IOMMU_4KB_BDY_PRT_CTRL_REG	0x004C	IOMMU 4KB Boundary Protect Control Register
IOMMU_TTB_REG	0x0050	IOMMU Translation Table Base Register
IOMMU_TLB_ENABLE_REG	0x0060	IOMMU TLB Enable Register
IOMMU_TLB_PREFETCH_REG	0x0070	IOMMU TLB Prefetch Register
IOMMU_TLB_FLUSH_ENABLE_REG	0x0080	IOMMU TLB Flush Enable Register
IOMMU_TLB_IVLD_ADDR_REG	0x0090	IOMMU TLB Invalidation Address Register
IOMMU_TLB_IVLD_ADDR_MASK_REG	0x0094	IOMMU TLB Invalidation Address Mask Register
IOMMU_TLB_IVLD_ENABLE_REG	0x0098	IOMMU TLB Invalidation Enable Register

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IOMMU_PC_IVLD_ADDR_REG	0x00A0	IOMMU PC Invalidation Address Register
IOMMU_PC_IVLD_ENABLE_REG	0x00A8	IOMMU PC Invalidation Enable Register
IOMMU_DM_AUT_CTRL_REG0	0x00B0	IOMMU Domain Authority Control Register 0
IOMMU_DM_AUT_CTRL_REG1	0x00B4	IOMMU Domain Authority Control Register 1
IOMMU_DM_AUT_CTRL_REG2	0x00B8	IOMMU Domain Authority Control Register 2
IOMMU_DM_AUT_CTRL_REG3	0x00BC	IOMMU Domain Authority Control Register 3
IOMMU_DM_AUT_CTRL_REG4	0x00C0	IOMMU Domain Authority Control Register 4
IOMMU_DM_AUT_CTRL_REG5	0x00C4	IOMMU Domain Authority Control Register 5
IOMMU_DM_AUT_CTRL_REG6	0x00C8	IOMMU Domain Authority Control Register 6
IOMMU_DM_AUT_CTRL_REG7	0x00CC	IOMMU Domain Authority Control Register 7
IOMMU_DM_AUT_OVWT_REG	0x00D0	IOMMU Domain Authority Overwrite Register
IOMMU_INT_ENABLE _REG	0x0100	IOMMU Interrupt Enable Register
IOMMU_INT_CLR _REG	0x0104	IOMMU Interrupt Clear Register
IOMMU_INT_STA _REG	0x0108	IOMMU Interrupt Status Register
IOMMU_INT_ERR_ADDR_REG0	0x0110	IOMMU Interrupt Error Address Register 0
IOMMU_INT_ERR_ADDR_REG1	0x0114	IOMMU Interrupt Error Address Register 1
IOMMU_INT_ERR_ADDR_REG2	0x0118	IOMMU Interrupt Error Address Register 2
IOMMU_INT_ERR_ADDR_REG3	0x011C	IOMMU Interrupt Error Address Register 3
IOMMU_INT_ERR_ADDR_REG4	0x0120	IOMMU Interrupt Error Address Register 4
IOMMU_INT_ERR_ADDR_REG5	0x0124	IOMMU Interrupt Error Address Register 5
IOMMU_INT_ERR_ADDR_REG6	0x0130	IOMMU Interrupt Error Address Register 6
IOMMU_INT_ERR_ADDR_REG7	0x0134	IOMMU Interrupt Error Address Register 7
IOMMU_INT_ERR_DATA_REG0	0x0150	IOMMU Interrupt Error Data Register 0
IOMMU_INT_ERR_DATA_REG1	0x0154	IOMMU Interrupt Error Data Register 1
IOMMU_INT_ERR_DATA_REG2	0x0158	IOMMU Interrupt Error Data Register 2
IOMMU_INT_ERR_DATA_REG3	0x015C	IOMMU Interrupt Error Data Register 3
IOMMU_INT_ERR_DATA_REG4	0x0160	IOMMU Interrupt Error Data Register 4
IOMMU_INT_ERR_DATA_REG5	0x0164	IOMMU Interrupt Error Data Register 5
IOMMU_INT_ERR_DATA_REG6	0x0170	IOMMU Interrupt Error Data Register 6
IOMMU_INT_ERR_DATA_REG7	0x0174	IOMMU Interrupt Error Data Register 7
IOMMU_L1PG_INT _REG	0x0180	IOMMU L1 Page Table Interrupt Register
IOMMU_L2PG_INT _REG	0x0184	IOMMU L2 Page Table Interrupt Register
IOMMU_VA_REG	0x0190	IOMMU Virtual Address Register
IOMMU_VA_DATA_REG	0x0194	IOMMU Virtual Address Data Register
IOMMU_VA_CONFIG_REG	0x0198	IOMMU Virtual Address Configuration Register
IOMMU_PMU_ENABLE _REG	0x0200	IOMMU PMU Enable Register
IOMMU_PMU_CLR _REG	0x0210	IOMMU PMU Clear Register
IOMMU_PMU_ACCESS_LOW_REG0	0x0230	IOMMU PMU Access Low Register 0
IOMMU_PMU_ACCESS_HIGH_REG0	0x0234	IOMMU PMU Access High Register 0
IOMMU_PMU_HIT_LOW_REG0	0x0238	IOMMU PMU Hit Low Register 0
IOMMU_PMU_HIT_HIGH_REG0	0x023C	IOMMU PMU Hit High Register 0
IOMMU_PMU_ACCESS_LOW_REG1	0x0240	IOMMU PMU Access Low Register 1
IOMMU_PMU_ACCESS_HIGH_REG1	0x0244	IOMMU PMU Access High Register 1
IOMMU_PMU_HIT_LOW_REG1	0x0248	IOMMU PMU Hit Low Register 1

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IOMMU_PMU_HIT_HIGH_REG1	0x024C	IOMMU PMU Hit High Register 1
IOMMU_PMU_ACCESS_LOW_REG2	0x0250	IOMMU PMU Access Low Register 2
IOMMU_PMU_ACCESS_HIGH_REG2	0x0254	IOMMU PMU Access High Register 2
IOMMU_PMU_HIT_LOW_REG2	0x0258	IOMMU PMU Hit Low Register 2
IOMMU_PMU_HIT_HIGH_REG2	0x025C	IOMMU PMU Hit High Register 2
IOMMU_PMU_ACCESS_LOW_REG3	0x0260	IOMMU PMU Access Low Register 3
IOMMU_PMU_ACCESS_HIGH_REG3	0x0264	IOMMU PMU Access High Register 3
IOMMU_PMU_HIT_LOW_REG3	0x0268	IOMMU PMU Hit Low Register 3
IOMMU_PMU_HIT_HIGH_REG3	0x026C	IOMMU PMU Hit High Register 3
IOMMU_PMU_ACCESS_LOW_REG4	0x0270	IOMMU PMU Access Low Register 4
IOMMU_PMU_ACCESS_HIGH_REG4	0x0274	IOMMU PMU Access High Register 4
IOMMU_PMU_HIT_LOW_REG4	0x0278	IOMMU PMU Hit Low Register 4
IOMMU_PMU_HIT_HIGH_REG4	0x027C	IOMMU PMU Hit High Register 4
IOMMU_PMU_ACCESS_LOW_REG5	0x0280	IOMMU PMU Access Low Register 5
IOMMU_PMU_ACCESS_HIGH_REG5	0x0284	IOMMU PMU Access High Register 5
IOMMU_PMU_HIT_LOW_REG5	0x0288	IOMMU PMU Hit Low Register 5
IOMMU_PMU_HIT_HIGH_REG5	0x028C	IOMMU PMU Hit High Register 5
IOMMU_PMU_ACCESS_LOW_REG6	0x02D0	IOMMU PMU Access Low Register 6
IOMMU_PMU_ACCESS_HIGH_REG6	0x02D4	IOMMU PMU Access High Register 6
IOMMU_PMU_HIT_LOW_REG6	0x02D8	IOMMU PMU Hit Low Register 6
IOMMU_PMU_HIT_HIGH_REG6	0x02DC	IOMMU PMU Hit High Register 6
IOMMU_PMU_ACCESS_LOW_REG7	0x02E0	IOMMU PMU Access Low Register 7
IOMMU_PMU_ACCESS_HIGH_REG7	0x02E4	IOMMU PMU Access High Register 7
IOMMU_PMU_HIT_LOW_REG7	0x02E8	IOMMU PMU Hit Low Register 7
IOMMU_PMU_HIT_HIGH_REG7	0x02EC	IOMMU PMU Hit High Register 7
IOMMU_PMU_TL _LOW_REG0	0x0300	IOMMU Total Latency Low Register 0
IOMMU_PMU_TL _HIGH_REG0	0x0304	IOMMU Total Latency High Register 0
IOMMU_PMU_TL _LOW_REG1	0x0310	IOMMU Total Latency Low Register 1
IOMMU_PMU_TL _HIGH_REG1	0x0314	IOMMU Total Latency High Register 1
IOMMU_PMU_TL _LOW_REG2	0x0320	IOMMU Total Latency Low Register 2
IOMMU_PMU_TL _HIGH_REG2	0x0324	IOMMU Total Latency High Register 2
IOMMU_PMU_TL _LOW_REG3	0x0330	IOMMU Total Latency Low Register 3
IOMMU_PMU_TL _HIGH_REG3	0x0334	IOMMU Total Latency High Register 3
IOMMU_PMU_TL _LOW_REG4	0x0340	IOMMU Total Latency Low Register 4
IOMMU_PMU_TL _HIGH_REG4	0x0344	IOMMU Total Latency High Register 4
IOMMU_PMU_TL _LOW_REG5	0x0350	IOMMU Total Latency Low Register 5
IOMMU_PMU_TL _HIGH_REG5	0x0354	IOMMU Total Latency High Register 5

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3.5.6. Register Description

3.5.6.1. IOMMU Reset Register (Default Value: 0x8003_003F)

Offset: 0x0010			Register Name: IOMMU_RESET _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	IOMMU_RESET IOMMU Software Reset Switch 0: Set reset signal 1: Release reset signal Before IOMMU software reset operation, ensure IOMMU never be opened; Or no unfinished bus operation; Or DRAM and the peripherals have opened the corresponding switch, for shielding the effects of IOMMU reset .
30:18	/	/	/
17	R/W	0x1	PTW_CACHE_RESET PTW Cache address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When PTW Cache occurs abnormal, the bit is used for resetting PTW Cache individually.
16	R/W	0x1	MACRO_TLB_RESET Macro TLB address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When PTW Cache occurs abnormal, the bit is used for resetting PTW Cache individually.
15:6	/	/	/
5	R/W	0x1	MASTER5_RESET Master5 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master5 occurs abnormal, the bit is used for resetting PTW Cache individually.
4	R/W	0x1	MASTER4_RESET Master4 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master4 occurs abnormal, the bit is used for resetting PTW Cache individually.
3	R/W	0x1	MASTER3_RESET Master3 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master3 occurs abnormal, the bit is used for resetting PTW Cache

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			individually.
2	R/W	0x1	MASTER2_RESET Master2 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master2 occurs abnormal, the bit is used for resetting PTW Cache individually.
1	R/W	0x1	MASTER1_RESET Master1 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master1 occurs abnormal, the bit is used for resetting PTW Cache individually.
0	R/W	0x1	MASTER0_RESET Master0 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master0 occurs abnormal, the bit is used for resetting PTW Cache individually.

3.5.6.2. IOMMU Enable Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: IOMMU_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ENABLE IOMMU module enable switch 0: Disable IOMMU 1: Enable IOMMU Before IOMMU address mapping function opens, configure the Translation Table Base register; or ensure all masters are in bypass status or no the status of sending bus demand （such as reset）

3.5.6.3. IOMMU Bypass Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: IOMMU_BYPASS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W	0x0	MASTER5_BYPASS Master5 bypass switch After open bypass function，IOMMU can not map the address of Master5 sending, and directly output the virtual address to MBUS as physical address.

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			0: Disable bypass function 1: Enable bypass function
4	R/W	0x0	MASTER4_BYPASS Master4 bypass switch After open bypass function，IOMMU can not map the address of Master4 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
3	R/W	0x0	MASTER3_BYPASS Master3 bypass switch After open bypass function，IOMMU can not map the address of Master3 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
2	R/W	0x0	MASTER2_BYPASS Master2 bypass switch After open bypass function，IOMMU can not map the address of Master2 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
1	R/W	0x0	MASTER1_BYPASS Master1 bypass switch After open bypass function，IOMMU can not map the address of Master1 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
0	R/W	0x0	MASTER0_BYPASS Master0 bypass switch After open bypass function，IOMMU can not map the address of Master0 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function

NOTE

Operating the register belongs to non-accurate timing sequence control function.That is, before the function is valid, master operation will complete address mapping function, and after the operation will not perform address mapping. It is suggested that master is in reset state or in no any bus operation before operating the register .

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3.5.6.4. IOMMU Auto Gating Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: IOMMU_AUTO_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	IOMMU_AUTO_GATING IOMMU circuit auto gating control. The purpose is decreasing power consumption of the module. 0: Disable auto gating function 1: Enable auto gating function

3.5.6.5. IOMMU Write Buffer Control Register (Default Value: 0x0000_003F)

Offset: 0x0044			Register Name: IOMMU_WBUF_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W	0x1	MASTER5_WBUF_CTRL Master5 write buffer control bit 0: Disable write buffer 1: Enable write buffer
4	R/W	0x1	MASTER4_WBUF_CTRL Master4 write buffer control bit 0: Disable write buffer 1: Enable write buffer
3	R/W	0x1	MASTER3_WBUF_CTRL Master3 write buffer control bit 0: Disable write buffer 1: Enable write buffer
2	R/W	0x1	MASTER2_WBUF_CTRL Master2 write buffer control bit 0: Disable write buffer 1: Enable write buffer
1	R/W	0x1	MASTER1_WBUF_CTRL Master1 write buffer control bit 0: Disable write buffer 1: Enable write buffer
0	R/W	0x1	MASTER0_WBUF_CTRL Master0 write buffer control bit 0: Disable write buffer 1: Enable write buffer

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3.5.6.6. IOMMU Out Of Order Control Register (Default Value: 0x0000_003F)

Offset: 0x0048			Register Name: IOMMU_OOO_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W	0x1	MASTER5_OOO_CTRL Master5 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order
4	R/W	0x1	MASTER4_OOO_CTRL Master4 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order
3	R/W	0x1	MASTER3_OOO_CTRL Master3 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order
2	R/W	0x1	MASTER2_OOO_CTRL Master2 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order
1	R/W	0x1	MASTER1_OOO_CTRL Master1 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order
0	R/W	0x1	MASTER0_OOO_CTRL Master0 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order

3.5.6.7. IOMMU 4KB Boundary Protect Control Register (Default Value: 0x0000_001F)

Offset: 0x004C			Register Name: IOMMU_4KB_BDY_PRT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/W	0x1	MASTER4_4KB_BDY_PRT_CTRL Master4 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect
3	R/W	0x1	MASTER3_4KB_BDY_PRT_CTRL Master3 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect
2	R/W	0x1	MASTER2_4KB_BDY_PRT_CTRL

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			Master2 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect
1	R/W	0x1	MASTER1_4KB_BDY_PRT_CTRL Master1 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect
0	R/W	0x1	MASTER0_4KB_BDY_PRT_CTRL Master0 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect  **NOTE** **When Master sends the burst of over 4KB boundary, IOMMU can split demand and data.**

3.5.6.8. IOMMU Translation Table Base Register (Default Value: 0x0000_0000)

Offset: 0x0050			**Register Name: IOMMU_TTB_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	R/W	0x0	TTB Level1 page table starting address, aligned to 16 KB.  **NOTE** **When operating the register , IOMMU address mapping function must be closed, namely IOMMU_ENABLE_REG is 0 ; Or Bypass function of all main equipment is set to 1 or not the state of transfer bus commands (such as setting).**
13:0	/	/	/

3.5.6.9. IOMMU TLB Enable Register (Default Value: 0x0003_003F)

Offset: 0x0060			**Register Name: IOMMU_TLB_ENABLE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x1	PTW_CACHE_ENABLE PTW Cache enable bit 0: Disable 1: Enable
16	R/W	0x1	MACRO_TLB_ENABLE Macro TLB enable bit 0: Disable

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			1: Enable
15:6	/	/	/
5	R/W	0x1	MICRO_TLB5_ENABLE Micro TLB5 enable bit 0: Disable 1: Enable
4	R/W	0x1	MICRO_TLB4_ENABLE Micro TLB4 enable bit 0: Disable 1: Enable
3	R/W	0x1	MICRO_TLB3_ENABLE Micro TLB3 enable bit 0: Disable 1: Enable
2	R/W	0x1	MICRO_TLB2_ENABLE Micro TLB2 enable bit 0: Disable 1: Enable
1	R/W	0x1	MICRO_TLB1_ENABLE Micro TLB1 enable bit 0: Disable 1: Enable
0	R/W	0x1	MICRO_TLB0_ENABLE Micro TLB0 enable bit 0: Disable 1: Enable

3.5.6.10. IOMMU TLB Prefetch Register (Default Value: 0x0000_0000)

Offset: 0x0070			Register Name: IOMMU_TLB_PREFETCH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W	0x0	MICRO_TLB5_PREFETCH Micro TLB5 prefetch enable 0: Disable 1: Enable
4	R/W	0x0	MICRO_TLB4_PREFETCH Micro TLB4 prefetch enable 0: Disable 1: Enable
3	R/W	0x0	MICRO_TLB3_PREFETCH Micro TLB3 prefetch enable 0: Disable 1: Enable

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2	R/W	0x0	MICRO_TLB2_PREFETCH Micro TLB2 prefetch enable 0: Disable 1: Enable
1	R/W	0x0	MICRO_TLB1_PREFETCH Micro TLB1 prefetch enable 0: Disable 1: Enable
0	R/W	0x0	MICRO_TLB0_PREFETCH Micro TLB0 prefetch enable 0: Disable 1: Enable

3.5.6.11. IOMMU TLB Flush Enable Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: IOMMU_TLB_FLUSH_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/WAC	0x0	PTW_CACHE_FLUSH Clear PTW Cache 0: No clear operation or clear operation completed 1: Enable is cleared After Flush operation completes, the bit can clear 0 automatically.
16	R/WAC	0x0	MACRO_TLB_FLUSH Clear Macro TLB 0: No clear operation or clear operation completed 1: Enable is cleared After Flush operation completes, the bit can clear 0 automatically.
15:6	/	/	/
5	R/WAC	0x0	MICRO_TLB5_FLUSH Clear Micro TLB5 0: No clear operation or clear operation completed 1: Enable is cleared After Flush operation completes, the bit can clear 0 automatically.
4	R/WAC	0x0	MICRO_TLB4_FLUSH Clear Micro TLB4 0: No clear operation or clear operation completed 1: Enable is cleared After Flush operation completes, the bit can clear 0 automatically.
3	R/WAC	0x0	MICRO_TLB3_FLUSH Clear Micro TLB3 0: No clear operation or clear operation completed 1: Enable is cleared After Flush operation completes, the bit can clear 0 automatically.

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2	R/WAC	0x0	MICRO_TLB2_FLUSH Clear Micro TLB2 0: No clear operation or clear operation completed 1: Enable is cleared After Flush operation completes, the bit can clear 0 automatically.
1	R/WAC	0x0	MICRO_TLB1_FLUSH Clear Micro TLB1 0: No clear operation or clear operation completed 1: Enable is cleared After Flush operation completes, the bit can clear 0 automatically.
0	R/WAC	0x0	MICRO_TLB0_FLUSH Clear Micro TLB1 0: No clear operation or clear operation completed 1: Enable is cleared After Flush operation completes, the bit can clear 0 automatically.

NOTE

When performing flush operation, all TLB/Cache access will be paused.
Before flush starts, the operation that has entered TLB continues to complete.

3.5.6.12. IOMMU TLB Invalidation Address Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: IOMMU_TLB_IVLD_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	0x0	TLB_IVLD_ADDR TLB invalid address, aligned to 4K
11:0	/	/	/

NOTE

When performing invalidation operation, TLB/Cache operation has not affected.
After or Before invalidation starts, there is no absolute relationship between same address switch operation and Invalidation operation.

3.5.6.13. IOMMU TLB Invalidation Address Mask Register (Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: IOMMU_TLB_IVLD_ADDR_MASK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:12	R/W	0x0	TLB_IVLD_ADDR_MASK TLB invalid address mask register, aligned to 4K
11:0	/	/	/

3.5.6.14. IOMMU TLB Invalidation Enable Register (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: IOMMU_TLB_IVLD_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/WAC	0x0	TLB_IVLD_ENABLE Enable TLB invalid operation 0: No-operation or operation completed 1: Enable is invalid After invalidation operation completed, the bit can clear 0 automatically. When operating Invalidation, TLB/Cache operation has not affected. After or Before Invalidation starts, there is no absolute relationship between same address switch operation and Invalidation operation.

3.5.6.15. IOMMU PC Invalidation Address Register (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: IOMMU_PC_IVLD_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	R/W	0x0	PC_IVLD_ADDR PTW Cache invalid address, aligned to 1M.
19:0	/	/	/

3.5.6.16. IOMMU PC Invalidation Enable Register (Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name: IOMMU_PC_IVLD_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/WAC	0x0	PC_IVLD_ENABLE Enable PTW Cache invalid operation 0: No-operation or operation completed 1: Enable is invalid After invalidation operation completed, the bit can clear 0 automatically. After or Before Invalidation starts, there is no absolute relationship between same address switch operation and Invalidation operation.

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3.5.6.17. IOMMU Domain Authority Control Register 0 (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: IOMMU_DM_AUT_CTRL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	0x0	DM1_M5_WT_AUT_CTRL Domain1 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
26	R/W	0x0	DM1_M5_RD_AUT_CTRL Domain1 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
25	R/W	0x0	DM1_M4_WT_AUT_CTRL Domain1 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
24	R/W	0x0	DM1_M4_RD_AUT_CTRL Domain1 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
23	R/W	0x0	DM1_M3_WT_AUT_CTRL Domain1 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
22	R/W	0x0	DM1_M3_RD_AUT_CTRL Domain1 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
21	R/W	0x0	DM1_M2_WT_AUT_CTRL Domain1 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
20	R/W	0x0	DM1_M2_RD_AUT_CTRL Domain1 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
19	R/W	0x0	DM1_M1_WT_AUT_CTRL Domain1 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
18	R/W	0x0	DM1_M1_RD_AUT_CTRL Domain1 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable

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17	R/W	0x0	DM1_M0_WT_AUT_CTRL Domain1 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
16	R/W	0x0	DM1_M0_RD_AUT_CTRL Domain1 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable
15:12	/	/	/
11	R	0x0	DM0_M5_WT_AUT_CTRL Domain0 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
10	R	0x0	DM0_M5_RD_AUT_CTRL Domain0 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
9	R	0x0	DM0_M4_WT_AUT_CTRL Domain0 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
8	R	0x0	DM0_M4_RD_AUT_CTRL Domain0 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
7	R	0x0	DM0_M3_WT_AUT_CTRL Domain0 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
6	R	0x0	DM0_M3_RD_AUT_CTRL Domain0 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
5	R	0x0	DM0_M2_WT_AUT_CTRL Domain0 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
4	R	0x0	DM0_M2_RD_AUT_CTRL Domain0 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
3	R	0x0	DM0_M1_WT_AUT_CTRL Domain0 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable

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2	R	0x0	DM0_M1_RD_AUT_CTRL Domain0 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
1	R	0x0	DM0_M0_WT_AUT_CTRL Domain0 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
0	R	0x0	DM0_M0_RD_AUT_CTRL Domain0 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable

NOTE

Software can be set up 15 different permission control type , which is set in IOMMU_DM_AUT_CTRL_REG0 ~ 7. As well as a default access control type, domain0. The read/write operation of DOMIAN1 ~ 15 is unlimited by default. Software needs set the corresponding permission control domain index of the page table item in the secondary page table entries[7:4], the default value is 0, use domian0, namely the read/write operation is not controlled.
Setting REG_ARD_OVWT can shield Domain control of IOMMU_DM_AUT_CTRL_REG0~7.All Level2 page table type are covered by the type of REG_ARD_OVWT. The read/write operation is permitted by default.

3.5.6.18. IOMMU Domain Authority Control Register 1 (Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: IOMMU_DM_AUT_CTRL_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	0x0	DM3_M5_WT_AUT_CTRL Domain3 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
26	R/W	0x0	DM3_M5_RD_AUT_CTRL Domain3 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
25	R/W	0x0	DM3_M4_WT_AUT_CTRL Domain3 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
24	R/W	0x0	DM3_M4_RD_AUT_CTRL Domain3 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable

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23	R/W	0x0	DM3_M3_WT_AUT_CTRL Domain3 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
22	R/W	0x0	DM3_M3_RD_AUT_CTRL Domain3 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
21	R/W	0x0	DM3_M2_WT_AUT_CTRL Domain3 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
20	R/W	0x0	DM3_M2_RD_AUT_CTRL Domain3 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
19	R/W	0x0	DM3_M1_WT_AUT_CTRL Domain3 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
18	R/W	0x0	DM3_M1_RD_AUT_CTRL Domain3 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
17	R/W	0x0	DM3_M0_WT_AUT_CTRL Domain3 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
16	R/W	0x0	DM3_M0_RD_AUT_CTRL Domain3 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable
15:12	/	/	/
11	R/W	0x0	DM2_M5_WT_AUT_CTRL Domain2 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
10	R/W	0x0	DM2_M5_RD_AUT_CTRL Domain2 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
9	R/W	0x0	DM2_M4_WT_AUT_CTRL Domain2 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable

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8	R/W	0x0	DM2_M4_RD_AUT_CTRL Domain2 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
7	R/W	0x0	DM2_M3_WT_AUT_CTRL Domain2 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
6	R/W	0x0	DM2_M3_RD_AUT_CTRL Domain2 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
5	R/W	0x0	DM2_M2_WT_AUT_CTRL Domain2 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
4	R/W	0x0	DM2_M2_RD_AUT_CTRL Domain2 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
3	R/W	0x0	DM2_M1_WT_AUT_CTRL Domain2 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
2	R/W	0x0	DM2_M1_RD_AUT_CTRL Domain2 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
1	R/W	0x0	DM2_M0_WT_AUT_CTRL Domain2 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
0	R/W	0x0	DM2_M0_RD_AUT_CTRL Domain2 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable

3.5.6.19. IOMMU Domain Authority Control Register 2 (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: IOMMU_DM_AUT_CTRL_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	0x0	DM5_M5_WT_AUT_CTRL Domain5 write permission control for master5

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			0: The write-operation is available 1: The write-operation is unavailable
26	R/W	0x0	DM5_M5_RD_AUT_CTRL Domain5 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
25	R/W	0x0	DM5_M4_WT_AUT_CTRL Domain5 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
24	R/W	0x0	DM5_M4_RD_AUT_CTRL Domain5 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
23	R/W	0x0	DM5_M3_WT_AUT_CTRL Domain5 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
22	R/W	0x0	DM5_M3_RD_AUT_CTRL Domain5 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
21	R/W	0x0	DM5_M2_WT_AUT_CTRL Domain5 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
20	R/W	0x0	DM5_M2_RD_AUT_CTRL Domain5 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
19	R/W	0x0	DM5_M1_WT_AUT_CTRL Domain5 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
18	R/W	0x0	DM5_M1_RD_AUT_CTRL Domain5 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
17	R/W	0x0	DM5_M0_WT_AUT_CTRL Domain5 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
16	R/W	0x0	DM5_M0_RD_AUT_CTRL Domain5 read permission control for master0 0: The read-operation is available

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			1: The read-operation is unavailable
15:12	/	/	/
11	R/W	0x0	DM4_M5_WT_AUT_CTRL Domain4 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
10	R/W	0x0	DM4_M5_RD_AUT_CTRL Domain4 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
9	R/W	0x0	DM4_M4_WT_AUT_CTRL Domain4 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
8	R/W	0x0	DM4_M4_RD_AUT_CTRL Domain4 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
7	R/W	0x0	DM4_M3_WT_AUT_CTRL Domain4 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
6	R/W	0x0	DM4_M3_RD_AUT_CTRL Domain4 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
5	R/W	0x0	DM4_M2_WT_AUT_CTRL Domain4 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
4	R/W	0x0	DM4_M2_RD_AUT_CTRL Domain4 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
3	R/W	0x0	DM4_M1_WT_AUT_CTRL Domain4 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
2	R/W	0x0	DM4_M1_RD_AUT_CTRL Domain4 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
1	R/W	0x0	DM4_M0_WT_AUT_CTRL Domain4 write permission control for master0 0: The write-operation is available

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			1: The write-operation is unavailable
0	R/W	0x0	DM4_M0_RD_AUT_CTRL Domain4 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable

3.5.6.20. IOMMU Domain Authority Control Register 3 (Default Value: 0x0000_0000)

Offset: 0x00BC			Register Name: IOMMU_DM_AUT_CTRL_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	0x0	DM7_M5_WT_AUT_CTRL Domain7 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
26	R/W	0x0	DM7_M5_RD_AUT_CTRL Domain7 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
25	R/W	0x0	DM7_M4_WT_AUT_CTRL Domain7 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
24	R/W	0x0	DM7_M4_RD_AUT_CTRL Domain7 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
23	R/W	0x0	DM7_M3_WT_AUT_CTRL Domain7 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
22	R/W	0x0	DM7_M3_RD_AUT_CTRL Domain7 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
21	R/W	0x0	DM7_M2_WT_AUT_CTRL Domain7 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
20	R/W	0x0	DM7_M2_RD_AUT_CTRL Domain7 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
19	R/W	0x0	DM7_M1_WT_AUT_CTRL

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			Domain7 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
18	R/W	0x0	DM7_M1_RD_AUT_CTRL Domain7 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
17	R/W	0x0	DM7_M0_WT_AUT_CTRL Domain7 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
16	R/W	0x0	DM7_M0_RD_AUT_CTRL Domain7 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable
15:12	/	/	/
11	R/W	0x0	DM6_M5_WT_AUT_CTRL Domain6 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
10	R/W	0x0	DM6_M5_RD_AUT_CTRL Domain6 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
9	R/W	0x0	DM6_M4_WT_AUT_CTRL Domain6 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
8	R/W	0x0	DM6_M4_RD_AUT_CTRL Domain6 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
7	R/W	0x0	DM6_M3_WT_AUT_CTRL Domain6 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
6	R/W	0x0	DM6_M3_RD_AUT_CTRL Domain6 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
5	R/W	0x0	DM6_M2_WT_AUT_CTRL Domain6 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
4	R/W	0x0	DM6_M2_RD_AUT_CTRL

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			Domain6 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
3	R/W	0x0	DM6_M1_WT_AUT_CTRL Domain6 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
2	R/W	0x0	DM6_M1_RD_AUT_CTRL Domain6 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
1	R/W	0x0	DM6_M0_WT_AUT_CTRL Domain6 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
0	R/W	0x0	DM6_M0_RD_AUT_CTRL Domain6 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable

3.5.6.21. IOMMU Domain Authority Control Register 4 (Default Value: 0x0000_0000)

Offset: 0x00C0			**Register Name: IOMMU_DM_AUT_CTRL_REG4**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	0x0	DM9_M5_WT_AUT_CTRL Domain9 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
26	R/W	0x0	DM9_M5_RD_AUT_CTRL Domain9 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
25	R/W	0x0	DM9_M4_WT_AUT_CTRL Domain9 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
24	R/W	0x0	DM9_M4_RD_AUT_CTRL Domain9 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
23	R/W	0x0	DM9_M3_WT_AUT_CTRL Domain9 write permission control for master3 0: The write-operation is available

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			1: The write-operation is unavailable
22	R/W	0x0	DM9_M3_RD_AUT_CTRL Domain9 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
21	R/W	0x0	DM9_M2_WT_AUT_CTRL Domain9 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
20	R/W	0x0	DM9_M2_RD_AUT_CTRL Domain9 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
19	R/W	0x0	DM9_M1_WT_AUT_CTRL Domain9 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
18	R/W	0x0	DM9_M1_RD_AUT_CTRL Domain9 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
17	R/W	0x0	DM9_M0_WT_AUT_CTRL Domain9 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
16	R/W	0x0	DM9_M0_RD_AUT_CTRL Domain9 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable
15:12	/	/	/
11	R/W	0x0	DM8_M5_WT_AUT_CTRL Domain8 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
10	R/W	0x0	DM8_M5_RD_AUT_CTRL Domain8 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
9	R/W	0x0	DM8_M4_WT_AUT_CTRL Domain8 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
8	R/W	0x0	DM8_M4_RD_AUT_CTRL Domain8 read permission control for master4 0: The read-operation is available

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			1: The read-operation is unavailable
7	R/W	0x0	DM8_M3_WT_AUT_CTRL Domain8 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
6	R/W	0x0	DM8_M3_RD_AUT_CTRL Domain8 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
5	R/W	0x0	DM8_M2_WT_AUT_CTRL Domain8 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
4	R/W	0x0	DM8_M2_RD_AUT_CTRL Domain8 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
3	R/W	0x0	DM8_M1_WT_AUT_CTRL Domain8 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
2	R/W	0x0	DM8_M1_RD_AUT_CTRL Domain8 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
1	R/W	0x0	DM8_M0_WT_AUT_CTRL Domain8 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
0	R/W	0x0	DM8_M0_RD_AUT_CTRL Domain8 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable

3.5.6.22. IOMMU Domain Authority Control Register 5 (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: IOMMU_DM_AUT_CTRL_REG5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	0x0	DM11_M5_WT_AUT_CTRL Domain11 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
26	R/W	0x0	DM11_M5_RD_AUT_CTRL

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			Domain11 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
25	R/W	0x0	DM11_M4_WT_AUT_CTRL Domain11 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
24	R/W	0x0	DM11_M4_RD_AUT_CTRL Domain11 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
23	R/W	0x0	DM11_M3_WT_AUT_CTRL Domain11 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
22	R/W	0x0	DM11_M3_RD_AUT_CTRL Domain11 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
21	R/W	0x0	DM11_M2_WT_AUT_CTRL Domain11 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
20	R/W	0x0	DM11_M2_RD_AUT_CTRL Domain11 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
19	R/W	0x0	DM11_M1_WT_AUT_CTRL Domain11 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
18	R/W	0x0	DM11_M1_RD_AUT_CTRL Domain11 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
17	R/W	0x0	DM11_M0_WT_AUT_CTRL Domain11 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
16	R/W	0x0	DM11_M0_RD_AUT_CTRL Domain11 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable
15:12	/	/	/
11	R/W	0x0	DM10_M5_WT_AUT_CTRL

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			Domain10 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
10	R/W	0x0	DM10_M5_RD_AUT_CTRL Domain10 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
9	R/W	0x0	DM10_M4_WT_AUT_CTRL Domain10 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
8	R/W	0x0	DM10_M4_RD_AUT_CTRL Domain10 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
7	R/W	0x0	DM10_M3_WT_AUT_CTRL Domain10 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
6	R/W	0x0	DM10_M3_RD_AUT_CTRL Domain10 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
5	R/W	0x0	DM10_M2_WT_AUT_CTRL Domain10 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
4	R/W	0x0	DM10_M2_RD_AUT_CTRL Domain10 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
3	R/W	0x0	DM10_M1_WT_AUT_CTRL Domain10 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
2	R/W	0x0	DM10_M1_RD_AUT_CTRL Domain10 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
1	R/W	0x0	DM10_M0_WT_AUT_CTRL Domain10 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
0	R/W	0x0	DM10_M0_RD_AUT_CTRL Domain10 read permission control for master0

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			0: The read-operation is available 1: The read-operation is unavailable

3.5.6.23. IOMMU Domain Authority Control Register 6 (Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: IOMMU_DM_AUT_CTRL_REG6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	0x0	DM13_M5_WT_AUT_CTRL Domain13 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
26	R/W	0x0	DM13_M5_RD_AUT_CTRL Domain13 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
25	R/W	0x0	DM13_M4_WT_AUT_CTRL Domain13 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
24	R/W	0x0	DM13_M4_RD_AUT_CTRL Domain13 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
23	R/W	0x0	DM13_M3_WT_AUT_CTRL Domain13 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
22	R/W	0x0	DM13_M3_RD_AUT_CTRL Domain13 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
21	R/W	0x0	DM13_M2_WT_AUT_CTRL Domain13 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
20	R/W	0x0	DM13_M2_RD_AUT_CTRL Domain13 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
19	R/W	0x0	DM13_M1_WT_AUT_CTRL Domain13 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable

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18	R/W	0x0	DM13_M1_RD_AUT_CTRL Domain13 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
17	R/W	0x0	DM13_M0_WT_AUT_CTRL Domain13 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
16	R/W	0x0	DM13_M0_RD_AUT_CTRL Domain13 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable
15:12	/	/	/
11	R/W	0x0	DM12_M5_WT_AUT_CTRL Domain12 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
10	R/W	0x0	DM12_M5_RD_AUT_CTRL Domain12 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
9	R/W	0x0	DM12_M4_WT_AUT_CTRL Domain12 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
8	R/W	0x0	DM12_M4_RD_AUT_CTRL Domain12 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
7	R/W	0x0	DM12_M3_WT_AUT_CTRL Domain12 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
6	R/W	0x0	DM12_M3_RD_AUT_CTRL Domain12 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
5	R/W	0x0	DM12_M2_WT_AUT_CTRL Domain12 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
4	R/W	0x0	DM12_M2_RD_AUT_CTRL Domain12 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable

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3	R/W	0x0	DM12_M1_WT_AUT_CTRL Domain12 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
2	R/W	0x0	DM12_M1_RD_AUT_CTRL Domain12 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
1	R/W	0x0	DM12_M0_WT_AUT_CTRL Domain12 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
0	R/W	0x0	DM12_M0_RD_AUT_CTRL Domain12 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable

3.5.6.24. IOMMU Domain Authority Control Register 7 (Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: IOMMU_DM_AUT_CTRL_REG7
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	0x0	DM15_M5_WT_AUT_CTRL Domain15 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
26	R/W	0x0	DM15_M5_RD_AUT_CTRL Domain15 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
25	R/W	0x0	DM15_M4_WT_AUT_CTRL Domain15 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
24	R/W	0x0	DM15_M4_RD_AUT_CTRL Domain15 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
23	R/W	0x0	DM15_M3_WT_AUT_CTRL Domain15 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
22	R/W	0x0	DM15_M3_RD_AUT_CTRL Domain15 read permission control for master3

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			0: The read-operation is available 1: The read-operation is unavailable
21	R/W	0x0	DM15_M2_WT_AUT_CTRL Domain15 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
20	R/W	0x0	DM15_M2_RD_AUT_CTRL Domain15 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
19	R/W	0x0	DM15_M1_WT_AUT_CTRL Domain15 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
18	R/W	0x0	DM15_M1_RD_AUT_CTRL Domain15 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
17	R/W	0x0	DM15_M0_WT_AUT_CTRL Domain15 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
16	R/W	0x0	DM15_M0_RD_AUT_CTRL Domain15 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable
15:12	/	/	/
11	R/W	0x0	DM14_M5_WT_AUT_CTRL Domain14 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
10	R/W	0x0	DM14_M5_RD_AUT_CTRL Domain14 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
9	R/W	0x0	DM14_M4_WT_AUT_CTRL Domain14 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
8	R/W	0x0	DM14_M4_RD_AUT_CTRL Domain14 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
7	R/W	0x0	DM14_M3_WT_AUT_CTRL Domain14 write permission control for master3

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			0: The write-operation is available 1: The write-operation is unavailable
6	R/W	0x0	DM14_M3_RD_AUT_CTRL Domain14 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
5	R/W	0x0	DM14_M2_WT_AUT_CTRL Domain14 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
4	R/W	0x0	DM14_M2_RD_AUT_CTRL Domain14 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
3	R/W	0x0	DM14_M1_WT_AUT_CTRL Domain14 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
2	R/W	0x0	DM14_M1_RD_AUT_CTRL Domain14 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
1	R/W	0x0	DM14_M0_WT_AUT_CTRL Domain14 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
0	R/W	0x0	DM14_M0_RD_AUT_CTRL Domain14 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable

3.5.6.25. IOMMU Domain Authority Overwrite Register (Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: IOMMU_DM_AUT_OVWT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DM_AUT_OVWT_ENABLE Domain write/read permission overwrite enable 0: Disable 1: Enable
30:12	/	/	/
11	R/W	0x0	M5_WT_AUT_OVWT_CTRL Master5 write permission overwrite control 0: The write-operation is available 1: The write-operation is unavailable

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10	R/W	0x0	M5_RD_AUT_OVWT_CTRL Master5 read permission overwrite control 0: The read-operation is available 1: The read-operation is unavailable
9	R/W	0x0	M4_WT_AUT_OVWT_CTRL Master5 write permission overwrite control 0: The write-operation is available 1: The write-operation is unavailable
8	R/W	0x0	M4_RD_AUT_OVWT_CTRL Master5 read permission overwrite control 0: The read-operation is available 1: The read-operation is unavailable
7	R/W	0x0	M3_WT_AUT_OVWT_CTRL Master3 write permission overwrite control 0: The write-operation is available 1: The write-operation is unavailable
6	R/W	0x0	M3_RD_AUT_OVWT_CTRL Master3 read permission overwrite control 0: The read-operation is available 1: The read-operation is unavailable
5	R/W	0x0	M2_WT_AUT_OVWT_CTRL Master2 write permission overwrite control 0: The write-operation is available 1: The write-operation is unavailable
4	R/W	0x0	M2_RD_AUT_OVWT_CTRL Master2 read permission overwrite control 0: The read-operation is available 1: The read-operation is unavailable
3	R/W	0x0	M1_WT_AUT_OVWT_CTRL Master1 write permission overwrite control 0: The write-operation is available 1: The write-operation is unavailable
2	R/W	0x0	M1_RD_AUT_OVWT_CTRL Master1 read permission overwrite control 0: The read-operation is available 1: The read-operation is unavailable
1	R/W	0x0	M0_WT_AUT_OVWT_CTRL Master0 write permission overwrite control 0: The write-operation is available 1: The write-operation is unavailable
0	R/W	0x0	M0_RD_AUT_OVWT_CTRL Master0 read permission overwrite control 0: The read-operation is available 1: The read-operation is unavailable

设置 REG_ARD_OVWT 可以屏蔽寄 IOMMU_DM_AUT_CTRL_REG0~7 定义的 Domain 的控制作用。全部的二级表项

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属性由 REG_ARD_OVWT 里面定义的属性覆盖。默认为允许全部读写。

3.5.6.26. IOMMU Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: IOMMU_INT_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	L2_PAGE_TABLE_INVALID_EN Level2 page table invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
16	R/W	0x0	L1_PAGE_TABLE_INVALID_EN Level1 page table invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
15:6	/	/	/
5	R/W	0x0	MICRO_TLB5_INVALID_EN Micro TLB5 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
4	R/W	0x0	MICRO_TLB4_INVALID_EN Micro TLB4 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
3	R/W	0x0	MICRO_TLB3_INVALID_EN Micro TLB3 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
2	R/W	0x0	MICRO_TLB2_INVALID_EN Micro TLB2 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
1	R/W	0x0	MICRO_TLB1_INVALID_EN Micro TLB1 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
0	R/W	0x0	MICRO_TLB0_INVALID_EN Micro TLB0 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt

NOTE

Invalid page table and permission error can not make one device or multi-devices in system work normally.

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Permission error usually happens in MicroTLB.The error generates interrupt,and waits for processing through software.

Invalid page table usually happens in MacroTLB.The error can not influence the access of other devices.So the error page table need go back the way it comes, but the error should not be written in each level TLB.

3.5.6.27. IOMMU Interrupt Clear Register (Default Value: 0x0000_0000)

Offset: 0x0104			Register Name: IOMMU_INT_CLR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	W	0x0	L2_PAGE_TABLE_INVALID_CLR Level2 page table invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
16	W	0x0	L1_PAGE_TABLE_INVALID_CLR Level1 page table invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
15:6	/	/	/
5	W	0x0	MICRO_TLB5_INVALID_CLR Micro TLB5 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
4	W	0x0	MICRO_TLB4_INVALID_CLR Micro TLB4 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
3	W	0x0	MICRO_TLB3_INVALID_CLR Micro TLB3 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
2	W	0x0	MICRO_TLB2_INVALID_CLR Micro TLB2 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
1	W	0x0	MICRO_TLB1_INVALID_CLR Micro TLB1 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
0	W	0x0	MICRO_TLB0_INVALID_CLR Micro TLB0 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt

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3.5.6.28. IOMMU Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: IOMMU_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R	0x0	L2_PAGE_TABLE_INVALID_STA Level2 page table invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
16	R	0x0	L1_PAGE_TABLE_INVALID_STA Level2 page table invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
15:6	/	/	/
5	R	0x0	MICRO_TLB5_INVALID_STA Micro TLB5 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
4	R	0x0	MICRO_TLB4_INVALID_STA Micro TLB4 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
3	R	0x0	MICRO_TLB3_INVALID_STA Micro TLB3 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
2	R	0x0	MICRO_TLB2_INVALID_STA Micro TLB2 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
1	R	0x0	MICRO_TLB1_INVALID_STA Micro TLB1 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
0	R	0x0	MICRO_TLB0_INVALID_STA Micro TLB0 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens

3.5.6.29. IOMMU Interrupt Error Address Register 0 (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: IOMMU_INT_ERR_ADDR_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_ADDR0

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			Virtual address causing Micro TLB0 occurs interrupt

3.5.6.30. IOMMU Interrupt Error Address Register 1 (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: IOMMU_INT_ERR_ADDR_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_ADDR1 Virtual address causing Micro TLB1 occurs interrupt

3.5.6.31. IOMMU Interrupt Error Address Register 2 (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: IOMMU_INT_ERR_ADDR_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_ADDR2 Virtual address causing Micro TLB2 occurs interrupt

3.5.6.32. IOMMU Interrupt Error Address Register 3 (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: IOMMU_INT_ERR_ADDR_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_ADDR3 Virtual address causing Micro TLB3 occurs interrupt

3.5.6.33. IOMMU Interrupt Error Address Register 4 (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: IOMMU_INT_ERR_ADDR_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_ADDR4 Virtual address causing Micro TLB4 occurs interrupt

3.5.6.34. IOMMU Interrupt Error Address Register 5 (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: IOMMU_INT_ERR_ADDR_REG5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_ADDR5 Virtual address causing Micro TLB5 occurs interrupt

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3.5.6.35. IOMMU Interrupt Error Address Register 6 (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: IOMMU_INT_ERR_ADDR_REG6
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR6 Virtual address causing Micro TLB6 occurs interrupt

3.5.6.36. IOMMU Interrupt Error Address Register 7 (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: IOMMU_INT_ERR_ADDR_REG7
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR7 Virtual address causing Micro TLB7 occurs interrupt

3.5.6.37. IOMMU Interrupt Error Data Register 0 (Default Value: 0x0000_0000)

Offset: 0x0150			Register Name: IOMMU_INT_ERR_DATA_REG0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA0 Corresponding page table of virtual address causing Micro TLB0 occurs interrupt

3.5.6.38. IOMMU Interrupt Error Data Register 1 (Default Value: 0x0000_0000)

Offset: 0x0154			Register Name: IOMMU_INT_ERR_DATA_REG1
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA1 Corresponding page table of virtual address causing Micro TLB1 occurs interrupt

3.5.6.39. IOMMU Interrupt Error Data Register 2 (Default Value: 0x0000_0000)

Offset: 0x0158			Register Name: IOMMU_INT_ERR_DATA_REG2
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA2 Corresponding page table of virtual address causing Micro TLB2 occurs interrupt

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3.5.6.40. IOMMU Interrupt Error Data Register 3 (Default Value: 0x0000_0000)

Offset: 0x015C			Register Name: IOMMU_INT_ERR_DATA_REG3
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA3 Corresponding page table of virtual address causing Micro TLB3 occurs interrupt

3.5.6.41. IOMMU Interrupt Error Data Register 4 (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: IOMMU_INT_ERR_DATA_REG4
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA4 Corresponding page table of virtual address causing Micro TLB4 occurs interrupt

3.5.6.42. IOMMU Interrupt Error Data Register 5 (Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: IOMMU_INT_ERR_DATA_REG5
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA5 Corresponding page table of virtual address causing Micro TLB5 occurs interrupt

3.5.6.43. IOMMU Interrupt Error Data Register 6 (Default Value: 0x0000_0000)

Offset: 0x0170			Register Name: IOMMU_INT_ERR_DATA_REG6
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA6 Corresponding page table of virtual address causing Micro TLB6 occurs interrupt

3.5.6.44. IOMMU Interrupt Error Data Register 7 (Default Value: 0x0000_0000)

Offset: 0x0174			Register Name: IOMMU_INT_ERR_DATA_REG7
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA7 Corresponding page table of virtual address causing Micro TLB7 occurs interrupt

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3.5.6.45. IOMMU L1 Page Table Interrupt Register (Default Value: 0x0000_0000)

Offset: 0x0180			Register Name: IOMMU_L1PG_INT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R	0x0	MASTER5_L1PG_INT Master5 address switch causes L1 page table to occur interrupt.
4	R	0x0	MASTER4_L1PG_INT Master4 address switch causes L1 page table to occur interrupt.
3	R	0x0	MASTER3_L1PG_INT Master3 address switch causes L1 page table to occur interrupt.
2	R	0x0	MASTER2_L1PG_INT Master2 address switch causes L1 page table to occur interrupt.
1	R	0x0	MASTER1_L1PG_INT Master1 address switch causes L1 page table to occur interrupt.
0	R	0x0	MASTER0_L1PG_INT Master0 address switch causes L1 page table to occur interrupt.

3.5.6.46. IOMMU L2 Page Table Interrupt Register (Default Value: 0x0000_0000)

Offset: 0x0184			Register Name: IOMMU_L2PG_INT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R	0x0	MASTER5_L2PG_INT Master5 address switch causes L2 page table to occur interrupt.
4	R	0x0	MASTER4_L2PG_INT Master4 address switch causes L2 page table to occur interrupt.
3	R	0x0	MASTER3_L2PG_INT Master3 address switch causes L2 page table to occur interrupt.
2	R	0x0	MASTER2_L2PG_INT Master2 address switch causes L2 page table to occur interrupt.
1	R	0x0	MASTER1_L2PG_INT Master1 address switch causes L2 page table to occur interrupt.
0	R	0x0	MASTER0_L2PG_INT Master0 address switch causes L2 page table to occur interrupt.

3.5.6.47. IOMMU Virtual Address Register (Default Value: 0x0000_0000)

Offset: 0x0190			Register Name: IOMMU_VA _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VA Virtual address of read/write

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3.5.6.48. IOMMU Virtual Address Data Register (Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: IOMMU_VA_DATA _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VA_DATA Data of read/write virtual address

3.5.6.49. IOMMU Virtual Address Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0198			Register Name: IOMMU_VA_CONFIG _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	VA_CONFIG 0: Read operation 1: Write operation
7:1	/	/	/
0	R/WAC	0x0	VA_CONFIG_START 0: No operation or operation completes 1: Start After the operation completes, the bit can clear to 0 automatically.

Read operation process:

a) Write IOMMU_VA_REG[31:0];

b) Write IOMMU_VA_CONFIG _REG[8] to 0;

c) Write IOMMU_VA_CONFIG _REG[0] to 1,start read-process;

d) Query IOMMU_VA_CONFIG _REG[0], until it is 0;

e) Read IOMMU_VA_DATA _REG[31:0]

Write operation process:

a) Write IOMMU_VA _REG[31:0];

b) Write IOMMU_VA_DATA _REG[31:0];

c) Write IOMMU_VA_CONFIG _REG[8] to 1;

d) Write IOMMU_VA_CONFIG _REG[0] to 1， start write-process;

e) QueryIOMMU_VA_CONFIG _REG[0],until it is 0

3.5.6.50. IOMMU PMU Enable Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: IOMMU_PMU_ENABLE _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	PMU_ENABLE 0: Disable statistical function 1: Enable statistical function

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3.5.6.51. IOMMU PMU Clear Register (Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: IOMMU_PMU_CLR _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/WAC	0x0	PMU_CLR 0: No clear operation or clear operation completes 1: Clear counter data After the operation completes, the bit can clear to 0 automatically.

3.5.6.52. IOMMU PMU Access Low Register 0 (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: IOMMU_PMU_ACCESS_LOW_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ACCESS_LOW0 Record total number of Micro TLB0 access , lower 32-bit register

3.5.6.53. IOMMU PMU Access High Register 0 (Default Value: 0x0000_0000)

Offset: 0x0234			Register Name: IOMMU_PMU_ACCESS_HIGH_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH0 Record total number of Micro TLB0 access , higher 11-bit register

3.5.6.54. IOMMU PMU Hit Low Register 0 (Default Value: 0x0000_0000)

Offset: 0x0238			Register Name: IOMMU_PMU_HIT_LOW_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_HIT_LOW0 Record total number of Micro TLB0 hit , lower 32-bit register

3.5.6.55. IOMMU PMU Hit High Register 0 (Default Value: 0x0000_0000)

Offset: 0x023C			Register Name: IOMMU_PMU_HIT_HIGH_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH0 Record total number of Micro TLB0 hit , higher 11-bit register

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3.5.6.56. IOMMU PMU Access Low Register 1 (Default Value: 0x0000_0000)

Offset: 0x0240			Register Name: IOMMU_PMU_ACCESS_LOW_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ACCESS_LOW1 Record total number of Micro TLB1 access , lower 32-bit register

3.5.6.57. IOMMU PMU Access High Register 1 (Default Value: 0x0000_0000)

Offset: 0x0244			Register Name: IOMMU_PMU_ACCESS_HIGH_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH1 Record total number of Micro TLB1 access , higher 11-bit register

3.5.6.58. IOMMU PMU Hit Low Register 1 (Default Value: 0x0000_0000)

Offset: 0x0248			Register Name: IOMMU_PMU_HIT_LOW_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_HIT_LOW1 Record total number of Micro TLB1 hit , lower 32-bit register

3.5.6.59. IOMMU PMU Hit High Register 1 (Default Value: 0x0000_0000)

Offset: 0x024C			Register Name: IOMMU_PMU_HIT_HIGH_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH1 Record total number of Micro TLB1 hit , higher 11-bit register

3.5.6.60. IOMMU PMU Access Low Register 2 (Default Value: 0x0000_0000)

Offset: 0x0250			Register Name: IOMMU_PMU_ACCESS_LOW_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ACCESS_LOW2 Record total number of Micro TLB2 access , lower 32-bit register

3.5.6.61. IOMMU PMU Access High Register 2 (Default Value: 0x0000_0000)

Offset: 0x0254	Register Name: IOMMU_PMU_ACCESS_HIGH_REG2

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Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH2 Record total number of Micro TLB2 access , higher 11-bit register

3.5.6.62. IOMMU PMU Hit Low Register 2 (Default Value: 0x0000_0000)

Offset: 0x0258			Register Name: IOMMU_PMU_HIT_LOW_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_HIT_LOW2 Record total number of Micro TLB2 hit , lower 32-bit register

3.5.6.63. IOMMU PMU Hit High Register 2 (Default Value: 0x0000_0000)

Offset: 0x025C			Register Name: IOMMU_PMU_HIT_HIGH_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH2 Record total number of Micro TLB2 hit , higher 11-bit register

3.5.6.64. IOMMU PMU Access Low Register 3 (Default Value: 0x0000_0000)

Offset: 0x0260			Register Name: IOMMU_PMU_ACCESS_LOW_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ACCESS_LOW3 Record total number of Micro TLB3 access, lower 32-bit register

3.5.6.65. IOMMU PMU Access High Register 3 (Default Value: 0x0000_0000)

Offset: 0x0264			Register Name: IOMMU_PMU_ACCESS_HIGH_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH3 Record total number of Micro TLB3 access , higher 11-bit register

3.5.6.66. IOMMU PMU Hit Low Register 3 (Default Value: 0x0000_0000)

Offset: 0x0268			Register Name: IOMMU_PMU_HIT_LOW_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_HIT_LOW3

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			Record total number of Micro TLB3 hit, lower 32-bit register

3.5.6.67. IOMMU PMU Hit High Register 3 (Default Value: 0x0000_0000)

Offset: 0x026C			Register Name: IOMMU_PMU_HIT_HIGH_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH3 Record total number of Micro TLB3 hit , higher 11-bit register

3.5.6.68. IOMMU PMU Access Low Register 4 (Default Value: 0x0000_0000)

Offset: 0x0270			Register Name: IOMMU_PMU_ACCESS_LOW_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ACCESS_LOW4 Record total number of Micro TLB4 access, lower 32-bit register

3.5.6.69. IOMMU PMU Access High Register 4 (Default Value: 0x0000_0000)

Offset: 0x0274			Register Name: IOMMU_PMU_ACCESS_HIGH_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH4 Record total number of Micro TLB4 access, higher 11-bit register

3.5.6.70. IOMMU PMU Hit Low Register 4 (Default Value: 0x0000_0000)

Offset: 0x0278			Register Name: IOMMU_PMU_HIT_LOW_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_HIT_LOW4 Record total number of Micro TLB4 hit, lower 32-bit register

3.5.6.71. IOMMU PMU Hit High Register 4 (Default Value: 0x0000_0000)

Offset: 0x027C			Register Name: IOMMU_PMU_HIT_HIGH_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH4 Record total number of Micro TLB4 hit, higher 11-bit register

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3.5.6.72. IOMMU PMU Access Low Register 5 (Default Value: 0x0000_0000)

Offset: 0x0280			Register Name: IOMMU_PMU_ACCESS_LOW_REG5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ACCESS_LOW5 Record total number of Micro TLB5 access, lower 32-bit register

3.5.6.73. IOMMU PMU Access High Register 5 (Default Value: 0x0000_0000)

Offset: 0x0284			Register Name: IOMMU_PMU_ACCESS_HIGH_REG5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH5 Record total number of Micro TLB5 access, higher 11-bit register

3.5.6.74. IOMMU PMU Hit Low Register 5 (Default Value: 0x0000_0000)

Offset: 0x0288			Register Name: IOMMU_PMU_HIT_LOW_REG5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_HIT_LOW5 Record total number of Micro TLB5 hit, lower 32-bit register

3.5.6.75. IOMMU PMU Hit High Register 5 (Default Value: 0x0000_0000)

Offset: 0x028C			Register Name: IOMMU_PMU_HIT_HIGH_REG5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH5 Record total number of Micro TLB5 hit, higher 11-bit register

3.5.6.76. IOMMU PMU Access Low Register 6 (Default Value: 0x0000_0000)

Offset: 0x02D0			Register Name: IOMMU_PMU_ACCESS_LOW_REG6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ACCESS_LOW6 Record total number of Micro TLB6 access, lower 32-bit register

3.5.6.77. IOMMU PMU Access High Register 6 (Default Value: 0x0000_0000)

Offset: 0x02D4	Register Name: IOMMU_PMU_ACCESS_HIGH_REG6

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Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH6 Record total number of Micro TLB6 access, higher 11-bit register

3.5.6.78. IOMMU PMU Hit Low Register 6 (Default Value: 0x0000_0000)

Offset: 0x02D8			Register Name: IOMMU_PMU_HIT_LOW_REG6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_HIT_LOW6 Record total number of Micro TLB6 hit, lower 32-bit register

3.5.6.79. IOMMU PMU Hit High Register 6 (Default Value: 0x0000_0000)

Offset: 0x02DC			Register Name: IOMMU_PMU_HIT_HIGH_REG6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH6 Record total number of Micro TLB6 hit, higher 11-bit register

3.5.6.80. IOMMU PMU Access Low Register 7 (Default Value: 0x0000_0000)

Offset: 0x02E0			Register Name: IOMMU_PMU_ACCESS_LOW_REG7
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ACCESS_LOW7 Record total number of PTW Cache access, lower 32-bit register

3.5.6.81. IOMMU PMU Access High Register 7 (Default Value: 0x0000_0000)

Offset: 0x02E4			Register Name: IOMMU_PMU_ACCESS_HIGH_REG7
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH7 Record total number of PTW Cache access, higher 11-bit register

3.5.6.82. IOMMU PMU Hit Low Register 7 (Default Value: 0x0000_0000)

Offset: 0x02E8			Register Name: IOMMU_PMU_HIT_LOW_REG7
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_HIT_LOW7

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			Record total number of PTW Cache hit, lower 32-bit register

3.5.6.83. IOMMU PMU Hit High Register 7 (Default Value: 0x0000_0000)

Offset: 0x02EC			Register Name: IOMMU_PMU_HIT_HIGH_REG7
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH7 Record total number of PTW Cache hit, higher 11-bit register

3.5.6.84. IOMMU Total Latency Low Register 0 (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: IOMMU_PMU_TL_LOW_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_TL_LOW0 Record total latency of Master0, lower 32-bit register

3.5.6.85. IOMMU Total Latency High Register 0 (Default Value: 0x0000_0000)

Offset: 0x0304			Register Name: IOMMU_PMU_TL_HIGH_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH0 Record total latency of Master0, higher 18-bit register

3.5.6.86. IOMMU Total Latency Low Register 1(Default Value: 0x0000_0000)

Offset: 0x0310			Register Name: IOMMU_PMU_TL_LOW_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_TL_LOW1 Record total latency of Master1, lower 32-bit register

3.5.6.87. IOMMU Total Latency High Register 1 (Default Value: 0x0000_0000)

Offset: 0x0314			Register Name: IOMMU_PMU_TL_HIGH_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH1 Record total latency of Master1, higher 18-bit register

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3.5.6.88. IOMMU Total Latency Low Register 2 (Default Value: 0x0000_0000)

Offset: 0x0320			Register Name: IOMMU_PMU_TL_LOW_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_TL_LOW2 Record total latency of Master2, lower 32-bit register

3.5.6.89. IOMMU Total Latency High Register 2 (Default Value: 0x0000_0000)

Offset: 0x0324			Register Name: IOMMU_PMU_TL_HIGH_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH2 Record total latency of Master2, higher 18-bit register

3.5.6.90. IOMMU Total Latency Low Register 3 (Default Value: 0x0000_0000)

Offset: 0x0330			Register Name: IOMMU_PMU_TL_LOW_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ TL_LOW3 Record total latency of Master3, lower 32-bit register

3.5.6.91. IOMMU Total Latency High Register 3 (Default Value: 0x0000_0000)

Offset: 0x0334			Register Name: IOMMU_PMU_TL_HIGH_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH3 Record total latency of Master3, higher 18-bit register

3.5.6.92. IOMMU Total Latency Low Register 4 (Default Value: 0x0000_0000)

Offset: 0x0340			Register Name: IOMMU_PMU_TL_LOW_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_TL_LOW4 Record total latency of Master4, lower 32-bit register

3.5.6.93. IOMMU Total Latency High Register 4 (Default Value: 0x0000_0000)

Offset: 0x0344	Register Name: IOMMU_PMU_TL_HIGH_REG4

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Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH4 Record total latency of Master4, higher 18-bit register

3.5.6.94. IOMMU Total Latency Low Register 5 (Default Value: 0x0000_0000)

Offset: 0x0350			Register Name: IOMMU_PMU_TL_LOW_REG5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_TL_LOW5 Record total latency of Master5, lower 32-bit register

3.5.6.95. IOMMU Total Latency High Register 5 (Default Value: 0x0000_0000)

Offset: 0x0354			Register Name: IOMMU_PMU_TL_HIGH_REG5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH5 Record total latency of Master5, higher 18-bit register

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3.6. System Configuration

3.6.1. Overview

System configuration module is used to configure parameter for system domain, such as SRAM, CPU, PLL,BROM and so on. This module has the following features:

- SRAM Bist function
- System parameter configuration
- PLL back door configuration
- BROM debug parameter configuration

The address range of SRAM is as follows.

Area	Address	Size(Bytes)
SRAM A1	0x0002 0000---0x0002 7FFF	32K
SRAM A2	0x0010 0000---0x0010 3FFF	16K
	0x0010 4000---0x0011 7FFF	80K
SRAM C	0x0002 8000---0x0004 5FFF	120K
Total		248K

3.6.2. Register List

Module Name	Base Address
SYS_CFG	0x0300 0000

Register Name	Offset	Description
VER_REG	0x0024	Version Register
EMAC_EPHY_CLK_REG0	0x0030	EMAC-EPHY Clock Register 0
BROM_OUTPUT_REG	0x00A4	BROM Output Register

3.6.3. Register Description

3.6.3.1. Version Register

Offset:0x0024			Register Name: VER_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	Reserved
15	R/W	0x0	Reserved

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14:10	/	/	/
9	R	UDF	BOOT_SEL_PAD_STA 0:SMHC0->SMHC2->NAND FLASH->SPI_NOR 1:SMHC0->NAND FLASH->SMHC2->SPI_NOR
8	R	UDF	FEL_SEL_PAD_STA Fel_Select_Pin_Status 0: Run_FEL 1:Try Media Boot
7:3	/	/	/
2:0	R	0x1	Reserved

3.6.3.2. EMAC-EPHY Clock Register 0(Default Value: 0x0005_8000)

Offset:0x0030			Register Name: EMAC_EPHY_CLK_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	BPS_EFFUSE
27	R/W	0x0	XMII_SEL 0: Internal SMI and MII 1: External SMI and MII
26:25	R/W	0x0	EPHY_MODE Operation Mode Selection 00 : Normal Mode 01 : Sim Mode 10 : AFE Test Mode 11 : /
24:20	R/W	0x0	PHY_ADDR PHY Address
19	R/W	0x0	Reserved
18	R/W	0x1	CLK_SEL 0 : 25MHz 1 : 24MHz
17	R/W	0x0	LED_POL 0 : High active 1 : Low active
16	R/W	0x1	SHUTDOWN 0 : Power up 1 : Shutdown
15	R/W	0x1	PHY_SELECT. 0 : External PHY 1 : Internal PHY
14	/	/	/
13	R/W	0x0	RMII_EN 0 : Disable RMII Module 1 : Enable RMII Module

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			When this bit assert, MII or RGMII interface is disabled(This means bit13 is prior to bit2)
12:10	R/W	0x0	ETXDC. Configure EMAC Transmit Clock Delay Chain.
9:5	R/W	0x0	ERXDC. Configure EMAC Receive Clock Delay Chain.
4	R/W	0x0	ERXIE Enable EMAC Receive Clock Invertor. 0: Disable 1: Enable
3	R/W	0x0	ETXIE Enable EMAC Transmit Clock Invertor. 0: Disable 1: Enable
2	R/W	0x0	EPIT EMAC PHY Interface Type 0: MII 1: RGMII
1:0	R/W	0x0	ETCS. EMAC Transmit Clock Source 00: Transmit clock source for MII 01: External transmit clock source for RMII and RGMII 10: Internal transmit clock source for RMII and RGMII 11: Reserved

3.6.3.3. BROM Output Register (Default Value: 0x0000_0000)

Offset:0x00A4			**Register Name: BROM_OUTPUT_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
1	R/W	0x0	BROM_OUTPUT_VALUE. 0: U-Boot pin output 0 1: U-Boot pin output 1
0	R/W	0x0	BROM_OUTPUT_ENALBE. 0: Disable U-Boot pin output 1: Enable U-Boot pin output

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3.7. Timer

3.7.1. Overview

The timer module implements the timing and counting functions.The timer module includes timer0 and timer1,watchdog, AVS and 64-bit counter.

The timer0 and timer1 are completely consistent.The timer0/1 has the following features:

- Configurable count clock: LOSC and OSC24M. LOSC is the internal low-frequency clock or the external low-frequency clock by setting LOSC_SRC_SEL. The external low-frequency has much accuracy.
- Configurable 8 prescale factor
- Programmable 32-bit down timer
- Supports two working modes: continue mode and single count mode
- Generates an interrupt when the count is decreased to 0

The watchdog is used to transimit a reset signal to reset the entire system after an exception occurs in the system.The watchdog has the following features:

- Single clock sourece: OSC24M/750
- Supports 12 initial values to configure
- Supports the generation of timeout interrupts
- Supports the generation of reset signal
- Supports watchdog restart the timing

The AVS is used to the synchronization of audio and video. The AVS module includes AVS0 and AVS1, the AVS0 and AVS1 are completely consistent.The AVS has the following features:

- Single clock source: OSC24M
- Programmable 33-bit up timer
- Initial value can be updated anytime
- 12-bit frequency divider factor
- Supports Pause/Start function

The 64-bit Counter is used to count timing for GPU.The 64-bit Counter has the following features:

- 64-bit counter
- Supports clear zero function
- Performs latch operation once before getting the current counter value

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3.7.2. Block Diagram

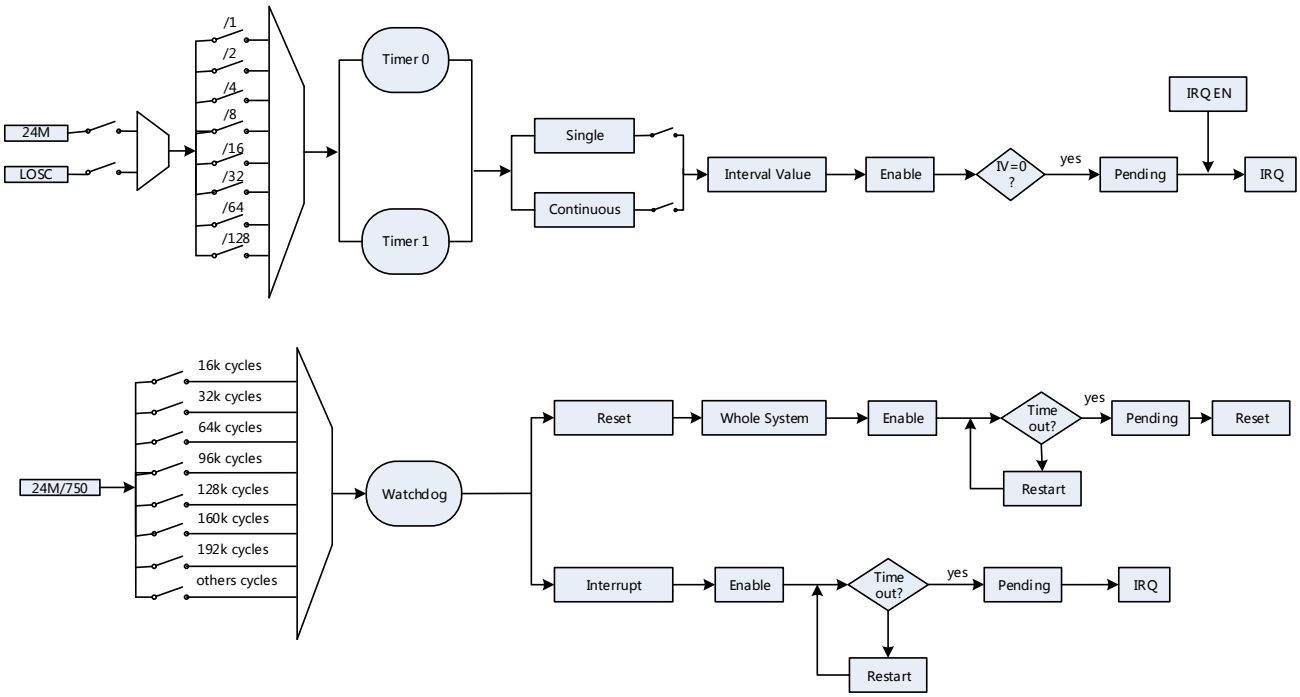


Figure 3-24. Timer Block Diagram

3.7.3. Operations and Functional Descriptions

3.7.3.1. Timer Formula

$$T_{timer0} = \frac{TMR0_INTV_VALUE_REG - TMR0_CUR_VALUE_REG}{TMR0_CLK_SRC} \times TMR0_CLK_PRES$$

TMR0_INTV_VALUE_REG: timer initial value;

TMR0_CUR_VALUE_REG: timer current counter;

TMR0_CLK_SRC: timer clock source;

TMR0_CLK_PRES: timer clock prescale ratio.

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3.7.3.2. Typical Application

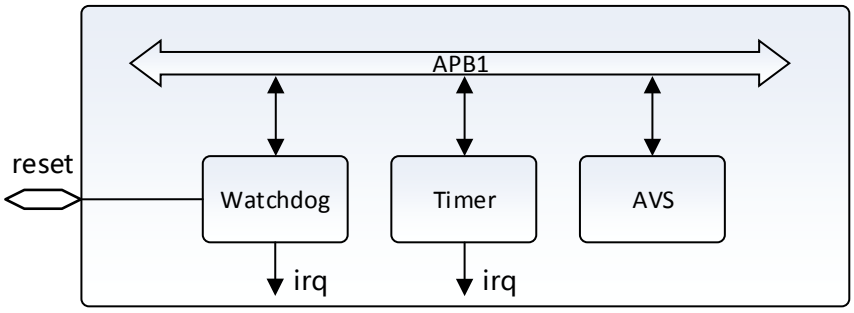


Figure 3-25. Timer Application Diagram

3.7.3.3. Function Implemention

3.7.3.3.1. Timer

The timer is a 32-bit down counter, the counter value is decreased by 1 on each rising edge of the count clock. Each timer has independent interrupt.

The timer has two operating modes.

- Continuous mode

The bit7 of TMRn_CTRL_REG is set to the continuous mode, when the count value is decreased to 0, the timer module reloads data from TMRn_INTV_VALUE_REG then continues to count.

- Single mode

The bit7 of TMRn_CTRL_REG is set to the single mode, when the count value is decreased to 0, the timer stops counting. The timer starts to count again only when a new initial value is loaded.

Each timer has a prescaler that divides the working clock frequency of each timer by 1,2,4,8,16,32,64,128.

3.7.3.3.2. Watchdog

The watchdog is a 32-bit down counter, the counter value is decreased by 1 on each rising edge of the count clock.

The watchdog has two operating modes.

- Interrupt mode

WDOG0_CFG_REG is set to 0x10, when the counter value reaches 0 and WDOG0_IRQ_EN_REG is enabled, the watchdog generates an interrupt.

- Reset mode

WDOG0_CFG_REG is set to 0x01, when the counter value reaches 0, the watchdog generates a reset signal to reset the

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entire system.

The clock source of the watchdog is OSC24M/750.There are 12 configurable initial count values.
The watchdog can restart to count by setting WDOG0_CTRL_REG: write 0xA57 to bit[12:1],then write 1 to bit[0].

3.7.3.3.3. AVS

The AVS is a 33-bit up counter.The counter value is increased by 1 on each rising edge of the count clock.

The AVS can be operated after its clock gating in CCU module is opened.

The AVS has an OSC24M clock source and a 12-bit division factor N. When the timer increases to N from 0, AVS counter adds 1; when the counter reaches 33-bit upper limit,the AVS will start to count from initial value again.

In counter working process, the division factor and initial counter of the AVS can be changed anytime.And the AVS can stop or start to operate counter anytime.

3.7.3.4. Operating Mode

3.7.3.4.1. Timer Initial

(1) Configure the timer parameters: clock source, prescale factor, working mode. The configuration of these parameters have no sequence,and implement by writing TMRn_CTRL_REG.
(2) Write the initial value: write TMRn_INTV_VALUE_REG to provide an initial value for the timer; write the bit[1] of TMRn_CTRL_REG to load the initial value to the timer, the bit[1] can not be written again before it is cleared automatically.
(3) Enable timer: write the bit[0] of TMRn_CTRL_REG to enable timer count; read TMRn_CUR_VALUE_REG to get the current count value.

3.7.3.4.2. Timer Interrupt

(1) Enable interrupt: write corresponding interrupt enable bit of TMR_IRQ_EN_REG, when timer counter time reaches, the corresponding interrupt generates.
(2) After enter interrupt process, write TMR_IRQ_STA_REG to clear the interrupt pending, and execute the process of waiting for the interrupt.
(3) Resume the interrupt and continue to execute the interrupted process.

3.7.3.4.3. Watchdog Initial

(1) Write WDOG0_CFG_REG to configure the generation of the interrupts and the output of reset signal.

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(2) Write WDOG0_MODE_REG to configure the initial count value.
(3) Write WDOG0_MODE_REG to enable the watchdog.

3.7.3.4.4. Watchdog Interrupt

Watchdog interrupt is only used for the counter.
(1) Write WDOG0_IRQ_EN_REG to enable the interrupt.
(2) After enter the interrupt process, write WDOG0_IRQ_STA_REG to clear the interrupt pending, and execute the process of waiting for the interrupt.
(3) Resume the interrupt and continue to execute the interrupted process.

3.7.3.4.5. AVS Start/Pause

(1) Write AVS_CNT_DIV_REG to configure the division factor.
(2) Write AVS_CNT_REG to configure the initial count value.
(3) Write AVS_CNT_CTL_REG to enable AVS counter.

3.7.4. Programming Guidelines

3.7.4.1. Timer

Take making a 1ms delay for an example, 24M clock source, single mode and 2 pre-scale will be selected in the instance.

```
writel(0x2EE0,TMR_0_INTV);                  //Set interval value
writel(0x94, TMR_0_CTRL);                   //Select Single mode,24MHz clock source,2 pre-scale
writel(readl(TMR_0_CTRL)|(1<<1), TMR_0_CTRL);  //Set Reload bit
while((readl(TMR_0_CTRL)>>1)&1);            //Waiting Reload bit turns to 0
writel(readl(TMR_0_CTRL)|(1<<0), TMR_0_CTRL);  //Enable Timer0
```

3.7.4.2. Watchdog Reset

In the following instance making configurations for Watchdog: configurate clock source as 24M/750, configurate Interval Value as 1s and configurate Watchdog Configuration as To whole system. This instance indicates that reset system after 1s.

```
writel(0x1, WDOG_CONFIG);                   //To whole system
writel(0x10, WDOG_MODE);                    //Interval Value set 1s
writel(readl(WDOG_MODE)|(1<<0), WDOG_MODE);    //Enable Watchdog
```

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3.7.4.3. Watchdog Restart

In the following instance making configurations for Watchdog: configurate clock source as 24M/750, configurate Interval Value as 1s and configurate Watchdog Configuration as To whole system. In the following instance, if the time of other codes is larger than 1s, watchdog will reset the whole system. If the sentence of restart watchdog is implemented inside 1s, watchdog will be restarted.

```
writel(0x1, WDOG_CONFIG);                          //To whole system
writel(0x10, WDOG_MODE);                           //Interval Value set 1s
writel(readl(WDOG_MODE)|(1<<0), WDOG_MODE);        //Enable Watchdog
----other codes---
writel(readl(WDOG_CTRL)|(0xA57<<1)|(1<<0)， WDOG_CTRL); //Writel 0xA57 at Key Field and Restart Watchdog
```

3.7.5. Register List

Module Name	Base Address
Timer	0x0300 9000

Register Name	Offset	Description
TMR_IRQ_EN_REG	0x0000	Timer IRQ Enable Register
TMR_IRQ_STA_REG	0x0004	Timer Status Register
TMR0_CTRL_REG	0x0010	Timer 0 Control Register
TMR0_INTV_VALUE_REG	0x0014	Timer 0 Interval Value Register
TMR0_CUR_VALUE_REG	0x0018	Timer 0 Current Value Register
TMR1_CTRL_REG	0x0020	Timer 1 Control Register
TMR1_INTV_VALUE_REG	0x0024	Timer 1 Interval Value Register
TMR1_CUR_VALUE_REG	0x0028	Timer 1 Current Value Register
CNT_TEST_REG	0x0094	Counter Test Mode Register
WDOG_IRQ_EN_REG	0x00A0	Watchdog IRQ Enable Register
WDOG_IRQ_STA_REG	0x00A4	Watchdog Status Register
WDOG_CTRL_REG	0x00B0	Watchdog Control Register
WDOG_CFG_REG	0x00B4	Watchdog Configuration Register
WDOG_MODE_REG	0x00B8	Watchdog Mode Register
AVS_CNT_CTL_REG	0x00C0	AVS Control Register
AVS_CNT0_REG	0x00C4	AVS Counter 0 Register
AVS_CNT1_REG	0x00C8	AVS Counter 1 Register
AVS_CNT_DIV_REG	0x00CC	AVS Divisor Register
CNT64_CTRL_REG	0x0100	64-bit Counter Control Register
CNT64_LOW_REG	0x0104	64-bit Counter Low Register
CNT64_HIGH_REG	0x0108	64-bit Counter High Register

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3.7.6. Register Description

3.7.6.1. Timer IRQ Enable Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TMR_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1S	0x0	TMR1_IRQ_EN. Timer 1 Interrupt Enable. 0: No effect 1: Timer 1 Interval Value reached interrupt enable
0	R/W1S	0x0	TMR0_IRQ_EN. Timer 0 Interrupt Enable. 0: No effect 1: Timer 0 Interval Value reached interrupt enable

3.7.6.2. Timer IRQ Status Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: TMR_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
1	R/W1C	0x0	TMR1_IRQ_PEND. Timer 1 IRQ Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending, timer 1 interval value is reached
0	R/W1C	0x0	TMR0_IRQ_PEND. Timer 0 IRQ Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending, timer 0 interval value is reached

3.7.6.3. Timer 0 Control Register(Default Value: 0x0000_0004)

Offset: 0x0010			Register Name: TMR0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TMR0_MODE. Timer 0 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR0_CLK_PRES.

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			Select the pre-scale of timer 0 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR0_CLK_SRC. 00:LOSC 01: OSC24M 10: / 11: /
1	R/W	0x0	TMR0_RELOAD. Timer 0 Reload. 0: No effect 1: Reload timer 0 Interval value After the bit is set, it can not be written again before it is cleared automatically.
0	R/W	0x0	TMR0_EN. Timer 0 Enable. 0: Stop/Pause 1: Start If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.7.6.4. Timer 0 Interval Value Register

Offset: 0x0014			Register Name: TMR0_INTV_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR0_INTV_VALUE. Timer 0 Interval Value.

NOTE

The value setting should consider the system clock and the timer clock source.

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3.7.6.5. Timer 0 Current Value Register

Offset: 0x0018			Register Name: TMR0_CUR_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR0_CUR_VALUE. Timer 0 Current Value.

NOTE

Timer 0 current value is a 32-bit down-counter (from interval value to 0).

3.7.6.6. Timer 1 Control Register(Default Value: 0x0000_0004)

Offset: 0x0020			Register Name: TMR1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TMR1_MODE. Timer 1 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR1_CLK_PRES. Select the pre-scale of timer 1 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR1_CLK_SRC. 00:LOSC 01: OSC24M 10: / 11: /
1	R/W	0x0	TMR1_RELOAD. Timer 1 Reload. 0: No effect 1: Reload timer 1 Interval value After the bit is set, it can not be written again before it's cleared automatically.
0	R/W	0x0	TMR1_EN. Timer 1 Enable.

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			0: Stop/Pause 1: Start If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.7.6.7. Timer 1 Interval Value Register

Offset: 0x0024			Register Name: TMR1_INTV_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR1_INTV_VALUE. Timer 1 Interval Value.

NOTE

The value should consider the system clock and the timer clock source.

3.7.6.8. Timer 1 Current Value Register

Offset: 0x0028			Register Name:TMR1_CUR_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR1_CUR_VALUE. Timer 1 Current Value.

NOTE

Timer 1 current value is a 32-bit down-counter (from interval value to 0).

3.7.6.9. Counter Test Mode Register(Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: CNT_TEST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/.
0	R/W	0x0	CNT64_TEST_EN. 64-bit Counter Test Mode Enable. 0: Normal Mode

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			1: Test Mode. In the Test Mode, this Counter Low/High registers will count simultaneously.

3.7.6.10. Watchdog IRQ Enable Register(Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name:WDOG_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1S	0x0	WDOG_IRQ_EN. Watchdog Interrupt Enable. 0: No effect 1: Watchdog interrupt enable.

3.7.6.11. Watchdog Status Register (Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name:WDOG_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1C	0x0	WDOG_IRQ _PEND. Watchdog IRQ Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending, Watchdog interval value is reached

3.7.6.12. Watchdog Control Register(Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name:WDOG_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:1	R/W	0x0	WDOG_KEY_FIELD. Watchdog Key Field. Should be written at value 0xA57. Writing any other value in this field aborts the write operation.
0	R/W1S	0x0	WDOG_RESTART. Watchdog Restart. 0: No effect 1: Restart the Watchdog 0

3.7.6.13. Watchdog Configuration Register (Default Value: 0x0000_0001)

Offset: 0x00B4			Register Name:WDOG_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:2	/	/	/
1:0	R/W	0x1	WDOG_CONFIG. 00:/ 01: to whole system 10: only interrupt 11: /

3.7.6.14. Watchdog Mode Register (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name:WDOG_MODE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:4	R/W	0x0	WDOG_INTV_VALUE. Watchdog Interval Value. Watchdog clock source is OSC24M / 750. If the clock source is turned off, Watchdog 0 will not work. 0000: 16000 cycles (0.5s) 0001: 32000 cycles (1s) 0010: 64000 cycles (2s) 0011: 96000 cycles (3s) 0100: 128000 cycles (4s) 0101: 160000 cycles (5s) 0110: 192000 cycles (6s) 0111: 256000 cycles (8s) 1000: 320000 cycles (10s) 1001: 384000 cycles (12s) 1010: 448000 cycles (14s) 1011: 512000 cycles (16s) 1100: / 1101: / 1110: / 1111: /
3:1	/	/	/
0	R/W1S	0x0	WDOG_EN. Watchdog Enable. 0: No effect 1: Enable the Watchdog

3.7.6.15. AVS Counter Control Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: AVS_CNT_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/

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9	R/W	0x0	AVS_CNT1_PS. Audio/Video Sync Counter 1 Pause Control 0: Not pause 1: Pause Counter 1
8	R/W	0x0	AVS_CNT0_PS. Audio/Video Sync Counter 0 Pause Control 0: Not pause 1: Pause Counter 0
7:2	/	/	/
1	R/W	0x0	AVS_CNT1_EN. Audio/Video Sync Counter 1 Enable/ Disable. The counter source is OSC24M. 0: Disable 1: Enable
0	R/W	0x0	AVS_CNT0_EN. Audio/Video Sync Counter 1 Enable/ Disable. The counter source is OSC24M. 0: Disable 1: Enable

3.7.6.16. AVS Counter 0 Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: AVS_CNT0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	AVS_CNT0. Counter 0 for Audio/ Video Sync Application The high 32 bits of the internal 33-bits counter register. The initial value of the internal 33-bits counter register can be set by software. The LSB bit of the 33-bits counter register should be zero when the initial value is updated. It will count from the initial value. The initial value can be updated at any time. It can also be paused by setting AVS_CNT0_PS to '1'. When it is paused, the counter will not increase.

3.7.6.17. AVS Counter 1 Register(Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name:AVS_CNT1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	AVS_CNT1. Counter 1 for Audio/ Video Sync Application The high 32 bits of the internal 33-bits counter register. The initial value of the internal 33-bits counter register can be set by software. The LSB bit of the 33-bits counter register should be zero when the initial value is updated. It will count from the initial value. The initial value can be updated at any time. It can also be paused by setting AVS_CNT1_PS to '1'. When it is paused, the counter will not increase.

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3.7.6.18. AVS Counter Divisor Register (Default Value: 0x05DB_05DB)

Offset: 0x00CC			Register Name: AVS_CNT_DIV_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x5DB	AVS_CNT1_D. Divisor N for AVS Counter 1 AVS CN1 CLK=24MHz/Divisor_N1. Divisor N1 = Bit [27:16] + 1. The number N is from 1 to 0x7ff. The zero value is reserved. The internal 33-bits counter engine will maintain another 12-bits counter. The 12-bits counter is used for counting the cycle number of one 24Mhz clock. When the 12-bits counter reaches (>= N) the divisor value, the internal 33-bits counter register will increase 1 and the 12-bits counter will reset to zero and restart again. It can be configured by software at any time.
15:12	/	/	/
11:0	R/W	0x5DB	AVS_CNT0_D. Divisor N for AVS Counter 0 AVS CN0 CLK=24MHz/Divisor_N0. Divisor N0 = Bit [11:0] + 1 The number N is from 1 to 0x7ff. The zero value is reserved. The internal 33-bits counter engine will maintain another 12-bits counter. The 12-bits counter is used for counting the cycle number of one 24Mhz clock. When the 12-bits counter reaches (>= N) the divisor value, the internal 33-bits counter register will increase 1 and the 12-bits counter will reset to zero and restart again. It can be configured by software at any time.

3.7.6.19. 64-bit Counter Control Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: CNT64_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/.
2	R/W	0x0	CNT64_CLK_SRC_SEL. 64-bit Counter Clock Source Select. 0: OSC24M 1: /
1	R/W	0x0	CNT64_RL_EN. 64-bit Counter Read Latch Enable. 0: no effect 1: to latch the 64-bit Counter to the Low/Hi registers and it will change to zero

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			after the registers are latched.
0	R/W	0x0	CNT64_CLR_EN. 64-bit Counter Clear Enable. 0: no effect 1: to clear the 64-bit Counter Low/Hi registers and it will change to zero after the registers are cleared. It is not recommended to clear this counter arbitrarily.

NOTE

This 64-bit up-counter will start to count as soon as the System Power On finished.

3.7.6.20. 64-bit Counter Low Register (Default Value: 0x0000_0000)

Offset: 0x0104			Register Name: CNT64_LOW_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CNT64_LO. 64-bit Counter [31:0].

3.7.6.21. 64-bit Counter High Register (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: CNT64_HIGH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CNT64_HI. 64-bit Counter [63:32].

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3.8. High Speed Timer

3.8.1. Overview

The high speed timer(HSTimer) module implements the timing and counting functions.The HSTimer has the following features:

- Timing clock is AHB1 that can provides more accurate timing clock, the normal working frequency is 200MHz
- Configurable 5 prescale factor
- Configurable 56-bit down timer
- Supports 2 working modes: continuous mode and single mode
- Supports test mode
- Generates an interrupt when the count is decreased to 0

3.8.2. Block Diagram

Figure3-26 shows a block diagram of the HSTimer.

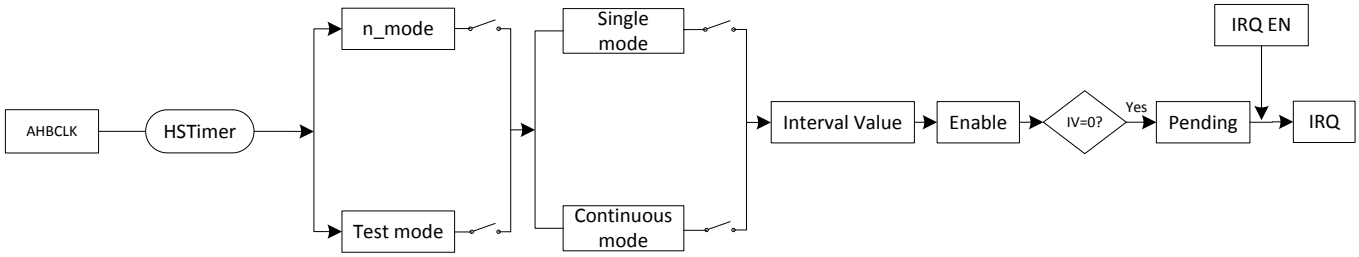


Figure 3-26. HSTimer Block Diagram

3.8.3. Operations and Functional Description

3.8.3.1. HSTimer Formula

$$\frac{(HS_TMR_INTV_HI_REG<<32 + HS_TMR_INTV_LO_REG) - (HS_TMR_CURNT_HI_REG<<32 + HS_TMR_CURNT_LO_REG)}{AHB1CLK} \times HS_TMR_CLK$$

HS_TMR_INTV_HI_REG: Initial of Counter Higher Bit

HS_TMR_INTV_LO_REG: Initial of Counter Lower Bit

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HS_TMR_CURNT_HI_REG: Current Value of Counter Higher Bit

HS_TMR_CURNT_LO_REG: Current Vaule of Counter Lower Bit

AHB1CLK: AHB1 Clock Frequency

HS_TMR_CLK: Time Prescale Ratio of Counter

3.8.3.2. Typical Application

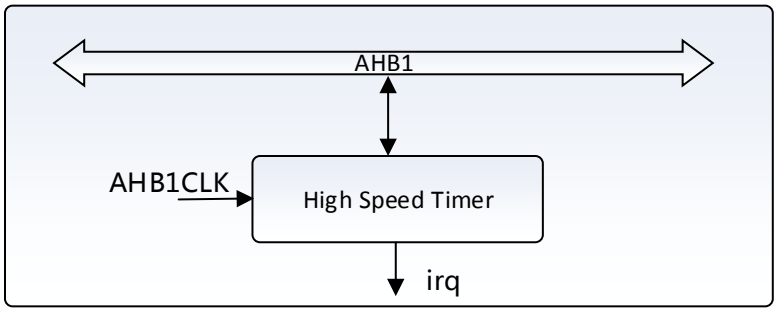


Figure 3-27. HSTimer Application Diagram

The high speed timer is on AHB1, and the high speed timer controls registers by AHB1.

The high speed timer has single clock source: AHB. The high speed timer can generate interrupt.

3.8.3.3. Function Implemention

The timer is a 56-bit down counter, the counter value is decreased by 1 on each rising edge of the count clock.

The high speed timer has two timing modes.

- Continuous mode : The bit7 of HS_TMR0_CTRL_REG is set to the continuous mode, when the count value is decreased to 0, the high speed timer module reloads data from HS_TMR_INTV_LO_REG and HS_TMR_INTV_HI_REG then continues to count.
- Single mode : The bit7 of HS_TMR0_CTRL_REG is set to the single mode, when the count value is decreased to 0, the high speed timer stops counting. The high speed timer starts to count again only when a new initial value is loaded.

The high speed timer has two operating modes.

- Normal mode: When the bit31 of HS_TMR0_CTRL_REG is set to the normal mode, the high speed timer is used as 56-bit down counter, which can continuous timing and single timing.
- Test mode: When the bit31 of HS_TMR0_CTRL_REG is set to the normal mode, then HS_TMR_INTV_LO_REG must be set to 0x1, the high speed timer is used as 24-bit down counter, and HS_TMR_INTV_HI_REG is the initial value of the high speed timer.

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Each high speed timer has a prescaler that divides the working clock frequency of each working timer by 1,2,4,8, 16.

3.8.3.4. Operating Mode

3.8.3.4.1. HSTimer Initial

(1) AHB1 clock management: Open the clock gating of AHB1 and de-assert the soft reset of AHB1 in CCU.
(2) Configure the corresponding parameters of the high speed timer: clock source, prescaler factor, working mode, counting mode. These parameters that are written to HS_TMR0_CTRL_REG have no sequences.
(3) Write the initial value: Firstly write the low-bit register HS_TMR_INTV_LO_REG, then write the high-bit register HS_TMR_INTV_HI_REG. Write the bit1 of HS_TMR0_CTRL_REG to load the initial value. If in timing stop stage of high speed timer, write the bit1 and bit0 of HS_TMR0_CTRL_REG to reload the initial value.
(4) Enable high speed timer: Write the bit[0] of HS_TMR0_CTRL_REG to enable high speed timer to count.

3.8.3.4.2. HSTimer Interrupt

(1) Enable interrupt: Write the corresponding interrupt enable bit of HS_TMR_IRQ_EN_REG, when the counting time of high speed timer reaches , the corresponding interrupt generates.
(2) After enter the interrupt process, write HS_TMR_IRQ_STAS_REG to clear the interrupt pending.
(3) Resume the interrupt and continue to execute the interrupted process.

3.8.4. Programming Guidelines

Take making a 1us delay using HSTimer0 for an instance as follow, AHB1CLK will be configurated as 100MHz and n_mode,Single mode and 2 pre-scale will be selected in this instance.

```
writel(0x0, HS_TMR0_INTV_HI);                          //Set interval value Hi 0x0
writel(0x32, HS_TMR0_INTV_LO);                         //Set interval value Lo 0x32
writel(0x90, HS_TMR0_CTRL);                            //Select n_mode,2 pre-scale,single mode
writel(readl(HS_TMR0_CTRL)|(1<<1), HS_TMR0_CTRL);      //Set Reload bit
writel(readl(HS_TMR0_CTRL)|(1<<0), HS_TMR0_CTRL);      //Enable HSTimer0
While(!(readl(HS_TMR_IRQ_STAT)&1));                    //Wait for HSTimer0 to generate pending
Writel(1,HS_TMR_IRQ_STAT);                             //Clear HSTimer0 pending
```

3.8.5. Register List

Module Name	Base Address
High Speed Timer	0x0300 5000

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Register Name	Offset	Description
HS_TMR_IRQ_EN_REG	0x0000	HS Timer IRQ Enable Register
HS_TMR_IRQ_STAS_REG	0x0004	HS Timer Status Register
HS_TMR0_CTRL_REG	0x0020	HS Timer 0 Control Register
HS_TMR0_INTV_LO_REG	0x0024	HS Timer 0 Interval Value Low Register
HS_TMR0_INTV_HI_REG	0x0028	HS Timer 0 Interval Value High Register
HS_TMR0_CURNT_LO_REG	0x002C	HS Timer 0 Current Value Low Register
HS_TMR0_CURNT_HI_REG	0x0030	HS Timer 0 Current Value High Register

3.8.6. Register Description

3.8.6.1. HS Timer IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: HS_TMR_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1S	0x0	HS_TMR0_INT_EN. High Speed Timer 0 Interrupt Enable. 0: No effect 1: High Speed Timer 0 Interval Value reached interrupt enable

3.8.6.2. HS Timer IRQ Status Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: HS_TMR_IRQ_STAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1C	0x0	HS_TMR0_IRQ_PEND. High Speed Timer 0 IRQ Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending, High speed timer 0 interval value is reached

3.8.6.3. HS Timer 0 Control Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: HS_TMR0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HS_TMR0_TEST. High speed timer 0 test mode. In test mode, the low register should be set to 0x1, the high register will down counter. The counter needs to be reloaded. 0: Normal mode 1: Test mode
30:8	/	/	/

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7	R/W	0x0	HS_TMR0_MODE. High Speed Timer 0 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	HS_TMR0_CLK Select the pre-scale of the high speed timer 0 clock sources. 000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: /
3:2	/	/	/
1	R/W1S	0x0	HS_TMR0_RELOAD. High Speed Timer 0 Reload. 0: No effect 1: Reload High Speed Timer 0 Interval Value
0	R/W	0x0	HS_TMR0_EN. High Speed Timer 0 Enable. 0: Stop/Pause 1: Start If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.8.6.4. HS Timer 0 Interval Value Lo Register(Default Value: 0x0000_0000)

Offset: 0x0024			**Register Name: HS_TMR0_INTV_LO_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HS_TMR0_INTV_VALUE_LO. High Speed Timer 0 Interval Value [31:0].

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3.8.6.5. HS Timer 0 Interval Value Hi Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: HS_TMR0_INTV_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	HS_TMR0_INTV_VALUE_HI. High Speed Timer 0 Interval Value [55:32].

NOTE

The interval value register is a 56-bit register. When read or write the interval value, the Lo register should be readed or written first. And the High register should be written after the Lo register.

3.8.6.6. HS Timer 0 Current Value Lo Register(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: HS_TMR0_CURNT_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HS_TMR0_CUR_VALUE_LO. High Speed Timer 0 Current Value [31:0].

3.8.6.7. HS Ticmer 0 Current Value Hi Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: HS_TMR0_CURNT_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	HS_TMR0_CUR_VALUE_HI. High Speed Timer 0 Current Value [55:32].

NOTE

HS timer current value is a 56-bit down-counter (from interval value to 0).
The current value register is a 56-bit register. When read or write the current value, the Low register should be readed or written first.

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3.9. PWM

3.9.1. Overview

The PWM is pulse width modulation module in the system domain. The PWM has the following features:

- Supports single pulse and cycle pulse output
- Supports frequency range from 0 to 24MHz
- Adjustable duty cycle from 0% to 100%
- The minimum resolution is 1/65536

3.9.2. Block Diagram

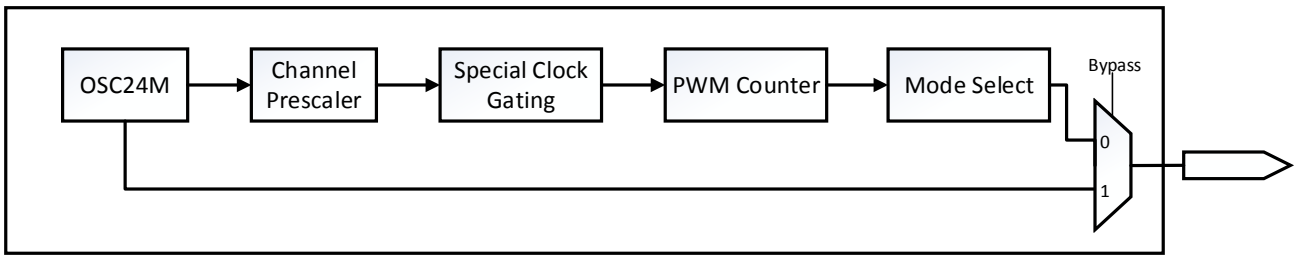


Figure 3-28. PWM Block Diagram

3.9.3. Operations and Functional Description

3.9.3.1. External Signal

The external signal of PWM has multiplexing function with other I/O pin. Configure multiplexing function of GPIO(General Purpose Input Output) by software in Port Controller module to use PWM.

3.9.3.2. Clock and Reset

The clock source of PWM is OSC24M. The PWM is on APB1 Bus. Ensure that open APB1 Bus gating and de-assert reset signal when accessed to the PWM.

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3.9.3.3. Typical Application

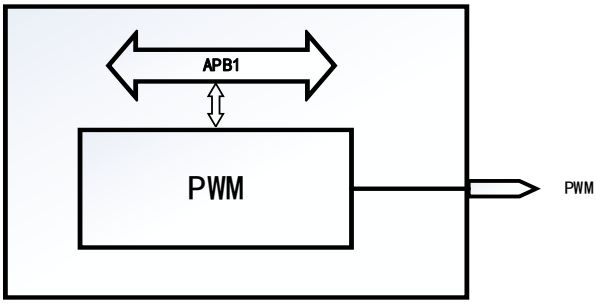


Figure 3-29. PWM Application Diagram

3.9.3.4. Function Implemention

3.9.3.4.1. Clock Control

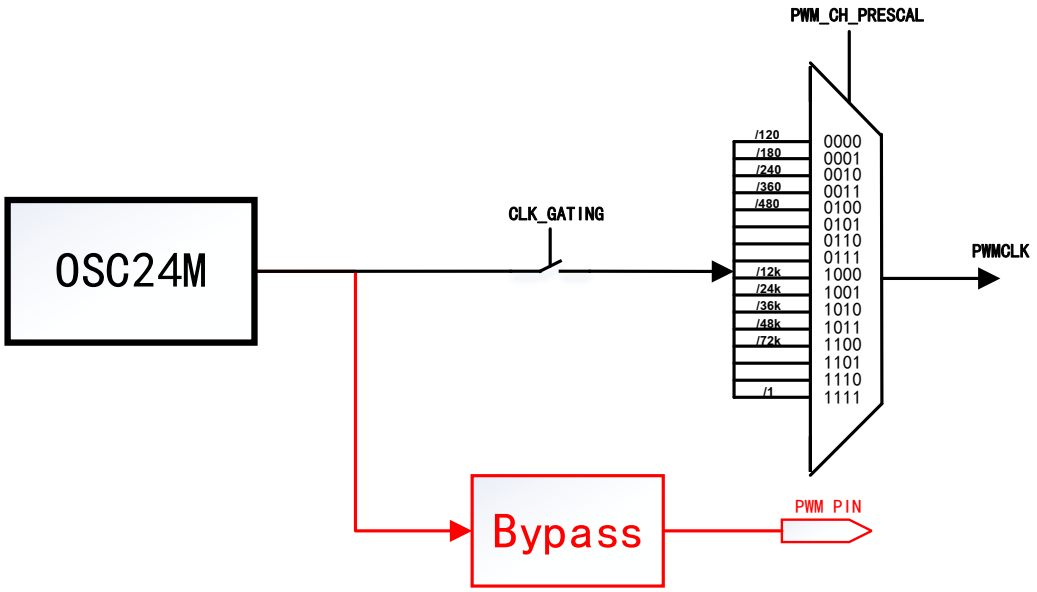


Figure 3-30. PWM Clock Control

The clock controller part of PWM includes clock switch (CLK_GATING), prescale factor selecting (PWM_CH_PRESCAL) and clock source bypass (PWM_BYPASS). Open CLK_GATING and configure prescale factor before used clock source, the output clock(PWMCLK) is delivered to the PWM module. OSC24M clock source is bypassed directly to the PWM output pin by clock source bypass part.

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3.9.3.4.2. Output Mode

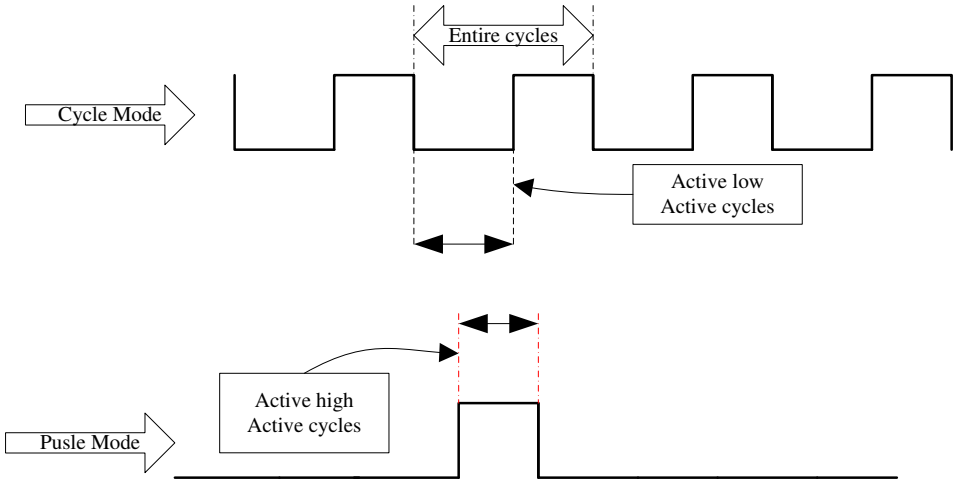


Figure 3-31. PWM Output Mode

PWM supports cycle mode and single pulse mode.

Cycle mode: When the value of up-counter reaches Entire Cycles, the value is decreased to 0 , PWM continues to count and outputs a continuous waveform.

Single pulse mode: When the value of up-counter reaches Entire Cycles, the value is decreased to 0, PWM stops counting and outputs a single pulse waveform.

3.9.3.4.3. Output Parameter

The period ,duty cycle and active state of PWM output waveform are decided by up-counter and comparator. The rule of comparator is as follows.

(1) Cycle mode

Counter < (Entire Cycles-Active Cycles), output active state

Counter > (Entire Cycles-Active Cycles), output inactive state

Active state can be set to high level or low level.

Output waveform period = （OSC24M/PWM_CH_PRESCAL）$^{-1}$ *PWM_CH_ENTIRE_CYS

Output active state time = （OSC24M/PWM_CH_PRESCAL）$^{-1}$ *PWM_CH_ENTIRE_ACT_CYS

Output inactive state time = （ OSC24M/PWM_CH_PRESCAL ）$^{-1}$ * （ PWM_CH_ENTIRE_CYS - PWM_CH_ENTIRE_ACT_CYS）

Duty cycle = PWM_CH_ENTIRE_ACT_CYS /PWM_CH_ENTIRE_CYS

(2) Single pulse mode

Pulse width = （OSC24M/PWM_CH_PRESCAL）$^{-1}$ *PWM_CH_ENTIRE_ACT_CYS

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3.9.3.5. Operating Mode

3.9.3.5.1. Clock Configuration

(1) Clock source bypass: After the bit 9 of **PWM_CTRL_REG** is enabled, PWM port can output OSC24M clock.
(2) Clock Gating: Enable the bit6 of **PWM_CTRL_REG** to use PWM clock.
(3) Prescale factor: Set the bit[3:0] of **PWM_CTRL_REG** to select corresponding prescale factor.

3.9.3.5.2. PWM Parameter

(1) Select mode: Select cycle mode or pulse mode by the bit7 of **PWM_CTRL_REG**.
(2) Output level: Select low level or high level by the bit5 of **PWM_CTRL_REG**.
(3) Initial value: Set **PWM_CH_ENTIRE_ACT_CYS** and **PWM_CH_ENTIRE_CYS** by **PWM_CH_PERIOD**.

3.9.4. Programming Guidelines

(1) The active cycles in **PWM_CH_PERIOD** must be less than entire cycles.
(2) Read the bit28 of **PWM_CTRL_REG** before writing **PWM_CH_PERIOD**.

3.9.5. Register List

Module Name	Base Address
PWM	0x0300 A000

Register Name	Offset	Description
PWM_CTRL_REG	0x0000	PWM Control Register
PWM_CH0_PERIOD	0x0004	PWM Channel 0 Period Register

3.9.6. Register Description

3.9.6.1. PWM Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: PWM_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	PWM0_BYPASS. PWM channel 0 bypass enable. If the bit is set to 1, PWM0's output is OSC24MHz. 0: Disable

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			1: Enable
8	R/W	0x0	PWM_CH0_PUL_START. PWM channel 0 pulse output start. 0: No effect 1: Output 1 pulse. The pulse width should be according to the period 0 register[15:0],and the pulse state should be according to the active state. After the pulse is finished,the bit will be cleared automatically.
7	R/W	0x0	PWM_CHANNEL0_MODE. 0: Cycle mode 1: Pulse mode
6	R/W	0x0	SCLK_CH0_GATING. Gating the Special Clock for PWM0 0: Mask 1: Pass
5	R/W	0x0	PWM_CH0_ACT_STA. PWM channel 0 active state. 0: Low Level 1: High Level
4	R/W	0x0	PWM_CH0_EN. PWM channel 0 enable. 0: Disable 1: Enable
3:0	R/W	0x0	PWM_CH0_PRESCAL. PWM channel 0 prescalar. These bits should be setting before the PWM channel 0 clock gate on. 0000: /120 0001: /180 0010: /240 0011: /360 0100: /480 0101: / 0110: / 0111: / 1000: /12k 1001: /24k 1010: /36k 1011: /48k 1100: /72k 1101: / 1110: / 1111: /1

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3.9.6.2. PWM Channel 0 Period Register

Offset: 0x0004			Register Name: PWM_CH0_PERIOD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	UDF	PWM_CH0_ENTIRE_CYS Number of the entire cycles in the PWM clock. 0 : 1 cycle 1: 2 cycles …… N: N+1 cycles If the register need to be modified dynamically, the PCLK should be faster than the PWM CLK(PWM CLK = 24MHz/pre-scale).
15:0	R/W	UDF	PWM_CH0_ENTIRE_ACT_CYS Number of the active cycles in the PWM clock. 0: 0 cycle 1: 1 cycles …… N : N cycles

NOTE

The active cycles should be no larger than the period cycles.

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3.10. DMA

3.10.1. Overview

The direction memory access (DMA) is used to transfer data between a peripheral and a memory, between peripherals, or between memories. DMA is a high-speed data transfer operation that reduces the CPU resources. DMA has the following features.

- 16 channels DMA
- Provides 32 peripheral DMA requests for data read and 32 peripheral DMA requests for data write
- Supports script memory
- Supports transfer with linked list
- DRQ response includes wait mode and handshake mode
- Memory Devices supports non-aligned transform
- DMA channel supports pause function

3.10.2. Block Diagram

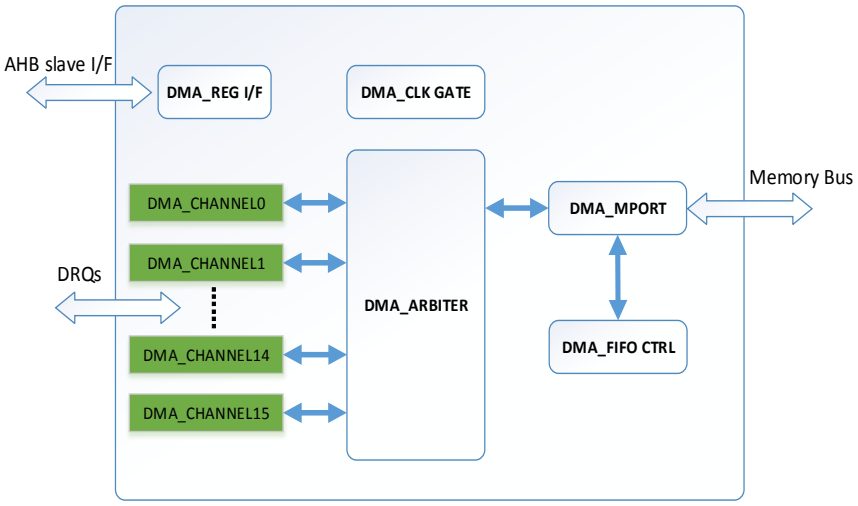


Figure 3-32. DMA Block Diagram

DMA_ARBITER: Arbitrate DMA read/write requirement of each channel, and convert to read/write requirement of each port.

DMA_CHANNEL: DMA transform engine.Each channel is independent. The priorities of DMA channels uses polling mechanism. When the DMA requests from two peripherals are valid simultaneously, if DMA_ARBITER is non-idle ,the next channel of the current channel has the higher priority; if DMA_ARBITER is idle, the channel0 has the highest

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priority, whereas the channel11 has the lowest priority.
DMA_MPORT: Receive read/write requirement of DMA_ARBITER ,and convert to the corresponding MBUS access.
DMA_FIFOCTL: Internal FIFO cell control module.
DMA_REGIF: Common register module, mainly used to resolve AHB1 demand.
DMA_CLKGATE: Hardware auto clock gating control module.

DMA integrates 16 independent DMA channels. When DMA channel starts, DMA gets DMA descriptor by DMA_DESC_ADDR_REG to use for the configuration information of the current DMA package transfer ,and DMA can transfer data between the specified peripherals through the configuration information. When a package transfer finished, DMA judges if the current channel transfer finished through the linked information in descriptor.

3.10.3. Operations and Functional Description

3.10.3.1. Clock and Reset

DMA is on AHB1.The clock of AHB1 influences the transfer efficiency of DMA.

3.10.3.2. Typical Application

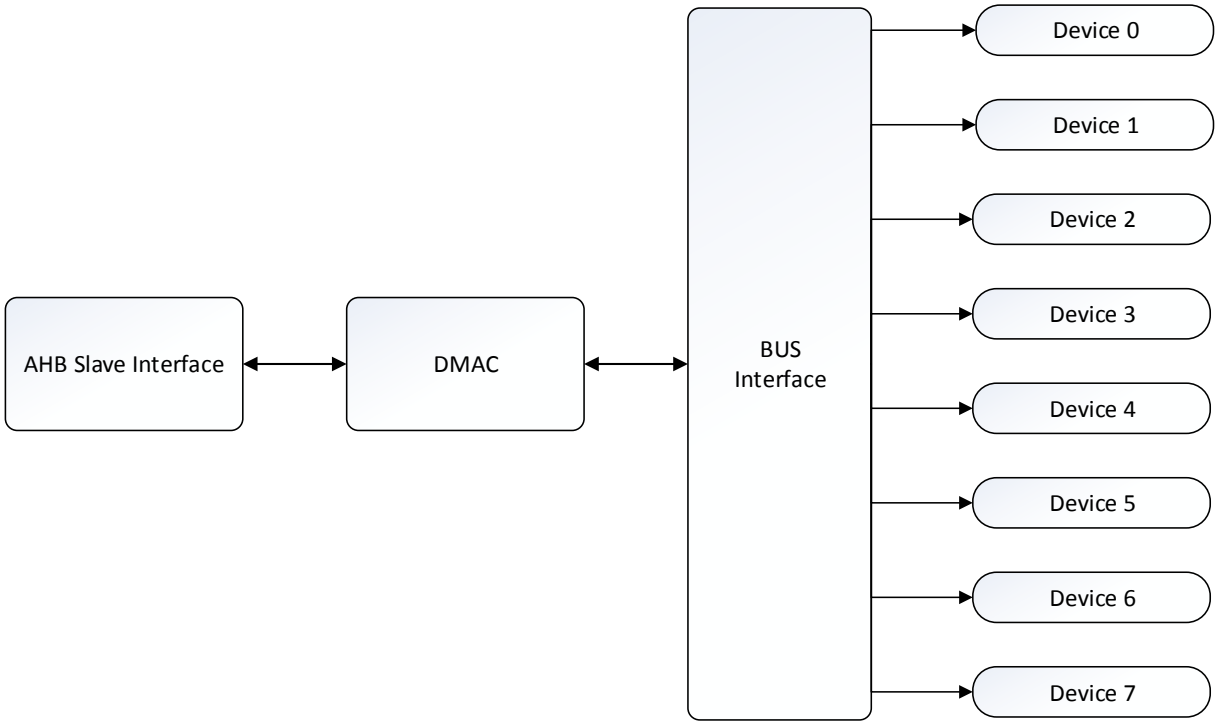


Figure 3-33. DMA Typical Application Diagram

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3.10.3.3. DRQ Type

Table 3-9. DMA DRQ Table

Source DRQ Type		Destination DRQ Type	
port0	SRAM	port0	SRAM
port1	DRAM	port1	DRAM
port2	OWA-RX	port2	OWA-TX
port3	I2S/PCM0-RX	port3	I2S/PCM0-TX
port4	I2S/PCM1-RX	port4	I2S/PCM1-TX
port5	I2S/PCM2-RX	port5	I2S/PCM2-TX
port6	I2S/PCM3-RX	port6	I2S/PCM3-TX
port7	DMIC	port7	
port8		port8	
port9	CE-RX	port9	CE-TX
port10	NAND0	port10	NAND0
port11		port11	
port12		port12	
port13		port13	CIR-TX
port14	UART0-RX	port14	UART0-TX
port15	UART1-RX	port15	UART1-TX
port16	UART2-RX	port16	UART2-TX
port17	UART3-RX	port17	UART3-TX
port18		port18	
port19		port19	
port20		port20	
port21		port21	
port22	SPI0-RX	port22	SPI0-TX
port23	SPI1-RX	port23	SPI1-TX
port24		port24	
port25		port25	
port26		port26	
port27		port27	
port28		port28	
port29		port29	
Port30	OTG_EP1	Port30	OTG_EP1
Port31	OTG_EP2	Port31	OTG_EP2
Port32	OTG_EP3	Port32	OTG_EP3
Port33	OTG_EP4	Port33	OTG_EP4
Port34		Port34	
Port35		Port35	
Port36		Port36	
Port37		Port37	
Port38		Port38	

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Port39		Port39	
Port40		Port40	
Port41		Port41	
Port42		Port42	
Port43	Audio_HUB0_RX	Port43	Audio_HUB0_TX
Port44	Audio_HUB1_RX	Port44	Audio_HUB1_TX
Port45	Audio_HUB2_RX	Port45	Audio_HUB2_TX

3.10.3.4. DMA Descriptor



Figure 3-34. DMA Descriptor

DMA descriptor is the configuration information of DMA transfer that decides the DMA working mode. Each descriptor includes 6 words, in turn, configuration, source address, destination address, byte counter, parameter, link.

Configuration : Configure the following information by DMA_CFG_REG.

- DRQ type of source and destination.
- Transferred address count mode : IO mode indicates the address is fixed during transfer; linear mode indicates the address is increasing during transfer.
- Transferred block length : block length is the amount of DMA transferred data in one-shot valid DRQ. The block length supports 1-bit,4-bit,8-bit or 16-bit mode.
- Transferred data width: data width indicates the data width of every operation, and supports 8-bit,16-bit,32-bit or 64-bit mode.

Source Address: Configure the transferred source address.

Destination Address: Configure the transferred destination address.

DMA reads data from the source address , then writes data to the destination address.

Byte counter: Configure the amount of a package. The maximum package is not more than (2^25-1) bytes. If the

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amount of the package reaches the maximum value, even if DRQ is valid, DMA should stop the current transfer.

Parameter: Configure the interval between data block. The parameter is valid for non-memory peripherals. When DMA detects that DRQ is high level, DMA transfers block cycle. And during time, the changing of DRQ is ignored.After transferred, DMA waits the setting cycle(WAIT_CYC), then executes the next DRQ detection.

If the value of the link is 0xFFFFF800, the current package is at the end of the linked list. DMA will stop transfer after the package is transferred; if the value of the link is not 0xFFFFF800, the value of the link is considered the descriptor address of the next package.

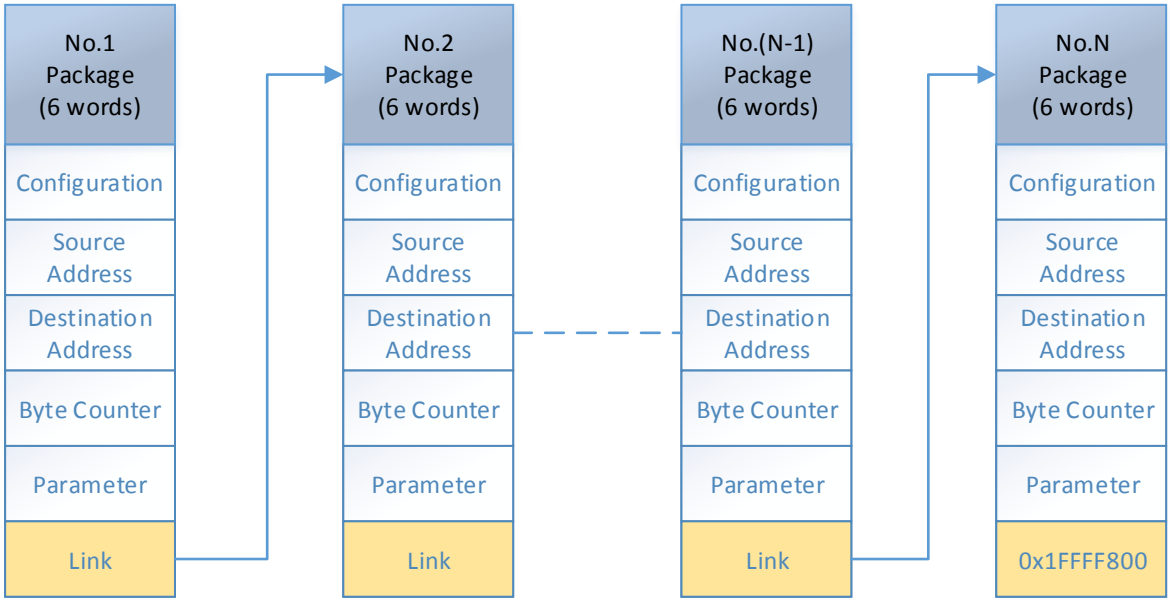


Figure 3-35. DMA Chain Transfer

3.10.3.5. Interrupt

The half package interrupt is enabled, DMA sends half package interrupt after the half package transfer completes. The total package interrupt is enabled, DMA sends package end interrupt after the total package transfer completes. The total queue interrupt is enabled, DMA sends queue end interrupt after the total queue completes. Notice that when CPU does not respond to the interrupts timely, or two DMA interrupts generate very closely, the later interrupt may override the former one. So DMA has only a system interrupt source.

3.10.3.6. Clock Gating

DMA CLK GATE module is the clock module of auto-controlled by hardware. DMA CLK GATE module is mainly used to generate the clock of DMA sub-module and the local circuit in module, including clock gating of channel and clock gating of public part.

The clock gating of the channel indicates DMA clock can auto-open when the system accesses the current DMA channel register and DMA channel is enabled. When DMA transfer is completed, DMA channel clock can auto-close after 16 HCLK delay, meanwhile the clock of the corresponding channel control and FIFO control will be closed.

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The clock gating of the common part indicates the clock of the common circuit can auto-close when all DMA channels are opened. The common circuit includes the common circuit of FIFO control module, MPORT module and memory bus clock.

DMA clock gating can support all the functions stated above or not by software.

3.10.3.7. Transfer Mode

DMA supports two data transfer modes: wait mode and handshake mode.

(1) Wait Mode

When device request signal enters DMA, the device request signal is transformed into the internal DRQ signal through block and wait counter. The transformed principle is as follows.

- When DMA detects the external request signal valid, DMA starts to operate the device, the internal DRQ always holds high level before the block operating amount reaches.
- When the transfer amount of DMA reaches the block operating amount, the internal DRQ pulls low automatically.
- After the internal DRQ holds low automatically to the DMA cycle of wait counter times, DMA restarts to detect the external request, if the external request signal is valid, then the next transfer starts.

(2) Handshake Mode

- When DMA detects the external request signal valid, DMA starts to operate the device, the internal DRQ always holds high level before the block operating amount reaches.
- When the transfer amount of DMA reaches the block operating amount, the internal DRQ pulls low automatically; meanwhile within the last operation , DMA follows the operating demand to send DMA last signal simultaneously.
- The DMA last signal that is used as a part of DMA demand transmits at BUS, when the device receives the operating demand of DMA last at BUS, the device can judge DMA transfer block length finished, that is before transmit the request again ,DMA operation cannot appear, and a DMA active signal is generated to the DMA controller. Notice that each DRQ signal of device corresponds to an active signal, if the device has many DRQ signals, then DMA returns different active signal through different bus operation.
- When DMA receives the transmitted active signal of devices, DMA ACK signal is returned to devices.
- After the device receives DMA ACK signal, if all operations of devices are completed , FIFO status and DRQ status are refreshed, then active signal is set as invalid.
- When DMA detects the falling edge of active signal, then the corresponding ACK signal is set as invalid, and DMA restarts to detect the external request signal. If the request signal is valid, then the next transfer starts.

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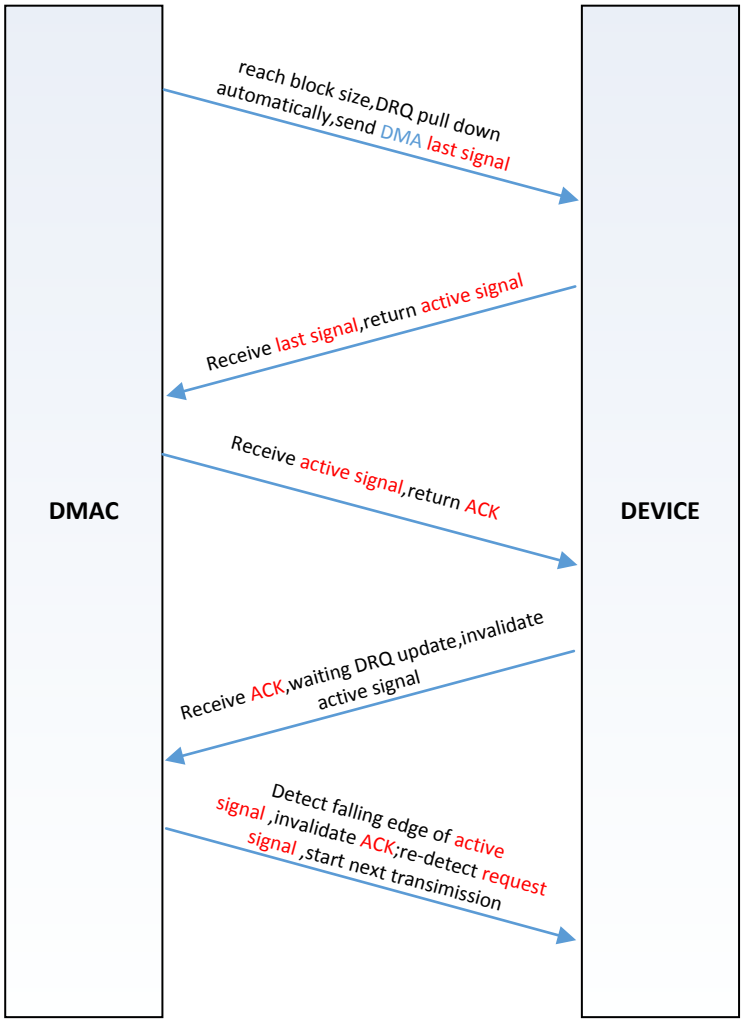


Figure 3-36. DMA Transfer Mode

3.10.3.8. Autoalignment Function

The DMA supports address alignment of non-IO devices, that is when the start address of non-IO devices is non 32-byte aligned, DMA firstly aligns the burst transfer within 32-byte to 32-byte. If the device of a DMA channel is configured to non-IO type, and the start address is 0x86, then DMA firstly aligns 26-byte burst transfer to 0xA0, then DMA transfers by 64-byte burst(maximum transfer amount of MBUS allowed). The address alignment function helps to improve the DRAM access efficiency.

IO devices does not support address alignment, so the bit width of IO devices must match the address offset, or not DMA ignores the non-consistency and indirectly transmits data of the corresponding bit width to the address.

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3.10.3.9. Operating Mode

3.10.3.9.1. Clock Control

- The DMA clock is synchronous with AHB1 clock. Make sure that open the DMA gating bit of AHB1 clock before access DMA register.
- The reset input signal of DMA is asynchronous with AHB1, and is low valid by default. Make sure that de-assert the reset signal of DMA before access DMA register.
- To avoid indefinite state within registers , firstly de-assert the reset signal, secondly open the gating bit of AHB1.
- DMA has the function of clock auto gating ,DMA clock can be disabled in DMA idle state using software to reduce power consumption. DMA enables clock auto gating by default.

3.10.3.9.2. DMA Transfer Process

The DMA transfer process is as follows.

(1) Request DMA channel, and judge the idle state of the channel by the enable or disable of DMA channel.
(2) Write the descriptor with 6-word into memory, the descriptor must be word-aligned. Refer to 3.10.3.4 DMA descriptor in detail.
(3) Write the start address of storing descriptor to **DMA_DESC_ADDR_REG**.
(4) Enable DMA channel, and write the corresponding channel to **DMA_EN_REG**.
(5) DMA obtains the descriptor information.
(6) Start to transmit a package ,when half package is completed, DMA sends **Half Package Transfer Interrupt**; when total package is completed, DMA sends **Package End Transfer Interrupt**. These interrupt status can be read by **DMA_IRQ_PEND_REG**.
(7) Set **DMA_PAU_REG** to pause or resume the data transfer.
(8) After completed the total package transfer, DMA decides to start the next package transfer or end the transfer by the link of the descriptor. If the link is 0xFFFFF800, the transfer ends; if the link is other value, the next package starts to transmit. When the transfer ends, DMA sends **Queue End Transfer Interrupt**.
(9) Disable the DMA channel.

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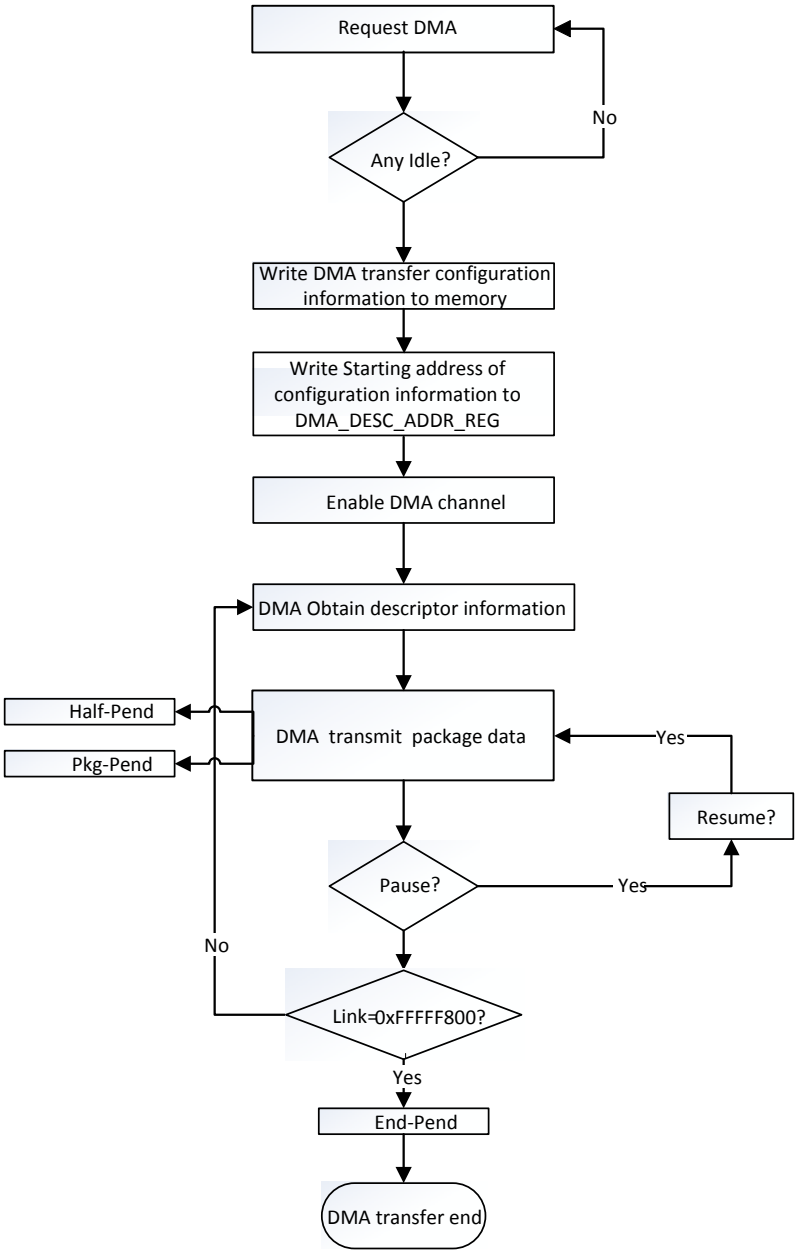


Figure 3-37. DMA Transfer Process

3.10.3.9.3. DMA Interrupt

(1) Enable interrupt: write the corresponding interrupt enable of DMA_IRQ_EN_REG, when the corresponding interrupt condition is satisfied,the corresponding interrupt generates.

(2) After enter the interrupt process, write DMA_IRQ_PEND_REG to clear the interrupt pending，and execute the process of waiting for the interrupt.

(3) Resume the interrupt and continue to execute the interrupted process.

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3.10.4. Programming Guidelines

When the DMA transfer is paused, this is equivalent to invalid DRQ. Because DMA transfer command has a certain time delay, DMA will not stop transfer immediately until the current command and the command in Arbiter finished, at most 32byte data.

DMA application example :

```
writel(0x00000000, mem_address + 0x00);   //Setting configuration, mem_address must be word-aligned
writel(0x00001000, mem_address + 0x04);    // Setting the start address for the source device
writel(0x20000000, mem_address + 0x08);   //Setting the start address for the destination device
writel(0x00000020, mem_address + 0x0C);   // Setting data package size
writel(0x00000000, mem_address + 0x10);   //Setting parameter
writel(0xFFFFF800, mem_address + 0x14);          //Setting the start address for the next descriptor
writel(mem_address, 0x01C02000+ 0x100 + 0x08); //Setting the start address for the DMA channel0 descriptor
do{
If(mem_address == readl(0x01C02000 + 0x100 + 0x08));
break;
}while(1);              //Make sure writing operation valid
writel(0x000000001, 0x01C02000 + 0x100 + 0x00);      // Enable DMA channel0 transfer
```

DMA supports increasing data package in transfer, there are a few points to note here.

- When the value of **DMA Channel Descriptor Address Register** is 0xFFFFF800, it indicates that DMA channel has got back the descriptor of the last package. When DMA channel completed the package data transfer, DMA channel will stop automatically data transfer.
- If needing increase data package,then at first it is essential to judge that whether DMA channel has got back the descriptor of the last package, if DMA channel has got back the descriptor of the last package, then this is impossible for increasing data package, DMA channel need start again. If DMA is not transmitting the last package,then the last descriptor address 0xFFFFF800 can be changed to the start address of the next descriptor.
- To ensure that the data changed valid, we can read again the value of *DMA Channel Descriptor Address Register* after changed the data. If there is not 0xFFFFF800,then it indicates that increasing data package is succeed, and fail otherwise. Because the process of increasing data package need some time, during this time,DMA channel may get back the descriptor of the last package.At the moment we can read again **DMA Channel Current Source Address Register** and **DMA Channel Current Destination Address Register**, if the increasing memory address accords with the information of the increasing data package, then the increasing data package is succeed, and fail otherwise.
- To ensure the higher success rate, it is suggested that increase data package before half package interrupt of penultimate data package.

3.10.5. Register List

Module Name	Base Address
DMA	0x0300 2000

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Register Name	Offset	Description
DMA_IRQ_EN_REG0	0x0000	DMA IRQ Enable Register 0
DMA_IRQ_EN_REG1	0x0004	DMA IRQ Enable Register 1
DMA_IRQ_PEND_REG0	0x0010	DMA IRQ Pending Register 0
DMA_IRQ_PEND_REG1	0x0014	DMA IRQ Pending Register 1
DMA_SEC_REG	0x0020	DMA Security Register
DMA_AUTO_GATE_REG	0x0028	DMA Auto Gating Register
DMA_STA_REG	0x0030	DMA Status Register
DMA_EN_REG	0x0100+N*0x0040	DMA Channel Enable Register (N=0~15)
DMA_PAU_REG	0x0100+N*0x0040+0x0004	DMA Channel Pause Register(N=0~15)
DMA_DESC_ADDR_REG	0x0100+N*0x0040+0x0008	DMA Channel Start Address Register(N=0~15)
DMA_CFG_REG	0x0100+N*0x0040+0x000C	DMA Channel Configuration Register(N=0~15)
DMA_CUR_SRC_REG	0x0100+N*0x0040+0x0010	DMA Channel Current Source Register(N=0~15)
DMA_CUR_DEST_REG	0x0100+N*0x0040+0x0014	DMA Channel Current Destination Register(N=0~15)
DMA_BCNT_LEFT_REG	0x0100+N*0x0040+0x0018	DMA Channel Byte Counter Left Register(N=0~15)
DMA_PARA_REG	0x0100+N*0x0040+0x001C	DMA Channel Parameter Register(N=0~15)
DMA_MODE_REG	0x0100+N*0x0040+0x0028	DMA Mode Register(N=0~15)
DMA_FDESC_ADDR_REG	0x0100+N*0x0040+0x002C	DMA Former Descriptor Address Register(N=0~15)
DMA_PKG_NUM_REG	0x0100+N*0x0040+0x0030	DMA Package Number Register(N=0~15)

3.10.6. Register Description

3.10.6.1. DMA IRQ Enable Register0 (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: DMA_IRQ_EN_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	DMA7_QUEUE_IRQ_EN DMA 7 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
29	R/W	0x0	DMA7_PKG_IRQ_EN DMA 7 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
28	R/W	0x0	DMA7_HLAF_IRQ_EN DMA 7 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
27	/	/	/
26	R/W	0x0	DMA6_QUEUE_IRQ_EN DMA 6 Queue End Transfer Interrupt Enable. 0: Disable

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			1: Enable
25	R/W	0x0	DMA6_PKG_IRQ_EN DMA 6 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
24	R/W	0x0	DMA6_HLAF_IRQ_EN DMA 6 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
23	/	/	/
22	R/W	0x0	DMA5_QUEUE_IRQ_EN DMA 5 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
21	R/W	0x0	DMA5_PKG_IRQ_EN DMA 5 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
20	R/W	0x0	DMA5_HLAF_IRQ_EN DMA 5 Half package Transfer Interrupt Enable. 0: Disable 1: Enable
19	/	/	/
18	R/W	0x0	DMA4_QUEUE_IRQ_EN DMA 4 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
17	R/W	0x0	DMA4_PKG_IRQ_EN DMA 4 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
16	R/W	0x0	DMA4_HLAF_IRQ_EN DMA 4 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
15	/	/	/
14	R/W	0x0	DMA3_QUEUE_IRQ_EN DMA 3 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
13	R/W	0x0	DMA3_PKG_IRQ_EN DMA 3 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
12	R/W	0x0	DMA3_HLAF_IRQ_EN

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			DMA 3 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
11	/	/	/
10	R/W	0x0	DMA2_QUEUE_IRQ_EN DMA 2 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
9	R/W	0x0	DMA2_PKG_IRQ_EN DMA 2 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
8	R/W	0x0	DMA2_HLAF_IRQ_EN DMA 2 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
7	/	/	/
6	R/W	0x0	DMA1_QUEUE_IRQ_EN DMA 1 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
5	R/W	0x0	DMA1_PKG_IRQ_EN DMA 1 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
4	R/W	0x0	DMA1_HLAF_IRQ_EN DMA 1 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	DMA0_QUEUE_IRQ_EN DMA 0 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
1	R/W	0x0	DMA0_PKG_IRQ_EN DMA 0 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
0	R/W	0x0	DMA0_HLAF_IRQ_EN DMA 0 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable

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3.10.6.2. DMA IRQ Enable Register1 (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: DMA_IRQ_EN_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	DMA15_QUEUE_IRQ_EN DMA 15 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
29	R/W	0x0	DMA15_PKG_IRQ_EN DMA 15 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
28	R/W	0x0	DMA15_HLAF_IRQ_EN DMA 15 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
27	/	/	/
26	R/W	0x0	DMA14_QUEUE_IRQ_EN DMA 14 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
25	R/W	0x0	DMA14_PKG_IRQ_EN DMA 14 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
24	R/W	0x0	DMA14_HLAF_IRQ_EN DMA 14 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
23	/	/	/
22	R/W	0x0	DMA13_QUEUE_IRQ_EN DMA 13 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
21	R/W	0x0	DMA13_PKG_IRQ_EN DMA 13 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
20	R/W	0x0	DMA13_HLAF_IRQ_EN DMA 13 Half package Transfer Interrupt Enable. 0: Disable 1: Enable
19	/	/	/
18	R/W	0x0	DMA12_QUEUE_IRQ_EN

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			DMA 12 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
17	R/W	0x0	DMA12_PKG_IRQ_EN DMA 12 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
16	R/W	0x0	DMA12_HLAF_IRQ_EN DMA 12 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
15	/	/	/
14	R/W	0x0	DMA11_QUEUE_IRQ_EN DMA 11 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
13	R/W	0x0	DMA11_PKG_IRQ_EN DMA 11 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
12	R/W	0x0	DMA11_HLAF_IRQ_EN DMA 11 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
11	/	/	/
10	R/W	0x0	DMA10_QUEUE_IRQ_EN DMA 10 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
9	R/W	0x0	DMA10_PKG_IRQ_EN DMA 10 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
8	R/W	0x0	DMA10_HLAF_IRQ_EN DMA 10 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
7	/	/	/
6	R/W	0x0	DMA9_QUEUE_IRQ_EN DMA 9 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
5	R/W	0x0	DMA9_PKG_IRQ_EN DMA 9 Package End Transfer Interrupt Enable. 0: Disable

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			1: Enable
4	R/W	0x0	DMA9_HLAF_IRQ_EN DMA 9 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	DMA8_QUEUE_IRQ_EN DMA 8 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
1	R/W	0x0	DMA8_PKG_IRQ_EN DMA 8 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
0	R/W	0x0	DMA8_HLAF_IRQ_EN DMA 8 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable

3.10.6.3. DMA IRQ Pending Status Register 0 (Default Value: 0x0000_0000)

Offset:0x0010			**Register Name: DMA_IRQ_PEND_REG0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W1C	0x0	DMA7_QUEUE_IRQ_PEND. DMA 7 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
29	R/W1C	0x0	DMA7_PKG_IRQ_ PEND DMA 7 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
28	R/W1C	0x0	DMA7_HLAF_IRQ_PEND. DMA 7 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
27	/	/	/
26	R/W1C	0x0	DMA6_QUEUE_IRQ_PEND. DMA 6 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending

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25	R/W1C	0x0	DMA6_PKG_IRQ_ PEND DMA 6 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
24	R/W1C	0x0	DMA6_HLAF_IRQ_PEND. DMA 6 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
23	/	/	/
22	R/W1C	0x0	DMA5_QUEUE_IRQ_PEND. DMA 5 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
21	R/W1C	0x0	DMA5_PKG_IRQ_ PEND DMA 5 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
20	R/W1C	0x0	DMA5_HLAF_IRQ_PEND. DMA 5 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
19	/	/	/
18	R/W1C	0x0	DMA4_QUEUE_IRQ_PEND. DMA 4 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
17	R/W1C	0x0	DMA4_PKG_IRQ_ PEND DMA 4 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
16	R/W1C	0x0	DMA4_HLAF_IRQ_PEND. DMA 4 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
15	/	/	/
14	R/W1C	0x0	DMA3_QUEUE_IRQ_PEND. DMA 3 Queue End Transfer Interrupt Pending. Setting 1 to the bit

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			will clear it. 0: No effect, 1: Pending.
13	R/W1C	0x0	DMA3_PKG_IRQ_ PEND DMA 3 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
12	R/W1C	0x0	DMA3_HLAF_IRQ_PEND. DMA 3 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
11	/	/	/
10	R/W1C	0x0	DMA2_QUEUE_IRQ_PEND. DMA 2 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
9	R/W1C	0x0	DMA2_PKG_IRQ_ PEND DMA 2 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
8	R/W1C	0x0	DMA2_HLAF_IRQ_PEND. DMA 2 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
7	/	/	/
6	R/W1C	0x0	DMA1_QUEUE_IRQ_PEND. DMA 1 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
5	R/W1C	0x0	DMA1_PKG_IRQ_ PEND DMA 1 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
4	R/W1C	0x0	DMA1_HLAF_IRQ_PEND. DMA 1 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
3	/	/	/

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2	R/W1C	0x0	DMA0_QUEUE_IRQ_PEND. DMA 0 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
1	R/W1C	0x0	DMA0_PKG_IRQ_ PEND DMA 0 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
0	R/W1C	0x0	DMA0_HLAF_IRQ_PEND. DMA 0 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending

3.10.6.4. DMA IRQ Pending Status Register 1 (Default Value: 0x0000_0000)

Offset:0x0014			**Register Name: DMA_IRQ_PEND_REG0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W1C	0x0	DMA15_QUEUE_IRQ_PEND. DMA 15 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
29	R/W1C	0x0	DMA15_PKG_IRQ_ PEND DMA 15 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
28	R/W1C	0x0	DMA15_HLAF_IRQ_PEND. DMA 15 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
27	/	/	/
26	R/W1C	0x0	DMA14_QUEUE_IRQ_PEND. DMA 14 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
25	R/W1C	0x0	DMA14_PKG_IRQ_ PEND DMA 14 Package End Transfer Interrupt Pending. Setting 1 to the

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			bit will clear it. 0: No effect 1: Pending
24	R/W1C	0x0	DMA14_HLAF_IRQ_PEND. DMA 14 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
23	/	/	/
22	R/W1C	0x0	DMA13_QUEUE_IRQ_PEND. DMA 13 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
21	R/W1C	0x0	DMA13_PKG_IRQ_ PEND DMA 13 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
20	R/W1C	0x0	DMA13_HLAF_IRQ_PEND. DMA 13 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
19	/	/	/
18	R/W1C	0x0	DMA12_QUEUE_IRQ_PEND. DMA 12 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
17	R/W1C	0x0	DMA12_PKG_IRQ_ PEND DMA 12 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
16	R/W1C	0x0	DMA12_HLAF_IRQ_PEND. DMA 12 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
15	/	/	/
14	R/W1C	0x0	DMA11_QUEUE_IRQ_PEND. DMA 11 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect, 1: Pending.

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13	R/W1C	0x0	DMA11_PKG_IRQ_ PEND DMA 11 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
12	R/W1C	0x0	DMA11_HLAF_IRQ_PEND. DMA 11 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
11	/	/	/
10	R/W1C	0x0	DMA10_QUEUE_IRQ_PEND. DMA 10 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
9	R/W1C	0x0	DMA10_PKG_IRQ_ PEND DMA 10 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
8	R/W1C	0x0	DMA10_HLAF_IRQ_PEND. DMA 10 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
7	/	/	/
6	R/W1C	0x0	DMA9_QUEUE_IRQ_PEND. DMA 9 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
5	R/W1C	0x0	DMA9_PKG_IRQ_ PEND DMA 9 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
4	R/W1C	0x0	DMA9_HLAF_IRQ_PEND. DMA 9 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
3	/	/	/
2	R/W1C	0x0	DMA8_QUEUE_IRQ_PEND. DMA 8 Queue End Transfer Interrupt Pending. Setting 1 to the bit

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			will clear it. 0: No effect 1: Pending
1	R/W1C	0x0	DMA8_PKG_IRQ_ PEND DMA 8 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
0	R/W1C	0x0	DMA8_HLAF_IRQ_PEND. DMA 8 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending

3.10.6.5. DMA Security Register (Default Value: 0x0000_0000)

Offset:0x0020			Register Name: DMA_SEC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	DMA15_SEC DMA channel 15 security. 0: Secure 1: Non-secure.
14	R/W	0x0	DMA14_SEC DMA channel 14 security. 0: Secure 1: Non-secure.
13	R/W	0x0	DMA13_SEC DMA channel 13 security. 0: Secure 1: Non-secure.
12	R/W	0x0	DMA12_SEC DMA channel 12 security. 0: Secure 1: Non-secure.
11	R/W	0x0	DMA11_SEC DMA channel 11 security. 0: Secure 1: Non-secure.
10	R/W	0x0	DMA10_SEC DMA channel 10 security. 0: Secure 1: Non-secure.
9	R/W	0x0	DMA9_SEC

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			DMA channel 9 security. 0: Secure 1: Non-secure.
8	R/W	0x0	DMA8_SEC DMA channel 8 security. 0: Secure 1: Non-secure.
7	R/W	0x0	DMA7_SEC DMA channel 7 security. 0: Secure 1: Non-secure.
6	R/W	0x0	DMA6_SEC DMA channel 6 security. 0: Secure 1: Non-secure.
5	R/W	0x0	DMA5_SEC DMA channel 5 security. 0: Secure 1: Non-secure.
4	R/W	0x0	DMA4_SEC DMA channel 4 security. 0: Secure 1: Non-secure.
3	R/W	0x0	DMA3_SEC DMA channel 3 security. 0: Secure 1: Non-secure.
2	R/W	0x0	DMA2_SEC DMA channel 2 security. 0: Secure 1: Non-secure.
1	R/W	0x0	DMA1_SEC DMA channel 1 security. 0: Secure 1: Non-secure.
0	R/W	0x0	DMA0_SEC DMA channel 0 security. 0: Secure 1: Non-secure.

3.10.6.6. DMA Auto Gating Register (Default Value: 0x0000_0000)

Offset:0x0028			Register Name: DMA_AUTO_GATE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:3	/	/	/
2	R/W	0x0	DMA_MCLK_CIRCUIT. DMA MCLK interface circuit auto gating bit. 0: Auto gating enable 1: Auto gating disable
1	R/W	0x0	DMA_COMMON_CIRCUIT. DMA common circuit auto gating bit. 0: Auto gating enable 1: Auto gating disable
0	R/W	0x0	DMA_CHAN_CIRCUIT. DMA channel circuit auto gating bit. 0: Auto gating enable 1: Auto gating disable

NOTE

When initializing DMA Controller, bit-2 should be set up.

3.10.6.7. DMA Status Register (Default Value: 0x0000_0000)

Offset:0x0030			Register Name: DMA_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R	0x0	MBUS FIFO Status 0: Empty 1: Not Empty
29:16	/	/	/
15	R	0x0	DMA15_STATUS DMA Channel 15 Status. 0: Idle 1: Busy
14	R	0x0	DMA14_STATUS DMA Channel 14 Status. 0: Idle 1: Busy
13	R	0x0	DMA13_STATUS DMA Channel 13 Status. 0: Idle 1: Busy
12	R	0x0	DMA12_STATUS DMA Channel 12 Status. 0: Idle 1: Busy
11	R	0x0	DMA11_STATUS

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			DMA Channel 11 Status. 0: Idle 1: Busy
10	R	0x0	DMA10_STATUS DMA Channel 10 Status. 0: Idle 1: Busy
9	R	0x0	DMA9_STATUS DMA Channel 9 Status. 0: Idle 1: Busy
8	R	0x0	DMA8_STATUS DMA Channel 8 Status. 0: Idle 1: Busy
7	R	0x0	DMA7_STATUS DMA Channel 7 Status. 0: Idle 1: Busy
6	R	0x0	DMA6_STATUS DMA Channel 6 Status. 0: Idle 1: Busy
5	R	0x0	DMA5_STATUS DMA Channel 5 Status. 0: Idle 1: Busy
4	R	0x0	DMA4_STATUS DMA Channel 4 Status. 0: Idle 1: Busy
3	R	0x0	DMA3_STATUS DMA Channel 3 Status. 0: Idle 1: Busy
2	R	0x0	DMA2_STATUS DMA Channel 2 Status. 0: Idle 1: Busy
1	R	0x0	DMA1_STATUS DMA Channel 1 Status. 0: Idle 1: Busy
0	R	0x0	DMA0_STATUS DMA Channel 0 Status.

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			0: Idle 1: Busy

3.10.6.8. DMA Channel Enable Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0000(N=0~15)			Register Name: DMA_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	DMA_EN. DMA Channel Enable 0: Disable 1: Enable

3.10.6.9. DMA Channel Pause Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0004(N=0~15)			Register Name: DMA_PAU_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	DMA_PAUSE. Pausing DMA Channel Transfer Data. 0: Resume Transferring 1: Pause Transferring

3.10.6.10. DMA Channel Descriptor Address Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0008(N=0~15)			Register Name: DMA_DESC_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DMA_DESC_ADDR DMA Channel Descriptor Address. The Descriptor Address must be word-aligned.

3.10.6.11. DMA Channel Configuration Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x000C(N=0~15)			Register Name: DMA_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:25	R	0x0	DMA_DEST_DATA_WIDTH. DMA Destination Data Width. 00: 8-bit 01: 16-bit 10: 32-bit

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			11: 64-bit
24	R	0x0	DMA_ADDR_MODE. DMA Destination Address Mode 0: Linear Mode 1: IO Mode
23:22	R	0x0	DMA_DEST_BLOCK_SIZE. DMA Destination Block Size. 00: 1 01: 4 10: 8 11: 16
21:16	R	0x0	DMA_DEST_DRQ_TYPE. DMA Destination DRQ Type The details in DRQ Type and Port Corresponding Relation.
15:11	/	/	/
10:9	R	0x0	DMA_SRC_DATA_WIDTH. DMA Source Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: 64-bit
8	R	0x0	DMA_SRC_ADDR_MODE. DMA Source Address Mode 0: Linear Mode 1: IO Mode
7:6	R	0x0	DMA_SRC_BLOCK_SIZE. DMA Source Block Size. 00: 1 01: 4 10: 8 11: 16
5:0	R	0x0	DMA_SRC_DRQ_TYPE. DMA Source DRQ Type The details in DRQ Type and Port Corresponding Relation.

3.10.6.12. DMA Channel Current Source Address Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0010(N=0~15)			Register Name: DMA_CUR_SRC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_CUR_SRC. DMA Channel Current Source Address, read only.

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3.10.6.13. DMA Chacnnel Current Destination Address Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0014(N=0~15)			Register Name: DMA_CUR_DEST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_CUR_DEST. DMA Channel Current Destination Address, read only.

3.10.6.14. DMA Channel Byte Counter Left Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0018(N=0~15)			Register Name: DMA_BCNT_LEFT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24:0	R	0x0	DMA_BCNT_LEFT. DMA Channel Byte Counter Left, read only.

3.10.6.15. DMA Channel Parameter Register (Default Value: 0x0000_0000)

Offset:0x100+N*0x40+0x1C(N=0~15)			Register Name: DMA_PARA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	WAIT_CYC. Wait Clock Cycles

3.10.6.16. DMA Mode Register (Default Value: 0x0000_0000)

Offset: 0x100+N*0x40+0x28(N=0~15)			Register Name: DMA_MODE_REG
Bit	**R/W**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	DMA_DST_MODE. 0: Wait mode. 1: Handshake mode.
2	R/W	0x0	DMA_SRC_MODE. 0: Wait mode. 1: Handshake mode.
1:0	/	/	/

3.10.6.17. DMA Former Descriptor Address Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x002C(N=0~15)			Register Name: DMA_FDESC_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_FDESC_ADDR.

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			This register is used to storing the former value of DMA Channel Descriptor Address Register.

3.10.6.18. DMA Package Number Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0030(N=0~15)			Register Name: DMA_PKG_NUM_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_PKG_NUM. This register will record the number of packages which has been completed in one transmission.

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3.11. GIC

3.11.1. Interrupt Source

Interrupt Number	Interrupt Source	Interrupt Vector	Description
0	SGI 0	0x0000	SGI 0 interrupt
1	SGI 1	0x0004	SGI 1 interrupt
2	SGI 2	0x0008	SGI 2 interrupt
3	SGI 3	0x000C	SGI 3 interrupt
4	SGI 4	0x0010	SGI 4 interrupt
5	SGI 5	0x0014	SGI 5 interrupt
6	SGI 6	0x0018	SGI 6 interrupt
7	SGI 7	0x001C	SGI 7 interrupt
8	SGI 8	0x0020	SGI 8 interrupt
9	SGI 9	0x0024	SGI 9 interrupt
10	SGI 10	0x0028	SGI 10 interrupt
11	SGI 11	0x002C	SGI 11 interrupt
12	SGI 12	0x0030	SGI 12 interrupt
13	SGI 13	0x0034	SGI 13 interrupt
14	SGI 14	0x0038	SGI 14 interrupt
15	SGI 15	0x003C	SGI 15 interrupt
16	PPI 0	0x0040	PPI 0 interrupt
17	PPI 1	0x0044	PPI 1 interrupt
18	PPI 2	0x0048	PPI 2 interrupt
19	PPI 3	0x004C	PPI 3 interrupt
20	PPI 4	0x0050	PPI 4 interrupt
21	PPI 5	0x0054	PPI 5 interrupt
22	PPI 6	0x0058	PPI 6 interrupt
23	PPI 7	0x005C	PPI 7 interrupt
24	PPI 8	0x0060	PPI 8 interrupt
25	PPI 9	0x0064	PPI 9 interrupt
26	PPI 10	0x0068	PPI 10 interrupt
27	PPI 11	0x006C	PPI 11 interrupt
28	PPI 12	0x0070	PPI 12 interrupt
29	PPI 13	0x0074	PPI 13 interrupt
30	PPI 14	0x0078	PPI 14 interrupt
31	PPI 15	0x007C	PPI 15 interrupt
32	UART0		UART0 interrupt
33	UART1		UART1 interrupt
34	UART2		UART2 interrupt
35	UART3		UART3 interrupt

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
36	TWI0		TWI0 interrupt
37	TWI1		TWI1 interrupt
38	TWI2		TWI2 interrupt
39	TWI3		TWI3 interrupt
40	SCR0		SCR0 interrupt
41	SCR1		SCR1 interrupt
42	SPI0		SPI0 interrupt
43	SPI1		SPI1 interrupt
44	GMAC0		EMAC0 interrupt
45			
46	TS0		TS0 interrupt
47	THS		THS interrupt
48			
49	CIR_TX		CIR_TX interrupt
50	I2S/PCM0		I2S/PCM0 interrupt
51	I2S/PCM1		I2S/PCM1 interrupt
52	I2S/PCM2		I2S/PCM2 interrupt
53	OWA		OWA interrupt
54	DMIC		DMIC interrupt
55	USB2.0_DRD_DEVICE		USB2.0_DRD_DEVICE interrupt
56	USB2.0_DRD_EHCI		USB2.0_DRD_EHCI interrupt
57	USB2.0_DRD_OHCI		USB2.0_DRD_OHCI interrupt
58	USB3.0_HOST		USB3.0_HOST interrupt
59			
60	USB2.0_HOST3_EHCI		USB2.0_HOST3_EHCI interrupt
61	USB2.0_HOST3_OHCI		USB2.0_HOST3_OHCI interrupt
62	I2S/PCM3		I2S/PCM3 interrupt
63	Audio_HUB		Audio_HUB interrupt
64			
65	DRAM		DRAM interrupt
66	NAND0		NAND0 interrupt
67	SMHC0		SMHC0 interrupt
68	SMHC1		SMHC1 interrupt
69	SMHC2		SMHC2 interrupt
75	DMA		DMA interrupt
76	MBOX		MessageBox interrupt
77	SPINLOCK		SPINLOCK interrupt
78	HSTIMER0		HSTIMER0 interrupt
79			
80	cTIMER0		TIMER0 interrupt
81	TIMER1		TIMER1 interrupt
82	WDOG		WDOG interrupt
83	GPIOB		GPIOB interrupt

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
84			
85	GPIOF		GPIOF interrupt
86	GPIOG		GPIOG interrupt
87	CLK_DET		Clock Detect interrupt
88	BUS_TIMEOUT		Bus Timeout interrupt
89	IOMMU		IOMMU interrupt
90	PSI		PSI interrupt
91	GPIOH		GPIOH
96	HDMI_TX0(1.4⁄2.0)		HDMI_TX0(1.4⁄2.0) interrupt
97	TCON_LCD0		TCON_LCD0 interrupt
98	TCON_TV0		TCON_TV0 interrupt
99	CSI0_DMA0		CSI0_DMA0 interrupt
100	CSI0_DMA1		CSI0_DMA1 interrupt
101			
102	CSI0_PARSER0		CSI0_PARSER0 interrupt
103			
104	CSI0_CCI0		CSI0_CCI0 interrupt
105			
106			
107			
110	DE		DE interrupt
111	DI0		DE-interlace0 interrupt
112			
113			
114			
115	IRQGPU		GPU interrupt request
116	IRQJOB		Job interrupt request
117	IRQMMU		MMU interrupt request
118			
119	CE_NS		CE_NS interrupt
120	CE_S		CE_S interrupt
121	VE		VE interrupt
122	VP9		VP9 interrupt
123	PCIE_HP_MSI		PCIE_HP_MSI interrupt
124	PCIE_HP_PME		PCIE_HP_PME interrupt
125	PCIE_RID_DI		PCIE_RID_DI interrupt
126	PCIE_RIC_DI		PCIE_RIC_DI interrupt
127	PCIE_RIB_DI		PCIE_RIB_DI interrupt
128	External NMI		External NMI interrupt
129	R_TIMER0		R_TIMER0 interrupt
130	R_TIMER1		R_TIMER1 interrupt
131	R_TIMER2		R_TIMER2 interrupt
132	R_TIMER3		R_TIMER3 interrupt

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
133	R_Alarm0		R_Alarm0 interrupt
134	R_Alarm1		R_Alarm1 interrupt
135	R_WDOG		R_WDOG interrupt
136	R_TWDOG		TWDOG interrupt
137	R_GPIOL		R_GPIOL interrupt
138	R_UART0		R_UART0 interrupt
139	R_TWI0		R_TWI0 interrupt
141	R_CIR_RX		R_CIR_RX interrupt
142	R_OWC		R_OWC interrupt
143	R_GPIOM		R_GPIOM interrupt
144	CPUIDLE		CPUIDLE interrupt
145	PCIE_RIA_DI		PCIE_RIA_DI interrupt
146	PCIE_RID_AI		PCIE_RID_AI interrupt
147	PCIE_RIC_AI		PCIE_RIC_AI interrupt
148	PCIE_RIB_AI		PCIE_RIB_AI interrupt
149	PCIE_RIA_AI		PCIE_RIA_AI interrupt
150	PCIE_PME_MSI		PCIE_PME_MSI interrupt
151	PCIE_AER_RC_ERR_MSI		PCIE_AER_RC_ERR_MSI interrupt
152	PCIE_AER_RC_ERR		PCIE_AER_RC_ERR interrupt
153	PCIE_PME		PCIE_PME interrupt
154	PCIE_HP		PCIE_HP interrupt
155	PCIE_LINK_AUTO_BW		PCIE_LINK_AUTO_BW interrupt
156	PCIE_BW_MGT		PCIE_BW_MGT interrupt
157	PCIE_EDMA		PCIE_EDMA interrupt
158	PCIE_LINK_UP		PCIE_LINK_UP interrupt
159	PCIE_MSI_CTRL		PCIE_MSI_CTRL interrupt
160	C0_CTI0		C0_CTI0 interrupt
161	C0_CTI1		C0_CTI1 interrupt
162	C0_CTI2		C0_CTI2 interrupt
163	C0_CTI3		C0_CTI3 interrupt
164	C0_COMMTX0		C0_COMMTX0 interrupt
165	C0_COMMTX1		C0_COMMTX1 interrupt
166	C0_COMMTX2		C0_COMMTX2 interrupt
167	C0_COMMTX3		C0_COMMTX3 interrupt
168	C0_COMMRX0		C0_COMMRX0 interrupt
169	C0_COMMRX1		C0_COMMRX1 interrupt
170	C0_COMMRX2		C0_COMMRX2 interrupt
171	C0_COMMRX3		C0_COMMRX3 interrupt
172	C0_PMU0		C0_PMU0 interrupt
173	C0_PMU1		C0_PMU1 interrupt
174	C0_PMU2		C0_PMU2 interrupt
175	C0_PMU3		C0_PMU3 interrupt
176	C0_INT_ERROR		C0_INT_ERROR interrupt

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
177	C0_AXI_WR		C0_AXI_WR interrupt
178	C0_AXI_RD		C0_AXI_RD interrupt

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3.12. Message Box

3.12.1. Overview

Message Box(MSGBOX) provides interrupt communication mechanism for on-chip processor. The module has the following features:

- The communication parties transmit information through channel
- FIFO depth is 4 x 32 bits
- The communication parties are CPUS and CPUX
- Interrupt alarm function

3.12.2. Block Diagram

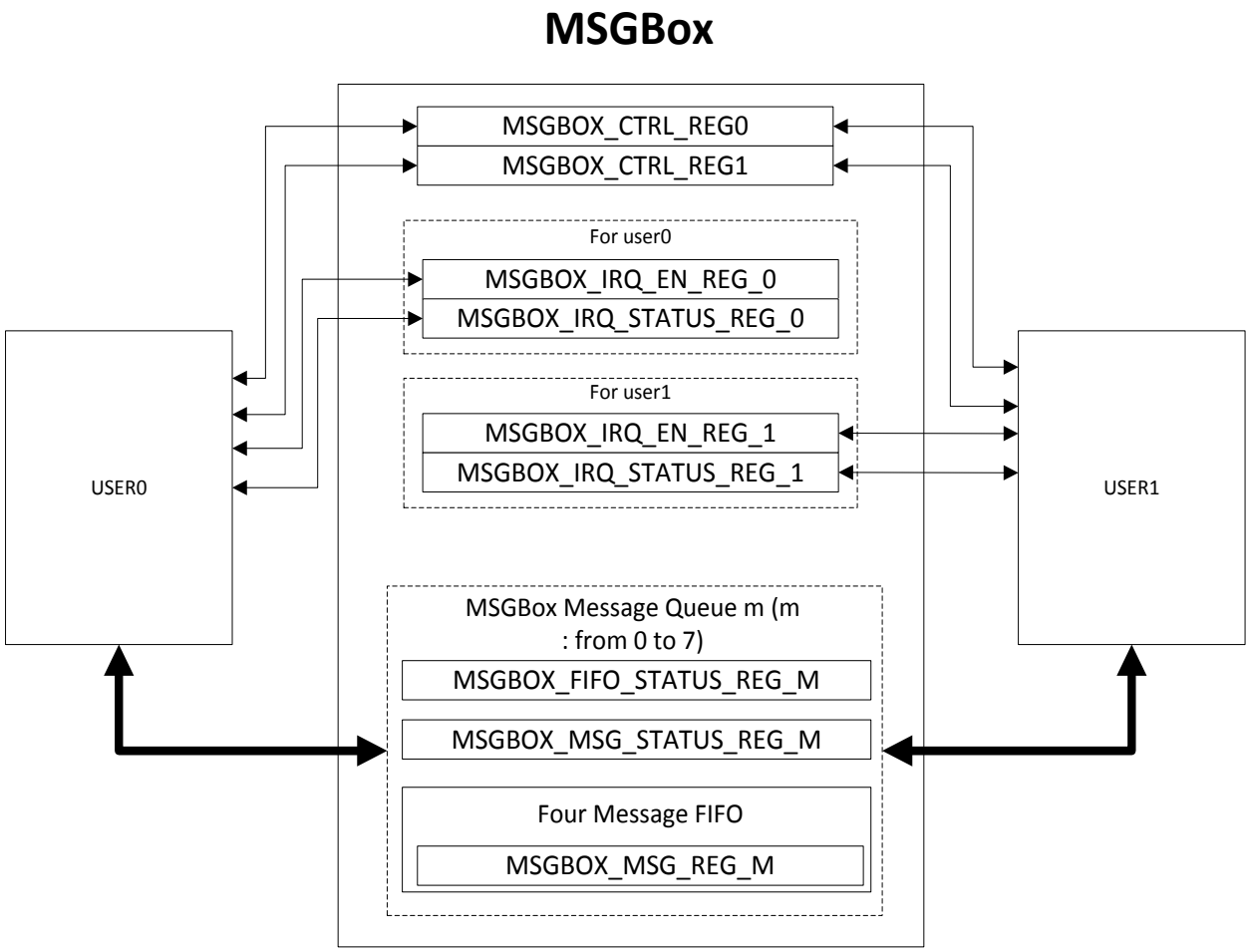


Figure 3-38. Message Box Block Diagram

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3.12.3. Operations and Functional Descriptions

3.12.3.1. Clock and Reset

MSGBOX is on AHB1 bus. To access MSGBOX, perform the following steps about AHB1 bus:

Step1: De-assert MSGBOX reset signal.

Step2: Open MSGBOX gating signal.

3.12.3.2. Typical Application

Two different CPU can build communication by configuring MSGBOX. The communication parties have 8 bidirectional channels. If a party is receiver, then another is transmitter. During communication process, the current status can be judged through interrupt or FIFO status.

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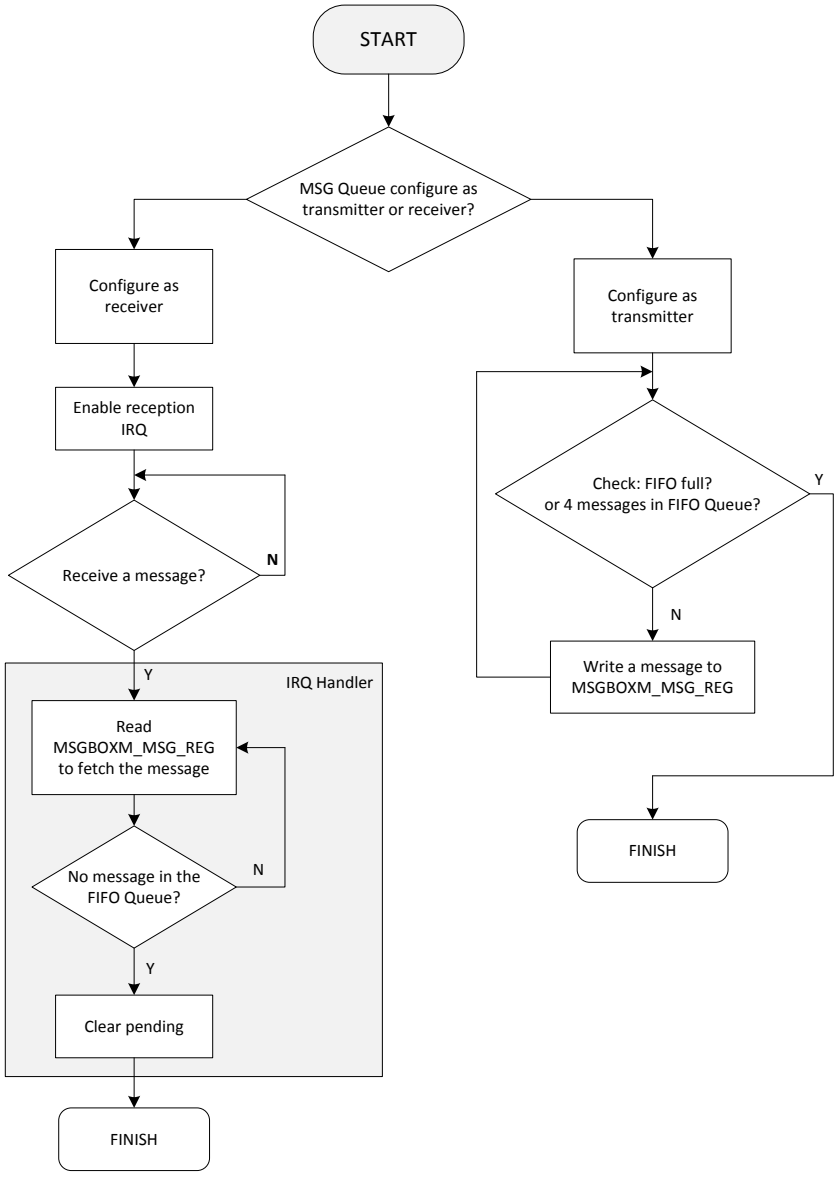


Figure 3-39. Message Box Typical Application Chart

3.12.3.3. Function Implemention

3.12.3.3.1. Transmitter and Receiver Mode

User0 and User1 can be configured as transmitter or receiver, but User0 and User1 cannot configure as same mode in the same channel, that is, User0 is transmitter, User1 must be receiver; User0 is receiver, User1 must be transmitter.

3.12.3.3.2. Interrupt

Interrupt has two types:

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- As receiver, when received new information, the interrupt signal can generate.
- As transmitter, when channel FIFO is not full, the interrupt signal can generate.

Eight channels can configure the interrupt enable bit individually, but interrupt controller only has a MSGBOX interrupt number.

3.12.3.3.3. FIFO Status

- When channel FIFO is not full, the value of FIFO_FULL_FLAG is 0, at this time ,FIFO can execute write operation.
- When channel FIFO is full, the value of FIFO_FULL_FLAG is 1, at this time, if writing data again to FIFO, the first data in FIFO can be overrided.
- FIFO status can be read by MSGBOXM_MSG_STATUS_REG.

3.12.3.3.4. Debug Mode

- In debug mode, User0 can transmit data to User0, User1 can transmit data to User1.
- In debug mode, FIFO function will close.

3.12.3.4. Operating Mode

3.12.3.4.1. Transfer Mode Configuration

- Queue n (n=0~3)transmitter mode: Write 1 to the bit[8*n+4] of MSGBOX_CTRL_REG0.
- Queue m (m=4~7)transmitter mode : Write 1 to the bit[8*(m-4)+4] of MSGBOX_CTRL_REG1.
- Queue n (n=0~3) receiver mode: Write 1 to the bit[8*n] of MSGBOX_CTRL_REG0.
- Queue m (m=4~7) receiver mode : Write 1 to the bit[8*(m-4)] of MSGBOX_CTRL_REG1.

3.12.3.4.2. Interrupt Check Transfer Status

(1) Configure transmitter and receiver mode through **3.12.3.4.1. Transfer Mode Configuration**.
(2) Interrupt enable bit: Configure the interrupt enable bit of transmitter/receiver through MSGBOX_IRQ_EN_REG.
(3) When FIFO is not full, an interrupt pending generates to remind the transmitter to transmit data, at this time, to write data to FIFO in interrupt handler ,and clear the pending bit and the enable bit of *Transmitter IRQ*.
(4) When FIFO has new data, an interrupt pending generates to remind the receiver to receive data, at this time, to read data from FIFO in interrupt handler, and clear the pending bit and the enable bit of *Receiver IRQ*.

3.12.3.4.3. FIFO Check Transfer Status

(1) Configure transmitter and receiver mode through **3.12.3.4.1. Transfer Mode Configuration**.

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(2) When FIFO is not full, the transmitter fills FIFO to 4*32 bits.
(3) When the receiver considers FIFO is full, then the receiver reads FIFO data, and reads **MSGBOXM_MSG_STATUS_REG** to require the current FIFO number.

3.12.3.4.4. Debug

To use MSGBOX in debug mode, performs the following steps:
(1) Write 1 to the bit0 of **MSGBOX_DEBUG_REG**.
(2) The control bit of the corresponding channel is set to 1.

3.12.4. Register List

Module Name	Base Address
MSGBOX	0x0300 3000

Register Name	Offset	Description
MSGBOX_CTRL_REG0	0x0000	Message Queue Attribute Control Register 0
MSGBOX_CTRL_REG1	0x0004	Message Queue Attribute Control Register 1
MSGBOXU_IRQ_EN_REG	0x0040+n*0x20	IRQ Enable for User n (n=0,1)
MSGBOXU_IRQ_STATUS_REG	0x0050+n*0x20	IRQ Status for User n (n=0,1)
MSGBOXM_FIFO_STATUS_REG	0x0100+N*0x4	FIFO Status for Message Queue N(N = 0~7)
MSGBOXM_MSG_STATUS_REG	0x0140+N*0x4	Message Status for Message Queue N(N=0~7)
MSGBOXM_MSG_REG	0x0180+N*0x4	Message Register for Message Queue N(N=0~7)
MSGBOX_DEBUG_REG	0x01C0	MSGBOX Debug Register

3.12.5. Register Description

3.12.5.1. MSGBox Control Register 0(Default Value: 0x1010_1010)

Offset: 0x0000			Register Name: MSGBOX_CTRL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x1	TRANSMIT_MQ3. Message Queue 3 is a Transmitter of user u. 0: user0 1: user1
27:25	/	/	/
24	R/W	0x0	RECEPTION_MQ3. Message Queue 3 is a Receiver of user u. 0: user0

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			1: user1
23:21	/	/	/
20	R/W	0x1	TRANSMIT_MQ2. Message Queue 2 is a Transmitter of user u. 0: user0 1: user1
19:17	/	/	/
16	R/W	0x0	RECEPTION_MQ2. Message Queue 2 is a Receiver of user u. 0: user0 1: user1
15:13	/	/	/
12	R/W	0x1	TRANSMIT_MQ1 Message Queue 1 is a Transmitter of user u. 0: user0 1: user1
11:9	/	/	/
8	R/W	0x0	RECEPTION_MQ1. Message Queue 1 is a Receiver of user u. 0: user0 1: user1
7:5	/	/	/
4	R/W	0x1	TRANSMIT_MQ0. Message Queue 0 is a Transmitter of user u. 0: user0 1: user1
3:1	/	/	/
0	R/W	0x0	RECEPTION_MQ0. Message Queue 0 is a Receiver of user u. 0: user0 1: user1

3.12.5.2. MSGBox Control Register 1(Default Value: 0x1010_1010)

Offset: 0x0004			**Register Name: MSGBOX_CTRL_REG1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x1	TRANSMIT_MQ7. Message Queue 7 is a Transmitter of user u. 0: user0 1: user1
27:25	/	/	/
24	R/W	0x0	RECEPTION_MQ7. Message Queue 7 is a Receiver of user u.

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			0: user0 1: user1
23:21	/	/	/
20	R/W	0x1	TRANSMIT_MQ6. Message Queue 6 is a Transmitter of user u. 0: user0 1: user1
19:17	/	/	/
16	R/W	0x0	RECEPTION_MQ6. Message Queue 6 is a Receiver of user u. 0: user0 1: user1
15:13	/	/	/
12	R/W	0x1	TRANSMIT_MQ5 Message Queue 5 is a Transmitter of user u. 0: user0 1: user1
11:9	/	/	/
8	R/W	0x0	RECEPTION_MQ5. Message Queue 5 is a Receiver of user u. 0: user0 1: user1
7:5	/	/	/
4	R/W	0x1	TRANSMIT_MQ4. Message Queue 4 is a Transmitter of user u. 0: user0 1: user1
3:1	/	/	/
0	R/W	0x0	RECEPTION_MQ4. Message Queue 4 is a Receiver of user u. 0: user0 1: user1

3.12.5.3. MSGBox IRQ Enable Register u(u=0,1)(Default Value: 0x0000_0000)

Offset:0x0040+N*0x20(N=0,1)			Register Name: MSGBOX_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	TRANSMIT_MQ7_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 7 is not full.)
14	R/W	0x0	RECEPTION_MQ7_IRQ_EN. 0: Disable

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			1: Enable (It will notify user u by interrupt when Message Queue 7 has received a new message.)
13	R/W	0x0	TRANSMIT_MQ6_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 6 is not full.)
12	R/W	0x0	RECEPTION_MQ6_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 6 has received a new message.)
11	R/W	0x0	TRANSMIT_MQ5_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 5 is not full.)
10	R/W	0x0	RECEPTION_MQ5_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 5 has received a new message.)
9	R/W	0x0	TRANSMIT_MQ4_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 4 is not full.)
8	R/W	0x0	RECEPTION_MQ4_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 4 has received a new message.)
7	R/W	0x0	TRANSMIT_MQ3_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 3 is not full.)
6	R/W	0x0	RECEPTION_MQ3_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 3 has received a new message.)
5	R/W	0x0	TRANSMIT_MQ2_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 2 is not full.)
4	R/W	0x0	RECEPTION_MQ2_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 2 has received a new message.)
3	R/W	0x0	TRANSMIT_MQ1_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 1 is not

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			full.)
2	R/W	0x0	RECEPTION_MQ1_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 1 has received a new message.)
1	R/W	0x0	TRANSMIT_MQ0_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 0 is not full.)
0	R/W	0x0	RECEPTION_MQ0_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 0 has received a new message.)

3.12.5.4. MSGBox IRQ Status Register u(Default Value: 0x0000_AAAA)

Offset:0x0050+N*0x20(N=0,1)			Register Name: MSGBOXU_IRQ_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x1	TRANSMIT_MQ7_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 7 is not full. Setting one to this bit will clear it.
14	R/W	0x0	RECEPTION_MQ7_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 7 has received a new message. Setting one to this bit will clear it.
13	R/W	0x1	TRANSMIT_MQ6_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 6 is not full. Setting one to this bit will clear it.
12	R/W	0x0	RECEPTION_MQ6_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 6 has received a new message. Setting one to this bit will clear it.
11	R/W	0x1	TRANSMIT_MQ5_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 5 is not full. Setting one to this bit will clear it.
10	R/W	0x0	RECEPTION_MQ5_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 5 has received a new message. Setting one to this bit will clear it.
9	R/W	0x1	TRANSMIT_MQ4_IRQ_PEND.

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			0: No effect 1: Pending. This bit will be pending for user u when Message Queue 4 is not full. Set one to this bit will clear it.
8	R/W	0x0	RECEPTION_MQ4_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 4 has received a new message. Setting one to this bit will clear it.
7	R/W	0x1	TRANSMIT_MQ3_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 3 is not full. Setting one to this bit will clear it.
6	R/W	0x0	RECEPTION_MQ3_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 3 has received a new message. Setting one to this bit will clear it.
5	R/W	0x1	TRANSMIT_MQ2_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 2 is not full. Setting one to this bit will clear it.
4	R/W	0x0	RECEPTION_MQ2_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 2 has received a new message. Setting one to this bit will clear it.
3	R/W	0x1	TRANSMIT_MQ1_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 1 is not full. Setting one to this bit will clear it.
2	R/W	0x0	RECEPTION_MQ1_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 1 has received a new message. Setting one to this bit will clear it.
1	R/W	01	TRANSMIT_MQ0_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 0 is not full. Setting one to this bit will clear it.
0	R/W	0x0	RECEPTION_MQ0_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 0 has received a new message. Setting one to this bit will clear it.

3.12.5.5. MSGBox FIFO Status Register m(Default Value: 0x0000_0000)

Offset:0x0100+N*0x4 (N=0~7)			Register Name: MSGBOXM_FIFO_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:1	/	/	/
0	R	0x0	FIFO_FULL_FLAG. 0: The Message FIFO queue is not full (space is available) 1: The Message FIFO queue is full. This FIFO status register has the status related to the message queue.

3.12.5.6. MSGBox Message Status Register m(Default Value: 0x0000_0000)

Offset:0x0140+N*0x4 (N=0~7)			Register Name: MSGBOXM_MSG_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R	0x0	MSG_NUM. Number of unread messages in the message queue. Here, limited to four messages per message queue. 000: There is no message in the message FIFO queue. 001: There is 1 message in the message FIFO queue. 010: There are 2 messages in the message FIFO queue. 011: There are 3 messages in the message FIFO queue. 100: There are 4 messages in the message FIFO queue. 101~111:/

3.12.5.7. MSGBox Message Queue Register m(Default Value : 0x0000_0000)

Offset:0x0180+N*0x4 (N=0~7)			Register Name: MSGBOXM_MSG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	The message register stores the next to be read message of the message FIFO queue. Reads remove the message from the FIFO queue.

3.12.5.8. MSGBox Debug Register(Default Value: 0x0000_0000)

Offset: 0x01C0			Register Name: MSGBOX_DEBUG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0x0	FIFO_CTRL. MQ[7:0] Control. In the debug mode, the corresponding FIFO channel will disable and only one register space valid for a message exchange. 0: Normal Mode. 1: Disable the corresponding FIFO (Clear FIFO).
7:1	/	/	/
0	R/W	0x0	DEBUG_MODE. In the Debug Mode, each user can transmit messages to itself through each Message Queue.

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			0: Normal Mode 1: Debug Mode.

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3.13. Spinlock

3.13.1. Overview

In multi-core system,the Spinlock offers hardware synchronization mechanism, lock operation can prevent multi processors from handling data-sharing at the same time, and ensure coherence of data. The Spinlock has the following features:

- Spinlock module includes 32 lock units
- Two kinds of lock status: locked and unlocked
- Lock time of the processor is predictable(less than 200 cycles)

3.13.2. Block Diagram

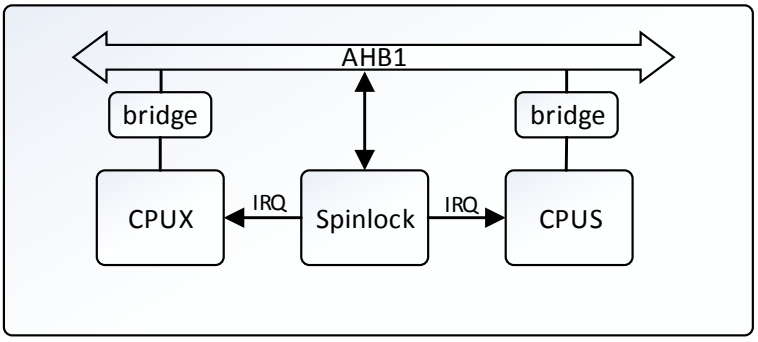


Figure 3-40. Spinlock Block Diagram

3.13.3. Operations and Functional Descriptions

3.13.3.1. Clock and Reset

The Spinlock is hung on AHB1. Before accessing Spinlock register, open the corresponding gating bit on AHB1 and de-assert reset signal. The correct operation order is to de-assert reset signal at first, and then open the corresponding gating signal.

3.13.3.2. Typical Application

A processor lock spinlock0, when the status is locked, the processor executes specific code, and then unlocks code.

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Other processors is released to start reading/writing operation.

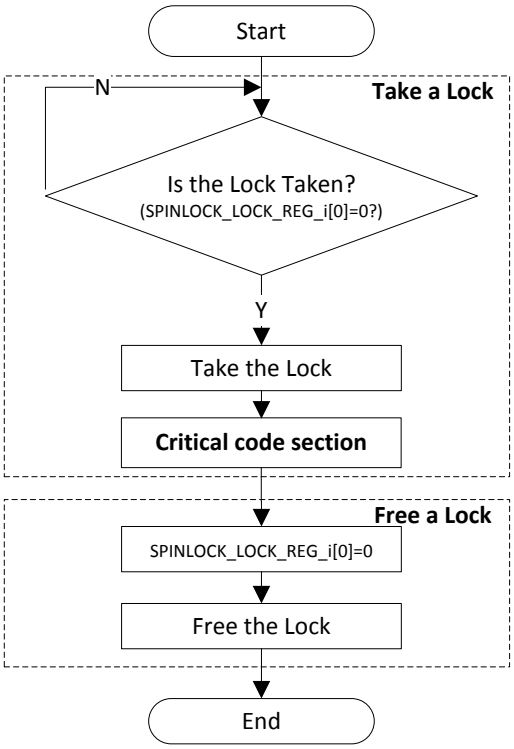


Figure 3-41. Spinlock Typical Application Diagram

3.13.3.3. Function Implemention

3.13.3.3.1. Spinlock State Machine

When a processor uses spinlock, it needs to acquire spinlock's status through *SPINLOCK_STATUS_REG*.

Reading Operation: when return to 0, spinlock comes into locked status; when read this status bit again, return to 1, spinlock comes into locked status.

Writing Operating: when the Spinlock is in locked status, the Spinlock can convert to unlocked status through writing 0. After reset, the Spinlock is in unlocked status by default.

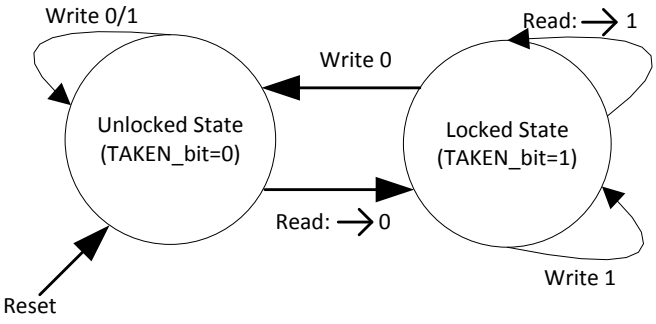


Figure 3-42. Spinlock State Machine

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3.13.3.3.2. Interrupt

When **Free Lock** is released(lock status is changed from locked to unlocked), interrupt is generated.

3.13.3.4. Operating Mode

3.13.3.4.1. Switch Status

(1) When the readed value from **SPINLOCKN_LOCK_REG** is 0,the Spinlock come into locked status.
(2) Execute application code, the status of **SPINLOCKN_STATUS_REG** is 1.
(3) Write 0 to **SPINLOCKN_LOCK_REG**, the Spinlock comes into unlocked status, corresponding spinlock is released.

3.13.4. Programming Guidelines

Take CPU0's synchronization with CPUS with Spinlock0 for an example, CPU0 takes the spinlock0 firstly in the instance.
CPU0 of Cluster0:

Step 1: CPU0 initializes Spinlock

```
put_wvalue(CCMU_SPINLOCK_BGR_REG,0x00010000);

put_wvalue(CCMU_SPINLOCK_BGR_REG,0x00010001);
```

Step 2: CPU0 requests to take spinlock0

```
rdata=readl(SPINLOCK_STATUS_REG0);                    //check lock register0 status, if it is taken, check
till

if(rdata != 0)    writel (0, SPINLOCK_LOCK_REG0);          //CPU0 frees spinlock0

rdata=readl(SPINLOCK_LOCK_REG0);                      //request to take spinlock0, if fail, retry till

if(rdata != 0)    rdata=readl(SPINLOCK_LOCK_REG0);        // lock register0 is taken
```

---------- CPU0 critical code section ----------

Step 3: CPU0 free spinlock0

```
writel (0, SPINLOCK_LOCK_REG0);                       //CPU0 frees spinlock0
```

Step 4: CPU0 waits for CPUS' freeing spinlock0

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writel (readl(SPINLOCK_STATUS_REG0) == 1); // CPU0 waits for CPUS' freeing spinlock0

CPUS:

Step 1: CPU0 has taken spinlock0, CPUS waits for CPU0' freeing spinlock0

while(readl(SPINLOCK_STATUS_REG0) == 1); // CPUS waits for CPU0' freeing spinlock0

Step 2: CPUS takes spinlock0 and go on

rdata=readl(SPINLOCK_LOCK_REG0); //request to take spinlock0, if fail, retry till

if(rdata != 0) rdata=readl(SPINLOCK_LOCK_REG0); // lock register0 is taken

---------- CPUS critical code section ----------

Step 3: CPUS frees spinlock0

writel (0, SPINLOCK_LOCK_REG0); //CPUS frees spinlock0

3.13.5. Register List

Module Name	Base Address
Spinlock	0x0300 4000

Register Name	Offset	Description
SPINLOCK_SYSTATUS_REG	0x0000	Spinlock System Status Register
SPINLOCK_STATUS_REG	0x0010	Spinlock Status Register
SPINLOCK_LOCK_REGN	0x0100+N*0x04	Spinlock Register N (N=0~31)

3.13.6. Register Description

3.13.6.1. Spinlock System Status Register (Default Value: 0x1000_0000)

Offset: 0x0000			Register Name: SPINLOCK_SYSTATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R	0x1	LOCKS_NUM. Number of lock registers implemented. 00: This instance has 32 lock registers. 01: This instance has 64 lock registers. 10: This instance has 128 lock registers. 11: This instance has 256 lock registers.

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27:16	/	/	/
15:9	/	/	/
8	R	0x0	IU0. In-Use flag0, covering lock register0-31. 0: All lock register 0-31 are in the NotTaken state. 1: At least one of the lock register 0-31 is in the Taken state.
7:0	/	/	/

3.13.6.2. Spinlock Register Status(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SPINLOCK_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[i] (i=0~31)	R	0x0	LOCK_REG_STATUS. SpinLock[i] status (i=0~31) 0: The Spinlock is free 1: The Spinlock is taken.

3.13.6.3. Spinlock Register N (N=0 to 31)(Default Value: 0x0000_0000)

Offset:0x0100+N*0x04 (N=0~31)			Register Name: SPINLOCKN_LOCK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	TAKEN. Lock State. Read 0x0: The lock was previously Not Taken (free).The requester is granted the lock. Write 0x0: Set the lock to Not Taken (free). Read 0x1: The lock was previously Taken. The requester is not granted the lock and must retry. Write 0x1: No update to the lock value.

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3.14. Crypto Engine

3.14.1. Overview

The Crypto Engine(CE) module is one encryption/decryption algorithms accelerator. It supports kinds of symmetric, asymmetric, HASH, and RNG algorithms. There are two software interfaces for secure and non-secure world each. Algorithm control information is written in memory by task descriptor, then CE automatically reads it when executing request. It supports parallel requests from 4 channels each world, and has an internal DMA controller to transfer data between CE and memory. It supports parallel running for symmetric, HASH, asymmetric algorithms.

Features:

- Supports Symmetrical Algorithm: AES, DES, 3DES, XTS
- Supports Hash Algorithm: MD5, SHA, HMAC
- Supports Public Key Algorithm: RSA, ECC
- Supports RNG Algorithm: PRNG, TRNG
- Supports 128-bit, 192-bit and 256-bit key size for AES
- Supports 256-bit, 512-bit key for XTS
- AES supports ECB, CBC, CTR, CTS, CFB, OFB, CBC-MAC modes
- AES-CFB mode support CFB1, CFB8, CFB64, CFB128
- AES-CTR supports CTR16, CTR32, CTR64, CTR128
- DES supports ECB, CBC, CTR, CBC-MAC mode
- DES-CTR supports CTR16, CTR32, CTR64 mode
- Supports SHA1, SHA224, SHA256, SHA384, SHA512 for SHA. Support HMAC-SHA1, HMAC-SHA256 for HMAC. Supports multi-package mode for Hash algorithm
- MD5, SHA, HMAC are padded using hardware, if not last package, input should aligned with computation block, namely 512 bits or 1024 bits
- RSA supports 512/1024/2048/3072/4096 bits width
- ECC supports 160/224/256/384/521 bits width
- Supports 160-bits hardware PRNG with 175 bits seed. Output aligns with 5 words
- Supports 256-bits hardware TRNG. Output aligns with 8 words
- Supports secure and non-secure interfaces respectively, each world issues task request through its own interface
- Each world has 4 channels for software request, each channel has an interrupt control and status bit, and channels are independent with each other
- Supports task chain mode for each request. Task or task chain are executed at request order
- Symmetric, asymmetric, HASH ctrl logics are separate, but them can handle task simultaneously. Symmetric logic can select instantiate 2 suits at implementation time
- 8 scatter group(sg) are supported for both input and output data. sg size is input/output word number. DMA reads and write at word aligned
- DMA has multiple channel, each corresponding to one suit of algorithms

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3.14.2. Block Diagram

The following figure shows the block diagram of Crypto Engine.

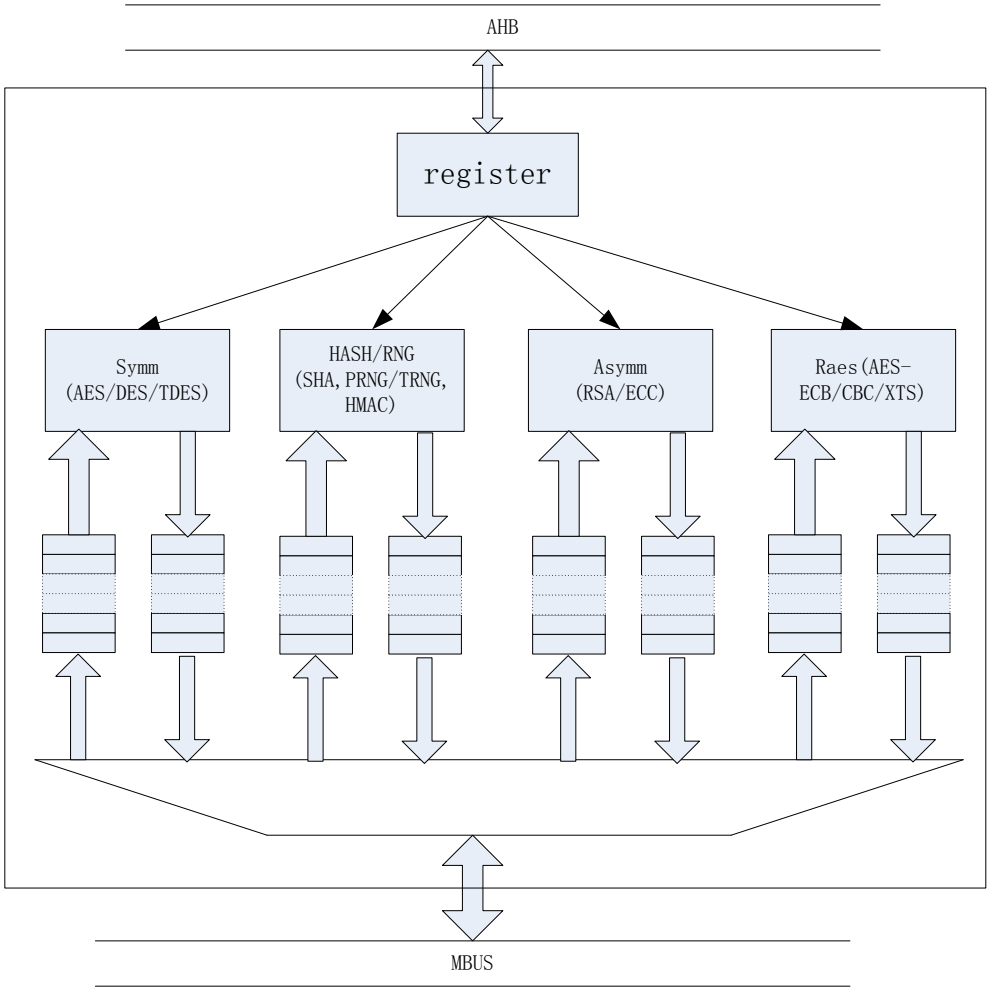


Figure 3-43. CE Block Diagram

3.14.3. Operations and Functional Descriptions

3.14.3.1. Crypto Engine Task Descriptor

Software make request through task descriptor, providing algorithm type, mode, key address, source/destination address and size, etc. The task descriptor is as follows.

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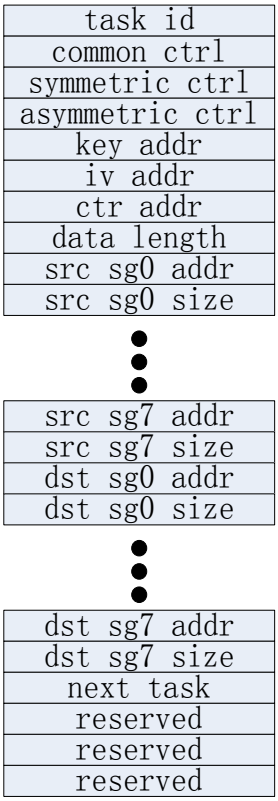


Figure 3-44. Crypto Engine Task Chaining

Task chaining id supports 0~3.

3.14.3.2. Task_descriptor_queue Common Control

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	Interrupt enable for current task 0: disable interrupt 1: enable interrupt
30:25	/	/	/
24:17	R/W	0x0	CBC_MAC_LEN The outcome bit length of CBC-MAC when in CBC-MAC mode.
16	R/W	0x0	IV Mode IV mode for SHA-1/SHA-224/SHA-256/SHA384/SHA512/MD5 or constants 0: use initial constants defined in FIPS-180 1: use input iv
15	R/W	0x0	HASH/HMAC plaintext last 0: not the last HASH/HMAC plaintext package, need not padding 1: the last HASH/HMAC plaintext package, need to padding
14:9	/	/	/
8	R/W	0x0	OP DIR Algorithm Operation Direction 0: Encryption

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			1: Decryption
7	/	/	/
6:0	R/W	0x0	Algorithm type 0x0: AES 0x1: DES 0x2: Triple DES (3DES) 0x3~0xf: reserved 0x10: MD5 0x11: SHA-1 0x12: SHA-224 0x13: SHA-256 0x14: SHA-384 0x15: SHA-512 0x16: HMAC-SHA1 0x17: HMAC-SHA256 0x18~0x1b: reserved 0x1c: TRNG 0x1d: PRNG others: reserved 0x20: RSA 0x21: ECC others: reserved 0x30: RAES Others: reserved

3.14.3.3. Task_descriptor_queue Symmetric Control

Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26	R/W	0x0	NO_MODK 0: have module key derivation function 1: no module key derivation function
25:24	R/W	0x0	Key ladder stage 00: no key ladder 01: 3-stage key ladder 10: 5-stage key ladder 11: reserved
23:20	R/W	0x0	KEY Select key select for AES 0000: Select input CE_KEYx (Normal Mode) 0001: Select {SSK}

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			0010: Select {HUK} 0011: Select {RSSK}, used for decrypt HDCP key, EK, BSSK 0100: select SCK0 for key ladder0 0101: select SCK1 for key ladder1 0110-0111: Reserved 1000-1111: Select internal Key n (n from 0 to 7)
19:18	R/W	0x0	CFB_WIDTH For AES-CFB width 00: CFB1 01: CFB8 10: CFB64 11: CFB128
17	R/W	0x0	PRNG_LD load new 15bits key into lfsr for PRNG
16	R/W	0x0	AES CTS last package flag When set to '1', it means this is the last package for AES-CTS mode(the size of the last package >128bit).
15:14	/	/	/
13	R/W	0x0	XTS_LAST 0: not last block for XTS 1: last block for XTS
12	R/W	0x0	XTS_FIRST 0: not first block for XTS 1: first block for XTS
11:8	R/W	0x0	AES/DES/3DES/RAES modes. DES/3DES only supports ECB/CBC/CTR. RAES only supports ECB/CBC/XTS. operation mode for symmetric 0000: Electronic Code Book (ECB) mode 0001: Cipher Block Chaining (CBC) mode 0010: Counter (CTR) mode 0011: CipherText Stealing (CTS) mode 0100: Output feedback (OFB)mode 0101: Cipher feedback (CFB)mode 0110: CBC-MAC mode 1001: XTS mode Other: reserved
7:4	/	/	/
3:2	R/W	0x0	CTR Width Counter Width for CTR Mode 00: 16-bit Counter 01: 32-bit Counter 10: 64-bit Counter 11: 128-bit Counter
1:0	R/W	0x0	AES Key Size 00: 128-bit

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			01: 192-bit 10: 256-bit 11: Reserved

3.14.3.4. Task_descriptor_queue Asymmetric Control

Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x0	PKC algorithm mode. For modular computation: 00000: modular exponent(RSA) 00001: modular add 00010: modular minus 00011: modular multiplication others: reserved For ECC: 00000: point add 00001: point double 00010: point multiplication 00011: point verification 00100: encryption 00101: decryption 00110: sign 00111: sign verify others: reserved
15:8	/	/	/
7:0	R/W	0x0	Asymmetric algorithms operation width field. It indicates how much width this request apply, as words.

key addr field is address for each algorithm's key, and for the total length address of Hash when last package, also for extension feature micro codes address. When indicate HASH's total length address, it must be 64-bit data length with 64-bit address align.

iv addr field is address for IV or modulus, or tweak value address for XTS.

ctr addr is address for next block's IV, and for HMAC K1 address.

src/dst sgX addr field indicates 32-bit address for source and destination data.

src/dst sgX size field indicates size for each sg respectively.

next task field should be set to 0 when no next task, else set to next task's descriptor.

3.14.3.5. Task Request

Basically, there are 4 steps for one task handling from software.

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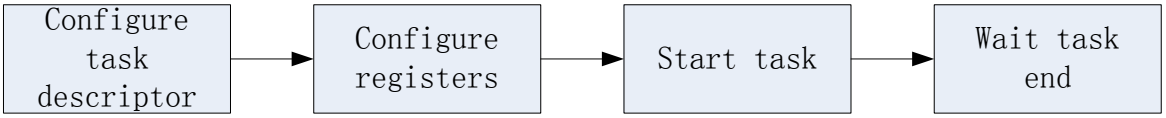


Figure 3-45. Task Request Process

Firstly, software should configure task descriptor in memory, including all fields in descriptor. Channel id corresponds to one channel in CE, from 0 to 3 for secure and non secure world respectively. According to algorithm type, software should set the fields in common control, symmetric control, asymmetric control, then provide key/iv/ctr address and the data length of this task. Source and destination sg address and size are set based on upper application. If there is another task concatenating after this task, then set its descriptor address at next descriptor field.

Secondly, software should set registers, including task descriptor address, interrupt control.

Thirdly, software read load register to ensure that the bit0 is zero, then starts request by pulled up the bit0 of the load register.

Lastly, wait interrupt status.

3.14.3.6. Security Operation

When CPU issues request to CE module, CE module will save the secure mode of CPU. When executing this request, this state bit works as access tag for inner and system resource. For HUK/RSSK/SSK from SID, only secure mode can access, or else these keys will be used as 0. For access to SID and keysram module through AHB bus, only secure mode can success, or else will read 0 or can not write. When issuing MBUS read and write requests, CE will use send this secure mode bit to BUS, so secure request can access secure and non secure space, but non secure request only can access non secure space.

3.14.3.7. Parallel Task

Algorithms are divided into 3 types: symmetric, HASH/RNG, asymmetric. Each type has a task queue with 8 elements for requests. Tasks in each queue are handled in sequence. Among these 3 types, task request and complete time are not sure. If one type uses the outcome of another type, software should make sure that start one type after another type is finished.

CE supports 4 channels in each world, and 3 suits algorithm type which can run in parallel. When software issues request, it first checks if load bit is low which means software can request. If load bit is high which means last request is not registered by CE, software should wait until load bit is low. If software makes several requests with the same type, these tasks will be executed in request sequence. If software makes several requests with different types, these tasks will be executed in parallel. Because parallel tasks would finish out of order, software should make different type request with different channel id, which results in generating different interrupt status bit.

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3.14.3.8. PKC Microcode

PKC module supports RSA, ECC asymmetric algorithms in the form of microcode. It implements basic modular add, minus, multiplication, point add, point double, and logic computing, etc. Complete RSA/ECC encryption, decryption, sign, verify are implemented with these microcode.

Asymmetric algorithms RSA/ECC are implemented as microcode in PKC module. Asymmetric encryption, decryption, signature and verification operations are composed with certain fixed microcode with hardware.

3.14.3.9. PKC Configuration

Before starting PKC, task description must be configured. Parameters to PKC are assigned to source sg, outcome is put to destination sg.

For RSA, parameters should be at the order of key, modulus, plaintext, for example key assigned to source sg 0, modulus assigned to source sg 1, plaintext assigned to source sg 2.

For ECC point add P2 = P0 + P1, parameters should be at the order of p, a, P0x, P0y, P1x, P1y. Output is at the order of P2x, P2y.

For ECC point double P2 = 2*P0, parameters should be at the order of p, a, P0x, P0y. Output is at the order of P2x, P2y.

For ECC point multiplication P2 = k*P0, parameters should be at the order of p, k, P0x, P0y. Output is at the order of P2x, P2y.

For ECC point verification, parameters should be at the order of p, a, P0x, P0y, b. Output is 1 or 0.

For ECC encryption, parameters should be at the order of random k, p, a, Gx, Gy, Qx, Qy, m. Output is at the order of Rx, Ry, c.

For ECC decryption, parameters should be at the order of random k, p, a, Rx, Ry, c. Output is m.

For ECC signature, parameters should be at the order of random k, p, a, Gx, Gy, n, d, e. Output is at the order of r, s.

For ECC signature verification, parameters should be at the order of n, s, e, r, p, a, Gx, Gy, Qx, Qy, n, r. Output is 1 or 0.

3.14.3.10. Error Check

CE module include error detection for task configuration, data computing error, and authentication invalid. When algorithm type in task description is read into module, CE will check if this type is supported through checking algorithm type field in common ctrl. If type value accede support scope, CE will issue interrupt signal and set error state. Each type has certain input and output data size. After getting task descriptor, input size and output size configuration will be checked to avoid size error. If size configuration is wrong, CE will issue interrupt signal and set error state. To protect keys would be put into keysram from disclose, if request using RSSK is for AES decryption and destination address is not in keysram space, CE would not execute this task. It will issue interrupt signal and set error state.

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3.14.3.11. Key Ladder

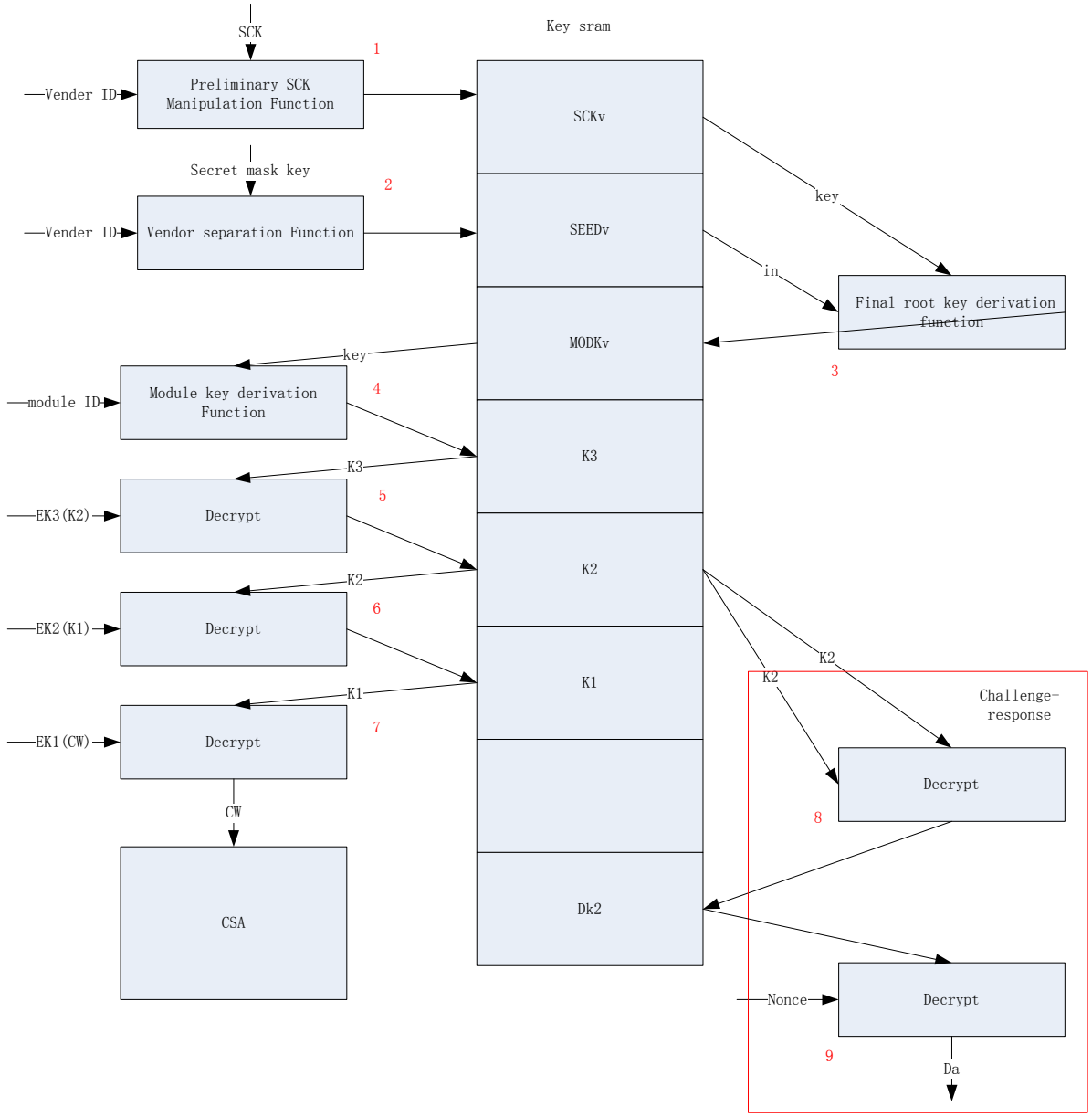


Figure 3-46 Key Ladder Task Chain

3.14.3.12. Clock Requirement

Clock Name	Description	Requirement
ahb_clk	AHB bus clock	24MHz – 200MHz
m_clk	MBUS clk	24MHz – 400MHz
ce_clk	CE work clock	24MHz – 300MHz

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3.14.4. Register List

Module Name	Base Address
CE_NS	0x01904000
CE_S	0x01904800

Register Name	Offset	Description
CE_TDA	0x0000	Task Descriptor Address
CE_ICR	0x0008	Interrupt Control Register
CE_ISR	0x000C	Interrupt Status Register
CE_TLR	0x0010	Task Load Register
CE_TSR	0x0014	Task Status Register
CE_ESR	0x0018	Error Status Register
CE_SCSA	0x0024	Symmetric Algorithm DMA Current Source Address
CE_SCDA	0x0028	Symmetric Algorithm DMA Current Destination Address
CE_HCSA	0x0034	HASH Algorithm DMA Current Source Address
CE_HCDA	0x0038	HASH Algorithm DMA Current Destination Address
CE_ACSA	0x0044	Asymmetric Algorithm DMA Current Source Address
CE_ACDA	0x0048	Asymmetric Algorithm DMA Current Destination Address
CE_XCSA	0x0054	XTS Algorithm DMA Current Source Address
CE_XCDA	0x0058	XTS Algorithm DMA Current Destination Address

3.14.5. Register Description

3.14.5.1. CE Task Descriptor Address Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CE_TDA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	Task Descriptor Address

3.14.5.2. CE Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CE_ICR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x0	Task channel0-3 interrupt enable 0: interrupt disable 1: interrupt enable

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3.14.5.3. CE Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: CE_ISR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W1C	0x0	Task channel0-3 end pending 0: not finished 1: finished It indicates if task has been completed . Write '1' to clear it.

3.14.5.4. CE Task Load Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: CE_TLR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:8	R/W	0x0	Algorithm type, the same with type field in description common control.
7:1	/	/	/
0	R/W	0x0	Task Load When set, CE can load the descriptor of task if task FIFO is not full.

3.14.5.5. CE Task Status Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: CE_TSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R	0x0	indicate which channel in run for XTS. 00: task channel0 01: task channel1 10: task channel2 11: task channel3
23:18	/	/	/
17:16	R	0x0	indicate which channel in run for asymmetric. 00: task channel0 01: task channel1 10: task channel2 11: task channel3
15:10	/	/	/
9:8	R	0x0	indicate which channel in run for digest. 00: task channel0 01: task channel1 10: task channel2 11: task channel3

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7:2	/	/	/
1:0	R	0x0	indicate which channel in run for symmetric. 00: task channel0 01: task channel1 10: task channel2 11: task channel3

3.14.5.6. CE Error Status Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: CE_ESR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W1C	0x0	Task channel 3 error type. (the same for other channels) Bit 24: algorithm not support Bit 25: data length error Bit 26: keysram access error. Write '1' to clear. Bit 29: address invalid Bit30: key ladder configuration error other: reserved
23:16	R/W1C	0x0	Task channel 2 error type. Bit 16: algorithm not support Bit 17: data length error Bit 18: keysram access error. Write '1' to clear. Bit 21: address invalid Bit 22: key ladder configuration error other: reserved
15:8	R/W1C	0x0	Task channel 1 error type. Bit 8: algorithm not support Bit 9: data length error Bit 10: keysram access error. Write '1' to clear. Bit 13: address invalid Bit 14: key ladder configuration error other: reserved
7:0	R/W1C	0x0	Task channel 0 error type. Bit 0: algorithm not support Bit 1: data length error Bit 2: keysram access error. Write '1' to clear. Bit 5: address invalid Bit 6: key ladder configuration error other: reserved

3.14.5.7. CE Symmetric Current Source Address Register(Default Value: 0x0000_0000)

Offset: 0x0024	Register Name: CE_SCSA

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Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	Symmetric algorithm current source address DMA reads.

3.14.5.8. CE Symmetric Current Destination Address Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: CE_SCDA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	Symmetric algorithm current destination address DMA writes.

3.14.5.9. CE HASH Current Source Address Register(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: CE_HCSA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	HASH algorithm current source address DMA reads.

3.14.5.10. CE HASH Current Destination Address Register(Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: CE_HCDA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	HASH algorithm current destination address DMA writes.

3.14.5.11. CE Asymmetric Current Source Address Register(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: CE_ACSA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	Asymmetric algorithm current source address DMA reads.

3.14.5.12. CE Asymmetric Current Destination Address Register(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: CE_ACDA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	Asymmetric algorithm current destination address DMA writes.

3.14.5.13. CE XTS Current Source Address Register(Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: CE_XCSA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	XTS algorithm current source address DMA reads.

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3.14.5.14. CE XTS Current Destination Address Register(Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: CE_XCDA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	XTS algorithm current destination address DMA writes.

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3.15. Embedded Crypto Engine

3.15.1. Overview

The Embedded Crypto Engine(EMCE) module is AES encryption/decryption algorithms accelerator. It connects directly to SMHC or NDFC for disc encryption application. Master key and salt, from software configuration through AHB, are used as AES key. Input data for AES is from SMHC/NDFC through FIFO, and after encryption or decryption, output data from AES is put to controller through FIFO.

Features:

- Supports Symmetrical Algorithm: AES
- Supports 128-bit, 192-bit and 256-bit key size for AES
- Supports ECB, CBC,XTS modes

3.15.2. Block Diagram

Figure 3-47 shows a block diagram of EMCE.

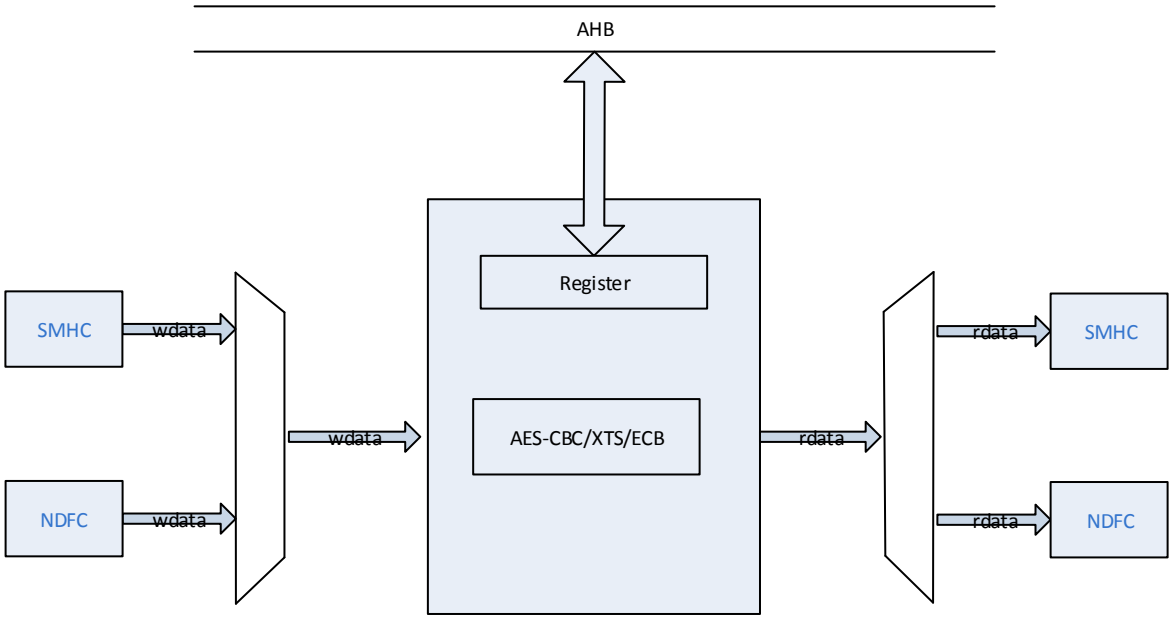


Figure 3-47. EMCE Block Diagram

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3.15.3. Operations and Functional Descriptions

3.15.3.1. Key Configuration

There are two keys for configuration when system initialization. Salt is the key for AES-ECB when computing iv. Master key is the key for AES-CBC/ECB/XTS when computing data. Sector is the input for AES-ECB when computing iv.

3.15.3.2. Controller Signals

Controller send start signal to EMCE to start computation for current sector. When computing finished, EMCE sends pulse end signal to controller for handshake.

Controller should tell EMCE algorithm mode(ECB or CBC or XTS), and key length(128-bit or 192-bit or 256-bit), and current computation direction(encryption or decryption).

When wrdy is valid, controller can write source data to src FIFO. When rrdy is valid, controller can read result from dst FIFO.

3.15.3.3. EMCE Timing

After received start signal from controller, EMCE synchronizes it to emce_clk, then generate up pulse signal as start. Then EMCE computes IV, transfers key(only for decryption), handles data from FIFO. The timing for each stage is as follows.

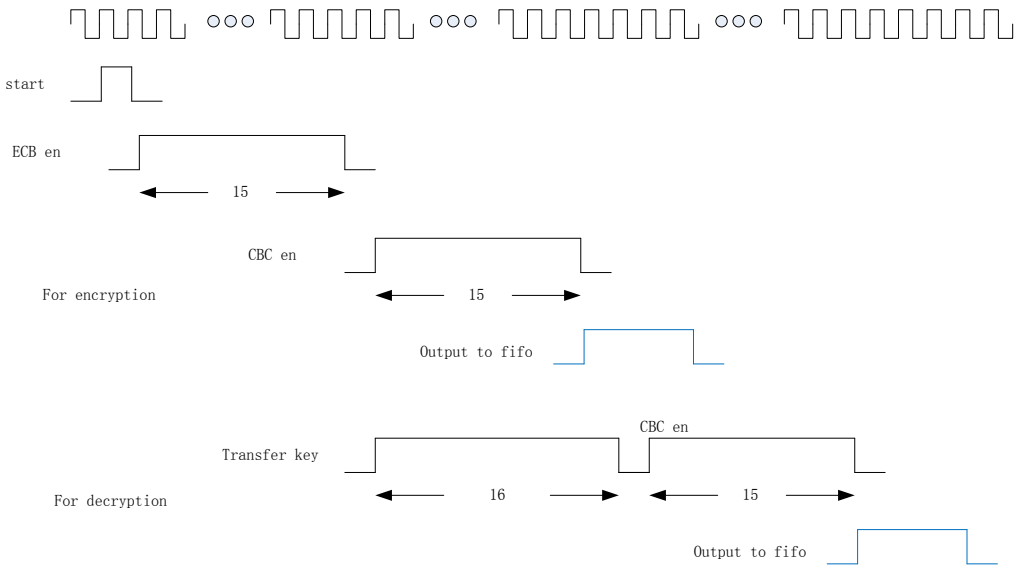


Figure 3-48. EMCE Timing

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3.15.4. Register List

Module Name	Base Address
EMCE	0x01905000

Register Name	Offset	Description
EMCE_KEY0	0x0000	EMCE Master Key's 1st Word
EMCE_KEY1	0x0004	EMCE Master key's 2nd Word
EMCE_KEY2	0x0008	EMCE Master Key's 3rd Word
EMCE_KEY3	0x000C	EMCE Master Key's 4th Word
EMCE_KEY4	0x0010	EMCE Master Key's 5th Word
EMCE_KEY5	0x0014	EMCE Master Key's 6th Word
EMCE_KEY6	0x0018	EMCE Master Key's 7th Word
EMCE_KEY7	0x001C	EMCE Master Key's 8th Word
EMCE_SALT0	0x0040	EMCE Master Salt's 1st Word
EMCE_SALT1	0x0044	EMCE Master Salt's 2nd Word
EMCE_SALT2	0x0048	EMCE Master Salt's 3rd Word
EMCE_SALT3	0x004C	EMCE Master Salt's 4th Word
EMCE_SALT4	0x0050	EMCE Master Salt's 5th Word
EMCE_SALT5	0x0054	EMCE Master Salt's 6th Word
EMCE_SALT6	0x0058	EMCE Master Salt's 7th Word
EMCE_SALT7	0x005C	EMCE Master Salt's 8th Word
EMCE_MODE	0x0080	AES Configuration for Key Length and Mode

3.15.5. Register Description

3.15.5.1. EMCE Master Key0 Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: EMCE_KEY0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	EMCE master key's 1st word

3.15.5.2. EMCE Master Key1 Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: EMCE_KEY1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	EMCE master key's 2nd word

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3.15.5.3. EMCE Master Key2 Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: EMCE_KEY2
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	EMCE master key's 3rd word

3.15.5.4. EMCE Master Key3 Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: EMCE_KEY3
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	EMCE master key's 4th word

3.15.5.5. EMCE Master Key4 Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: EMCE_KEY4
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	EMCE master key's 5th word

3.15.5.6. EMCE Master Key5 Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: EMCE_KEY5
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	EMCE master key's 6th word

3.15.5.7. EMCE Master Key6 Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: EMCE_KEY6
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	EMCE master key's 7th word

3.15.5.8. EMCE Master Key7 Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: EMCE_KEY7
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	EMCE master key's 8th word

3.15.5.9. EMCE Salt0 Register(Default Value: 0x0000_0000)

Offset: 0x0040	Register Name: EMCE_SALT0

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Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	EMCE salt's 1st word

3.15.5.10. EMCE Salt1 Register(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: EMCE_SALT1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	EMCE salt's 2nd word

3.15.5.11. EMCE Salt2 Register(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: EMCE_SALT2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	EMCE salt's 3rd word

3.15.5.12. EMCE Salt3 Register(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: EMCE_SALT3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	EMCE salt's 4th word

3.15.5.13. EMCE Salt4 Register(Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: EMCE_SALT4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	EMCE salt's 5th word

3.15.5.14. EMCE Salt5 Register(Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: EMCE_SALT5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	EMCE salt's 6th word

3.15.5.15. EMCE Salt6 Register(Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: EMCE_SALT6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	EMCE salt's 7th word

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3.15.5.16. EMCE Salt7 Register(Default Value: 0x0000_0000)

Offset: 0x005C			Register Name: EMCE_SALT7
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	EMCE salt's 8th word

3.15.5.17. EMCE Configuration Register(Default Value: 0x0200_0801)

Offset: 0x0080			Register Name: EMCE_MODE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x200	Sector Size for Controller
15:13	/	/	/
12	R/W	0x0	NAND_OR_EMMC 0: current controller is NDFC 1: current controller is SMHC
11:10	R/W	0x2	IV_KEY_LEN AES key length when computing IV 00: 128-bit 01: 192-bit 10: 256-bit 11: reserved
9:6	/	/	/
5:4	R/W	0x0	KEY_LEN 00: 128-bit 01: 192-bit 10: 256-bit 11: reserved
3:0	R/W	0x1	Mode 0000: ECB 0001: CBC 1001:XTS Others: reserved

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3.16. Security ID

3.16.1. Overview

The SID module is 4 Kbits electrical fuse for saving key, which includes chip ID, thermal sensor, HASH code and security key. The module has the following features.

- The module is secure forever, only secure CPUX can access it
- A fuse only can program one time
- SID_SRAM is used for backuping efuse information

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3.17. Thermal Sensor Controller

3.17.1. Overview

Thermal sensors have become common elements in wide range of modern system on chip (SOC) platform. Thermal sensors are used to constantly monitor the temperature on the chip.

The Thermal Sensor Controller embeds two thermal sensors, sensor0 for CPU,sensor1 for GPU .Thermal sensors can generate interrupt to SW to lower temperature via DVFS, on reaching a certain thermal threshold.

Features:

- Temperature Accuracy : ±3℃ from 0℃ to +100℃, ±5℃ from -20℃ to +125℃
- Power supply voltage:1.8V
- Averaging filter for thermal sensor reading
- Supports over-temperature protection interrupt and over-temperature alarm interrupt

3.17.2. Block Diagram

Figure 3-51 shows a block diagram of the Thermal Sensor.

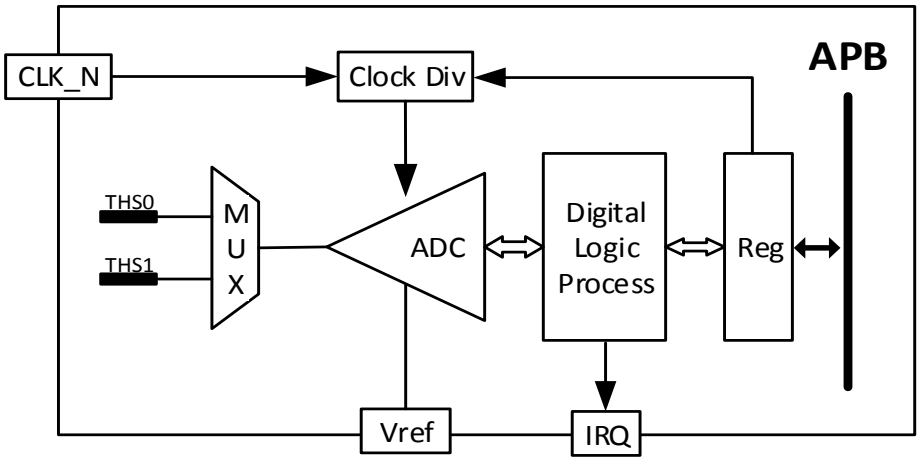


Figure 3-49. Thermal Sensor Block Diagram

3.17.3. Operations and Functional Descriptions

3.17.3.1. Clock Sources

Thermal Sensor get one clock source. Table 3-18 describes the clock source for Thermal Sensor. Users can see **Clock**

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Controller Unit(CCU) for clock setting, configuration and gating information.

Table 3-10. Thermal Sensor Clock Sources

Clock Sources	Description
OSC24M	24MHz OSC

3.17.3.2. Timing Requirements

CLK_IN = 24MHz

CONV_TIME(Conversion Time) = 1/(24MHz/14Cycles) =0.583 (us)

SENSOR_ACQ> 1/(24MHz/24Cycles)

THERMAL_PER > SENSOR_ACQ+CONV_TIME

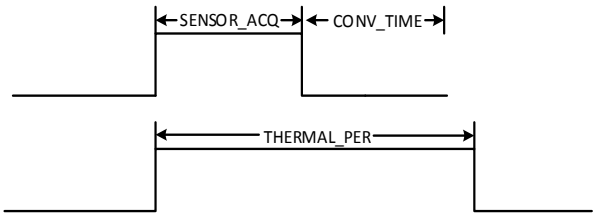


Figure 3-50. Thermal Sensor Time Requirement

3.17.3.3. Interrupt

The thermal sensor has four interrupt source, such as DATA_IRQ , SHUTDOWN_IRQ,ALARM_IRQ and ALARM_OFF_IRQ. Figure 3-53 shows the thermal sensor interrupt sources.

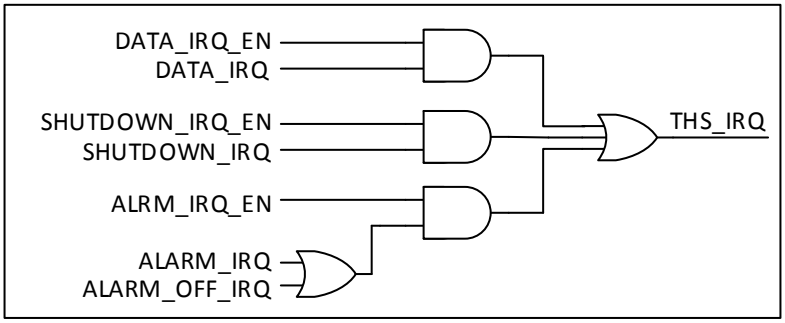


Figure 3-51. Thermal Sensor Interrupt Source

When temperature is higher than Alarm_Threshold, ALARM_IRQ is generated. When temperature is lower than Alarm_Off_Thershold, ALARM_OFF_IRQ is generated. ALARM_OFF_IRQ is fall edge trigger.

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3.17.4. Programming Guidelines

3.17.4.1. Initial Process

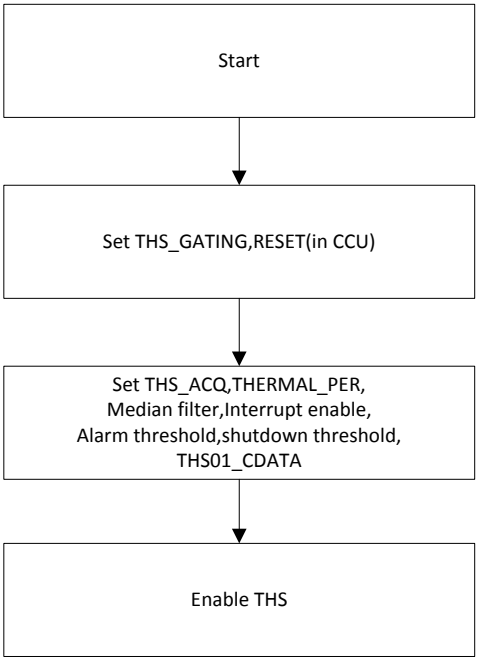


Figure 3-52. Initial Process

NOTE

The formula of THS is y=-ax+b. In FT stage, THS is calibrated according to ambient temperature, the calibration value is written in EFUSE. Please refer to SID Spec about EFUSE information.

Before enable THS, read EFUSE value and write the value to THS01_CDATA.

3.17.5. Register List

Module Name	Base Address
Thermal Sensor	0x05070400

Register Name	Offset	Description
THS_CTRL	0x0000	THS Control Register
THS_EN	0x0004	THS Enable Register
THS_PER	0x0008	THS Period Control Register
/	/	/
THS_DATA_INTC	0x0010	THS Data Interrupt Control Register
THS_SHUT_INTC	0x0014	THS Shut Interrupt Control Register

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THS_ALARM_INTC	0x0018	THS Alarm Interrupt Control Register
/	/	/
THS_DATA_INTS	0x0020	THS Data Interrupt Status Register
THS_SHUT_INTS	0x0024	THS Shut Interrupt Status Register
THS_ALARMO_INTS	0x0028	THS Alarm off Interrupt Status Register
THS_ALARM_INTS	0x002C	THS Alarm Interrupt Status Register
THS_FILTER	0x0030	THS Median Filter Control Register
/	/	/
THS0_ALARM_CTRL	0x0040	THS0 Alarm threshold Control Register
THS1_ALARM_CTRL	0x0044	THS1 Alarm threshold Control Register
/	/	/
THS01_SHUTDOWN_CTRL	0x0080	THS0&1 Alarm threshold Control Register
/	/	/
THS01_CDATA	0x00A0	THS0&1 Calibration Data
/	/	/
THS0_DATA	0x00C0	THS0 Data Register
THS1_DATA	0x00C4	THS1 Data Register
/	/	/

3.17.6. Register Description

3.17.6.1. THS Control Register(Default Value : 0x01DF_0000)

Offset: 0x0000			Register Name: THS_CTRL
Bit	**Rear/Write**	**Default/Hex**	**Description**
31:16	R/W	0x1DF(20us)	SENSOR_ACQ Sensor acquire time CLK_IN/(N+1)
15:0	/	/	/

3.17.6.2. THS Enable Register(Default Value : 0x0000_0000)

Offset: 0x0004			Register Name: THS_EN
Bit	**Rear/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	SENSE1_EN Enable temperature measurement sensor1 0:Disable 1:Enable
0	R/W	0x0	SENSE0_EN Enable temperature measurement sensor0 0:Disable

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			1:Enable

3.17.6.3. THS Period Control Register(Default Value: 0x0003_A000)

Offset: 0x0008			Register Name: THS_PER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	0x3A(10ms)	THERMAL_PER 4096*(n+1)/CLK_IN
11:0	/	/	/

3.17.6.4. THS Data Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: THS_DATA_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	THS1_DATA_IRQ_EN Selects temperature measurement data of sensor1 0:Disable 1:Enable
0	R/W	0x0	THS0_DATA_IRQ_EN Selects temperature measurement data of sensor0 0:Disable 1:Enable

3.17.6.5. THS Shut Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: THS_SHUT_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	SHUT_INT1_EN Selects shutdown interrupt for sensor1 0:Disable 1:Enable
0	R/W	0x0	SHUT_INT0_EN Selects shutdown interrupt for sensor0 0:Disable 1:Enable

3.17.6.6. THS Alarm Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0018	Register Name: THS_ALARM_INTC

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Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	ALARM_INT1_EN Selects alarm interrupt for sensor1 0:Disable 1:Enable
0	R/W	0x0	ALARM_INT0_EN Selects alarm interrupt for sensor0 0:Disable 1:Enable

3.17.6.7. THS Data Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: THS_DATA_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1C	0x0	THS1_DATA_IRQ _STS Data interrupt status for sensor1 Write ‘1’ to clear this interrupt or automatic clear if interrupt condition fails.
0	R/W1C	0x0	THS0_DATA_IRQ _STS Data interrupt status for sensor0 Write ‘1’ to clear this interrupt or automatic clear if interrupt condition fails.

3.17.6.8. THS Shut Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: THS_SHUT_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1C	0x0	SHUT_INT1_STS Shutdown interrupt status for sensor1 Write ‘1’ to clear this interrupt or automatic clear if interrupt condition fails.
0	R/W1C	0x0	SHUT_INT0_STS Shutdown interrupt status for sensor0 Write ‘1’ to clear this interrupt or automatic clear if interrupt condition fails

3.17.6.9. THS Alarm off Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0028	Register Name: THS_ALARMO_INTS

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Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W1C	0x0	ALARM_ OFF1_STS Alarm interrupt off pending for sensor1 Write '1' to clear this interrupt or automatic clear if interrupt condition fails.
0	R/W1C	0x0	ALARM_ OFF0_STS Alarm interrupt off pending for sensor0 Write '1' to clear this interrupt or automatic clear if interrupt condition fails

3.17.6.10. THS Alarm Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: THS_ALARM_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1C	0x0	ALARM_INT1_STS Alarm interrupt pending for sensor1 Write '1' to clear this interrupt or automatic clear if interrupt condition fails
0	R/W1C	0x0	ALARM_INT0_STS Alarm interrupt pending for sensor0 Write '1' to clear this interrupt or automatic clear if interrupt condition fails

3.17.6.11. Median filter Control Register(Default Value: 0x0000_0001)

Offset: 0x0030			Register Name: THS_FILTER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	FILTER_EN. Filter Enable 0: Disable 1: Enable
1:0	R/W	0x1	FILTER_TYPE. Average Filter Type 00: 2 01: 4 10: 8 11: 16

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3.17.6.12. THS0 Alarm threshold Control Register(Default Value: 0x05A0_0684)

Offset: 0x0040			Register Name: THS0_ALARM_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x5A0	ALARM0_T_HOT Thermal Sensor0 Alarm Threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM0_T_HYST Thermal Sensor0 Alarm threshold for hysteresis temperature

3.17.6.13. THS1 Alarm threshold Control Register (Default Value: 0x05A0_0684)

Offset: 0x0044			Register Name: THS1_ALARM_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x5A0	ALARM1_T_HOT Thermal sensor1 Alarm Threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM1_T_HYST Thermal sensor1 Alarm threshold for hysteresis temperature

3.17.6.14. THS0&1 Shutdown threshold Control Register (Default Value: 0x04E9_04E9)

Offset: 0x0080			Register Name: THS01_SHUTDOWN_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x4E9	SHUT1_T_HOT Thermal Sensor1 Shutdown Threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x4E9	SHUT0_T_HOT Thermal Sensor0 Shutdown Threshold for hot temperature

3.17.6.15. THS0&1 Calibration Data(Default Value: 0x0800_0800)

Offset: 0x00A0			Register Name: THS01_CDATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
27:16	R/W	0x800	THS1_CDATA. Thermal Sensor1 calibration data
15:12	/	/	/
11:0	R/W	0x800	THS0_CDATA.

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			Thermal Sensor0 calibration data

3.17.6.16. THS0 Data Register(Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: THS0_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x0	THS0_DATA. Temperature measurement data of sensor0

3.17.6.17. THS1 Data Register(Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: THS1_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x0	THS1_DATA. Temperature measurement data of sensor1

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3.18. RTC

3.18.1. Overview

The RTC(Real Time Clock) is used to display the real time and periodically wakeup .The RTC can display the year, month, day, week, hour, minute, second in real time. The RTC has the independent power to continue to work in system power-off. The RTC has the following features:

- Provides a 7-bit counter for counting year, 4-bit counter for counting month, 5-bit counter for counting day, 3-bit counter for counting week, 5-bit counter for counting hour, 6-bit counter for counting minute, 6-bit counter for counting second
- External connect a 32768Hz low-frequency oscillator for count clock
- Configurable initial value by software anytime
- Periodically alarm to wakeup the external devices
- Stores power-off information in eight 32-bit general purpose register

3.18.2. Block Diagram

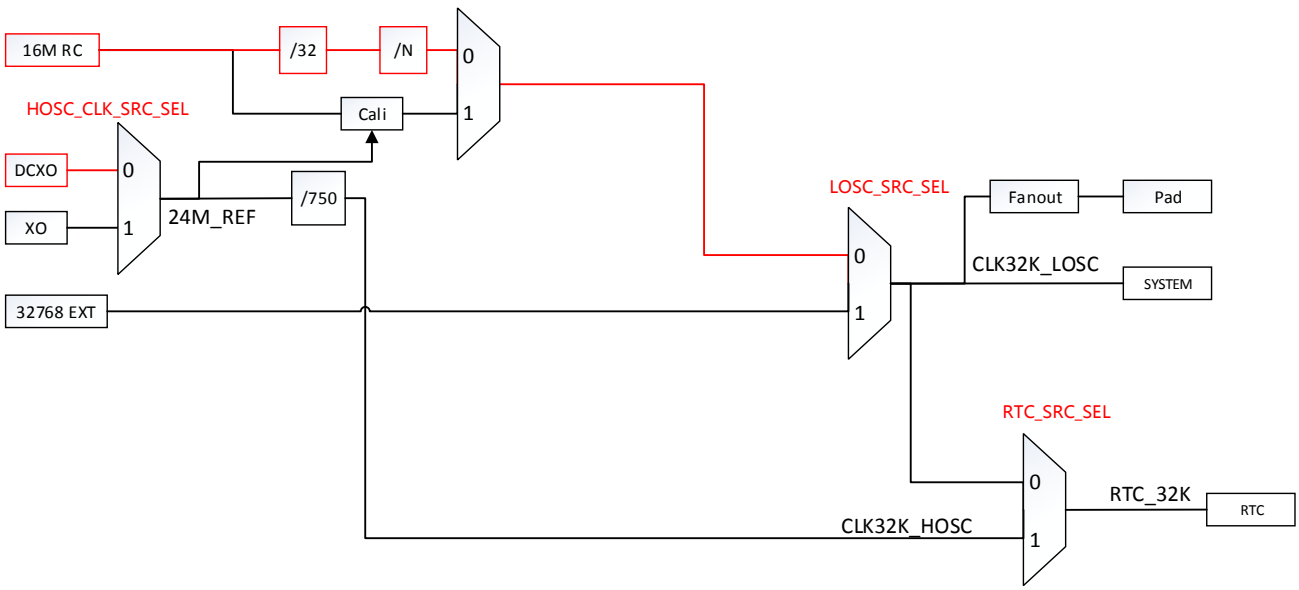


Figure 3-53. RTC Block Diagram

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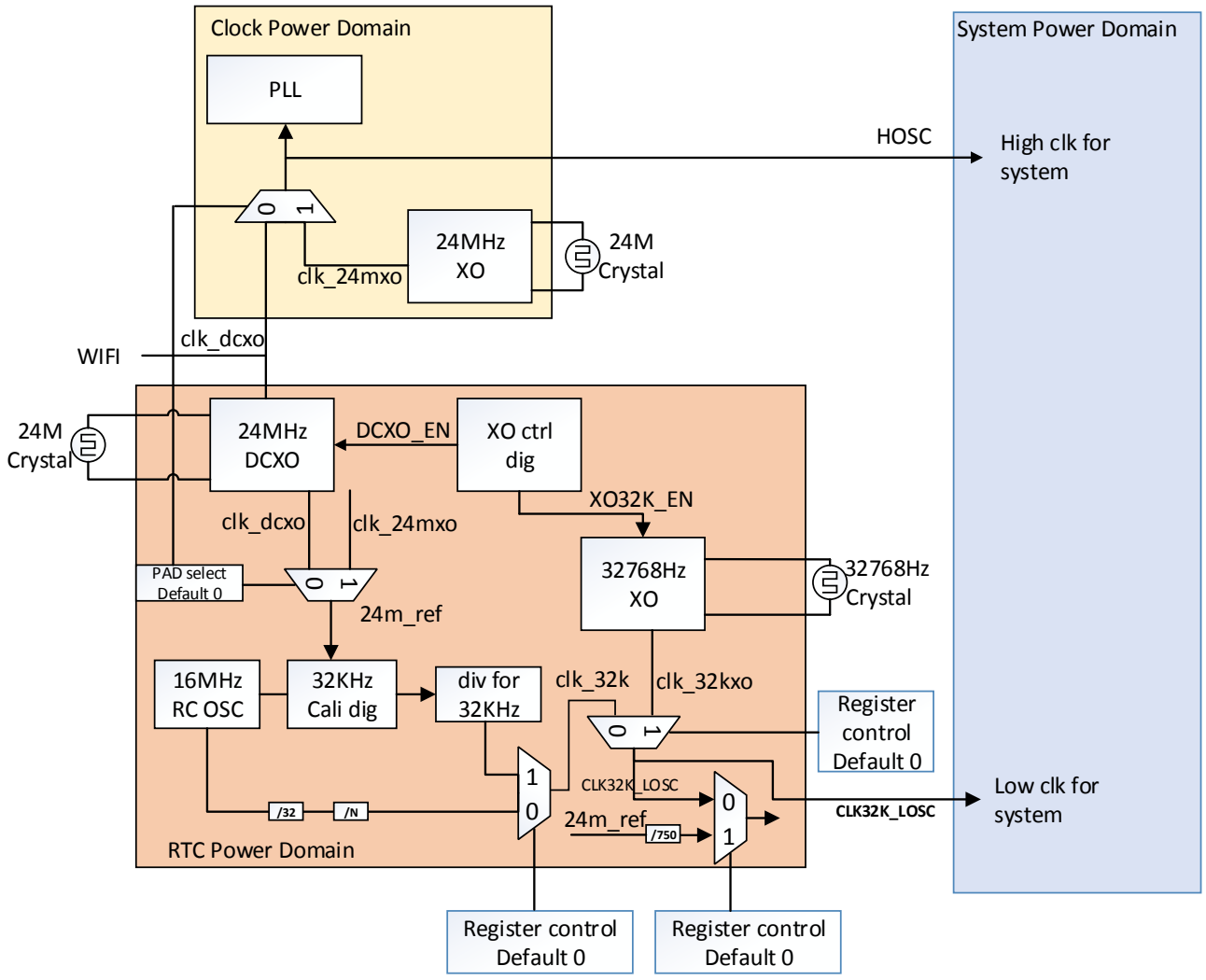


Figure 3-54. RTC Power Domain

Clock sources: 24MHz high-frequency crystal oscillator, 32768Hz low-frequency crystal oscillator, internal 16MHz RC

Oscillating circuit: 32768Hz XO, 24MHz XO, 24MHz DCXO

Controlling circuit: oscillator enable circuit, 32KHz calibration circuit, 32KHz frequency divider circuit,24MHz clock select circuit,32KHz clock select circuit, low-frequency clock source select circuit

Output clock: HOSC,CLK32K_LOSC,RTC_32K

3.18.3. Operations and Functional Descriptions

3.18.3.1. External Signals

Table 3-11. RTC External Signals

Signal	Description
X32KIN	32KHz oscillator input

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X32KOUT	32KHz oscillator output
X32KFOUT	32KHz clock fanout, provides low frequency clock for external devices
NMI	Alarm wakeup generates low level into NMI
RTC-VIO	RTC low voltage,generated via internal LDO
VCC-RTC	RTC high voltage,generated via external power

3.18.3.2. Clock and Reset

The RTC module has the independent reset signal, the signal follows VCC-RTC. When VCC-RTC powers on, the reset signal resets the RTC module; after VCC-RTC reaches stable, the reset signal always holds high level.

The RTC module accesses its register by APB1.

3.18.3.3. Typical Application

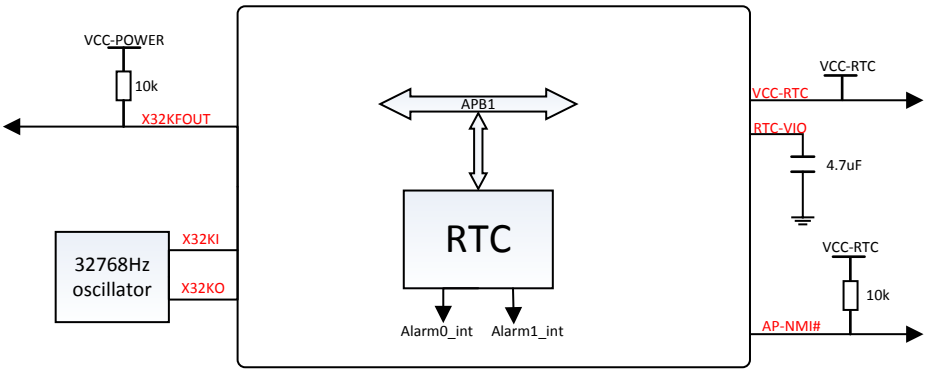


Figure 3-55. RTC Application Diagram

The system accesses RTC register by APB1 to generate the real time.
The external low-frequency oscillator must be 32.768 kHz.
If the external devices need low-frequency oscillator, X32KFOUT can provide.
AP-NMI# and alarm0 in common generate low level signal.

3.18.3.4. Function Implementation

3.18.3.4.1. Clock Sources

The RTC has two clock sources: internal RC , external low frequency oscillator.
The internal RC can change RTC clock by changing division ratio ;the external clock can not change clock.
The RTC selects the internal RC by default, when the system starts, the RTC can select by software the external low frequency oscillator to provide much accuracy clock.
The clock accurate of the RTC is related to the accurate of the external low frequency oscillator. The external oscillator usually selects 32.768 kHz oscillator with ±20ppm frequency tolerance.

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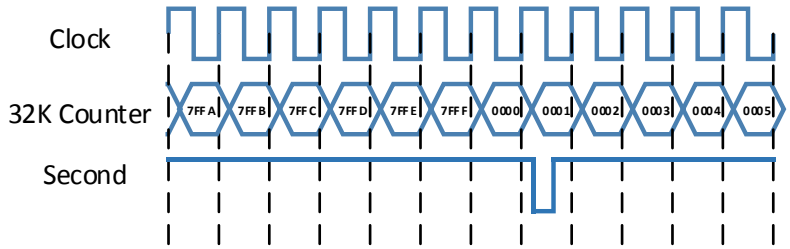


Figure 3-56. RTC Counter

The 32K counter adds 1 on each rising edge of the clock. When the clock number reaches 0x8000,32KHz counter starts to count again from 0, and the second counter adds 1. The 32KHz counter block diagram is as follows.

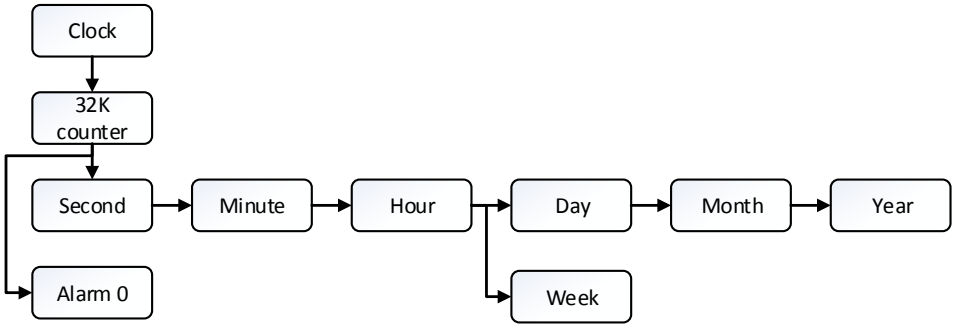


Figure 3-57. RTC 32KHz Counter Block Diagram

According to above implementation, the changing range of each counter is as follows.

Table 3-12. RTC Counter Changing Range

Counter	Range
Second	If the counter value is not in the range from 0 to 59, then the counter value can change to 59 automatically.
Minute	If the counter value is not in the range from 0 to 59, then the counter value can change to 59 automatically.
Hour	If the counter value is not in the range from 0 to 23, then the counter value can change to 23 automatically.
Week	If the counter value is not in the range from 0 to 6, then the counter value can change to 6 automatically.
Day	If the counter value is not in the range from 1 to 31, then the counter value can change to the maximum value of that month automatically.
Month	If the counter value is not in the range from 1 to 12, then the counter value can change to 12 automatically.
Year	The software can set a reference year, the leap year can only set by software.

3.18.3.4.2. Alarm 0

The principle of alarm0 is similar to the second counter, the difference is that alarm0 is a 32-bit down counter. When the counter decreases to 0 from the initial value, the RTC generates the interrupt, or outputs low level signal by NMI pin to wakeup power management chip.

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3.18.3.4.3. Alarm 1

The alrm1 can set alarm response time and the response cycle. When the system real time satisfies the setting time, the RTC generates alram1 interrupt to handle alarm interrupt function.

3.18.3.4.4. Power-off Storage

The RTC provides eight 32-bit general purpose register to store power-off information.

Because VCC-RTC always holds non-power-off state after VCC-RTC cold starts, when the system is in shutdown or standby scene, CPU can judge software process by the storing information.

3.18.3.4.5. RTC-VIO

The RTC module has a LDO ,the input source of the LDO is VCC-RTC,the output of the LDO is RTC-VIO,the value of RTC-VIO is adjustable,it is mainly used for internal digital logic.

3.18.3.4.6. RC Calibration

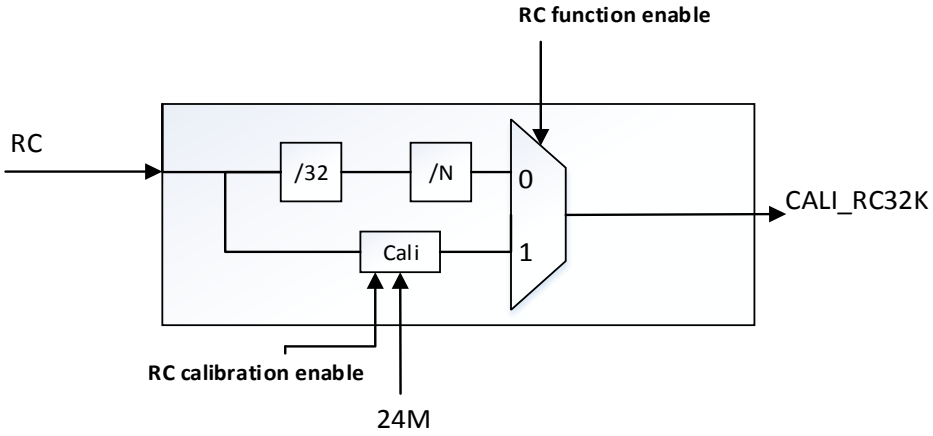


Figure 3-58. RC Calibration Block Diagram

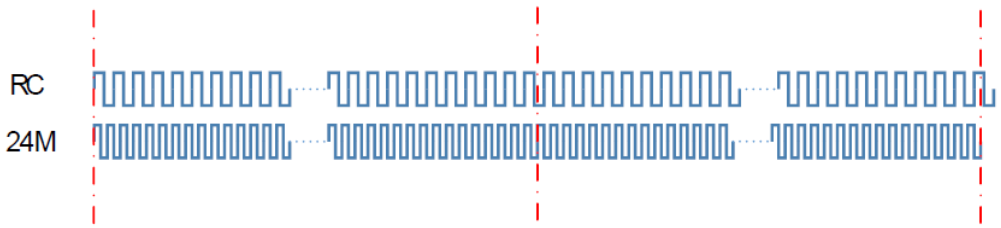


Figure 3-59. RC and 24MHz Waveform

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(1) 24MHz as a reference clock, calculate the counter number(M) of RC clock within 1ms/16ms.
(2) After calibration, the value of internal RC is get, and division factor(K) of 32768Hz from RC clock divided is get.
(3) K has 28-bit,the lower 16-bit is decimal, the higher 12-bit is integer.
(4) The implementation of calibration is to output 32.768kHz.

3.18.3.5. Operating Mode

3.18.3.5.1. RTC Clock Control

(1) Select clock source: Select clock source by the bit0 of **LOSC_CTRL_REG**, the clock source is the internal RC oscillator by default, when the system starts, the clock source can be switched to the external 32K oscillator by software.
(2) Auto switch: After enabled the bit[14] of **LOSC_CTRL_REG**, the RTC automatically switches clock source to the internal oscillator when the external oscillator could not output waveform, the switch status can query by the bit[1] of **LOSC_AUTO_SWT_STA_REG**.
(3) After auto switch is valid, the clock source status bit cannot be changed, because the two functions are independent.

3.18.3.5.2. RTC Calendar

(1) Write time initial value: Write the current time to **RTC_HH_MM_SS_REG** and **RTC_YY_MM_DD_REG**.
(2) After update time, the RTC restarts to count again .The software can read the current time anytime.
(3) The leap year function can be set only by the software.

3.18.3.5.3. Alarm0

(1) Enable alram0 interrupt by writing **ALARM0_IRQ_EN**.
(2) Set the counter initial value, write the count- down second number to **ALARM0_COUNTER_REG**.
(3) Enable alarm0 function by writing **ALARM0_ENABLE_REG**, then the software can query alarm count value in real time.
(4) After enter the interrupt process, write **ALARM0_IRQ_STA_REG** to clear the interrupt pending, and execute the process of waiting for the interrupt.
(5) Resume the interrupt and continue to execute the interrupted process.
(6) Power-off wakeup is generated via SoC hardware and PMIC, software only need set pending condition of alarm0, and set 1 to **ALARM0_CONFIG_REG**.

3.18.3.5.4. Alarm 1

(1) Set alarm1 initial value : write the hour,minute,second of alarm1 to **ALARM1_WK_HH_MM_SS**.
(2) Write alarm week number enable bit to **ALARM1_EN_REG**.
(3) When the bit[20:0] of **RTC_HH_MM_SS_REG** is equal to **ALARM1_WK_HH_MM-SS,** and the bit[31:29] of

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RTC_HH_MM_SS_REG is equal to the week number of **ALARM1_EN_REG**, then the condition of alarm 1 is satisfied, pending is set automatically by hardware.

(4) When **ALARM0_IRQ_EN** is set to 1, the RTC enters into the interrupt process, write **ALARM0_IRQ_STA_REG** to clear the interrupt pending, and execute the process of waiting for the interrupt.

(5) Resume the interrupt and continue to execute the interrupted process.

3.18.3.5.5. Fanout

The bit0 of **LOSC_OUT_GATING_REG** is set to 1, and external pull-up resistor and voltage is normal, then 32.768kHz square wave can be outputted.

3.18.3.5.6. Pad Hold

When the corresponding bit of **GPL_HOLD_OUTPUT_REG** and **GPM_HOLD_OUTPUT_REG** is set to 1, the corresponding pin can hold in stable state(high level,low level or high impedance). The function is used to prevent output pin from changing when corresponding power changes.

3.18.3.5.7. RC Calibration Usage Scenario

(1) Power-on: Select non-accurate 32KHz clock divided by internal RC.

(2) Normal scenario: RTC can select 32KHz clock divided by 24MHz, or use calibration clock.If threr has fanout requirement, then calibration clock is needed.

(3) Standby or power-off scenario: Select accurate 32KHz generated by DCXO24M calibrates RC clock.

3.18.4. Programming Guildlines

3.18.4.1. RTC Clock Sources Setting

```
writel(0x16aa4000,LOSC_Ctrl);          //writing key field
writel(0x16aa4001,LOSC_Ctrl);    //select external clock
```

3.18.4.2. Real Time Clock

```
writel(0x00173b3b,RTC_HMS);
writel(1<<22|1<<8|31<<0,RTC_YMD);
readl(RTC_HMS);
readl(RTC_YMD);
```

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3.18.4.3. Alarm 0

```
irq_request(GIC_SRC_R_Alarm0,Alm0_handler);
irq_enable(GIC_SRC_R_Alarm0);
writel(1,ALM0_COUNTER);                    //set 1 second corresponding to normal mode;
writel(1,ALM0_EN);
writel(1,ALM_CONFIG); //NMI output
while(!readl(ALM0_IRQ_STA));
writel(1,ALM0_IRQ_EN);
while(readl(ALM0_IRQ_STA));
```

3.18.4.4. Alarm 1

```
irq_request(GIC_SRC_R_Alarm1,Alm1_handler);
irq_enable(GIC_SRC_R_Alarm1);
writel(0,ALM1_WK_HMS);
writel(0x7f,ALM1_EN);
writel(1,ALM1_IRQ_STA);
writel(0x00173b3b | week<<29,RTC_HMS);  //set 1 second corresponding to normal mode;
while(readl(RTC_HMS)&0xff);
while(!readl(ALM1_IRQ_STA));
writel(1,ALM1_IRQ_EN);
while(readl(ALM1_IRQ_STA));
```

3.18.5. Register List

Module Name	Base Address
RTC	0x07000000

Register Name	Offset	Description
LOSC_CTRL_REG	0x0000	Low Oscillator Control Register
LOSC_AUTO_SWT_STA_REG	0x0004	LOSC Auto Switch Status Register
INTOSC_CLK_PRESCAL_REG	0x0008	Internal OSC Clock Prescalar Register
INTOSC_CLK_AUTO_CALI_REG	0x000C	Internal OSC Clock Auto Calibration Register
RTC_YY_MM_DD_REG	0x0010	RTC Year-Month-Day Register
RTC_HH_MM_SS_REG	0x0014	RTC Hour-Minute-Second Register
ALARM0_COUNTER_REG	0x0020	Alarm 0 Counter Register
ALARM0_CUR_VLU_REG	0x0024	Alarm 0 Counter Current Value Register
ALARM0_ENABLE_REG	0x0028	Alarm 0 Enable Register
ALARM0_IRQ_EN	0x002C	Alarm 0 IRQ Enable Register
ALARM0_IRQ_STA_REG	0x0030	Alarm 0 IRQ Status Register
ALARM1_WK_HH_MM-SS	0x0040	Alarm 1 Week HMS Register

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ALARM1_ENABLE_REG	0x0044	Alarm 1 Enable Register
ALARM1_IRQ_EN	0x0048	Alarm 1 IRQ Enable Register
ALARM1_IRQ_STA_REG	0x004C	Alarm 1 IRQ Status Register
ALARM_CONFIG_REG	0x0050	Alarm Configuration Register
LOSC_OUT_GATING_REG	0x0060	LOSC Output Gating Register
GP_DATA_REG	0x0100 + N*0x04	General Purpose Register (N=0~7)
XO_CTRL_REG	0x0160	XO Control Register
CALI_CTRL_REG	0x0164	Calibration Control Register
GPL_HOLD_OUTPUT_REG	0x0180	GPL Hold Output Register
GPM Hold Output Register	0x0184	GPM Hold Output Register
RTC_PWR_MODE_SEL_REG	0x0188	RTC POWER MODE SELECT Register
RTC-VIO_REG	0x0190	RTC-VIO Regulate Register
BOOT_CPU_HP_FLAG_REG	0x01B8	Boot CPU Hot Plug Flag Register
CPU_SOFT_ENT_REG0	0x01BC	CPU Software Entry Register 0
IC_CHARA_REG	0x01F0	IC Characteristic Register
SUP_STAN_FLAG_REG	0x01F8	Super Standby Flag Register
CPU_SOFT_ENT_REG1	0x01FC	CPU Software Entry Register 1
CRY_CONFIG_REG	0x0210	Crypto Configuration Register
CRY_KEY_REG	0x0214	Crypto Key Register
CRY_EN_REG	0x0218	Crypto Enable Register

3.18.6. Register Description

3.18.6.1. LOSC Control Register (Default Value: 0x0000_4010)

Offset:0x0000			**Register Name: LOSC_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	W	0x0	KEY_FIELD. Key Field. This field should be filled with 0x16AA, and then the bit 0 can be written with the new value.
15	/	/	/
14	R/W	0x1	LOSC_AUTO_SWT_EN. LOSC Auto Switch Enable. 0: Disable 1: Enable.
13:10	/	/	/
9	R/W	0x0	ALM_DDHHMMSS_ACCE. ALARM DD-HH-MM-SS access. After writing the **Alarm 1 Week HH-MM-SS Register**, this bit is set and it will be cleared until the real writing operation is finished.
8	R/W	0x0	RTC_HHMMSS_ACCE. RTC HH-MM-SS access.

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			After writing the **RTC HH-MM-SS Register**, this bit is set and it will be cleared until the real writing operation is finished. After writing the **RTC HH-MM-SS Register**, the **RTC HH-MM-SS Register** will be refreshed for at most one second.
7	R/W	0x0	RTC_YYMMDD_ACCE. RTC YY-MM-DD access. After writing the **RTC YY-MM-DD Register**, this bit is set and it will be cleared until the real writing operation is finished. After writing the **RTC YY-MM-DD Register**, the **RTC YY-MM-DD Register** will be refreshed for at most one second.
6:5	/	/	/
4	R/W	0x1	EXT_LOSC_EN. External 32768Hz Crystal Enable. 0: Disable 1: Enable
3:2	R/W	0x0	EXT_LOSC_GSM. External 32768Hz Crystal GSM. 00: Low 01: / 10: / 11 High
1	/	/	/
0	R/W	0x0	LOSC_SRC_SEL. LOSC Clock source Select. '**N**' is the value of **Internal OSC Clock Prescalar Register**. 0: InternalOSC /32/ N 1: External 32.768kHz OSC. (InternalOSC = 16MHz)

NOTE

If the bit[9:7] of LOSC_CTRL_REG is set, the corresponding of Alarm 1 Week HH-MM-SS Register, RTC HH-MM-SS Register, RTC YY-MM-DD Register can't be written.

3.18.6.2. LOSC Auto Switch Status Register (Default Value: 0x0000_0000)

Offset:0x0004			**Register Name: LOSC_AUTO_SWT_STA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R	0x0	EXT_LOSC_STA. 0: External 32.768k OSC work normally. 1: External 32.768k OSC work abnormally.
1	R/W1C	0x0	LOSC_AUTO_SWT_PEND. LOSC auto switch pending.

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			0: No effect 1: Auto switches pending Setting 1 to this bit will clear it.
0	R	0x0	LOSC_SRC_SEL_STA. Checking LOSC Clock Source Status. '**N**' is the value of **Internal OSC Clock Prescalar Register**. 0: InternalOSC /32/ N 1: External 32.768kHz OSC (InternalOSC = 16MHz)

3.18.6.3. Internal OSC Clock Prescalar Register (Default Value: 0x0000_000F)

Offset:0x0008			**Register Name: INTOSC_CLK_PRESCAL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xF	INTOSC_CLK_PRESCAL. Internal OSC Clock Prescalar value N. 0x000: 1 0x001: 2 0x002: 3 ..... 0x1F: 32

3.18.6.4. Internal OSC Clock Auto Calibration Register (Default Value: 0x1E80_0000)

Offset:0x000C			**Register Name: INTOSC_CLK_AUTO_CALI_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	RO	0x1e8	32K Calibration Integer Divide Factor.
19:4	RO	0x0	32K Calibration Decimal Divide Factor.
3	/	/	/
2	R/W	0x0	RC Calibration Precise Selection 0: 1ms calibration precise 1: 16ms calibration precise
1	R/W	0x0	RC calibration enable 0 : Close Calibration circuit 1 : Open Calibration circuit
0	R/W	0x0	RC calibration function enable 0： Normal RC 1： Calibrated RC

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3.18.6.5. RTC YY-MM-DD Register

Offset:0x0010			Register Name: RTC_YY_MM_DD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22	R/W	0x0	LEAP. Leap Year. 0: Not 1: Leap year. This bit can not set by hardware. It should be set or cleared by software.
21:16	R/W	UDF	YEAR. Year. Range from 0~63.
15:12	/	/	/
11:8	R/W	UDF	MONTH. Month. Range from 1~12.
7:5	/	/	/
4:0	R/W	UDF	DAY. Day. Range from 1~31.

NOTE

If the written value is not from 1 to 31 in Day Area, it turns into 31 automatically. Month Area and Year Area are similar to Day Area. The number of days in different month may be different.

3.18.6.6. RTC HH-MM-SS Register

Offset:0x0014			Register Name: RTC_HH_MM_SS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	R/W	0x0	WK_NO. Week number. 000: Monday 001: Tuesday 010: Wednesday 011: Thursday 100: Friday 101: Saturday 110: Sunday 111: /
28:21	/	/	/
20:16	R/W	UDF	HOUR. Range from 0~23

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15:14	/	/	/
13:8	R/W	UDF	MINUTE. Range from 0~59
7:6	/	/	/
5:0	R/W	UDF	SECOND. Range from 0~59

NOTE

If the written value is not from 0 to 59 in Second Area, it turns into 59 automatically. Minute Area and Hour Area are similar to Second Area.

3.18.6.7. Alarm 0 Counter Register (Default Value: 0x0000_0000)

Offset:0x0020			**Register Name: ALARM0_COUNTER_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	ALARM0_COUNTER. Alarm 0 Counter is based on second.

NOTE

If the second is set to 0, it will be 1 second in fact.

3.18.6.8. Alarm 0 Current Value Register

Offset:0x0024			**Register Name: ALARM0_CUR_VLU_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	UDF	ALARM0_CUR_VLU. Check Alarm 0 Counter Current Values.

NOTE

If the second is set to 0, it will be 1 second in fact.

3.18.6.9. Alarm 0 Enable Register (Default Value: 0x0000_0000)

Offset:0x0028			**Register Name: ALARM0_ENABLE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALM_0_EN Alarm 0 Enable. If this bit is set to “1”, the valid bits of **Alarm 0 Counter Register** will down

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			count to zero, and the alarm pending bit will be set to “1”. 0: Disable 1: Enable

3.18.6.10. Alarm 0 IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x002C			Register Name: ALARM0_IRQ_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALARM0_IRQ_EN. Alarm 0 IRQ Enable. 0: Disable 1: Enable

3.18.6.11. Alarm 0 IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x0030			Register Name: ALARM0_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1C	0x0	ALARM0_IRQ_PEND. Alarm 0 IRQ Pending bit. 0: No effect 1: Pending, alarm 0 counter value is reached If alarm 0 irq enable is set to 1, the pending bit will be sent to the interrupt controller.

3.18.6.12. Alarm 1 Week HH-MM-SS Register

Offset:0x0040			Register Name: ALARM1_WK_HH_MM_SS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	UDF	HOUR. Range from 0~23.
15:14	/	/	/
13:8	R/W	UDF	MINUTE. Range from 0~59.
7:6	/	/	/
5:0	R/W	UDF	SECOND. Range from 0~59.

NOTE

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If the written value is not from 0 to 59 in Second Area, it turns into 59 automatically. Minute Area and Hour Area are similar to Second Area.

3.18.6.13. Alarm 1 Enable Register (Default Value: 0x0000_0000)

Offset:0x0044			Register Name: ALARM1_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x0	WK6_ALM1_EN. Week 6 (Sunday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to "1", only when the valid bits of **Alarm 1 Week HH-MM-SS Register** is equal to the bit[20:0] of **RTC HH-MM-SS Register** and the bit[31:29] of **RTC HH-MM-SS Register** is 6, the week 6 alarm irq pending bit will be set to "1".
5	R/W	0x0	WK5_ALM1_EN. Week 5 (Saturday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to "1", only when the valid bits of **Alarm 1 Week HH-MM-SS Register** is equal to the bit[20:0] of **RTC HH-MM-SS Register** and the bit[31:29] of **RTC HH-MM-SS Register** is 5, the week 5 alarm irq pending bit will be set to "1".
4	R/W	0x0	WK4_ALM1_EN. Week 4 (Friday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to "1", only when the valid bits of **Alarm 1 Week HH-MM-SS Register** is equal to the bit[20:0] of **RTC HH-MM-SS Register** and the register bit[31:29] of **RTC HH-MM-SS Register** is 4, the week 4 alarm irq pending bit will be set to "1".
3	R/W	0x0	WK3_ALM1_EN. Week 3 (Thursday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to "1", only when the valid bits of **Alarm 1 Week HH-MM-SS Register** is equal to the bit[20:0] of **RTC HH-MM-SS Register** and the bit[31:29] of **RTC HH-MM-SS Register** is 3, the week 3 alarm irq pending bit will be set to "1".
2	R/W	0x0	WK2_ALM1_EN. Week 2 (Wednesday) Alarm 1 Enable. 0: Disable 1: Enable

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			If this bit is set to “1”, only when the valid bits of **Alarm 1 Week HH-MM-SS Register** is equal to the bit[20:0] of **RTC HH-MM-SS Register** and the bit[31:29] of **RTC HH-MM-SS Register** is 2, the week 2 alarm irq pending bit will be set to “1”.
1	R/W	0x0	WK1_ALM1_EN. Week 1 (Tuesday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to “1”, only when the valid bits of **Alarm 1 Week HH-MM-SS Register** is equal to the bit[20:0] of **RTC HH-MM-SS Register** and the bit[31:29] of **RTC HH-MM-SS Register** is 1, the week 1 alarm irq pending bit will be set to “1”.
0	R/W	0x0	WK0_ALM1_EN. Week 0 (Monday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to “1”, only when the valid bits of **Alarm 1 Week HH-MM-SS Register** is equal to the bit[20:0] of **RTC HH-MM-SS Register** and the bit[31:29] of **RTC HH-MM-SS Register** is 0, the week 0 alarm irq pending bit will be set to “1”.

3.18.6.14. Alarm 1 IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x0048			**Register Name: ALARM1_IRQ_EN**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALARM1_IRQ_EN. Alarm 1 IRQ Enable. 0: Disable 1: Enable

3.18.6.15. Alarm 1 IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x004C			**Register Name: ALARM1_IRQ_STA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1C	0x0	ALARM1_WEEK_IRQ_PEND. Alarm 1 Week (0/1/2/3/4/5/6) IRQ Pending. 0: No effect 1: Pending, week counter value is reached If alarm 1 week irq enable is set to 1, the pending bit will be sent to the interrupt controller.

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3.18.6.16. Alarm Configuration Register (Default Value: 0x0000_0000)

Offset:0x0050			Register Name: ALARM_CONFIG_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	ALARM_WAKEUP. Configuration of alarm wake up output. 0: Disable alarm wake up output 1: Enable alarm wake up output

3.18.6.17. LOSC Output Gating Register (Default Value: 0x0000_0000)

Offset:0x0060			Register Name: LOSC_OUT_GATING_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	LOSC_OUT_GATING. Configuration of LOSC output, and without LOSC output by default. 0: Enable LOSC output gating 1: Disable LOSC output gating

3.18.6.18. General Purpose Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0004 (N=0~7)			Register Name: GP_DATA_REGN
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	GP_DATA. Data [31:0].

NOTE

General purpose register 0~7 value can be stored if the RTC-VIO is larger than 1.0V.

3.18.6.19. DCXO Control Register (Default Value: 0x083F_10F2)

Offset:0x0160			Register Name: DCXO_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CLK_REQ_ENB. 0: Enable DCXO wake up function 1: Disable DCXO wake up function
30:28	/	/	/
27:24	R/W	0x8	DCXO_ICTRL DCXO current control value
23	/	/	/

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22:16	R/W	0x3F	DCXO_TRIM DCXO cap array value cap cell is 55fF
15:13	/	/	/
12:8	R/W	0x10	DCXO_BG DCXO bandgap output voltage
7	R/W	0x1	DCXO_LDO_INRUSHB DCXO LDO driving capacity signal, active high
6	R/W	0x1	XTAL_MODE Xtal mode enable signal, active high 0: for external clk input mode. 1: for normal mode.
5:4	R/W	0x3	DCXO_RFCLK_ENHANCE DCXO rfclk enhance Enhance driving capacity of output OUT_RF_REFCLK, 0x0 for 5pF, 0x1 for 10pF, 0x2 for 15pF, 0x3 for 20pF
3	U	UDF	OSC_CLK_SRC_SEL.(Pad select) High frequency clock source select. 0: XO24M 1: DCXO
2	/	/	/
1	R/W	0x1	DCXO_EN DCXO enable. 1: Enable 0: Disable
0	/	/	/

3.18.6.20. Calibration Control Register (Default Value: 0x0000_0003)

Offset:0x0164			**Register Name: CALI_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	WAKEUP_DCXO_EN Wake up DCXO circuit enable.
30:15	/	/	/
16	R/W	0x0	WAKEUP_READY_SLEEP_MODE Calibration wake up ready sleep mode 0: Disable 1: Enable
15:12	R/W	0x0	TIMER FOR READY SLEEP Total timer for ready sleep 0000: 15s 0001: 30s 0010: 45s 0011: 60s

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			0100: 90s 0101: 120s 0110: 150s Others: /
11:8	R/W	0x0	WAKEUP_CNT FOR READY SLEEP Wake up counter for ready sleep 0000: 250ms 0001: 500ms 0010: 750ms 0011: 1s 0100: 1.25s 0101: 1.5s 0110: 1.75s 0111: 2s 1000: 2.25s 1001: 2.5s 1010: 2.75s 1011: 3s 1100: 3.25s 1101: 3.5s 1110: 3.75s 1111: 4s
7:4	R/W	0x0	WAKEUP_CNT FOR SLEEP Wake up counter for sleep 0000: 250ms 0001: 500ms 0010: 1s 0011: 2s 0100: 3s 0101: 4s 0110: 5s 0111: 6s 1000: 7s 1001: 8s 1010: 9s 1011: 10s 1100: 11s 1101: 12s 1110: 30s 1111: 60s
3:0	R/W	0x3	WAIT DCXO SEL Select for DCXO active after DCXO enable 0000:1ms 0001:2ms 0010:3ms

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			0011:4ms ... 1111: 16ms

3.18.6.21. GPL Hold Output Register (Default Value: 0x0000_0000)

Offset:0x0180			Register Name: GPL_HOLD_OUTPUT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10	R/W	0x0	GPL10_HOLD_OUTPUT. Hold the output of GPIOL10 when the power of system is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
9	R/W	0x0	GPL9_HOLD_OUTPUT. Hold the output of GPIOL9 when the power of system is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
8	R/W	0x0	GPL8_HOLD_OUTPUT. Hold the output of GPIOL8 when the power of system is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
7	R/W	0x0	GPL7_HOLD_OUTPUT. Hold the output of GPIOL7 when the power of system is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
6	R/W	0x0	GPL6_HOLD_OUTPUT. Hold the output of GPIOL6 when the power of system is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
5	R/W	0x0	GPL5_HOLD_OUTPUT. Hold the output of GPIOL5 when the power of system is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable

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			1: Hold enable
4	R/W	0x0	GPL4_HOLD_OUTPUT. Hold the output of GPIOL4 when the power of system is changing. The output must be low level (0) or high level (1) or High-Z; any other output may not hold on. 0: Hold disable 1: Hold enable
3	R/W	0x0	GPL3_HOLD_OUTPUT. Hold the output of GPIOL3 when the power of system is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
2	R/W	0x0	GPL2_HOLD_OUTPUT. Hold the output of GPIOL2 when the power of system is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
1	R/W	0x0	GPL1_HOLD_OUTPUT. Hold the output of GPIOL1 when the power of system is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
0	R/W	0x0	GPL0_HOLD_OUTPUT. Hold the output of GPIOL0 when the power of system is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable

3.18.6.22. GPM Hold Output Register (Default Value: 0x0000_0000)

Offset:0x0184			**Register Name: GPM_HOLD_OUTPUT_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/W	0x0	GPM4_HOLD_OUTPUT. Hold the output of GPIOL4 when system's power is changing. The outputs must be low level (0) or high level (1) or High-Z; any other output may not hold on. 0: Hold disable 1: Hold enable

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3	R/W	0x0	GPM3_HOLD_OUTPUT. Hold the output of GPIOL3 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
2	R/W	0x0	GPM2_HOLD_OUTPUT. Hold the output of GPIOL2 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
1	R/W	0x0	GPM1_HOLD_OUTPUT. Hold the output of GPIOL1 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
0	R/W	0x0	GPM0_HOLD_OUTPUT. Hold the output of GPIOL0 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable

3.18.6.23. RTC Power Mode Select Register (Default Value: 0x0000_0001)

Offset:0x0188			Register Name: RTC_PWR_MODE_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x1	RTC_POW_MOD_SELECT. VCC-RTC POWER MODE SELECT. 0: 3.3V 1:1.8V

3.18.6.24. RTC-VIO Regulation Register (Default Value: 0x0000_0004)

Offset:0x0190			Register Name: RTC-VIO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x4	RTC-VIO_REGU. These bits are useful for regulating the RTC-VIO from 0.6V to 1.3V. 000: 1.0V

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			001: 0.6V 010: 0.7V 011: 0.8V 100: 0.9V 101: 1.1V 110: 1.2V 111: 1.3V

3.18.6.25. Boot CPU Hot Plug Flag Register (Default Value: 0x0000_0000)

Offset:0x01B8			Register Name: BOOT_CPU_HP_FLAG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	Boot CPU software flag when acting from hot plug.

3.18.6.26. CPU Software Entry Register (Default Value: 0x0000_0000)

Offset:0x01BC			Register Name: CPU_SOFT_ENT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	Boot CPU software entry register when acting from hot plug or Non-boot CPU software entry register.

3.18.6.27. IC Characteristic Register (Default Value: 0x0000_0000)

Offset:0x01F0			Register Name: IC_CHARA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	IC_CHARA. Key Field.
15:0	R/W	0x0	ID_DATA.

3.18.6.28. Super Standby Flag Register (Default Value: 0x0000_0000)

Offset:0x01F8			Register Name: SUP_STAN_FLAG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	SUP_STANDBY_FLAG. Key Field. Any value can be written and read back in the key field, but if the values are not appropriate, the lower 16 bits will not change in this register. Only fellow the appropriate process, the super standby flag can be written in the lower 16 bits. Refer to Description and Diagram.
15:0	R/W	0x0	SUP_STANBY_FLAG_DATA. Refer to Description and Diagram

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NOTE

When system is turned on, the low 16 bits in the Super Standby Flag Register should be 0x0. If software programmer wants to write correct super standby flag ID in low 16 bits, the high 16 bits should be written 0x16AA at first. Then, software programmer must write 0xAA16XXXX in the Super Standby Flag Register, the 'XXXX' means the correct super standby flag ID.

3.18.6.29. CPU Software Entry Register1 (Default Value: 0x0000_0000)

Offset:0x01FC			Register Name: CPU_SOFT_ENT_REG1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CPU software entry register when acting from super standby.

3.18.6.30. Crypto Configuration Register (Default Value: 0x0000_0000)

Offset:0x0210			Register Name: CRY_CONFIG_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	KEY_FIELD Key Field

3.18.6.31. Crypto Key Register (Default Value: 0x0000_0000)

Offset:0x0214			Register Name: CRY_KEY_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CRY_KEY Crypto Key

3.18.6.32. Crypto Enable Register (Default Value: 0x0000_0000)

Offset:0x0218			Register Name: CRY_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	CRY_EN Crypto Enable

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3.19. PSI

3.19.1. Overview

PSI（Peripheral System Interconnect）is a peripheral bus interconnect device based on AHB and APB protocol, which supports 16 AHB master and 16 slave bus. The type of slave bus can be AHB bus or APB bus. Each bus supports 64 slave devices.

3.19.2. Block Diagram

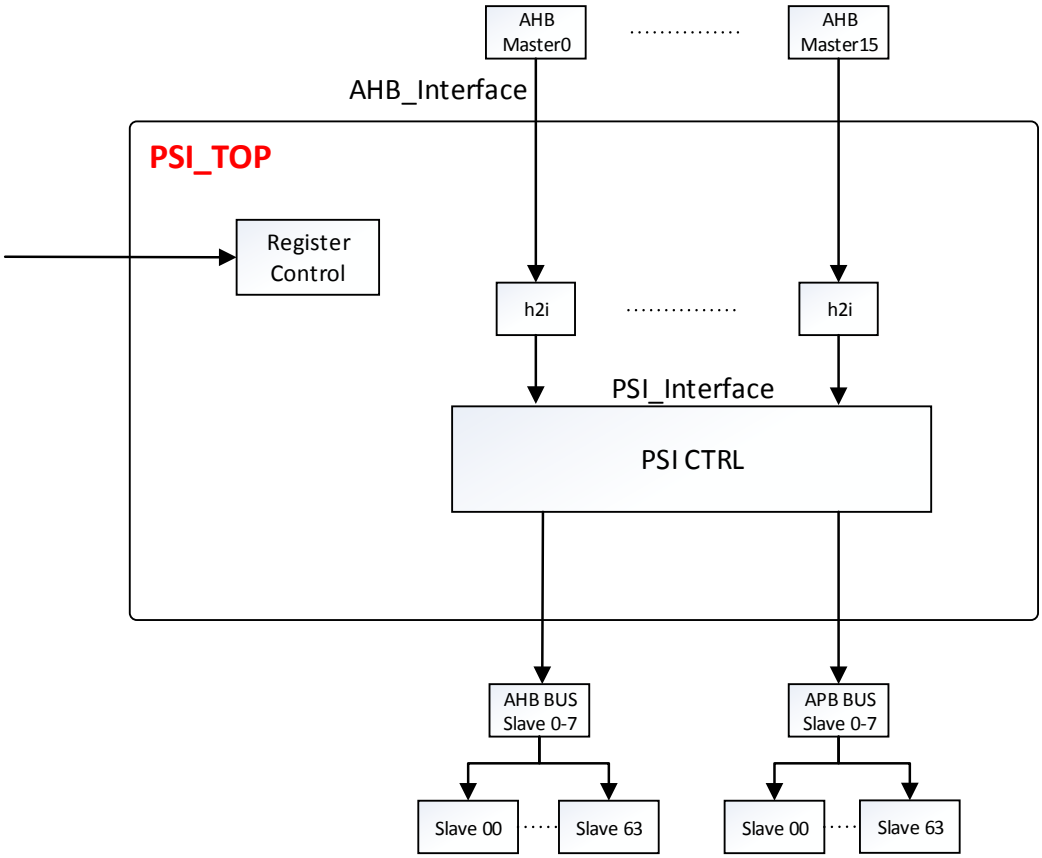


Figure 3-60. PSI Block Diagram

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3.20. ATE(Audio Codec, TVE, EPHY) controller

3.20.1. Overview

The ATE Controller consists of Audio Codec, TVE and EPHY. It is used to configure the system resources of Auido Codec, TVE and EPHY module.

3.20.2. Register List

Register Name	Address	Description
ATE_SYS_CONTROL	0002h	ATE System Control Register
ATE_SYS_IRQ_ENABLE	0004h	ATE System IRQ Enable Register
ATE_SYS_IRQ_STATUS	0006h	ATE System IRQ Status Register
ATE_SYS_CLK_CTL	0008h	ATE System Clock Control Register
ATE_SYS_DLDO_OSC_CTL	000Ah	ATE System DLDO and OSC Control Register
ATE_SYS_PLL_CTL0	000Ch	ATE System PLL Control 0 Register
ATE_SYS_AUDIO_CTL0	0010h	ATE System AUDIO Control 0 Register
ATE_SYS_AUDIO_CTL1	0012h	ATE System AUDIO Control 1 Register
ATE_SYS_EPHY_CTL0	0014h	ATE System EPHY Control 0 Register
ATE_SYS_EPHY_CTL1	0016h	ATE System EPHY Control 1 Register
ATE_SYS_TVE_CTL0	0018h	ATE System TVE Control 0 Register
ATE_SYS_TVE_CTL1	001Ah	ATE System TVE Control 1 Register

3.20.3. Register Description

3.20.3.1. ATE System Control Register(Default Value: 0x0000)

Address: 0x0002			Register Name: ATE_SYS_CONTROL
Bit	**Read/Write**	**Default/Hex**	**Description**
15:1	/	/	/
0	R/W	0x0	CHIP_RESET 0 : reset all register to their default state. 1 : reset invalid

3.20.3.2. ATE System IRQ Enable Register(Default Value: 0x0000)

Address: 0x0004			Register Name: ATE_SYS_IRQ_ENABLE
Bit	**Read/Write**	**Default/Hex**	**Description**

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15	R/W	0x0	INTB_OUTPUT_ENABLE 0 : INTB pin disable 1 : INTB pin output
14	R/W	0x0	INTB_OUTPUT_CFG 0 : Default high level, any irq status with irq enable is '1',set INBT output low level 1 : Default low level, any irq status with irq enable is '1' ,set INBT output high level
13	/	/	/
12	R/W	0x0	RTC_IRQ_ENABLE 0 : IRQ is disable 1 : IRQ is enable
11:9	/	/	/
8	R/W	0x0	EPHY_IRQ_ENABLE 0 : IRQ is disable 1 : IRQ is enable
7:5	/	/	/
4	R/W	0x0	TVE_IRQ_ENABLE 0 : IRQ is disable 1 : IRQ is enable
3:1	/	/	/
0	/	/	/

3.20.3.3. ATE System IRQ Status Register(Default Value: 0x0000)

Address: 0x0006			**Register Name: ATE_SYS_IRQ_STATUS**
Bit	**Read/Write**	**Default/Hex**	**Description**
15:13	/	/	/
12	R	0x0	RTC_IRQ_ STATUS 0 : IRQ is waiting 1 : IRQ is pending
11:9	/	/	/
8	R	0x0	EPHY_IRQ_ STATUS 0 : IRQ is waiting 1 : IRQ is pending
7:5	/	/	/
4	R	0x0	TVE_IRQ_STATUS 0 : IRQ is waiting 1 : IRQ is pending
3:1	/	/	/
0	/	/	/

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3.20.3.4. ATE System Clock Control Register(Default Value: 0x0007)

Address: 0x0008			Register Name: ATE_SYS_CLK_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
15:6	/	/	/
5	R/W	0x0	Reserved
4	R/W	0x0	SYS_CLK_SEL 0 : SYS_CLK from CKI_24M_PIN 1 : SYS_CLK from PLL_CKO_DIV
3	/	/	/
2	R/W	0x1	CKI_24M_ENABLE 0 : CKI_24M PIN disable 1 : CKI_24M PIN input
1	R/W	0x1	Reserved
0	R/W	0x1	Reserved

3.20.3.5. ATE System DLDO OSC Control Register(Default Value: 0xC80C)

Address: 0x000A			Register Name: ATE_SYS_DLDO_OSC_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
15	R/W	0x1	DLDOEN Digital LDO enable 0: disable 1: enable
14:12	R/W	0x4	DLDOVOL DLDO Voltage select 000: 0.825V 001: 0.880V 010: 0.943V 011: 1.015V 100: 1.1V 101: 1.2V 110: 1.32V 111: 1.467V
11	R/W	0x1	Reserved
10	R/W	0x0	Reserved
9:4	R/W	0x0	/
3	R/W	0x1	Reserved
2:0	R/W	0x4	/

3.20.3.6. ATE System PLL Control0 Register(Default Value: 0x0200)

Address: 0x000C	Register Name: ATE_SYS_PLL_CTL0

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Bit	Read/Write	Default/Hex	Description
15	R/W	0x0	PLL_ENABLE 0: disable 1: enable The PLL Output cko = (ccir_clk/M)*N The PLL Output cko_div = The PLL Output / PLL_POST_DIV
14	R/W	0x0	PLL_BIAS_EN Mbias enable 0: disable 1: enable
13:12	/	/	/
11	R/W	0x0	PLL_LDO1_EN On-chip LDO1 enable 0: disable 1: enable
10	R/W	0x0	PLL_LDO_EN On-chip LDO enable 0: disable 1: enable
9	R/W	0x1	PLL_POST_DIV PLL post div factor 0: div 8 1: div 9
8:4	/	/	/
3:0	R/W	0x0	PLL_PRE_DIV_M PLL pre-divider control bit

3.20.3.7. ATE System Audio Control0 Register(Default Value: 0x0000)

Address: 0x0010			Register Name: ATE_SYS_AUDIO_CTL0
Bit	**Read/Write**	**Default/Hex**	**Description**
15:2	/	/	/
1	R/W	0x0	AC_MCLK_GATING 0 : Clock is gating 1 : Clock is enable
0	R/W	0x0	AC_RESET_INVALID 0 : Reset 1 : Reset Invalid

3.20.3.8. ATE System Audio Control1 Register(Default Value: 0x0000)

Address: 0x0012			Register Name: ATE_SYS_AUDIO_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**

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15:1	/	/	/
0	R/W	0x0	AC_AIF_IO_EN 0 : all AIF io is disable 1 : AIF

3.20.3.9. ATE System EPHY Control0 Register(Default Value: 0x0000)

Address: 0x0014			Register Name: ATE_SYS_EPHY_CTL0
Bit	**Read/Write**	**Default/Hex**	**Description**
15:4	/	/	/
3:2	/	/	/
1	R/W	0x0	EPHY_SYSCLK_GATING 0 : Clock is OFF 1 : Clock is ON
0	R/W	0x0	EPHY_RESET_INVALID 0 : Reset 1 : Reset Invalid

3.20.3.10. ATE System EPHY Control1 Register(Default Value: 0x0000)

Address: 0x0016			Register Name: ATE_SYS_EPHY_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
15	R/W	0x0	Reserved
14	R/W	0x0	Reserved
13:1	/	/	/
3	R/W	0x0	E_DPX_LED_IO_EN 0 : E_DPX_LED io is disable 1 : E_DPX_LED io is enable
2	R/W	0x0	E_SPD_LED_IO_EN 0 : E_SPD_LED io is disable 1 : E_SPD_LED io is enable
1	R/W	0x0	E_LNK_LED_IO_EN 0 : E_LNK_LED io is disable 1 : E_LNK_LED io is enable
0	R/W	0x0	EPHY_MII_IO_EN 0 : all MII io is disable,include FE_TEST_MDI and FE_TEST_MDO 1 : MII

3.20.3.11. ATE System TVE Control0 Register(Default Value: 0x0000)

Address: 0x0018			Register Name: ATE_SYS_TVE_CTL0
Bit	**Read/Write**	**Default/Hex**	**Description**

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15:4	/	/	/
3	R/W	0x0	TVE_SYSCLK_GATING 0 : Clock is gating 1 : Clock is enable
2	R/W	0x0	TVE_SCLK_GATING(PLL_216M) 0 : Clock is gating 1 : Clock is enable
1	R/W	0x0	TVE_DCLK_GATING(CCIR_CLK) 0 : Clock is gating 1 : Clock is enable
0	R/W	0x0	TVE_RESET_INVALID 0 : Reset 1 : Reset Invalid

3.20.3.12. ATE System TVE Control1 Register(Default Value: 0x0000)

Address: 0x001A			**Register Name: ATE_SYS_TVE_CTL1**
Bit	**Read/Write**	**Default/Hex**	**Description**
15:2	/	/	/
1	R/W	0x0	TVE_CCIR_CLK_IO_EN 0 : IO ccir_clk is disable 1 : IO ccir_clk is enable
0	R/W	0x0	TVE_CCIR_SYNC_DATA_IO_EN 0 : IO ccir_hs,ccir_vs,ccir_data is disable 1 : IO ccir_hs,ccir_vs,ccir_data is enable

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3.21. Port Controller(CPUX-PORT)

3.21.1. Overview

The Port Controller can be configured with multi-functional input/output pins. All these ports can be configured as GPIO only if multiplexed functions not used. The total 3 group external PIO interrupt sources are supported and interrupt mode can be configured by software.

The features of Port Controller are as follows:

- 5 ports(PC,PD,PF,PG,PH)
- Software control for each signal pin
- GPIO peripheral can produce interrupt
- Pull-up/Pull-down/no-Pull register control
- Control the direction of every signal
- 4 drive strengths in each operating mode
- Configurable interrupt edges

3.21.2. Block Diagram

The block diagram of port controller is shown in Figure 3-61.

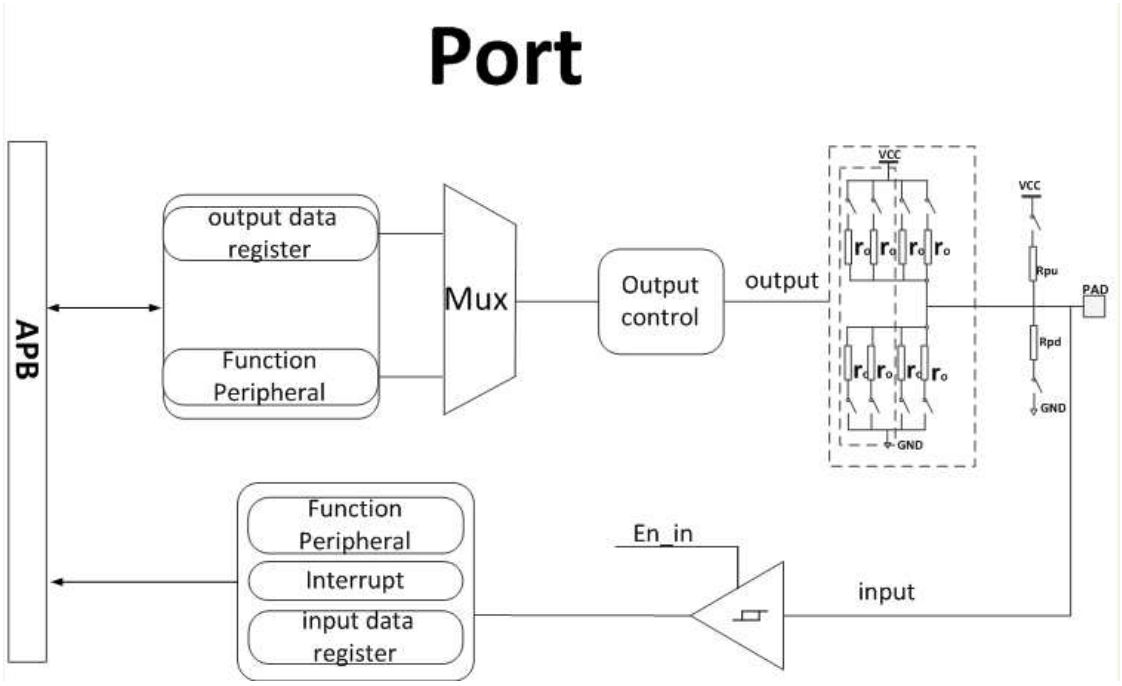


Figure 3-61. Port Controller Block Diagram

Port controller consists of digital part(GPIO, external interface) and IO analog part(output buffer, dual pull down, pad,

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etc). Digital part can select output interface by MUX switch; analog part can configure pull up/down, buffer strength.

When executing GPIO read state, the port controller reads the current level of pin into internal register bus. When not executing GPIO read state, external pin and internal register bus is off-status, that is high-impedance.

3.21.3. Operations and Functional Descriptions

3.21.3.1. Multi-function Port Table

H6 V200 includes 77 multi-functional input/output port pins in CPUX.There are 5 ports as listed below:

Table 3-13. Multi-function Port Table

Port Name	Number of Pins	Input Driver	Output Driver	Multiplex Pins	Power
PC	17	Schmitt	CMOS	NAND/SDC/SPI	1.8/3.3V
PD	27	Schmitt	CMOS	LCD/TS/RGMII/CSI/DMIC/TWI/UART/ JTAG/PWM	1.8/2.5/3.3V
PF	7	Schmitt	CMOS	SDC/UART/JTAG	3.3V
PG	15	Schmitt	CMOS	SDC/UART/PCM/SCR	1.8/3.3V
PH	11	Schmitt	CMOS	UART/PCM/OWA/SCR/TWI/CIR/SPI	3.3V

3.21.3.2. Port Functiom

Port Controller supports 5 GPIOs, every GPIO can configure as Input,Output,Function Peripheral,IO disable or Interrupt function. The configuration instruction of every function is as follows.

Table 3-14. Port Function

	Function	Buffer Strength	Pull Up	Pull Down
Input	GPIO/Multiplexing Input	/	X	X
Output	GPIO/Multiplexing Output	Y	X	X
Disable	Pull Up	/	Y	N
	Pull Down	/	N	Y
Interrupt	Trigger	/	X	X

/ : non-configure, configuration is invalid

Y : configure

X : Select configuration according to actual situation

N : Forbid to configure

3.21.3.3. Pull up/down Logic

Each IO pin can configure the internal pull-up/down function or high-impedance.

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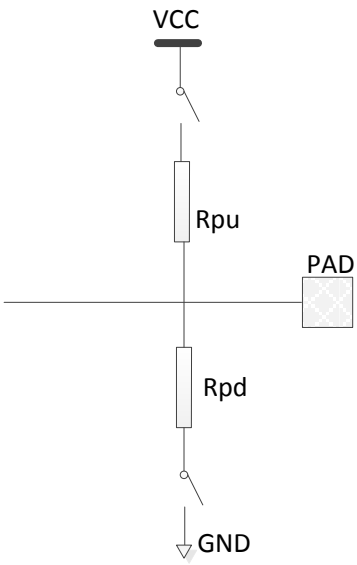


Figure 3-62. Pull up/down Logic

High-impedance, the output is float state, all buffer is off, the level is decided by external high/low level. When high-impedance, software configures the switch on Rpu and Rpd as off ,and the multiplexing function of IO is set as IO disable or input by software.

Pull-up, an uncertain signal is pulled high by a resistance, the resistance has current-limiting function. When pulling up, the switch on Rpu is breakover by software configuration, IO is pulled up to VCC by Rpu.

Pull-down, an uncertain signal is pulled low by a resistance. When pulling down, the switch on Rpd is breakover by software configuration, IO is pulled down to GND by Rpd.

The pull-up/down of each IO is weak pull-up/down, the resistance is about 100kΩ.

The setting of pull-down,pull-up,high-impledance is decided by external circuit.

3.21.3.4. Buffer Strength

Each IO can be set as different buffer strength.The IO buffer diagram is as follows.

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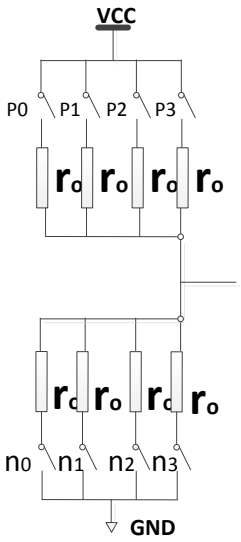


Figure 3-63. IO Buffer Strength Diagram

When output high level, the n0,n1,n2,n3 of NMOS is off, the p0,p1,p2,p3 of PMOS is on. When buffer strength is set to 0(buffer strength is weakest), only p0 is on, the output impedance is maximum ,the impedance value is r0. When buffer strength is set to 1, only p0 and p1 is on, the output impedance is equivalent to two r0 in parallel, the impedance value is r0/2.When buffer strength is 2, only p0,p1 and p2 is on, the output impedance is equivalent to three r0 in parallel, the impedance value is r0/3.When buffer strength is 3, p0,p1,p2 and p3 is on, the output impedance is equivalent to four r0 in parallel, the impedance value is r0/4.

When output low level, the p0,p1,p2,p3 of PMOS is off, the n0,n1,n2,n3 of NMOS is on. When buffer strength is set to 0(buffer strength is weakest), only n0 is on, the output impedance is maximum ,the impedance value is r0. When buffer strength is set to 1, only n0 and n1 is on, the output impedance is equivalent to two r0 in parallel, the impedance value is r0/2. When buffer strength is 2, only n0,n1 and n2 is on, the output impedance is equivalent to three r0 in parallel, the impedance value is r0/3. When buffer strength is 3, n0,n1,n2 and n3 is on, the output impedance is equivalent to four r0 in parallel, the impedance value is r0/4.

When GPIO is set to input or interrupt function, between output driver circuit and port is unconnected, driver configuration is invalid.

3.21.3.5. Interrupt

Each group IO has independent interrupt number.IO within group uses one interrupt number, when one IO generates interrupt, Port Controller sent interrupt request to GIC. External Interrupt Status Register is used to query which IO generates interrupt.

Interrupt trigger of GPIO supports the following trigger types.

- Positive Edge : When low level changes to high level, the interrupt will generate. No matter how long high level keeps, the interrupt generates only once.
- Negative Edge: When high level changes to low level, the interrupt will generate. No matter how long low level keeps, the interrupt generates only once.

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- High Level : Just keep high level and the interrupt will always generate.
- Low Level : Just keep low level and the interrupt will always generate.
- Double Edge : Positive and negative edge.

External Interrupt Configure Register is used to configure trigger type.

GPIO interrupt supports hardware debounce function by setting External Interrupt Debounce Register. Sample trigger signal using lower sample clock, to reach the debounce effect because of the dither frequency of signal is higher than sample frequency.

Set sample clock source by PIO_INT_CLK_SELECT and prescale factor by DEB_CLK_PRE_SCALE.

3.21.4. Register List

Module Name	Base Address
PIO	0x0300B000

Register Name	Offset	Description
Pn_CFG0	n*0x0024+0x00	Port n Configure Register 0 (n =2,3,5,6,7)
Pn_CFG1	n*0x0024+0x04	Port n Configure Register 1 (n =2,3,5,6,7)
Pn_CFG2	n*0x0024+0x08	Port n Configure Register 2 (n =2,3,5,6,7)
Pn_CFG3	n*0x0024+0x0C	Port n Configure Register 3 (n =2,3,5,6,7)
Pn_DAT	n*0x0024+0x10	Port n Data Register (n =2,3,5,6,7)
Pn_DRV0	n*0x0024+0x14	Port n Multi-Driving Register 0 (n =2,3,5,6,7)
Pn_DRV1	n*0x0024+0x18	Port n Multi-Driving Register 1 (n =2,3,5,6,7)
Pn_PUL0	n*0x0024+0x1C	Port n Pull Register 0 (n =2,3,5,6,7)
Pn_PUL1	n*0x0024+0x20	Port n Pull Register 1 (n =2,3,5,6,7)
Pn_INT_CFG0	0x200+n*0x20+0x00	PIO Interrupt Configure Register 0(n =5,6,7)
Pn _INT_CFG1	0x200+n*0x20+0x04	PIO Interrupt Configure Register 1(n =5,6,7)
Pn _INT_CFG2	0x200+n*0x20+0x08	PIO Interrupt Configure Register 2(n =5,6,7)
Pn _INT_CFG3	0x200+n*0x20+0x0C	PIO Interrupt Configure Register 3(n =5,6,7)
Pn _INT_CTL	0x200+n*0x20+0x10	PIO Interrupt Control Register(n =5,6,7)
Pn _INT_STA	0x200+n*0x20+0x14	PIO Interrupt Status Register(n =5,6,7)
Pn _INT_DEB	0x200+n*0x20+0x18	PIO Interrupt Debounce Register(n =5,6,7)
PIO_POW_MOD_SEL	0x0340	PIO Group Withstand Voltage Mode Select Register
PIO_POW_Val	0x0348	PIO Group Power Value Register

3.21.5. Register Description

3.21.5.1. PC Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x0048			Register Name: PC_CFG0
Bit	Read/Write	Default/Hex	Description

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31	/	/	/	
30:28	R/W	0x7	PC7_SELECT 000:Input 010:NAND_DQ1 100:SPI0_WP 110:Reserved	001:Output 011:SDC2_D1 101:Reserved 111:IO Disable
27	/	/	/	
26:24	R/W	0x7	PC6_SELECT 000:Input 010:NAND_DQ0 100:SPI0_HOLD 110:Reserved	001:Output 011:SDC2_D0 101:Reserved 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PC5_SELECT 000:Input 010:NAND_RB0 100:SPI0_CS 110:Reserved	001:Output 011:SDC2_CMD 101:Reserved 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PC4_SELECT 000:Input 010:NAND_RE 100:Reserved 110:Reserved	001:Output 011:SDC2_CLK 101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PC3_SELECT 000:Input 010:NAND_CE0 100:SPI0_MISO 110:Reserved	001:Output 011:Reserved 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PC2_SELECT 000:Input 010:NAND_CLE 100:SPI0_MOSI 110:Reserved	001:Output 011:Reserved 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PC1_SELECT 000:Input 010:NAND_ALE 100:Reserved 110:Reserved	001:Output 011:SDC2_DS 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PC0_SELECT 000:Input	001:Output

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			010:NAND_WE	011:Reserved
			100:SPI0_CLK	101:Reserved
			110:Reserved	111:IO Disable

3.21.5.2. PC Configure Register 1 (Default Value: 0x7777_7777)

Offset: 0x004C			Register Name: PC_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PC15_SELECT 000:Input 010:NAND_CE1 100:Reserved 110:Reserved	 001:Output 011:Reserved 101:Reserved 111:IO Disable
27	/	/	/	
26:24	R/W	0x7	PC14_SELECT 000:Input 010:NAND_DQS 100:Reserved 110:Reserved	 001:Output 011:SDC2_RST 101:Reserved 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PC13_SELECT 000:Input 010:NAND_DQ7 100:Reserved 110:Reserved	 001:Output 011:SDC2_D7 101:Reserved 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PC12_SELECT 000:Input 010:NAND_DQ6 100:Reserved 110:Reserved	 001:Output 011:SDC2_D6 101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PC11_SELECT 000:Input 010:NAND_DQ5 100:Reserved 110:Reserved	 001:Output 011:SDC2_D5 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PC10_SELECT 000:Input 010:NAND_DQ4 100:Reserved 110:Reserved	 001:Output 011:SDC2_D4 101:Reserved 111:IO Disable

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7	/	/	/
6:4	R/W	0x7	PC9_SELECT 000:Input 001:Output 010:NAND_DQ3 011:SDC2_D3 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PC8_SELECT 000:Input 001:Output 010:NAND_DQ2 011:SDC2_D2 100:Reserved 101:Reserved 110:Reserved 111:IO Disable

3.21.5.3. PC Configure Register 2 (Default Value: 0x0000_0007)

Offset: 0x0050			Register Name: PC_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x7	PC16_SELECT 000:Input 001:Output 010:NAND_RB1 011:Reserved 100:Reserved 101:Reserved 110:Reserved 111:IO Disable

3.21.5.4. PC Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: PC_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

3.21.5.5. PC Data Register (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: PC_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16:0	R/W	0x0	PC_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

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3.21.5.6. PC Multi-Driving Register 0 (Default Value: 0x5555_5555)

Offset: 0x005C			Register Name: PC_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x1	PC15_DRV PC15 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
29:28	R/W	0x1	PC14_DRV PC14 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
27:26	R/W	0x1	PC13_DRV PC13 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
25:24	R/W	0x1	PC12_DRV PC12 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
23:22	R/W	0x1	PC11_DRV PC11 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
21:20	R/W	0x1	PC10_DRV PC10 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
19:18	R/W	0x1	PC9_DRV PC9 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PC8_DRV PC8 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PC7_DRV PC7 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PC6_DRV PC6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PC5_DRV

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			PC5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PC4_DRV PC4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PC3_DRV PC3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PC2_DRV PC2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PC1_DRV PC1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PC0_DRV PC0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.21.5.7. PC Multi-Driving Register 1 (Default Value: 0x0000_0001)

Offset: 0x0060			Register Name: PC_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x1	PC16_DRV PC16 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.21.5.8. PC Pull Register 0 (Default Value: 0x4000_0440)

Offset: 0x0064			Register Name: PC_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x1	PC15_PULL PC15 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
29:28	R/W	0x0	PC14_PULL

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			PC14 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
27:26	R/W	0x0	PC13_PULL PC13 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
25:24	R/W	0x0	PC12_PULL PC12 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
23:22	R/W	0x0	PC11_PULL PC11 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
21:20	R/W	0x0	PC10_PULL PC10 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
19:18	R/W	0x0	PC9_PULL PC9 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
17:16	R/W	0x0	PC8_PULL PC8 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
15:14	R/W	0x0	PC7_PULL PC7 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
13:12	R/W	0x0	PC6_PULL PC6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x1	PC5_PULL PC5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PC4_PULL PC4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x1	PC3_PULL PC3 Pull-up/down Select

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			00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PC2_PULL PC2 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PC1_PULL PC Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PC0_PULL PC0 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.21.5.9. PC Pull Register 1 (Default Value: 0x0000_0001)

Offset: 0x0068			Register Name: PC_PULL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x1	PC16_PULL PC16 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.21.5.10. PD Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x006C			Register Name: PD_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PD7_SELECT 000:Input 001:Output 010:LCD0_D11 011:TS0_D3 100:CSI_D3 101:RGMII_TXD3/RMII_NULL 110:Reserved 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PD6_SELECT 000:Input 001:Output 010:LCD0_D10 011:TS0_D2 100:CSI_D2 101:RGMII_NULL/RMII_RXER 110:Reserved 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PD5_SELECT

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			000:Input 010:LCD0_D7 100:CSI_D1 110:Reserved	001:Output 011:TS0_D1 101:RGMII_RXCTL/RMII_CRS_DV 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PD4_SELECT 000:Input 010:LCD0_D6 100:CSI_D0 110:Reserved	 001:Output 011:TS0_D0 101:RGMII_RXCK/RMII_NULL 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PD3_SELECT 000:Input 010:LCD0_D5 100:CSI_VSYNC 110:Reserved	 001:Output 011:TS0_DVLD 101:RGMII_RXD0/RMII_RXD0 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PD2_SELECT 000:Input 010:LCD0_D4 100:CSI_HSYNC 110:Reserved	 001:Output 011:TS0_SYNC 101:RGMII_RXD1/RMII_RXD1 111:IO Disable
7:0	/	/	/	
6:4	R/W	0x7	PD1_SELECT 000:Input 010:LCD0_D3 100:CSI_MCLK 110:Reserved	 001:Output 011:TS0_ERR 101:RGMII_RXD2/RMII_NULL 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PD0_SELECT 000:Input 010:LCD0_D2 100:CSI_PCLK 110:Reserved	 001:Output 011:TS0_CLK 101:RGMII_RXD3/RMII_NULL 111:IO Disable

3.21.5.11. PD Configure Register 1 (Default Value: 0x7777_7777)

Offset: 0x0070			Register Name: PD_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PD15_SELECT 000:Input 010:LCD0_D21 100:DMIC_DATA0	 001:Output 011:TS1_DVLD 101:CSI_D9

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			110:Reserved	111:IO Disable
27	/	/	/	
26:24	R/W	0x7	PD14_SELECT 000:Input 010:LCD0_D20 100:DMIC_CLK 110:Reserved	001:Output 011:TS1_SYNC 101:CSI_D8 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PD13_SELECT 000:Input 010:LCD0_D19 100:CSI_SDA 110:Reserved	001:Output 011:TS1_ERR 101:RGMII_CLKIN/RMII_NULL 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PD12_SELECT 000:Input 010:LCD0_D18 100:CSI_SCK 110:Reserved	001:Output 011:TS1_CLK 101:RGMII_TXCTL/RMII_TXEN 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PD11_SELECT 000:Input 010:LCD0_D15 100:CSI_D7 110:Reserved	001:Output 011:TS0_D7 101:RGMII_TXCK/RMII_TXCK 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PD10_SELECT 000:Input 010:LCD0_D14 100:CSI_D6 110:Reserved	001:Output 011:TS0_D6 101:RGMII_TXD0/RMII_TXD0 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PD9_SELECT 000:Input 010:LCD0_D13 100:CSI_D5 110:Reserved	001:Output 011:TS0_D5 101:RGMII_TXD1/RMII_TXD1 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PD8_SELECT 000:Input 010:LCD0_D12 100:CSI_D4 110:Reserved	001:Output 011:TS0_D4 101:RGMII_TXD2/RMII_NULL 111:IO Disable

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3.21.5.12. PD Configure Register 2 (Default Value: 0x7777_7777)

Offset: 0x0074			Register Name: PD_CFG2	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PD23_SELECT 000:Input 010:TWI2_SCK 100:UART3_TX 110:Reserved	 001:Output 011:TS3_ERR 101:JTAG_MS 111:IO Disable
27	/	/	/	
26:24	R/W	0x7	PD22_SELECT 000:Input 010:PWM0 100:UART2_CTS 110:Reserved	 001:Output 011:TS3_CLK 101:Reserved 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PD21_SELECT 000:Input 010:LCD0_VSYNC 100:UART2_RTS 110:Reserved	 001:Output 011:TS2_D0 101:Reserved 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PD20_SELECT 000:Input 010:LCD0_HSYNC 100:UART2_RX 110:Reserved	 001:Output 011:TS2_DVLD 101:MDIO 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PD19_SELECT 000:Input 010:LCD0_DE 100:UART2_TX 110:Reserved	 001:Output 011:TS2_SYNC 101:MDC 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PD18_SELECT 000:Input 010:LCD0_CLK 100:DMIC_DATA3 110:Reserved	 001:Output 011:TS2_ERR 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PD17_SELECT 000:Input 010:LCD0_D23 100:DMIC_DATA2	 001:Output 011:TS2_CLK 101:Reserved

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			110:Reserved	111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PD16_SELECT 000:Input 010:LCD0_D22 100:DMIC_DATA1 110:Reserved	001:Output 011:TS1_D0 101:Reserved 111:IO Disable

3.21.5.13. PD Configure Register 3 (Default Value: 0x0000_0777)

Offset: 0x0078			Register Name: PD_CFG3	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:11	/	/	/	
10:8	R/W	0x7	PD26_SELECT 000:Input 010:TWI0_SDA 100:UART3_CTS 110:Reserved	001:Output 011:TS3_D0 101:JTAG_DI 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PD25_SELECT 000:Input 010:TWI0_SCK 100:UART3_RTS 110:Reserved	001:Output 011:TS3_DVLD 101:JTAG_DO 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PD24_SELECT 000:Input 010:TWI2_SDA 100:UART3_RX 110:Reserved	001:Output 011:TS3_SYNC 101:JTAG_CK 111:IO Disable

3.21.5.14. PD Data Register (Default Value: 0x0000_0000)

Offset: 0x007C			Register Name: PD_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:0	R/W	0x0	PD_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

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3.21.5.15. PD Multi-Driving Register 0 (Default Value: 0x5555_5555)

Offset: 0x0080			Register Name: PD_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x1	PD15_DRV PD15 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
29:28	R/W	0x1	PD14_DRV PD14 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
27:26	R/W	0x1	PD13_DRV PD13 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
25:24	R/W	0x1	PD12_DRV PD12 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
23:22	R/W	0x1	PD11_DRV PD11 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
21:20	R/W	0x1	PD10_DRV PD10 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
19:18	R/W	0x1	PD9_DRV PD9 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PD8_DRV PD8 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PD7_DRV PD7 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PD6_DRV PD6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PD5_DRV

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			PD5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PD4_DRV PD4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PD3_DRV PD3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PD2_DRV PD2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PD1_DRV PD1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PD0_DRV PD0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.21.5.16. PD Multi-Driving Register 1 (Default Value: 0x0015_5555)

Offset: 0x0084			Register Name: PD_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x1	PD26_DRV PD26 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
19:18	R/W	0x1	PD25_DRV PD25 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PD24_DRV PD24 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PD23_DRV PD23 Multi-Driving Select 00: Level 0 01: Level 1

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			10: Level 2	11: Level 3
13:12	R/W	0x1	PD22_DRV PD22 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
11:10	R/W	0x1	PD21_DRV PD21 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
9:8	R/W	0x1	PD20_DRV PD20 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
7:6	R/W	0x1	PD19_DRV PD19 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
5:4	R/W	0x1	PD18_DRV PD18 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
3:2	R/W	0x1	PD17_DRV PD17 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
1:0	R/W	0x1	PD16_DRV PD16 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3

3.21.5.17. PD Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: PD_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x0	PD15_PULL PD15 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
29:28	R/W	0x0	PD14_PULL PD14 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
27:26	R/W	0x0	PD13_PULL PD13 Pull-up/down Select	

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			00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
25:24	R/W	0x0	PD12_PULL PD12 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
23:22	R/W	0x0	PD11_PULL PD11 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
21:20	R/W	0x0	PD10_PULL PD10 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
19:18	R/W	0x0	PD9_PULL PD9 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
17:16	R/W	0x0	PD8_PULL PD8 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
15:14	R/W	0x0	PD7_PULL PD7 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
13:12	R/W	0x0	PD6_PULL PD6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PD5_PULL PD5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PD4_PULL PD4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PD3_PULL PD3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PD2_PULL PD2 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up

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			10: Pull-down 11: Reserved
3:2	R/W	0x0	PD1_PULL PD1 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PD0_PULL PD0 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.21.5.18. PD Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: PD_PULL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x0	PD26_PULL PD26 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
19:18	R/W	0x0	PD25_PULL PD25 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
17:16	R/W	0x0	PD24_PULL PD24 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
15:14	R/W	0x0	PD23_PULL PD23 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
13:12	R/W	0x0	PD22_PULL PD22 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PD21_PULL PD21 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PD20_PULL PD20 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PD19_PULL

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			PD19 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PD18_PULL PD18 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PD17_PULL PD17 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PD16_PULL PD16 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.21.5.19. PF Configure Register 0 (Default Value: 0x0777_7777)

Offset: 0x00B4			Register Name: PF_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:24	R/W	0x7	PF6_SELECT 000:Input 001:Output 010:Reserved 011:Reserved 100:Reserved 101:Reserved 110:PF_EINT6 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PF5_SELECT 000:Input 001:Output 010:SDC0_D2 011:JTAG_CK1 100:Reserved 101:Reserved 110:PF_EINT5 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PF4_SELECT 000:Input 001:Output 010:SDC0_D3 011:UART0_RX 100:Reserved 101:Reserved 110:PF_EINT4 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PF3_SELECT 000:Input 001:Output 010:SDC0_CMD 011:JTAG_DO1 100:Reserved 101:Reserved 110:PF_EINT3 111:IO Disable

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11	/	/	/
10:8	R/W	0x7	PF2_SELECT 000:Input 001:Output 010:SDC0_CLK 011:UART0_TX 100:Reserved 101:Reserved 110:PF_EINT2 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PF1_SELECT 000:Input 001:Output 010:SDC0_D0 011:JTAG_DI1 100:Reserved 101:Reserved 110:PF_EINT1 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PF0_SELECT 000:Input 001:Output 010:SDC0_D1 011:JTAG_MS1 100:Reserved 101:Reserved 110:PF_EINT0 111:IO Disable

3.21.5.20. PF Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: PF_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

3.21.5.21. PF Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x00BC			Register Name: PF_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

3.21.5.22. PF Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: PF_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

3.21.5.23. PF Data Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: PF_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:7	/	/	/
6:0	R/W	0x0	PF_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.21.5.24. PF Multi-Driving Register 0 (Default Value: 0x0000_1555)

Offset: 0x00C8			Register Name: PF_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x1	PF6_DRV PF6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PF5_DRV PF5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PF4_DRV PF4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PF3_DRV PF3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PF2_DRV PF2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PF1_DRV PF1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PF0_DRV PF0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

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3.21.5.25. PF Multi-Driving Register 1 (Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: PF_DRV1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

3.21.5.26. PF Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: PF_PULL0
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:12	R/W	0x0	PF6_PULL PF6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PF5_PULL PF5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PF4_PULL PF4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PF3_PULL PF3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PF2_PULL PF2 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PF1_PULL PF1 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PF0_PULL PF0 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.21.5.27. PF Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x00D4	Register Name: PF_PULL1

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Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

3.21.5.28. PG Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x00D8			Register Name: PG_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PG7_SELECT 000:Input 001:Output 010:UART1_RX 011:Reserved 100:Reserved 101:Reserved 110:PG_EINT7 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PG6_SELECT 000:Input 001:Output 010:UART1_TX 011:Reserved 100:Reserved 101:Reserved 110:PG_EINT6 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PG5_SELECT 000:Input 001:Output 010:SDC1_D3 011:Reserved 100:Reserved 101:Reserved 110:PG_EINT5 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PG4_SELECT 000:Input 001:Output 010:SDC1_D2 011:Reserved 100:Reserved 101:Reserved 110:PG_EINT4 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PG3_SELECT 000:Input 001:Output 010:SDC1_D1 011:Reserved 100:Reserved 101:Reserved 110:PG_EINT3 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PG2_SELECT 000:Input 001:Output 010:SDC1_D0 011:Reserved 100:Reserved 101:Reserved 110:PG_EINT2 111:IO Disable
7	/	/	/

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6:4	R/W	0x7	PG1_SELECT 000:Input 010:SDC1_CMD 100:Reserved 110:PG_EINT1	 001:Output 011:Reserved 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PG0_SELECT 000:Input 010:SDC1_CLK 100:Reserved 110:PG_EINT0	 001:Output 011:Reserved 101:Reserved 111:IO Disable

3.21.5.29. PG Configure Register 1 (Default Value: 0x0777_7777)

Offset: 0x00DC			Register Name: PG_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:27	/	/	/	
26:24	R/W	0x7	PG14_SELECT 000:Input 010:PCM2_MCLK 100:SIM0_DET 110:PG_EINT14	 001:Output 011:H_PCM2_MCLK 101:Reserved 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PG13_SELECT 000:Input 010:PCM2_DIN 100:SIM0_RST 110:PG_EINT13	 001:Output 011:H_PCM2_DIN 101:Reserved 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PG12_SELECT 000:Input 010:PCM2_DOUT 100:SIM0_DATA 110:PG_EINT12	 001:Output 011:H_PCM2_DOUT 101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PG11_SELECT 000:Input 010:PCM2_CLK 100:SIM0_CLK 110:PG_EINT11	 001:Output 011:H_PCM2_CLK 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PG10_SELECT 000:Input 010:PCM2_SYNC	 001:Output 011:H_PCM2_SYNC

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			100:SIM0_PWREN 110:PG_EINT10	101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PG9_SELECT 000:Input 010:UART1_CTS 100:SIM0_VPPPP 110:PG_EINT9	 001:Output 011:Reserved 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PG8_SELECT 000:Input 010:UART1_RTS 100:SIM0_VPPEN 110:PG_EINT8	 001:Output 011:Reserved 101:Reserved 111:IO Disable

3.21.5.30. PG Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x00E0			Register Name: PG_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

3.21.5.31. PG Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x00E4			Register Name: PG_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

3.21.5.32. PG Data Register (Default Value: 0x0000_0000)

Offset: 0x00E8			Register Name: PG_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:0	R/W	0	PG_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

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3.21.5.33. PG Multi-Driving Register 0 (Default Value: 0x1555_5555)

Offset: 0x00EC			Register Name: PG_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R/W	0x1	PG14_DRV PG14 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
27:26	R/W	0x1	PG13_DRV PG13 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
25:24	R/W	0x1	PG12_DRV PG12 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
23:22	R/W	0x1	PG11_DRV PG11 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
21:20	R/W	0x1	PG10_DRV PG10 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
19:18	R/W	0x1	PG9_DRV PG9 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PG8_DRV PG8 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PG7_DRV PG7 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PG6_DRV PG6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PG5_DRV PG5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

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9:8	R/W	0x1	PG4_DRV PG4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PG3_DRV PG3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PG2_DRV PG2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PG1_DRV PG1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PG0_DRV PG0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.21.5.34. PG Multi-Driving Register 1 (Default Value: 0x0000_0000)

Offset: 0x00F0			Register Name: PG_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

3.21.5.35. PG Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x00F4			Register Name: PG_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R/W	0x0	PG14_PULL PG14 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
27:26	R/W	0x0	PG13_PULL PG13 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
25:24	R/W	0x0	PG12_PULL PG12 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up

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			10: Pull-down	11: Reserved
23:22	R/W	0x0	PG11_PULL PG11 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
21:20	R/W	0x0	PG10_PULL PG10 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
19:18	R/W	0x0	PG9_PULL PG9 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
17:16	R/W	0x0	PG8_PULL PG8 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
15:14	R/W	0x0	PG7_PULL PG7 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
13:12	R/W	0x0	PG6_PULL PG6 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
11:10	R/W	0x0	PG5_PULL PG5 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
9:8	R/W	0x0	PG4_PULL PG4 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
7:6	R/W	0x0	PG3_PULL PG3 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
5:4	R/W	0x0	PG2_PULL PG2 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
3:2	R/W	0x0	PG1_PULL PG1 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved

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1:0	R/W	0x0	PG0_PULL PG0 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.21.5.36. PG Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x00F8			Register Name: PG_PULL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

3.21.5.37. PH Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x00FC			Register Name: PH_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PH7_SELECT 000:Input 001:Output 010:Reserved 011:OWA_OUT 100:Reserved 101:Reserved 110:PH_EINT7 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PH6_SELECT 000:Input 001:Output 010:SPI1_MISO 011:OWA_IN 100:TWI1_SDA 101:SIM1_DET 110:PH_EINT6 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PH5_SELECT 000:Input 001:Output 010:SPI1_MOSI 011:OWA_MCLK 100:TWI1_SCK 101:SIM1_RST 110:PH_EINT5 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PH4_SELECT 000:Input 001:Output 010:SPI1_CLK 011:PCM0_MCLK 100:H_PCM0_MCLK 101:SIM1_DATA 110:PH_EINT4 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PH3_SELECT 000:Input 001:Output 010:SPI1_CS 011:PCM0_DIN

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			100:H_PCM0_DIN	101:SIM1_CLK
			110:PH_EINT3	111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PH2_SELECT 000:Input 010:CIR_TX 100:H_PCM0_DOUT 110:PH_EINT2	 001:Output 011:PCM0_DOUT 101:SIM1_PWREN 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PH1_SELECT 000:Input 010:UART0_RX 100:H_PCM0_CLK 110:PH_EINT1	 001:Output 011:PCM0_CLK 101:SIM1_VPPPP 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PH0_SELECT 000:Input 010:UART0_TX 100:H_PCM0_SYNC 110:PH_EINT0	 001:Output 011:PCM0_SYNC 101:SIM1_VPPEN 111:IO Disable

3.21.5.38. PH Configure Register 1 (Default Value: 0x0000_0777)

Offset: 0x0100			Register Name: PH_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:11	/	/	/	
10:8	R/W	0x7	PH10_SELECT 000:Input 010:HCEC 100:Reserved 110:PH_EINT10	 001:Output 011:Reserved 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PH9_SELECT 000:Input 010:HSDA 100:Reserved 110:PH_EINT9	 001:Output 011:Reserved 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PH8_SELECT 000:Input 010:HSCL 100:Reserved 110:PH_EINT8	 001:Output 011:Reserved 101:Reserved 111:IO Disable

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3.21.5.39. PH Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x104			Register Name: PH_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

3.21.5.40. PH Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x108			Register Name: PH_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

3.21.5.41. PH Data Register (Default Value: 0x0000_0000)

Offset: 0x10C			Register Name: PH_DAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0	PH_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.21.5.42. PH Multi-Driving Register 0 (Default Value: 0x0015_5555)

Offset: 0x110			Register Name: PH_DRV0
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:20	R/W	0x1	PH10_DRV PH10 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
19:18	R/W	0x1	PH9_DRV PH9 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PH8_DRV PH8 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PH7_DRV

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			PH7 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PH6_DRV PH6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PH5_DRV PH5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PH4_DRV PH4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PH3_DRV PH3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PH2_DRV PH2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PH1_DRV PH1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PH0_DRV PH0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.21.5.43. PH Multi-Driving Register 1 (Default Value: 0x0000_0000)

Offset: 0x114			Register Name: PH_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

3.21.5.44. PH Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x118			Register Name: PH_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/

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21:20	R/W	0x0	PH10_PULL PH10 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
19:18	R/W	0x0	PH9_PULL PH9 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
17:16	R/W	0x0	PH8_PULL PH8 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
15:14	R/W	0x0	PH7_PULL PH7 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
13:12	R/W	0x0	PH6_PULL PH6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PH5_PULL PH5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PH4_PULL PH4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PH3_PULL PH3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PH2_PULL PH2 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PH1_PULL PH1 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PH0_PULL PH0 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

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3.21.5.45. PH Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: PH_PULL1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

3.21.5.46. PF External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x02A0			Register Name: PF_EINT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG

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			External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

3.21.5.47. PF External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x02A4			Register Name: PF_EINT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

3.21.5.48. PF External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x02A8			Register Name: PF_EINT_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

3.21.5.49. PF External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x02AC			Register Name: PF_EINT_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

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3.21.5.50. PF External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x02B0			Register Name: PF_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

3.21.5.51. PF External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x02B4			Register Name: PF_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear

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5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

3.21.5.52. PF External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x02B8			Register Name: PF_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

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3.21.5.53. PG External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x02C0			Register Name:PG_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative)

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			Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

3.21.5.54. PG External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x02C4			**Register Name: PG_EINT_CFG1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level

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			0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

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3.21.5.55. PG External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x02C8			Register Name: PG_EINT_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

3.21.5.56. PG External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x02CC			Register Name: PG_EINT_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

3.21.5.57. PG External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x02D0			Register Name: PG_EINT_CTL
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable

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			0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

3.21.5.58. PG External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x02D4			Register Name: PG_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14	R/W	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending

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			Write ‘1’ to clear
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending

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			Write ‘1’ to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear

3.21.5.59. PG External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x02D8			**Register Name: PG_EINT_DEB**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

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3.21.5.60. PH External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x02E0			Register Name:PH_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG

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			External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

3.21.5.61. PH External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x02E4			Register Name: PH_EINT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative)

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			Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

3.21.5.62. PH External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x02E8			Register Name: PH_EINT_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

3.21.5.63. PH External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x02EC			Register Name: PH_EINT_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

3.21.5.64. PH External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x02F0			Register Name: PH_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable

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			1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

3.21.5.65. PH External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x02F4			Register Name: PH_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending

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			Write ‘1’ to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending

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			Write ‘1’ to clear

3.21.5.66. PH External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x02F8			Register Name: PH_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

3.21.5.67. PIO Group Withstand Voltage Mode Select Register (Default Value: 0x0000_0000)

Offset: 0x0340			Register Name: PIO_POW_MOD_SEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	VCC-IO POWER MODE Select 0: 3.3V 1: 1.8V
15:10	/	/	/
9	/	/	/
8	/	/	/
7	R/W	/	PH_POWER MODE Select invalid
6	R/W	0x0	PG_POWER MODE Select 0: 3.3V 1: 1.8V If PG_Port Power Source selects VCC-IO,this bit is invalid
5	/	/	PF_POWER MODE Select invalid
4	/	/	/
3	R/W	0x0	PD_POWER MODE Select 0: 3.3V 1: 1.8V If PD_Port Power Source selects VCC-IO,this bit is invalid
2	R/W	0x0	PC_POWER MODE Select 0: 3.3V

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			1: 1.8V If PC_Port Power Source selects VCC-IO,this bit is invalid
1	/	/	PB_POWER MODE Select invalid
0	/	/	PA_POWER MODE Select invalid

NOTE

For 0x0340 register ,when the power domain of GPIO is larger than 1.8V, then the withstand voltage is set to 3.3V mode, that is, the corresponding register value is set to 0; when the power domain of GPIO is 1.8V,then the withstand voltage is set to 1.8V mode, that is, the corresponding register value is set to 1.

3.21.5.68. PIO Group Power Value Register

Offset: 0x0348			Register Name: PIO_POW_Val
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R	/	VCC-IO Power Value
15:10	/	/	/
9	/	/	/
8	/	/	/
7	/	/	PH_Port Power Value invalid
6	R	/	PG_Port Power Value If PG_Port Power Source selects VCC-IO,this bit is invalid
5	/	/	PF_Port Power Value invalid
4	/	/	/
3	R	/	PD_Port Power Value If PD_Port Power Source selects VCC-IO,this bit is invalid
2	R	/	PC_Port Power Value If PC_Port Power Source selects VCC-IO,this bit is invalid
1	/	/	PB_Port Power Value invalid
0	R	/	PA_Port Power Value invalid

NOTE

IO pressure mode is 3.3V when reading 0;IO pressure mode is 1.8V when reading 1.

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3.22. Port Controller(CPUS-PORT)

3.22.1. Overview

The chip has 2 ports for multi-functional input/output pins. They are shown below:

- Port L(PL): 11 input/output port
- Port M(PM): 5 input/output port

3.22.2. Register List

Module Name	Base Address
PIO	0x07022000

Register Name	Offset	Description
Pn_CFG0	n*0x0024+0x00	Port n Configure Register 0 (n =0,1)
Pn_CFG1	n*0x0024+0x04	Port n Configure Register 1 (n =0,1)
Pn_CFG2	n*0x0024+0x08	Port n Configure Register 2 (n =0,1)
Pn_CFG3	n*0x0024+0x0C	Port n Configure Register 3 (n =0,1)
Pn_DAT	n*0x0024+0x10	Port n Data Register (n =0,1)
Pn_DRV0	n*0x0024+0x14	Port n Multi-Driving Register 0 (n =0,1)
Pn_DRV1	n*0x0024+0x18	Port n Multi-Driving Register 1 (n =0,1)
Pn_PUL0	n*0x0024+0x1C	Port n Pull Register 0 (n =0,1)
Pn_PUL1	n*0x0024+0x20	Port n Pull Register 1 (n =0,1)
Pn_INT_CFG0	0x200+n*0x20+0x00	PIO Interrupt Configure Register 0 (n =0,1)
Pn _INT_CFG1	0x200+n*0x20+0x04	PIO Interrupt Configure Register 1 (n =0,1)
Pn _INT_CFG2	0x200+n*0x20+0x08	PIO Interrupt Configure Register 2 (n =0,1)
Pn _INT_CFG3	0x200+n*0x20+0x0C	PIO Interrupt Configure Register 3 (n =0,1)
Pn _INT_CTL	0x200+n*0x20+0x10	PIO Interrupt Control Register (n =0,1)
Pn _INT_STA	0x200+n*0x20+0x14	PIO Interrupt Status Register (n =0,1)
Pn _INT_DEB	0x200+n*0x20+0x18	PIO Interrupt Debounce Register (n =0,1)
PIO_POW_MOD_SEL	0x0340	PIO Group Withstand Voltage Mode Select Register
PIO_POW_Val	0x0348	PIO Group Power Value Register

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3.22.3. Register Description

3.22.3.1. PL Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x0000			Register Name: PL_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PL7_SELECT 000:Input 001:Output 010:S_JTAG_DI 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT7 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PL6_SELECT 000:Input 001:Output 010:S_JTAG_DO 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT6 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PL5_SELECT 000:Input 001:Output 010:S_JTAG_CK 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT5 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PL4_SELECT 000:Input 001:Output 010:S_JTAG_MS 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT4 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PL3_SELECT 000:Input 001:Output 010:S_UART_RX 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT3 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PL2_SELECT 000:Input 001:Output 010:S_UART_TX 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT2 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PL1_SELECT

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			000:Input 010:Reserved 100:Reserved 110:S_PL_EINT1	001:Output 011:S_TWI_SDA 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PL0_SELECT 000:Input 010:Reserved 100:Reserved 110:S_PL_EINT0	 001:Output 011:S_TWI_SCK 101:Reserved 111:IO Disable

3.22.3.2. PL Configure Register 1 (Default Value: 0x000_0777)

Offset: 0x0004			Register Name: PL_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:11	/	/	/	
10:8	R/W	0x7	PL10_SELECT 000:Input 010:S_OWC 100:Reserved 110:S_PL_EINT10	 001:Output 011:S_PWM1 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PL9_SELECT 000:Input 010:S_CIR_RX 100:Reserved 110:S_PL_EINT9	 001:Output 011:Reserved 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PL8_SELECT 000:Input 010:S_PWM0 100:Reserved 110:S_PL_EINT8	 001:Output 011:Reserved 101:Reserved 111:IO Disable

3.22.3.3. PL Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: PL_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

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3.22.3.4. PL Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: PL_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

3.22.3.5. PL Data Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: PL_DAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0	PL_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.22.3.6. PL Multi-Driving Register 0 (Default Value: 0x0015_5555)

Offset: 0x0014			Register Name: PL_DRV0
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:20	R/W	0x1	PL10_DRV PL10 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
19:18	R/W	0x1	PL9_DRV PL9 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PL8_DRV PL8 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PL7_DRV PL7 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PL6_DRV PL6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

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11:10	R/W	0x1	PL5_DRV PL5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PL4_DRV PL4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PL3_DRV PL3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PL2_DRV PL2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PL1_DRV PL1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PL0_DRV PL0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.22.3.7. PL Multi-Driving Register 1 (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: PL_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

3.22.3.8. PL Pull Register 0 (Default Value: 0x0000_0005)

Offset: 0x001C			Register Name: PL_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x0	PL10_PULL PL10 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
19:18	R/W	0x0	PL9_PULL PL9 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up

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			10: Pull-down	11: Reserved
17:16	R/W	0x0	PL8_PULL PL8 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
15:14	R/W	0x0	PL7_PULL PL7 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
13:12	R/W	0x0	PL6_PULL PL6 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
11:10	R/W	0x0	PL5_PULL PL5 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
9:8	R/W	0x0	PL4_PULL PL4 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
7:6	R/W	0x0	PL3_PULL PL3 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
5:4	R/W	0x0	PL2_PULL PL2 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
3:2	R/W	0x1	PL1_PULL PL1 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
1:0	R/W	0x1	PL0_PULL PL0 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved

3.22.3.9. PL Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x0020			**Register Name: PL_PULL1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

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3.22.3.10. PM Configure Register 0 (Default Value: 0x0007_7777)

Offset: 0x0024			Register Name: PM_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:19	/	/	/	
18:16	R/W	0x7	PM4_SELECT 000:Input 010:Reserved 100:Reserved 110:S_PM_EINT4	 001:Output 011:Reserved 101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PM3_SELECT 000:Input 010:Reserved 100:Reserved 110:S_PM_EINT3	 001:Output 011:Reserved 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PM2_SELECT 000:Input 010:Reserved 100:Reserved 110:S_PM_EINT2	 001:Output 011:Reserved 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PM1_SELECT 000:Input 010:Reserved 100:Reserved 110:S_PM_EINT1	 001:Output 011:Reserved 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PM0_SELECT 000:Input 010:Reserved 100:Reserved 110:S_PM_EINT0	 001:Output 011:Reserved 101:Reserved 111:IO Disable

3.22.3.11. PM Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: PM_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

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3.22.3.12. PM Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: PM_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

3.22.3.13. PM Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: PM_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

3.22.3.14. PM Data Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: PM_DAT
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4:0	R/W	0x0	PM_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.22.3.15. PM Multi-Driving Register 0 (Default Value: 0x0000_0155)

Offset: 0x0038			Register Name: PM_DRV0
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:8	R/W	0x1	PM4_DRV PM4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PM3_DRV PM3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PM2_DRV PM2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PM1_DRV

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			PM1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PM0_DRV PM0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.22.3.16. PM Multi-Driving Register 1 (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: PM_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

3.22.3.17. PM Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: PM_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0x0	PM4_PULL PM4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PM3_PULL PM3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PM2_PULL PM2 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PM1_PULL PM1 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PM0_PULL PM0 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

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3.22.3.18. PM Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: PM_PULL1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

3.22.3.19. PL External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name:PL_EINT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode

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			0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

3.22.3.20. PL External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0204			Register Name: PL_EINT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

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7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

3.22.3.21. PL External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0208			Register Name: PL_EINT_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

3.22.3.22. PL External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x020C			Register Name: PL_EINT_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

3.22.3.23. PL External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: PL_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable

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8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

3.22.3.24. PL External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0214			Register Name: PL_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit

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			0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit

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			0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

3.22.3.25. PL External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0218			Register Name: PL_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

3.22.3.26. PM External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0220			Register Name:PM_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative)

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			Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

3.22.3.27. PM External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0224			Register Name: PM_EINT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

3.22.3.28. PM External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0228			Register Name: PM_EINT_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

3.22.3.29. PM External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x22C			Register Name: PM_EINT_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:0	/	/	/

3.22.3.30. PM External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: PM_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

3.22.3.31. PM External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0234			Register Name: PM_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear

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2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

3.22.3.32. PM External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0238			Register Name: PM_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

3.22.3.33. PIO Group Withstand Voltage Mode Select Register (Default Value: 0x0000_0000)

Offset: 0x0340			Register Name: PIO_POW_MOD_SEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	VCC-IO POWER MODE Select 0: 3.3V 1: 1.8V
15:2	/	/	/
1	R/W	0x0	PM_POWER MODE Select 0: 3.3V 1: 1.8V If PM_Port Power Source selects VCC-IO,this bit is invalid

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0	R/W	0x0	PL_POWER MODE Select 0: 3.3V 1: 1.8V If PL_Port Power Source selects VCC-IO,this bit is invalid

NOTE

For 0x0340 register ,when the power domain of GPIO is larger than 1.8V, then the withstand voltage is set to 3.3V mode, that is, the corresponding register value is set to 0; when the power domain of GPIO is 1.8V,then the withstand voltage is set to 1.8V mode, that is, the corresponding register value is set to 1.

3.22.3.34. PIO Group Power Value Register

Offset: 0x0348			Register Name: PIO_POW_Val
Bit	**Read/Write**	**Default /Hex**	**Description**
31:17	/	/	/
16	R	/	VCC-IO Power Value
15:2	/	/	/
1	R	/	PM_Port Power Value If PM_Port Power Source selects VCC-IO,this bit is invalid
0	R	/	PL_Port Power Value If PL_ Port Power Source selects VCC-IO,this bit is invalid

NOTE

IO pressure mode is 3.3V when reading 0;IO pressure mode is 1.8V when reading 1.

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Chapter 4 Memory

This section describes the H6 V200 memory from three aspects:

- SDRAM Controller(DRAMC)
- NAND Flash Controller(NDFC)
- SD/MMC Host Controller(SMHC)

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4.1. SDRAM Controller(DRAMC)

4.1.1. Overview

The SDRAM Controller (DRAMC) provides a simple, flexible, burst-optimized interface to the industy-standard DDR4/DDR3/DDR3L SDRAM and Low Power DDR2/3 SDRAM. It supports up to a 16G bits memory address space.

The DRAMC automatically handles memory management, initialization, and refresh operations. It gives the host CPU a simple command interface, hiding details of the required address, page, and burst handling procedures. All memory parameters are runtime-configurable, including timing, memory setting, SDRAM type, and Extended-Mode-Register setting. To simplify chip system integration,DDR controller works in half rate mode.

Features:

- 32-bit bus width
- Supports 2 chip selects
- Supports DDR4/DDR3/DDR3L/LPDDR2/LPDDR3 SDRAM
- Supports different memory device's power voltage of 1.2V,1.5V,1.35V,1.2V,1.2V
- Supports clock frequency up to 933 MHz(DDR4)
- Supports clock frequency up to 933 MHz(DDR3/DDR3L)
- Supports clock frequency up to 800 MHz(LPDDR3)
- Supports clock frequency up to 533 MHz(LPDDR2)
- Supports memory capacity up to 16G bits (2G bytes)
- Supports 18 address lines and 3 bank address lines
- Automatically generates initialization and refresh sequences
- Runtime-configurable parameters setting for application flexibility
- Priority of transferring through multiple ports is programmable
- Random read or write operation is supported

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4.2. NAND Flash Controller(NDFC)

4.2.1. Overview

The NDFC is the NAND Flash Controller which supports all NAND flash memory available in the market. New type flash can be supported by software re-configuration.

The On-the-fly error correction code (ECC) is built-in NDFC for enhancing reliability. BCH is implemented and it can detect and correct up to 80 bits error per 1024 bytes data. The on chip ECC and parity checking circuit of NDFC frees CPU for other tasks. The ECC function can be disabled by software.

The data can be transferred by DMA or by CPU memory-mapped IO method. The NDFC provides automatic timing control for reading or writing external Flash. The NDFC maintains the proper relativity for CLE, CE# and ALE control signal lines. There are three different kinds of modes for serial read access, mode0 is for conventional serial access , mode1 is for EDO type and the mode2 is for extension EDO type. NDFC can monitor the status of R/B# signal line.

Block management and wear leveling management are implemented in software.

Features:

- Supports all SLC/MLC/TLC flash and EF-NAND memory available in the market
- Software configure seed for randomize engine
- Software configure method for adaptability to a variety of system and memory types
- Supports 2CE/2RB
- Support 3.3V/1.8V IO Voltage
- Supports 8-bit data bus width
- Supports 1024, 2048, 4096, 8192, 16384, 32768 bytes size per page
- Supports Conventional and EDO serial access method for serial reading Flash
- On-the-fly BCH error correction code which correcting up to 80 bits per 1024 bytes
- Corrected Error bits number information report
- ECC automatic disable function for all 0xff data
- Supports full disk encryption(FDE) function
- NDFC status information is reported by its' registers and interrupt is supported
- One Command FIFO
- Support internal DMA controller based on chain-structured descriptor list
- Two 256x32-bit RAM for Pipeline Procession
- Support SDR, ONFI DDR and Toggle DDR NAND
- Support self –debug for NDFC debug

4.2.2. Block Diagram

The NDFC system block diagram is shown below:

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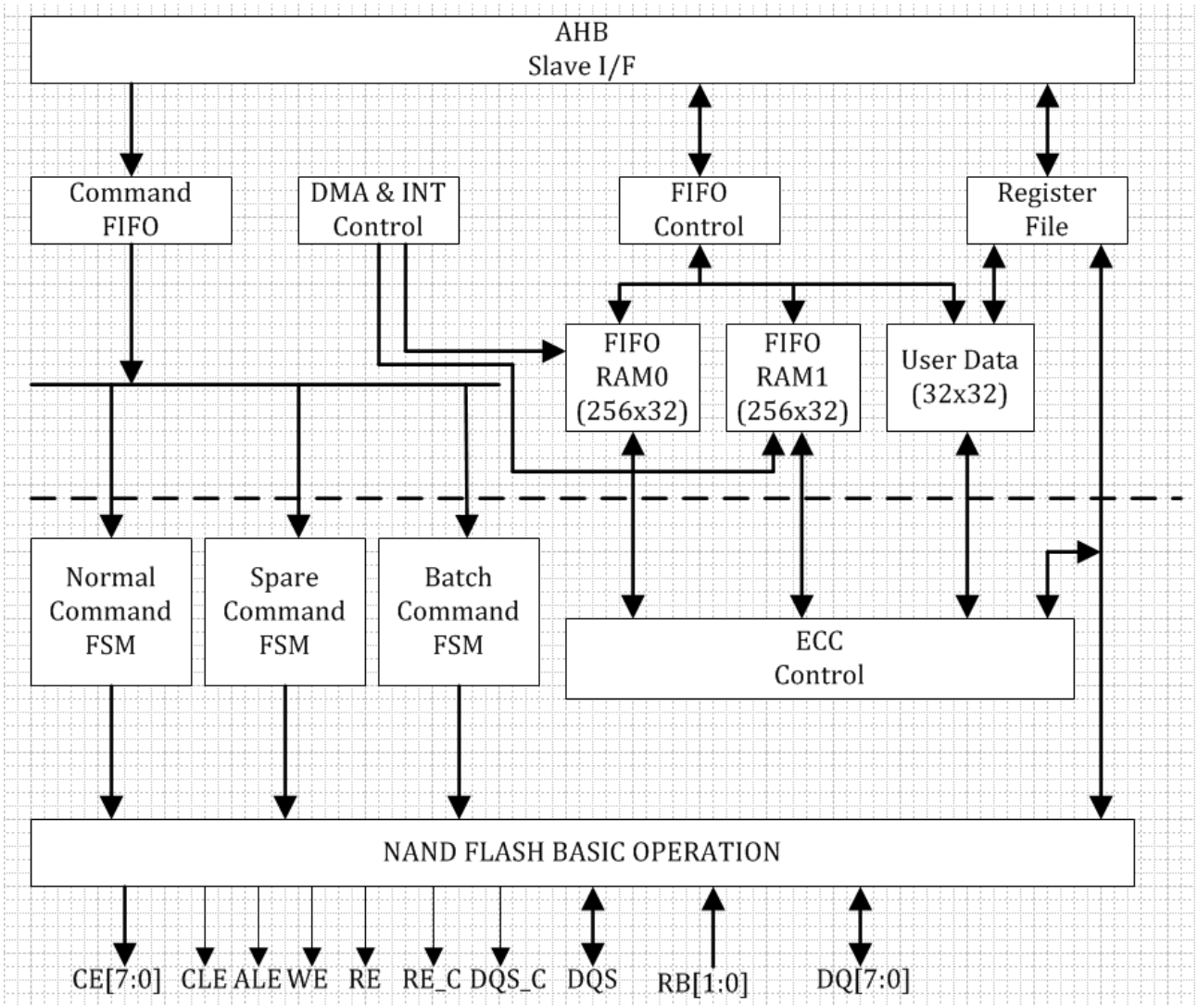


Figure 4-1. NDFC Block Diagram

4.2.3. Operations and Functional Descriptions

4.2.3.1. External Signals

Table 4-1 describes the external signals of NDFC.DQ0~DQ7 and DQS are bidirectional I/O.WE,ALE,CLE,CE,RE are output pin, RB is input pin. The RB pin in the NAND device is an open-drain driver, which must need a pull-up resistor.

Table 4-1. NDFC External Signals

Signal	Description	Type
NAND_WE	Write Enable	O
NAND_RE	Read Enable	O
NAND_ALE	Address Latch Enable, High is Active	O

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NAND_CLE	Command Latch Enable, High is Active	O
/	/	/
NAND_CE0	Chip Enable, Low is Active	O
NAND_CE1	Chip Enable, Low is Active	O
/	/	/
NAND_RB0	Ready/Busy, Low is Active	I
NAND_RB1	Ready/Busy, Low is Active	I
/	/	/
NAND_DQ0	Data Input / Output	I/O
NAND_DQ1	Data Input / Output	I/O
NAND_DQ2	Data Input / Output	I/O
NAND_DQ3	Data Input / Output	I/O
NAND_DQ4	Data Input / Output	I/O
NAND_DQ5	Data Input / Output	I/O
NAND_DQ6	Data Input / Output	I/O
NAND_DQ7	Data Input / Output	I/O
NAND_DQS	Data Strobe	I/O

4.2.3.2. Clock Sources

NDFC gets three different clocks. Users can select one of them to make NDFC clock source. Table 4-2 describles the clock sources of NDFC. Users can see CCU in chapter 3.3 for clock setting, configuration and gating information.

Table 4-2. NDFC Clock Sources

Clock Sources	Description
OSC24M	24MHz Crystal
PLL_PERIPH0(1X)	Peripheral Clock, default value is 600MHz
PLL_PERIPH1(1X)	Peripheral Clock, default value is 600MHz
PLL_PERIPH0(2X)	Peripheral Clock, default value is 1200MHz
PLL_PERIPH1(2X)	Peripheral Clock, default value is 1200MHz

4.2.3.3. NDFC Timing Diagram

Typically, there are two kinds of serial access methods. One method is conventional method which fetching data at the rise edge of NDFC_RE# signal line. Another one is EDO type which fetching data at the next fall edge of NDFC_RE# signal line.

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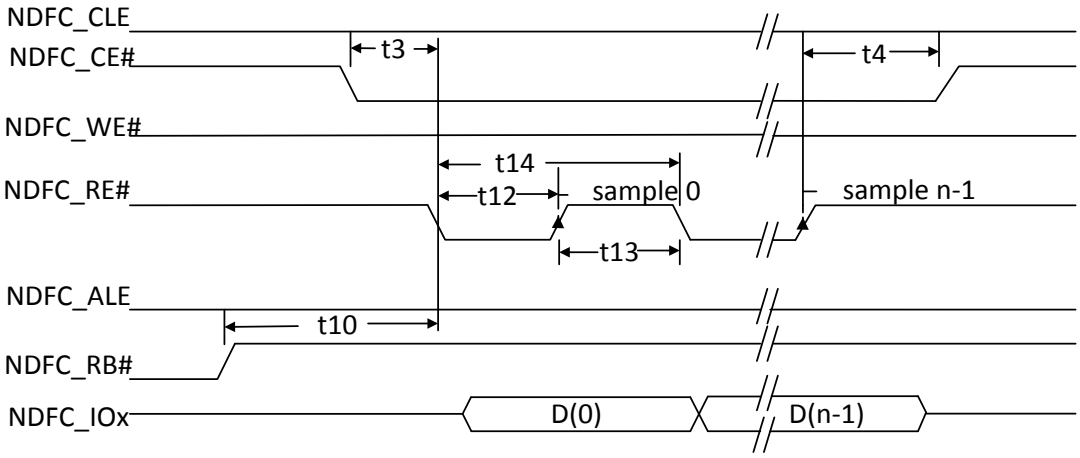


Figure 4-2. Conventional Serial Access Cycle Diagram (SAM0)

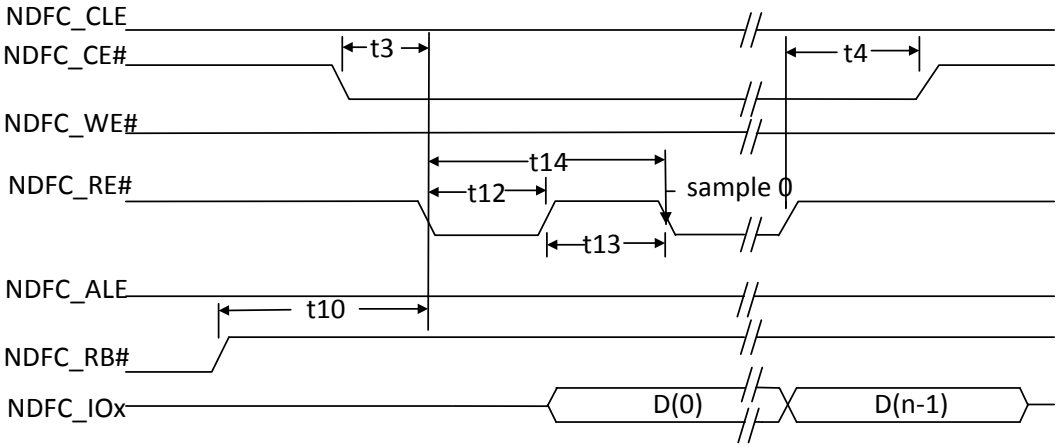


Figure 4-3. EDO Type Serial Access after Read Cycle (SAM1)

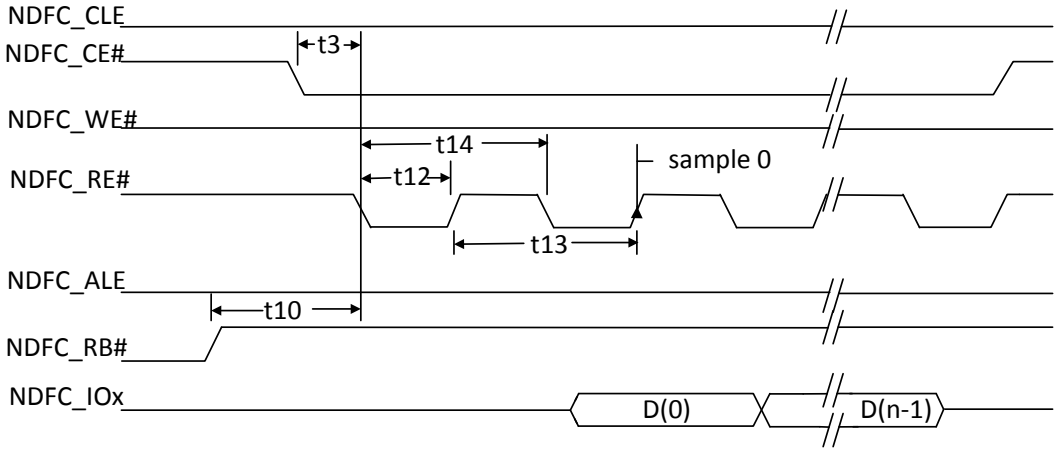


Figure 4-4. Extending EDO Type Serial Access Mode (SAM2)

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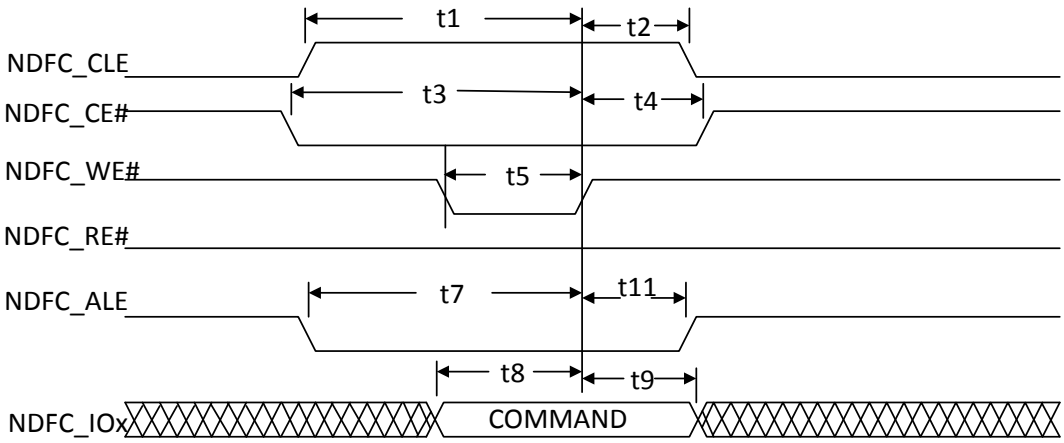


Figure 4-5. Command Latch Cycle

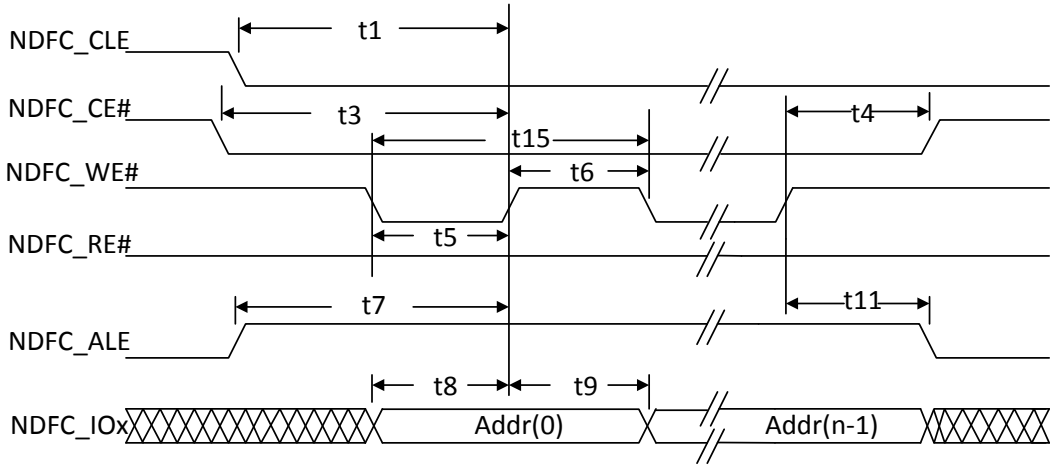


Figure 4-6. Address Latch Cycle

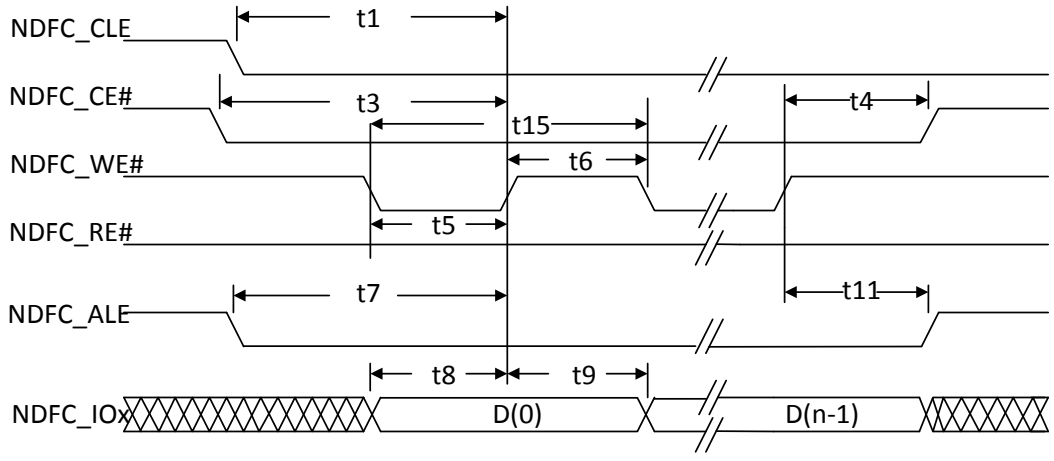


Figure 4-7. Write Data to Flash Cycle

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Figure 4-8. Waiting R/B# Ready Diagram

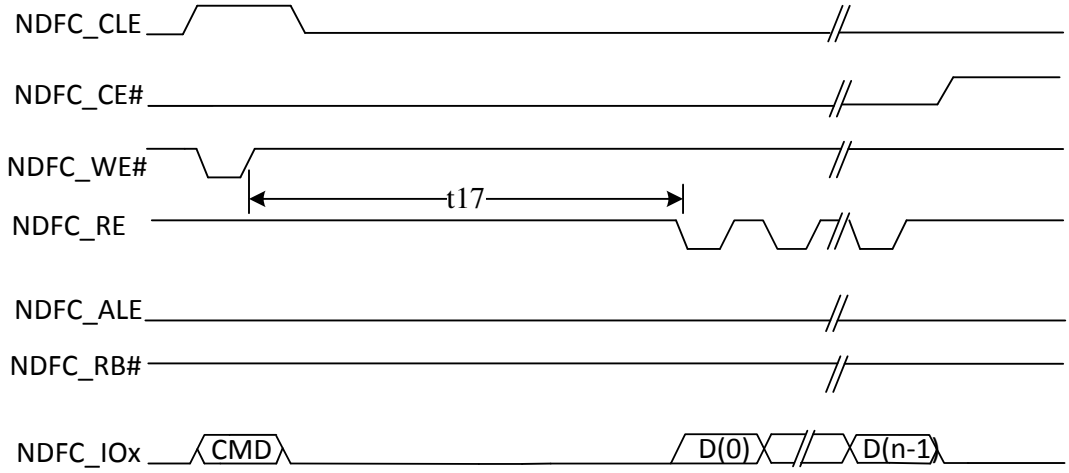


Figure 4-9. WE# High to RE# Low Timing Diagram

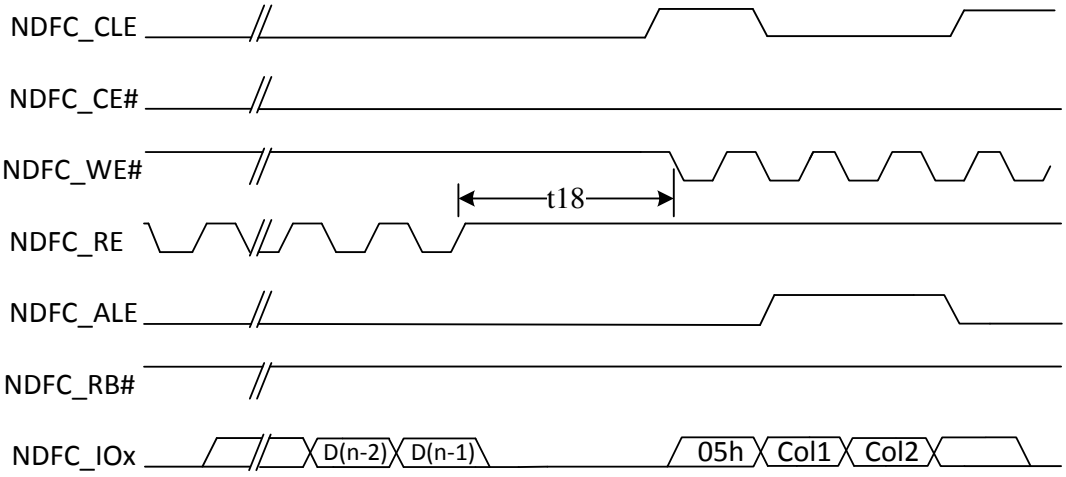


Figure 4-10. RE# High to WE# Low Timing Diagram

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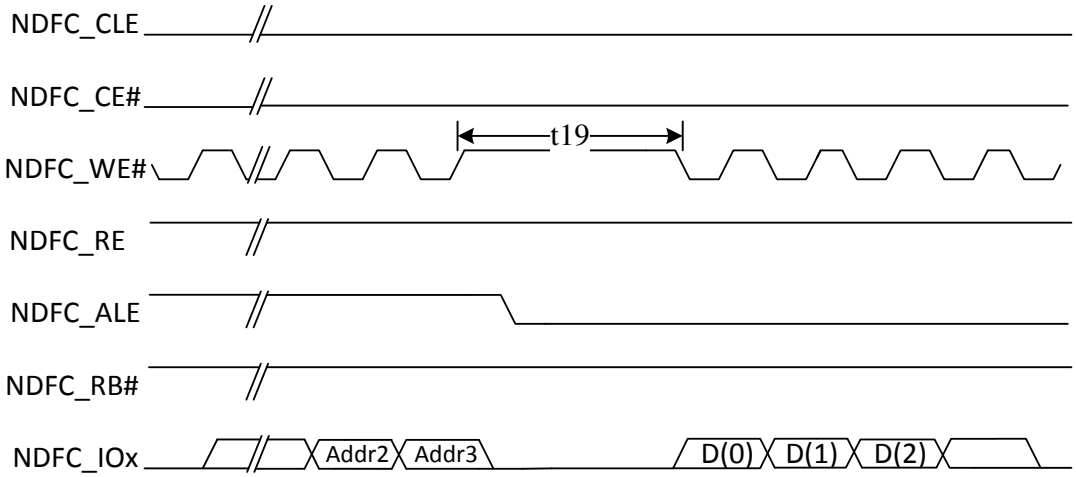


Figure 4-11. Address to Data Loading Timing Diagram

Timing cycle list:

ID	Parameter	Timing	Notes
t1	NDFC_CLE setup time	2T	
t2	NDFC_CLE hold time	2T	
t3	NDFC_CE setup time	2T	
t4	NDFC_CE hold time	2T	
t5	NDFC_WE# pulse width	T(1)	
t6	NDFC_WE# hold time	T	
t7	NDFC_ALE setup time	2T	
t8	Data setup time	T	
t9	Data hold time	T	
t10	Ready to NDFC_RE# low	3T	
t11	NDFC_ALE hold time	2T	
t12	NDFC_RE# pulse width	T	
t13	NDFC_RE# hold time	T	
t14	Read cycle time	2T	
t15	Write cycle time	2T	
t16	NDFC_WE# high to R/B# busy	T_WB(2)	Specified by timing configure register (NDFC_TIMING_CFG)
t17	NDFC_WE# high to NDFC_RE# low	T_WHR(3)	Specified by timing configure register (NDFC_TIMING_CFG)
t18	NDFC_RE# high to NDFC_WE# low	T_RHW(4)	Specified by timing configure register (NDFC_TIMING_CFG)
t19	Address to Data Loading time	T_ADL(5)	Specified by timing configure register (NDFC_TIMING_CFG)

(1): T is the cycle of the internal clock.

(2),(3),(4),(5): These values are configurable in nand flash controller. The value of T_WB could be 14*2T/22*2T/30*2T/38*2T, the value of T_WHR could be 0*2T/6*2T/14*2T/22*2T, the value of T_RHW could be 4*2T/12*2T/20*2T/28*2T, the value of T_ADL could be 0*2T/6*2T/14*2T/22*2T.

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4.2.3.4. NDFC Operation Guide

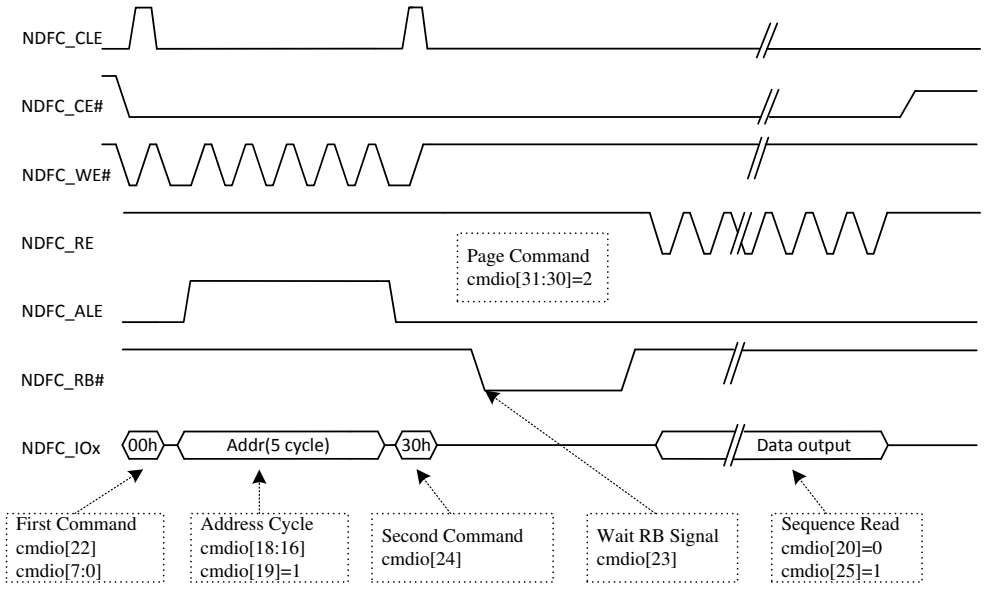


Figure 4-12. Page Read Command Diagram

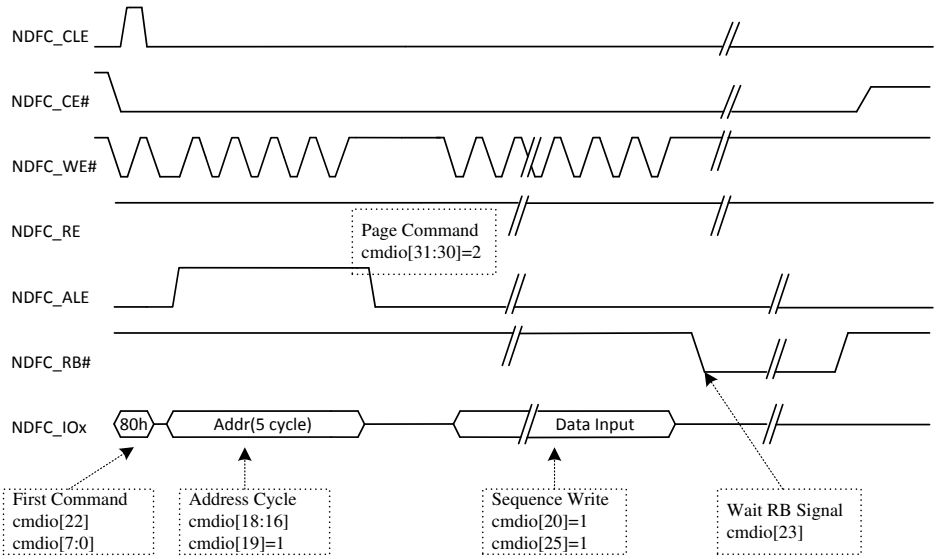


Figure 4-13. Page Program Diagram

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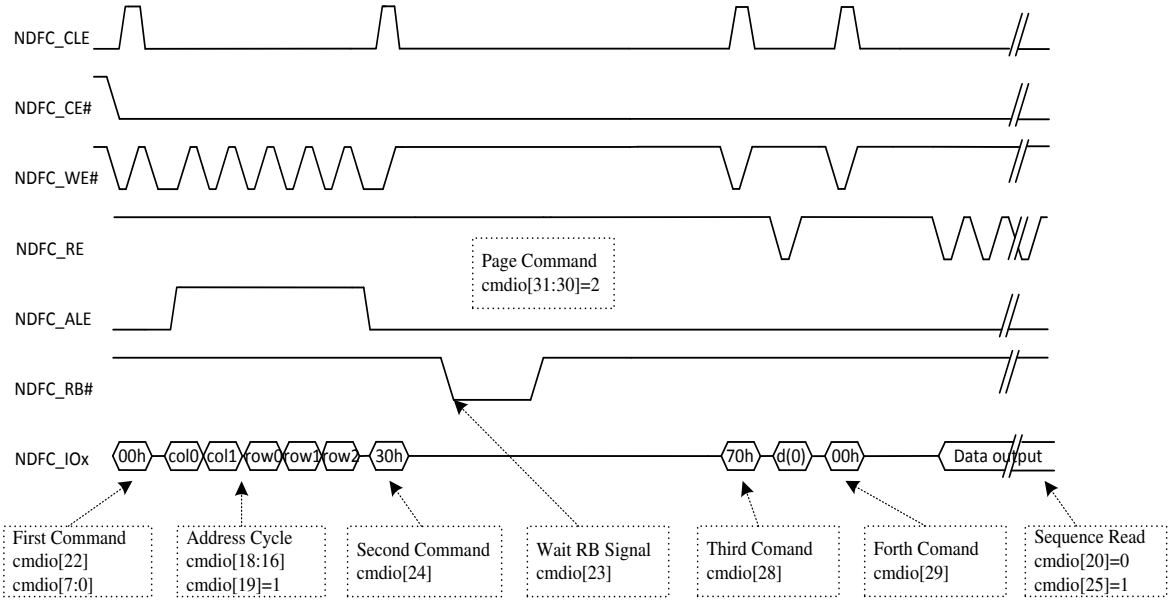


Figure 4-14. EF-NAND Page Read Diagram

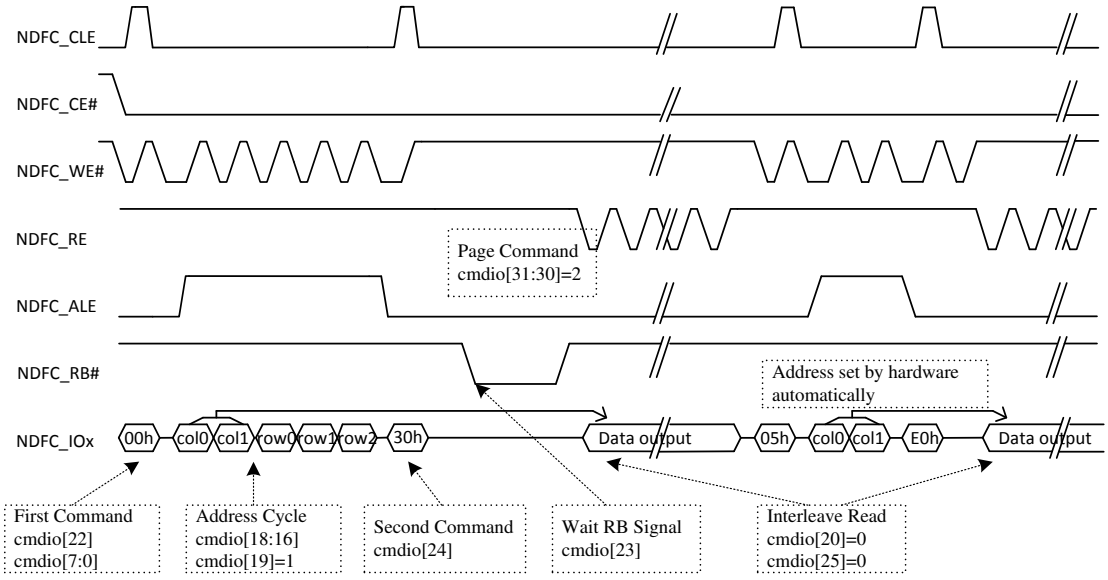


Figure 4-15. Interleave Page Read Diagram

4.2.3.5. NDFC Internal DMA Controller Descriptors

4.2.3.5.1. Descriptor Structure

NDFC internal DMA controller can transfer data between DMA FIFO in NDFC and DMA buffer in host memory using DMA descriptors. DMA descriptors reside in the host memory with chain structure shown in Figure 4-16.

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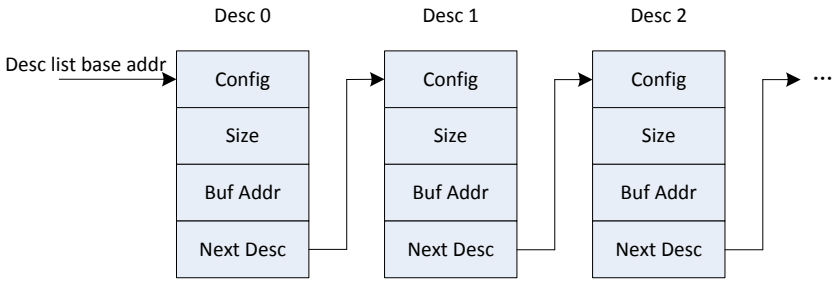


Figure 4-16. Internal DMA Descriptor Chain Structure

The start address of DMA descriptor list must be word (32-bit) aligned, and will be configured to NDFC DMA Descriptor List Base Address Register. Each DMA descriptor is consisted of four words(32-bit).

4.2.3.5.2. Descriptor Definition

Config	
Bit	**Description**
31:4	/
3	FIRST_FLAG When set, this bit indicates that this descriptor contains the first buffer of data. Must be set to 1 in first descriptor.
2	LAST_FLAG When set, this bit indicates that the buffers pointed to by this descriptor are the last data buffer
1:0	/

Size	
Bit	**Description**
31:16	/
15:0	BUFF_SIZE These bits indicate the data buffer byte size, which must be a multiple of 8 bytes. If this filed is 0, the DMA ignores this buffer and proceeds to the next descriptor.

Buff Addr	
Bit	**Description**
31:0	BUFF_ADDR These bits indicate the physical address of DMA data buffer in host memory. The buffer address must be 4 bytes aligned.

Next Description	
Bit	**Description**
31:0	NEXT_DESC_ADDR These bits indicate the pointer to the physical host memory where the next descriptor is present.

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4.2.4. Register List

Module Name	Base Address
NDFC0	0x04011000

Register Name	Offset	Description
NDFC_CTL	0x0000	NDFC Configure and Control Register
NDFC_ST	0x0004	NDFC Status Information Register
NDFC_INT	0x0008	NDFC Interrupt Control Register
NDFC_TIMING_CTL	0x000C	NDFC Timing Control Register
NDFC_TIMING_CFG	0x0010	NDFC Timing Configure Register
NDFC_ADDR_LOW	0x0014	NDFC Low Word Address Register
NDFC_ADDR_HIGH	0x0018	NDFC High Word Address Register
NDFC_DATA_BLOCK_ MASK	0x001C	NDFC Data Block Mask Register
NDFC_CNT	0x0020	NDFC Data Counter for data transfer Register
NDFC_CMD	0x0024	Set up NDFC commands Register
NDFC_RCMD_SET	0x0028	Read Command Set Register for vendor's NAND memory
NDFC_WCMD_SET	0x002C	Write Command Set Register for vendor's NAND memory
/	/	/
NDFC_ECC_CTL	0x0034	ECC Configure and Control Register
NDFC_ECC_ST	0x0038	ECC Status and Operation information Register
NDFC_DATA_PAT_STA	0x003C	NDFC Data Pattern Status Register
NDFC_EFR	0x0040	NDFC Enhanced Feature Register
NDFC_RDATA_STA_CTL	0x0044	Read Data Status Control Register
NDFC_RDATA_STA_0	0x0048	Read Data Status Register 0
NDFC_RDATA_STA_1	0x004C	Read Data Status Register 1
NDFC_ERR_CNT_N	0x0050+0x04*N	NDFC Error Counter Register(N from 0 to 7)
NDFC_USER_DATA_LEN_N	0x0070+0x04*N	NDFC User Data Length Register(N from 0 to 3)
NDFC_USER_DATA_N	0x0080+0x04*N	User Data Field Register N (N from 0 to 31)
NDFC_EFNAND_STA	0x0110	EFNAND Status Register
NDFC_SPARE_AREA	0x0114	Spare Area Configure Register
NDFC_PAT_ID	0x0118	Pattern ID Register
NDFC_DDR2_SPEC_CTL	0x011C	NDFC DDR2 Configuration Control Register
NDFC_NDMA_MODE_CTL	0x0120	NDFC Normal DMA Mode Control Register
NDFC_MDMA_DLBA_REG	0x0200	NDFC MBUS DMA Descriptor List Base Address Register
NDFC_MDMA_STA	0x0204	NDFC MBUS DMA Interrupt Status Register
NDFC_DMA_INT_MASK	0x0208	NDFC MBUS DMA Interrupt Enable Register
NDFC_MDMA_CUR_DESC_ADDR	0x020C	NDFC MBUS DMA Current Descriptor Address Register
NDFC_MDMA_CUR_BUF_ADDR	0x0210	NDFC MBUS DMA Current Buffer Address Register
NDFC_DMA_CNT	0x0214	NDFC DMA Byte Counter Register
NDFC_EMCE_CTL	0x0218	NDFC EMCE Control Register
NDFC_EMCE_IV_FAC_CMP_VAL	0x021C	NDFC EMCE IV_FAC Compare Value Register
NDFC_EMCE_IV_CAL_FACTOR_N	0x0220+0x04*N	NDFC EMCE IV Calculate Factor Register N(N from 0 to 31)

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NDFC_IO_DATA	0x0300	Data Input/Output Port Address Register

4.2.5. Register Description

4.2.5.1. NDFC Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: NDFC_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	NDFC_DDR_TYPE The type of DDR data interface. This bit is valid when NF_TYPE is 0x2 or 0x3. 0: DDR 1: DDR2
27:24	R/W	0x0	NDFC_CE_SEL Chip Select for NAND Flash Chips 0000: NDFC Select Chip 0 0001: NDFC Select Chip 1 0010: NDFC Select Chip 2 0011: NDFC Select Chip 3 0100: NDFC Select Chip 4 0101: NDFC Select Chip 5 0110: NDFC Select Chip 6 0111: NDFC Select Chip 7 1000: NDFC Select Chip 8 1001: NDFC Select Chip 9 1010: NDFC Select Chip 10 1011: NDFC Select Chip 11 1100: NDFC Select Chip 12 1101: NDFC Select Chip 13 1110: NDFC Select Chip 14 1111: NDFC Select Chip 15
23:22	/	/	/
21	R/W	0x0	NDFC_DDR_RM DDR Repeat data mode 0: Lower byte 1: Higher byte
20	R/W	0x0	NDFC_DDR_REN DDR Repeat Enable 0: Disable 1: Enable
19:18	R/W	0x0	NF_TYPE NAND Flash Type 00: Normal SDR NAND 01: Reserved

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			10: ONFI DDR NAND 11: Toggle DDR NAND
17	R/W	0x0	NDFC_CLE_POL NDFC Command Latch Enable (CLE) Signal Polarity Select 0: High active 1: Low active
16	R/W	0x0	NDFC_ALE_POL NDFC Address Latch Enable (ALE) Signal Polarity Select 0: High active 1: Low active
15	R/W	0x0	NDFC_DMA_TYPE 0: Dedicated DMA 1: Normal DMA
14	R/W	0x0	NDFC_RAM_METHOD Access internal RAM method 0: Access internal RAM by AHB method 1: Access internal RAM by DMA method
13:12	/	/	/
11:8	R/W	0x0	NDFC_PAGE_SIZE 000: 1KB 001: 2KB 010: 4KB 011: 8KB 100: 16KB 101: 32KB The page size is for main field data.
7	/	/	/
6	R/W	0x0	NDFC_CE_ACT Chip Select Signal CE# Control During NAND operation 0: De-active Chip Select Signal NDFC_CE# during data loading, serial access and other no operation stage for power consumption. NDFC automatic control Chip Select Signals. 1: Chip select signal NDFC_CE# is always active after NDFC is enabled
5	/	/	/
4:3	R/W	0x0	NDFC_RB_SEL NDFC external R/B Signal select The value 0-3 selects the external R/B signal. The same R/B signal can be used for multiple chip select flash.
2	R/W	0x0	NDFC_BUS_WIDTH 0: 8-bit bus 1: 16-bit bus
1	R/W1C	0x0	NDFC_RESET NDFC Reset Write 1 to reset NDFC and clear to 0 after reset
0	R/W	0x0	NDFC_EN

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			NDFC Enable Control 0: Disable NDFC 1: Enable NDFC

4.2.5.2. NDFC Status Register (Default Value: 0x0000_0F00)

Offset: 0x0004			Register Name: NDFC_ST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R	0x0	NDFC_RDATA_STA_0 0: The number of bit 1 during current read operation is more than threshold value. 1: The number of bit 1 during current read operation is less than or equal to threshold value. This field only is valid when NDFC_RDATA_STA_EN is 1. The threshold value is configured in NDFC_RDATA_STA_TH.
12	R	0x0	NDFC_RDATA_STA_1 0: The number of bit 0 during current read operation is more than threshold value. 1: The number of bit 0 during current read operation is less than or equal to the threshold value. This field only is valid when NDFC_RDATA_STA_EN is 1. The threshold value is configured in NDFC_RDATA_STA_TH.
11	R	0x1	NDFC_RB_STATE3 NAND Flash R/B 3 Line State 0: NAND Flash in BUSY State 1: NAND Flash in READY State
10	R	0x1	NDFC_RB_STATE2 NAND Flash R/B 2 Line State 0: NAND Flash in BUSY State 1: NAND Flash in READY State
9	R	0x1	NDFC_RB_STATE1 NAND Flash R/B 1 Line State 0: NAND Flash in BUSY State 1: NAND Flash in READY State
8	R	0x1	NDFC_RB_STATE0 NAND Flash R/B 0 Line State 0: NAND Flash in BUSY State 1: NAND Flash in READY State
7:5	/	/	/
4	R	0x0	NDFC_STA 0: NDFC FSM in IDLE state 1: NDFC FSM in BUSY state When NDFC_STA is 0, NDFC can accept new command and process command.

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3	R	0x0	NDFC_CMD_FIFO_STATUS 0: Command FIFO not full and can receive new command 1: Full and waiting NDFC to process commands in FIFO Since there is only one 32-bit FIFO for command. When NDFC latches one command, command FIFO is free and can accept another new command.
2	R/W1C	0x0	NDFC_DMA_INT_FLAG When it is 1, it means that a pending DMA is completed. It will be clear after writing 1 to this bit or it will be automatically clear before FSM processing an new command.
1	R/W1C	0x0	NDFC_CMD_INT_FLAG When it is 1, it means that NDFC has finished one Normal Command Mode or one Batch Command Work Mode. It will be clear after writing 1 to this bit or it will be automatically clear before FSM processing an new command.
0	R/W1C	0x0	NDFC_RB_B2R When it is 1, it means that NDFC_R/B# signal is transferred from BUSY state to READY state. It will be clear after writing 1 to this bit.

4.2.5.3. NDFC Interrupt and DMA Enable Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: NDFC_INT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	NDFC_DMA_INT_ENABLE Enable or disable interrupt when a pending DMA is completed.
1	R/W	0x0	NDFC_CMD_INT_ENABLE Enable or disable interrupt when NDFC has finished the procession of a single command in Normal Command Work Mode or one Batch Command Work Mode. 0: Disable 1: Enable
0	R/W	0x0	NDFC_B2R_INT_ENABLE Enable or disable interrupt when NDFC_RB# signal is transferring from BUSY state to READY state 0: Disable 1: Enable

4.2.5.4. NDFC Timing Control Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: NDFC_TIMING_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:8	R/W	0x0	NDFC_READ_PIPE

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			In SDR mode: 00: Normal 01: EDO 10: E-EDO Others: Reserved In DDR mode: 1~15 is valid.(These bits configure the number of clock when data is valid after RE#'s falling edge)
7:6	/	/	/
5:0	R/W	0x0	NDFC_DC_CTL NDFC Delay Chain Control. (These bits are only valid in DDR data interface, and configure the relative phase between DQS and DQ[0…7])

4.2.5.5. NDFC Timing Configure Register(Default Value: 0x0000_0095)

Offset: 0x0010			Register Name: NDFC_TIMING_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:18	R/W	0x0	T_WC Write Cycle Time 00: 1*2T 01: 2*2T 10: 3*2T 11: 4*2T
17:16	R/W	0x0	T_CCS Change Column Setup Time 00: 12*2T 01: 20*2T 10: 28*2T 11: 60*2T
15:14	R/W	0x0	T_CLHZ CLE High to Output Hi-z 00: 2*2T 01: 8*2T 10: 16*2T 11: 31*2T
13:12	R/W	0x0	T_CS CE Setup Time 00: 2*2T 01: 8*2T 10: 16*2T 11: 31*2T
11	R/W	0x0	T_CDQSS

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			DQS Setup Time for data input start 0: 4*2T 1: 20*2T
10:8	R/W	0x0	T_CAD Command, Address, Data Delay 000: 2*2T 001: 6*2T 010: 10*2T 011: 14*2T 100: 22*2T 101: 30*2T 110/111: 62*2T
7:6	R/W	0x2	T_RHW RE# high to WE# low cycle number 00: 4*2T 01: 12*2T 10: 20*2T 11: 28*2T
5:4	R/W	0x1	T_WHR WE# high to RE# low cycle number 00: 0*2T 01: 6*2T 10: 14*2T 11: 22*2T
3:2	R/W	0x1	T_ADL Address to Data Loading cycle number 00: 0*2T 01: 6*2T 10: 14*2T 11: 22*2T
1:0	R/W	0x1	T_WB WE# high to busy cycle number 00:14*2T 01: 22*2T 10: 30*2T 11: 38*2T

4.2.5.6. NDFC Address Low Word Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: NDFC_ADDR_LOW
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	ADDR_DATA4 NAND Flash 4th Cycle Address Data
23:16	R/W	0x0	ADDR_DATA3

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			NAND Flash 3rd Cycle Address Data
15:8	R/W	0x0	ADDR_DATA2 NAND Flash 2nd Cycle Address Data
7:0	R/W	0x0	ADDR_DATA1 NAND Flash 1st Cycle Address Data

4.2.5.7. NDFC Address High Word Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: NDFC_ADDR_HIGH
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	ADDR_DATA8 NAND Flash 8th Cycle Address Data
23:16	R/W	0x0	ADDR_DATA7 NAND Flash 7th Cycle Address Data
15:8	R/W	0x0	ADDR_DATA6 NAND Flash 6th Cycle Address Data
7:0	R/W	0x0	ADDR_DATA5 NAND Flash 5th Cycle Address Data

4.2.5.8. NDFC Data Block Mask Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: NDFC_DATA_BLOCK_MASK
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 31 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
30	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 30 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
29	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 29 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
28	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 28 should be written or read during batch

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			command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
27	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 27 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
26	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 26 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
25	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 25 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
24	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 24 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
23	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 23 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
22	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 22 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
21	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 21 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable

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			1 data block = 1024 bytes main field data.
20	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 20 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
19	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 19 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
18	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 18 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
17	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 17 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
16	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 16 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
15	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 15 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
14	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 14 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
13	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 13 should be written or read during batch

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			command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
12	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 12 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
11	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 11 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
10	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 10 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
9	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 9 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
8	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 8 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
7	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 7 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
6	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 6 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable

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			1 data block = 1024 bytes main field data.
5	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 5 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
4	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 4 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
3	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 3 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
2	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 2 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
1	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 1 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.
0	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 0 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in ***NDFC_CMD***). 0: disable 1: enable 1 data block = 1024 bytes main field data.

4.2.5.9. NDFC Data Counter Register(Default Value: 0x0000_0000)

Offset: 0x0020			**Register Name: NDFC_CNT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	NDFC_DATA_CNT

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			Transfer Data Byte Counter The length can be set from 1 byte to 1024 bytes. However, 1024 bytes is set when it is zero.

4.2.5.10. NDFC Command IO Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: NDFC_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x0	NDFC_CMD_TYPE 00: Common Command for normal operation 01: Special Command for Flash Spare Field Operation 10: Page Command for batch process operation 11: Reserved
29	R/W	0x0	NDFC_SEND_FOURTH_CMD 0: Don't send third set command 1: Send it on the external memory's bus It is used for EF-NAND page read.
28	R/W	0x0	NDFC_SEND_THIRD_CMD 0: Don't send third set command 1: Send it on the external memory's bus It is used for EF-NAND page read.
27	R/W	0x0	NDFC_SEND_RANDOM_CMD2_CTL 0: Don't send random cmd2 (NDFC_RANDOM_CMD2) 1: Send random cmd2 **NOTE** **It is only valid in batch cmd operation. It is only valid in writing operation.**
26	R/W	0x0	NDFC_DATA_METHOD Data swap method when the internal RAM and system memory It is only active for Common Command and Special Command. 0: No action 1: DMA transfer automatically It only is active when NDFC_RAM_METHOD is 1. If this bit is set to 1, NDFC should setup DRQ to fetching data before output to Flash or NDFC should setup DRQ to sending out to system memory after fetching data from Flash. If this bit is set to 0, NDFC output the data in internal RAM or do nothing after fetching data from Flash.
25	R/W	0x0	NDFC_SEQ User data & BCH check word position. It only is active for Page Command, don't care about this bit for other two commands 0: Interleave Method (on page spare area) 1: Sequence Method (following data block)
24	R/W	0x0	NDFC_SEND_SECOND_CMD

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			0: Don't send second set command 1: Send it on the external memory's bus
23	R/W	0x0	NDFC_WAIT_FLAG 0: NDFC can transfer data regardless of the internal NDFC_RB wire 1: NDFC can transfer data when the internal NDFC_RB wire is READY; otherwise it can't when the internal NDFC_RB wire is BUSY.
22	R/W	0x0	NDFC_SEND_FIRST_CMD 0: Don't send first set command 1: Send it on the external memory's bus
21	R/W	0x0	NDFC_DATA_TRANS 0: No data transfer on external memory bus 1: Data transfer and direction is decided by the field NDFC_ACCESS_DIR
20	R/W	0x0	NDFC_ACCESS_DIR 0: Read NAND Flash 1: Write NAND Flash
19	R/W	0x0	NDFC_SEND_ADR 0: Don't send ADDRESS 1: Send N cycles ADDRESS, the number N is specified by NDFC_ADR_NUM field
18:16	R/W	0x0	NDFC_ADR_NUM Address Cycles' Number 000: 1 cycle address field 001: 2 cycles address field 010: 3 cycles address field 011: 4 cycles address field 100: 5 cycles address field 101: 6 cycles address field 110: 7 cycles address field 111: 8 cycles address field
15:10	/	/	/
9:8	R/W	0x0	NDFC_ADR_NUM_IN_PAGE_CMD The number of address cycles during page command. 00: 2 address cycles 11: 5 address cycles Others: reserved
7:0	R/W	0x0	NDFC_CMD_LOW_BYTE NDFC Command low byte data This command will be sent to external Flash by NDFC.

4.2.5.11. NDFC Command Set Register 0(Default Value: 0x00E0_0530)

Offset: 0x0028			Register Name: NDFC_CMD_SET0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x00	NDFC_RANDOM_CMD2 Used for Batch Operation

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23:16	R/W	0xE0	NDFC_RANDOM_READ_CMD1 Used for Batch Read Operation
15:8	R/W	0x05	NDFC_RANDOM_READ_CMD0 Used for Batch Read Operation
7:0	R/W	0x30	NDFC_READ_CMD Used for Batch Read Operation

4.2.5.12. NDFC Command Set Register 1(Default Value: 0x7000_8510)

Offset: 0x002C			Register Name: NDFC_CMD_SET1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x70	NDFC_READ_CMD0 Used for EF-NAND Page Read operation
23:16	R/W	0x00	NDFC_READ_CMD1 Used for EF-NAND Page Read operation
15:8	R/W	0x85	NDFC_RANDOM_WRITE_CMD Used for Batch Write Operation
7:0	R/W	0x10	NDFC_PROGRAM_CMD Used for Batch Write Operation

4.2.5.13. NDFC ECC Control Register(Default Value: 0x4a80_0008)

Offset: 0x0034			Register Name: NDFC_ECC_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:16	R/W	0x4a80	NDFC_RANDOM_SEED The seed value for randomize engine. It is only active when NDFC_RANDOM_EN is set to '1'.
15:8	R/W	0x0	NDFC_ECC_MODE 00000000: BCH-16 00000001: BCH-24 00000010: BCH-28 00000011: BCH-32 00000100: BCH-40 00000101: BCH-44 00000110: BCH-48 00000111: BCH-52 00001000: BCH-56 00001001: BCH-60 00001010: BCH-64 00001011: BCH-68 00001100: BCH-72 00001101: BCH-76

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			00001110: BCH-80 Others : Reserved
7	R/W	0x0	NDFC_RANDOM_SIZE 0: ECC block size 1: Page size
6	R/W	0x0	NDFC_RANDOM_DIRECTION 0: LSB first 1: MSB first
5	R/W	0x0	NDFC_RANDOM_EN 0: Disable Data Randomize 1: Enable Data Randomize
4	R/W	0x0	NDFC_ECC_EXCEPTION 0: Normal ECC 1: For ECC, there is an exception. If all data is 0xff or 0x00 for the block. When reading this page, ECC assumes that it is right. For this case, no error information is reported. It only is active when ECC is ON
3	R/W	0x1	NDFC_ECC_PIPELINE Pipeline function enable or disable for batch command 0: Error Correction function no pipeline with next block operation 1: Error Correction pipeline
2:1	/	/	/
0	R/W	0x0	NDFC_ECC_EN 0: ECC is OFF 1: ECC is ON

4.2.5.14. NDFC ECC Status Register(Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: NDFC_ECC_ST
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 31 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[31] of this register is corresponding the thirty-first ECC data block. 1 ECC Data Block = 1024 bytes.
30	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 30 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[30] of this register is corresponding the thirtieth ECC data block. 1 ECC Data Block = 1024 bytes.
29	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 29

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			0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[29] of this register is corresponding the twenty-ninth ECC data block. 1 ECC Data Block = 1024 bytes.
28	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 28 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[28] of this register is corresponding the twenty-eighth ECC data block. 1 ECC Data Block = 1024 bytes.
27	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 27 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[27] of this register is corresponding the twenty-seventh ECC data block. 1 ECC Data Block = 1024 bytes.
26	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 26 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[26] of this register is corresponding the twenty-sixth ECC data block. 1 ECC Data Block = 1024 bytes.
25	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 25 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[25] of this register is corresponding the twenty-fifth ECC data block. 1 ECC Data Block = 1024 bytes.
24	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 24 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[24] of this register is corresponding the twenty-fourth ECC data block. 1 ECC Data Block = 1024 bytes.
23	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 23 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[23] of this register is corresponding the twenty-third ECC data block. 1 ECC Data Block = 1024 bytes.
22	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 22 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[22] of this register is corresponding the twenty-second ECC data block. 1

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			ECC Data Block = 1024 bytes.
21	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 21 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[21] of this register is corresponding the twenty-first ECC data block. 1 ECC Data Block = 1024 bytes.
20	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 20 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[20] of this register is corresponding the twentieth ECC data block. 1 ECC Data Block = 1024 bytes.
19	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 19 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[19] of this register is corresponding the nineteenth ECC data block. 1 ECC Data Block = 1024 bytes.
18	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 18 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[18] of this register is corresponding the eighteenth ECC data block. 1 ECC Data Block = 1024 bytes.
17	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 17 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[17] of this register is corresponding the seventeenth ECC data block. 1 ECC Data Block = 1024 bytes.
16	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 16 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[16] of this register is corresponding the sixteenth ECC data block. 1 ECC Data Block = 1024 bytes.
15	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 15 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[15] of this register is corresponding the fifteenth ECC data block. 1 ECC Data Block = 1024 bytes.
14	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 14

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			0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[14] of this register is corresponding the fourteenth ECC data block. 1 ECC Data Block = 1024 bytes.
13	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 13 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[13] of this register is corresponding the thirteenth ECC data block. 1 ECC Data Block = 1024 bytes.
12	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 12 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[12] of this register is corresponding the twelfth ECC data block. 1 ECC Data Block = 1024 bytes.
11	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 11 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[11] of this register is corresponding the eleventh ECC data block. 1 ECC Data Block = 1024 bytes.
10	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 10 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[10] of this register is corresponding the Tenth ECC data block. 1 ECC Data Block = 1024 bytes.
9	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 9 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[9] of this register is corresponding the ninth ECC data block. 1 ECC Data Block = 1024 bytes.
8	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 8 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[8] of this register is corresponding the eighth ECC data block. 1 ECC Data Block = 1024 bytes.
7	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 7 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[7] of this register is corresponding the seventh ECC data block. 1 ECC Data

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			Block = 1024 bytes.
6	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 6 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[6] of this register is corresponding the sixth ECC data block. 1 ECC Data Block = 1024 bytes.
5	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 5 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[5] of this register is corresponding the fifth ECC data block. 1 ECC Data Block = 1024 bytes.
4	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 4 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[4] of this register is corresponding the fourth ECC data block. 1 ECC Data Block = 1024 bytes.
3	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 3 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[3] of this register is corresponding the third ECC data block. 1 ECC Data Block = 1024 bytes.
2	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 2 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[2] of this register is corresponding the second ECC data block. 1 ECC Data Block = 1024 bytes.
1	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 1 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[1] of this register is corresponding the first ECC data block. 1 ECC Data Block = 1024 bytes.
0	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 0 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them The bit[0] of this register is corresponding the zero one ECC data block. 1 ECC Data Block = 1024 bytes.

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4.2.5.15. NDFC Data Pattern Status Register(Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: NDFC_DATA_PAT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 31 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
30	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 30 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
29	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 29 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
28	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 28 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
27	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 27 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
26	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 26 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
25	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 25 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
24	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 24 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
23	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 23 when read from

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			external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
22	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 22 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
21	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 21 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
20	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 20 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
19	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 19 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
18	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 18 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
17	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 17 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
16	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 16 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
15	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 15 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
14	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 14 when read from

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			external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
13	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 13 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
12	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 12 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
11	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 11 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
10	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 10 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
9	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 9 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
8	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 8 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
7	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 7 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
6	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 6 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
5	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 5 when read from

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			external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
4	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 4 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
3	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 3 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
2	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 2 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
1	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 1 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
0	R	0x0	Special pattern (all 0x00 or all x0ff) Found Flag for Data Block 0 when read from external NAND flash. 0: No Found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.

4.2.5.16. NDFC Enhanced Feature Register(Default Value: 0x0000_0000)

Offset: 0x0040			**Register Name: NDFC_EFR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DB_CNT_EN Dummy_Byte_Count_EN 0:Disable fill Dummy Byte. 1:Enable fill Dummy Byte.
23:16	R/W	0x0	DB_CNT Dummy_Byte_Count After PAGE CMD operation finishing sending out the main data , user data and ECC code, controller would send dummy byte to fill the unused space in one page.

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			NOTE **It is only valid in PAGE CMD operation(*NDFC_CMD_TYPE*=0x3).** **This function is disable when *Dummy_Byte_Count_EN*=0.**
15:9	/	/	/
8	R/W	0x0	NDFC_WP_CTRL NAND Flash Write Protect Control Bit 0: Write Protect is active 1: Write Protect is not active When this bit is '0', WP signal line is low level and external NAND flash is on protected state.
7	/	/	/
6:0	R/W	0x0	NDFC_ECC_DEBUG For the purpose of debugging ECC engine, special bits error are inserted before writing external Flash Memory. 0: No error is inserted (ECC Normal Operation) n: N bits error are inserted

4.2.5.17. NDFC Read Data Status Control Register(Default Value: 0x0100_0000)

Offset: 0x0044			**Register Name: NDFC_RDATA_STA_CTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x1	NDFC_RDATA_STA_EN 0: Disable to count the number of bit 1 and bit 0 during current read operation; 1: Enable to count the number of bit 1 and bit 0 during current read operation; The number of bit 1 and bit 0 during current read operation can be used to check whether a page is blank or bad.
23:19	/	/	/
18:0	R/W	0x0	NDFC_RDATA_STA_TH The threshold value to generate data status. If the number of bit 1 during current read operation is less than or equal to threshold value, the bit 13 of NDFC_ST register will be set. If the number of bit 0 during current read operation is less than or equal to threshold value, the bit 12 of NDFC_ST register will be set.

4.2.5.18. NDFC Read Data Status Register 0(Default Value: 0x0000_0000)

Offset: 0x0048			**Register Name: NDFC_RDATA_STA_0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	BIT_CNT_1 The number of input bit 1 during current command. It will be cleared automatically when next command is executed.

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4.2.5.19. NDFC Read Data Status Register 1(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: NDFC_RDATA_STA_1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	BIT_CNT_0 The number of input bit 0 during current command. It will be cleared automatically when next command is executed.

4.2.5.20. NDFC Error Counter Register N(Default Value: 0x0000_0000)

Offset: 0x0050+N*0x04(N=0~7)			Register Name: NDFC_ERR_CNT_N
Bit	**Read/Write**	**Default/Hex**	**Description**
[8M+7: 8M] (M=0~3)	R	0x00	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[N*0x04+M] 00000000: No corrected bits 00000001: 1 corrected bit 00000010: 2 corrected bits ..... 01010000 : 80 corrected bits Others: Reserved 1 ECC Data Block =1024 bytes

4.2.5.21. NDFC User Data Length Register N(Default Value: 0x0000_0000)

Offset: 0x0070 + N*0x04(N=0~3)			Register Name: NDFC_USER_DATA_LEN_N
Bit	**Read/Write**	**Default/Hex**	**Description**
[M*4+3:M*4] (M=0~7)	R/W	0x0	It's used to indicate user data's length of ECC DATA BLOCK[0x08*N+M]. 0000 : no user data 0001 : 04bytes user data 0010 : 08bytes user data 0011 : 12bytes user data 0100 : 16bytes user data 0101 : 20bytes user data 0110 : 24bytes user data 0111 : 28bytes user data 1000 : 32bytes user data Other : reserved

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4.2.5.22. NDFC User Data Register N(Default Value: 0xffff_ffff)

Offset: 0x0080 + N*0x04(N=0~31)			Register Name: NDFC_USER_DATA_N
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0xffffffff	USER_DATA All of the user data in one page is stored in these NDFC_USER_DATA_N. The start register address of each ECC DATA BLOCK's user data is determined by its length configured in NDFC_USER_DATA_LEN_N. For example: ECC DATA BLOCK[0] user data len = 8 Bytes, address = 0x80 ECC DATA BLOCK[1] user data len = 0 Bytes, ECC DATA BLOCK[2] user data len = 4 Bytes, address = 0x80+8 ECC DATA BLOCK[3] user data len = 4 Bytes, address = 0x80+8+4 ECC DATA BLOCK[4] user data len = 0 Bytes ECC DATA BLOCK[5] user data len = 16 Bytes, address = 0x80+8+4+4 ECC DATA BLOCK[6] user data len = 0 Bytes ECC DATA BLOCK[7] user data len = 0 Bytes

4.2.5.23. NDFC EFNAND STATUS Register(Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: NDFC_EFNAND_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	EF_NAND_STATUS The Status Value for EF-NAND Page Read operation

4.2.5.24. NDFC Spare Area Register(Default Value: 0x0000_0400)

Offset: 0x0114			Register Name: NDFC_SPARE_AREA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x400	NDFC_SPARE_ADR This value indicates the spare area first byte address for NDFC interleave page operation.

4.2.5.25. NDFC Pattern ID Register(Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: NDFC_PAT_ID
Bit	**Read/Write**	**Default/Hex**	**Description**
n (n=0~31)	R	0x0	PAT_ID Special Pattern ID for ECC data block[n] 0: All 0x00 is found

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			1: All 0xFF is found

4.2.5.26. NDFC DDR2 Specific Control Register(Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: NDFC_DDR2_SPEC_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:12	R/W	0x0	DLEN_WR The number of latency DQS cycle for write. 0000: No latency 0001: One latency DQS cycle 0010: Two latency DQS cycle 0011: Four latency DQS cycle
11:8	R/W	0x0	DLEN_RD The number of latency DQS cycle for read. 0000: No latency 0001: One latency DQS cycle 0010: Two latency DQS cycle 0011: Four latency DQS cycle
7:3	/	/	/
2	R/W	0x0	EN_RE_C Enable the complementary RE# signal. 0: Disable 1: Enable
1	R/W	0x0	EN_DQS_C Enable the complementary DQS signal. 0: Disable 1: Enable
0	/	/	/

4.2.5.27. NDFC Normal DMA Mode Control Register(Default Value: 0x0000_00E5)

Offset: 0x0120			Register Name: NDFC_NDMA_MODE_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R/W	0x11	DMA_ACT_STA 00:dma_active is low 01:dma_active is high 10:dma_active is controlled by dma_request(DRQ) 11:dma_active is controlled by controller
5	R/W	0x1	DMA_ACK_EN 0: active fall do not care ack 1: active fall must after detect ack is high

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4:0	R/W	0x05	DELAY_CYCLE The delay cycles The counts of hold cycles from DMA last signal high to dma_active high

4.2.5.28. NDFC MBUS DMA Descriptor List Base Address Register(Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: NDFC_MDMA_DLBA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	NFC_MDMA_DESC_BASE_ADDR Start Address of Descriptor List. Contains the base address of the First Descriptor. The LSB bits [1:0] are ignored and taken as all-zero by the DMA internally. Hence these LSB bits are read-only.

4.2.5.29. NDFC MBUS DMA Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0204			Register Name: NDFC_MDMA_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	NFC_MDMA_TRANS_FINISH_INT Transfer Finish Interrupt. Indicates that data transmission is finished for a descriptor. Writing a '1' clears this bit. Bit 0: Corresponding DMA descriptor 0 Bit 1: Corresponding DMA descriptor 1 … Bit 31: Corresponding DMA descriptor 31

4.2.5.30. NDFC MBUS DMA Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: 0x0208			Register Name: NDFC_DMA_INT_MASK
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	NFC_MDMA_TRANS _INT_ENB Transfer Interrupt Enable. When set, Transmit Interrupt is enabled. When reset, Transmit Interrupt is disabled. Bit 0: Corresponding DMA descriptor 0 Bit 1: Corresponding DMA descriptor 1 … Bit 31: Corresponding DMA descriptor 31

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4.2.5.31. NDFC MBUS DMA Current Descriptor Address Register(Default Value: 0x0000_0000)

Offset: 0x020C			Register Name: NDFC_MDMA_CUR_DESC_ADDR
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CUR_DESC_ADDR Current Descriptor Address Pointer. Cleared on reset. Pointer updated by DMA during operation. This register points to the start address of the current descriptor read by the DMA.

4.2.5.32. NDFC MBUS DMA Current Buffer Address Register(Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: NDFC_MDMA_CUR_BUF_ADDR
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CUR_BUFF_ADDR Current Buffer Address Pointer. Cleared on Reset. Pointer updated by DMA during operation. This register points to the current Data Buffer Address being accessed by the DMA.

4.2.5.33. NDFC DMA Byte Counter Register(Default Value: 0x0000_0000)

Offset: 0x214			Register Name: NDFC_DMA_CNT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	DMA_CNT DMA data counter for DMA, only is valid for Normal DMA

4.2.5.34. NDFC EMCE Control Register(Default Value: 0x0000_0000)

Offset: 0x218			Register Name: NDFC_EMCE_CTL
Bit	Read/Write	Default	Description
31:2	/	/	/
1:0	R/W	0x0	NDFC_EMCE_ENABLE_TYPE 00 : Disable encryption/decryption and bypass the EMCE module. 01 : Reserved 10: Disable encryption/decryption but not bypass the EMCE module. 11: Enable encryption/decryption.

4.2.5.35. NDFC EMCE IV_FAC Compare Value Register(Default Value: 0x0000_0000)

Offset: 0x21C			Register Name: NDFC_EMCE_IV_FAC_CMP_VAL
Bit	Read/Write	Default/Hex	Description

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31:0	R/W	0x0	NDFC_EMCE_IV_FAC_CMP_VAL This value is set by user. It is EMCE IV factor compare value.

4.2.5.36. NDFC EMCE IV Calculate Factor Register N(Default Value: 0x0000_0000)

Offset: 0x220+0x04*N(N=0 to 31)			Register Name: NDFC_EMCE_IV_CAL_FACTOR_N
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	NDFC_EMCE_IV_CAL_FACTOR_N This factor is set by user. If factor is equal to NDFC_EMCE_CMP_VAL, the corresponding sector don't need encryption. If factor is not equal to NDFC_EMCE_CMP_VAL, the corresponding sector need encryption, and its IV factor specified by this register. **NOTE** **NDFC EMCE don't support 32KB page_size.**

4.2.5.37. NDFC IO Data Register(Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: NDFC_IO_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	NDFC_IO_DATA Read/ Write data into internal RAM Access unit is 32-bit.

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4.3. SD/MMC Host Controller(SMHC)

4.3.1. Overview

The SD-MMC Host controller(SMHC) can be configured either as a Secure Digital Multimedia Card controller, which simultaneously supports Secure Digital memory (SD Memory), UHS-1 Card, Secure Digital I/O (SDIO), Multimedia Cards (MMC), eMMC.

Features:

- Supports eMMC boot operation and alternative boot operation
- Supports Command Completion signal and interrupt to host processor and Command Completion Signal disable feature
- SMHC0 supports SD (Verson1.0 to 3.0),4-bit bus width
  - SDR mode 50MHz@3.3V IO pad
- SMHC1 supports SDIO(Version1.1 to 3.0),4-bit bus width
  - SDR mode 50MHz@3.3V IO pad
  - SDR mode 150MHz@1.8V IO pad
  - DDR mode 50MHz@1.8V IO pad
- SMHC2 supports MMC(Verson3.x to 4.2),eMMC(Verson4.3-5.0,compatible with 5.1),8-bit bus width
  - SDR mode 150Mhz@1.8V IO pad
  - DDR mode 100Mhz@1.8V IO pad
  - DDR mode 50Mhz@3.3V IO pad
- Supports hardware CRC generation and error detection
- Supports programmable baud rate
- Supports host pull-up control
- Supports SDIO interrupts in 1-bit and 4-bit modes
- Supports SDIO suspend and resume operation
- Supports SDIO read wait
- Supports block size of 1 to 65535 bytes
- Supports descriptor-based internal DMA controller
- Internal 1KB FIFO for data transfer
- Supports inline encryption and decryption based on EMCE(Embedded Crypto Engine)

4.3.2. Block Diagram

Figure 4-17 shows a block diagram of the SMHC.

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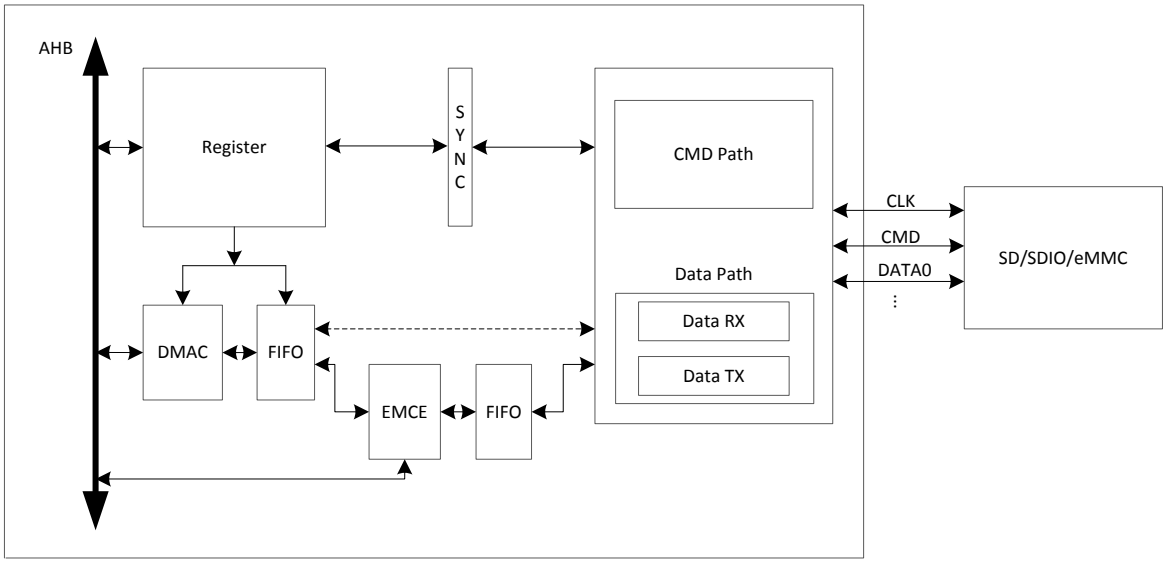


Figure 4-17. SMHC Block Diagram

4.3.3. Operations and Functional Descriptions

4.3.3.1. External Signals

Table 4-3 describes the external signals of SMHC.

Table 4-3. SMHC External Signals

Port Name	Width	Direction	Description
SDC0_CLK	1	O	Clock output for SD/TF card
SDC0_CMD	1	I/O	CMD line for SD/TF card
SDC0_D[i] (i=0~3)	4	I/O	Data line for SD/TF card
SDC1_CLK	1	O	Clock output for SDIO Wi-Fi
SDC1_CMD	1	I/O	CMD line for SDIO Wi-Fi
SDC1_D[i] (i=0~3)	4	I/O	Data line for SDIO Wi-Fi
SDC2_CLK	1	O	Clock output for MMC
SDC2_CMD	1	I/O	CMD line for MMC
SDC2_D[i] (i=0~7)	8	I/O	Data line for MMC
SDC2_RST	1	O	Reset signal for MMC
SDC2_DS	1	I	Data Strobe for MMC

4.3.3.2. Clock Sources

Each SMHC gets three different clocks. User can select one of them to make SMHC clock source. Table 4-4 describes the clock sources of SMHC. Users can see CCU in chapter 3.3 for clock setting, configuration and gating information.

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Table 4-4. SMHC Clock Sources

Clock Sources	Description
OSC24M	24MHz Crystal
PLL_PERIPH0(2X)	Peripheral Clock, the default value is 1.2GHz
PLL_PERIPH1(2X)	Peripheral Clock, the default value is 1.2GHz

4.3.3.3. SMHC Timing Diagram

Please refer to relative specifications:

- Physical Layer Specification Ver3.00 Final
- SDIO Specification Ver2.00
- Multimedia Cards (MMC – version 4.2)
- JEDEC Standard – JESD84-44, Embedded Multimedia Card(eMMC) Card Product Standard
- JEDEC Standard – JESD84-B45, Embedded Multimedia Card(eMMC) Electrical Standard(4.5 Device)
- JEDEC Standard – JESD84-B50, Embedded Multimedia Card (eMMC) Electrical Standard(5.0)

4.3.3.4. Internal DMA Controller Description

SD/MMC controller has an internal DMA controller (IDMAC) to transfer data between host memory and SDMMC port. With a descriptor, IDMAC can efficiently move data from source to destination by automatically loading next DMA transfer arguments, which need less CPU intervention. Before transfer data in IDMAC, host driver should construct a descriptor list, configure arguments of every DMA transfer, then launch the descriptor and start the DMA. IDMAC has an interrupt controller, when enabled, it can interrupt the HOST CPU in situations such as data transmission completed or some errors happened.

4.3.3.4.1. IDMAC Descriptor Structure

The IDMAC uses a descriptor with a chain structure, and each descriptor points to a unique buffer and the next descriptor.

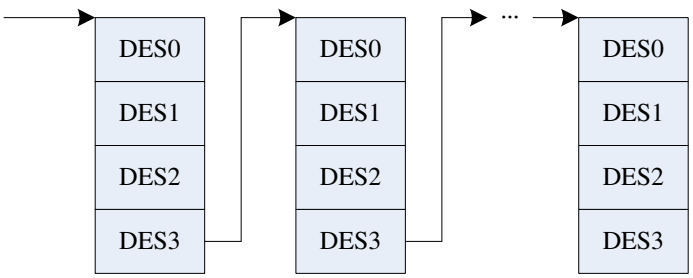


Figure 4-18. IDMAC Descriptor Structure Diagram

This figure illustrates the internal formats of a descriptor. The descriptor address must be aligned to the bus width used for 32-bit buses. Each descriptor contains 16 bytes of control and status information.

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DES0 is a notation used to denote the [31:0] bits, DES1 to denote [63:32] bits, DES2 to denote [95:64] bits, and DES3 to denote [127:96] bits in a descriptor.

4.3.3.4.2. DES0 Definition

Bits	Name	Descriptor
31	HOLD	DES_OWN_FLAG When set, this bit indicates that the descriptor is owned by the IDMAC. When this bit is reset, it indicates that the descriptor is owned by the host. This bit is cleared when transfer is over.
30	ERROR	ERR_FLAG When some error happened in transfer, this bit will be set.
29:5	/	/
4	Chain Flag	CHAIM_MOD When set, this bit indicates that the second address in descriptor is the next descriptor address. Must be set 1.
3	First DES Flag	FIRST_FLAG When set, this bit indicates that this descriptor contains the first buffer of data. Must be set to 1 in first DES.
2	Last DES Flag	LAST_FLAG When set, this bit indicates that the buffers pointed to by this descriptor are the last data buffer
1	Disable Interrupt on completion	CUR_TXRX_OVER_INT_DIS When set, this bit will prevent the setting of the TX/RX interrupt bit of the IDMAC status register for data that ends in the buffer pointed to by this descriptor
0	/	/

4.3.3.4.3. DES1 Definition

SMHC0/SMCH1

Bits	Name	Descriptor
31:16	/	/
15:0	Buffer size	BUFF_SIZE These bits indicate the data buffer byte size, which must be a multiple of 4 bytes. If this filed is 0, the DMA ignores this buffer and proceeds to the next descriptor.

SMHC2

Bits	Name	Descriptor
31:13	/	/

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12:0	Buffer size	BUFF_SIZE These bits indicate the data buffer byte size, which must be a multiple of 4 bytes. If this filed is 0, the DMA ignores this buffer and proceeds to the next descriptor.

4.3.3.4.4. DES2 Definition

Bits	Name	Descriptor
31:0	Buffer address pointer	BUFF_ADDR These bits indicate the physical address of data buffer. The IDMAC ignores DES2[1:0], corresponding to the bus width of 32.

4.3.3.4.5. DES3 Definition

Bits	Name	Descriptor
31:0	Next descriptor address	NEXT_DESP_ADDR These bits indicate the pointer to the physical memory where the next descriptor is present.

4.3.3.5. Calibrate Delay Chain

The sample clock delay chain and Data Strobe delay chain(only in SMHC2) are used to generate delay to make proper timing between sample clock/Data Strobe and data signals. Each delay chain is made up with 64 delay cells. The delay time of one delay cell can be estimated through delay chain calibration.

The steps to calibrate delay chain are as follows:

Step1: Enable SMHC. In order to calibrate delay chain by operation registers in SMHC, SMHC must be enabled through *SMHC Bus Gating Reset Register* and *SMHC2 Clock Register*.

Step2: Configure a proper clock for SMHC. Calibration delay chain is based on the clock for SMHC from Clock Control Unit(CCU). Calibration delay chain a internal function in SMHC and don't need device. So, it is unnecessary to open clock signal for device. The recommended clock frequency is 200MHz.

Step3: Set proper initial delay value. Writing 0xA0 to *delay control register* enables *Delay Software Enable*_(bit[7]) and sets initial delay value 0x20 to *Delay chain*(bit[5:0]). Then write 0x0 to *delay control register* to clear the value.

Step4: Write 0x8000 to *delay control register* to start calibrate delay chain.

Step5: Wait until the flag(Bit14 in *delay control register*) of calibration done is set. The number of delay cells is shown at Bit8~Bit13 in *delay control register*. The delay time generated by these delay cells is equal to the cycle of SMHC's clock nearly. This value is the result of calibration.

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Step6: Calculate the delay time of one delay cell according to the cycle of SMHC's clock and the result of calibration.

NOTE

In the above descriptions,*delay control register* contains SMHC Sample Delay Control Register and SMHC Data Strobe Delay Control Register.*Delay Software Enable* contains Sample Delay Software Enable and Data Strobe Delay Software Enable. *Delay chain* contains Sample Delay Software and Data Strobe Delay Software.

4.3.4. Register List

Module Name	Base Address
SMHC0	0x04020000
SMHC1	0x04021000
SMHC2	0x04022000

Register Name	Offset	Description
SMHC_CTRL	0x0000	Control Register
SMHC_CLKDIV	0x0004	Clock Control Register
SMHC_TMOUT	0x0008	Time Out Register
SMHC_CTYPE	0x000C	Bus Width Register
SMHC_BLKSIZ	0x0010	Block Size Register
SMHC_BYTCNT	0x0014	Byte Count Register
SMHC_CMD	0x0018	Command Register
SMHC_CMDARG	0x001C	Command Argument Register
SMHC_RESP0	0x0020	Response 0 Register
SMHC_RESP1	0x0024	Response 1 Register
SMHC_RESP2	0x0028	Response 2 Register
SMHC_RESP3	0x002C	Response 3 Register
SMHC_INTMASK	0x0030	Interrupt Mask Register
SMHC_MINTSTS	0x0034	Masked interrupt Status Register
SMHC_RINTSTS	0x0038	Raw Interrupt Status Register
SMHC_STATUS	0x003C	Status Register
SMHC_FIFOTH	0x0040	FIFO Water Level Register
SMHC_FUNS	0x0044	FIFO Function Select Register
SMHC_TCBCNT	0x0048	Transferred Byte Count between Controller and Card
SMHC_TBBCNT	0x004C	Transferred Byte Count between Host Memory and Internal FIFO
SMHC_CSDC	0x0054	CRC Status Detect Control Register
SMHC_A12A	0x0058	Auto Command 12 Argument Register
SMHC_NTSR	0x005C	SD New Timing Set Register
SMHC_SDBG	0x0060	SD New Timing Set Debug Register
SMHC_EMCE	0x0064	Embedded Encrypt and Decrypt Control Register

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SMHC_EMCE_DBG	0x0068	Embedded Encrypt and Decrypt Debug Register
/	0x006C-0x0074	Reserved
SMHC_HWRST	0x0078	Hardware Reset Register
/	0x007C	Reserved
SMHC_DMAC	0x0080	DMA Control Register
SMHC_DLBA	0x0084	Descriptor List Base Address Register
SMHC_IDST	0x0088	DMAC Status Register
SMHC_IDIE	0x008C	DMAC Interrupt Enable Register
/	0x0098-0x00FC	Reserved
SMHC_THLD	0x0100	Card Threshold Control Register
/	0x0104-0x0108	Reserved
SMHC_EDSD	0x010C	eMMC4.5 DDR Start Bit Detection Control Register
SMHC_RES_CRC	0x0110	Response CRC from Device
SMHC_D7_CRC	0x0114	CRC in Data7 from Device
SMHC_D6_CRC	0x0118	CRC in Data6 from Device
SMHC_D5_CRC	0x011C	CRC in Data5 from Device
SMHC_D4_CRC	0x0120	CRC in Data4 from Device
SMHC_D3_CRC	0x0124	CRC in Data3 from Device
SMHC_D2_CRC	0x0128	CRC in Data2 from Device
SMHC_D1_CRC	0x012C	CRC in Data1 from Device
SMHC_D0_CRC	0x0130	CRC in Data0 from Device
SMHC_CRC_STA	0x0134	CRC Status from Device in Write Operation
/	0x0138-0x013C	Reserved
SMHC_DRV_DL	0x0140	Drive Delay Control Register
SMHC_SMAP_DL	0x0144	Sample Delay Control Register
SMHC_DS_DL	0x0148	Data Strobe Delay Control Register
/	0x014C	Reserved
SMHC_EMCE_BMN	0x0150-0x01CC	Embedded Encrypt and Decrypt Bitmap Register n(n:0~31)
/	0x01D0-0x01FC	Reserved
SMHC_FIFO	0x0200	Read/ Write FIFO

4.3.5. Register Description

4.3.5.1. SMHC Global Control Register(Default Value: 0x0000_0100)

Offset: 0x0000			**Register Name: SMHC_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	FIFO_AC_MOD FIFO Access Mode 1: AHB bus 0: DMA bus
30:13	/	/	/
12	R/W	0x0	TIME_UNIT_CMD

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			Time unit for command line Time unit used to calculate command line time out value defined in RTO_LMT. 0: 1 card clock period 1: 256 card clock period
11	R/W	0x0	TIME_UNIT_DAT Time unit for data line Time unit used to calculate data line time out value defined in DTO_LMT. 0: 1 card clock period 1: 256 card clock period
10	R/W	0x0	DDR_MOD_SEL DDR Mode Select Although eMMC's HS400 speed mode is 8-bit DDR, this filed should be cleared when HS400_MD_EN is set. 0: SDR mode 1: DDR mode
9	/	/	/
8	R/W	0x1	CD_DBC_ENB Card Detect (Data[3] status) De-bounce Enable 0: Disable de-bounce 1: Enable de-bounce
7:6	/	/	/
5	R/W	0x0	DMA_ENB DMA Global Enable 0: Disable DMA to transfer data, using AHB bus 1: Enable DMA to transfer data
4	R/W	0x0	INT_ENB Global Interrupt Enable 0: Disable interrupts 1: Enable interrupts
3	/	/	/
2	R/W	0x0	DMA_RST DMA Reset
1	R/W	0x0	FIFO_RST FIFO Reset 0: No change 1: Reset FIFO This bit is auto-cleared after completion of reset operation.
0	R/W	0x0	SOFT_RST Software Reset 0: No change 1: Reset SD/MMC controller This bit is auto-cleared after completion of reset operation.

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4.3.5.2. SMHC Clock Control Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: SMHC_CLKDIV
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MASK_DATA0 0: Do not mask data0 when update clock 1: Mask data0 when update clock
30:18	/	/	/
17	R/W	0x0	CCLK_CTRL Card Clock Output Control 0 : Card clock always on 1 : Turn off card clock when FSM in IDLE state
16	R/W	0x0	CCLK_ENB Card Clock Enable 0: Card Clock off 1: Card Clock on
15:8	/	/	/
7:0	R/W	0x0	CCLK_DIV Card clock divider n: Source clock is divided by 2*n.(n=0~255) when HS400_MD_EN is set, this field must be cleared.

4.3.5.3. SMHC Timeout Register(Default Value:0xFFFF_FF40)

Offset: 0x0008			Register Name: SMHC_TMOUT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	R/W	0xffffff	DTO_LMT Data Timeout Limit
7:0	R/W	0x40	RTO_LMT Response Timeout Limit

4.3.5.4. SMHC Bus Width Register(Default Value:0x0000_0000)

Offset: 0x000C			Register Name: SMHC_CTYPE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	CARD_WID Card Width 00: 1-bit width 01: 4-bit width 1x: 8-bit width

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4.3.5.5. SMHC Block Size Register(Default Value:0x0000_0200)

Offset: 0x0010			Register Name: SMHC_BLKSIZ
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x200	BLK_SZ Block Size

4.3.5.6. SMHC Byte Count Register(Default Value:0x0000_0200)

Offset: 0x0014			Register Name: SMHC_BYTCNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x200	BYTE_CNT Byte counter Number of bytes to be transferred; should be integer multiple of Block Size for block transfers.

4.3.5.7. SMHC Command Register(Default Value:0x0000_0000)

Offset: 0x0018			Register Name: SMHC_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CMD_LOAD Start Command. This bit is auto cleared when current command is sent. If there is no any response error happened, a command complete interrupt bit (CMD_OVER) will be set in interrupt register. You should not write any other command before this bit is cleared, or a command busy interrupt bit (CMD_BUSY) will be set in interrupt register.
30:29	/	/	/
28	R/W	0x0	VOL_SW Voltage Switch 0: normal command 1: Voltage switch command, set for CMD11 only
27	R/W	0x0	BOOT_ABT Boot Abort Setting this bit will terminate the boot operation.
26	R/W	0x0	EXP_BOOT_ACK Expect Boot Acknowledge. When Software sets this bit along in mandatory boot operation, controller expects a boot acknowledge start pattern of 0-1-0 from the selected card.
25:24	R/W	0x0	BOOT_MOD Boot Mode

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			00: Normal command 01: Mandatory Boot operation 10: Alternate Boot operation 11: Reserved
23:22	/	/	/
21	R/W	0x0	PRG_CLK Change Clock 0: Normal command 1: Change Card Clock; when this bit is set, controller will change clock domain and clock output. No command will be sent.
20:16	/	/	/
15	R/W	0x0	SEND_INIT_SEQ Send Initialization 0: Normal command sending 1: Send initialization sequence before sending this command.
14	R/W	0x0	STOP_ABT_CMD Stop Abort Command 0: Normal command sending 1: Send Stop or abort command to stop current data transfer in progress.(CMD12, CMD52 for writing “I/O Abort” in SDIO CCCR)
13	R/W	0x0	WAIT_PRE_OVER Wait Data Transfer Over 0: Send command at once, do not care of data transferring 1: Wait for data transfer completion before sending current command
12	R/W	0x0	STOP_CMD_FLAG Send Stop CMD Automatically (CMD12) 0: Do not send stop command at end of data transfer 1: Send stop command automatically at end of data transfer
11	R/W	0x0	TRANS_MODE Transfer Mode 0: Block data transfer command 1: Stream data transfer command
10	R/W	0x0	TRANS_DIR Transfer Direction 0: Read operation 1: Write operation
9	R/W	0x0	DATA_TRANS Data Transfer 0: without data transfer 1: with data transfer
8	R/W	0x0	CHK_RESP_CRC Check Response CRC 0: Do not check response CRC 1: Check response CRC
7	R/W	0x0	LONG_RESP

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			Response Type 0:Short Response (48 bits) 1:Long Response (136 bits)
6	R/W	0x0	RESP_RCV Response Receive 0: Command without Response 1: Command with Response
5:0	R/W	0x0	CMD_IDX CMD Index Command index value

4.3.5.8. SMHC Command Argument Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: SMHC_CMDARG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CMD_ARG Command argument

4.3.5.9. SMHC Response 0 Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SMHC_RESP0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP0 Response 0 Bit[31:0] of response

4.3.5.10. SMHC Response 1 Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: SMHC_RESP1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP1 Response 1 Bit[63:31] of response

4.3.5.11. SMHC Response 2 Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: SMHC_RESP2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP2 Response 2 Bit[95:64] of response

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4.3.5.12. SMHC Response 3 Register(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: SMHC_RESP3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP3 Response 3 Bit[127:96] of response

4.3.5.13. SMHC Interrupt Mask Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: SMHC_INTMASK
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CARD_REMOVAL_INT_EN Card Removed Interrupt Enable
30	R/W	0x0	CARD_INSERT_INT_EN Card Inserted Interrupt Enable
29:17	/	/	/
16	R/W	0x0	SDIO_INT_EN SDIO Interrupt Enable
15	R/W	0x0	DEE_INT_EN Data End-bit Error Interrupt Enable
14	R/W	0x0	ACD_INT_EN Auto Command Done Interrupt Enable
13	R/W	0x0	DSE_BC_INT_EN Data Start Error Interrupt Enable
12	R/W	0x0	CB_IW_INT_EN Command Busy and Illegal Write Interrupt Enable
11	R/W	0x0	FU_FO_INT_EN FIFO Underrun/Overflow Interrupt Enable
10	R/W	0x0	DSTO_VSD_INT_EN Data Starvation Timeout/V1.8 Switch Done Interrupt Enable
9	R/W	0x0	DTO_BDS_INT_EN Data Timeout/Boot Data Start Interrupt Enable
8	R/W	0x0	RTO_BACK_INT_EN Response Timeout/Boot ACK Received Interrupt Enable
7	R/W	0x0	DCE_INT_EN Data CRC Error Interrupt Enable
6	R/W	0x0	RCE_INT_EN Response CRC Error Interrupt Enable
5	R/W	0x0	DRR_INT_EN Data Receive Request Interrupt Enable
4	R/W	0x0	DTR_INT_EN

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			Data Transmit Request Interrupt Enable
3	R/W	0x0	DTC_INT_EN Data Transfer Complete Interrupt Enable
2	R/W	0x0	CC_INT_EN Command Complete Interrupt Enable
1	R/W	0x0	RE_INT_EN Response Error Interrupt Enable
0	/	/	/

4.3.5.14. SMHC Masked Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: SMHC_MINTSTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	M_CARD_REMOVAL_INT Card Removed
30	R/W	0x0	M_CARD_INSERT Card Inserted
29:17	/	/	/
16	R/W	0x0	M_SDIO_INT SDIO Interrupt
15	R/W	0x0	M_DEE_INT Data End-bit Error When set during receiving data, it means that host controller does not receive valid data end bit. When set during transmitting data, it means that host controller does not receive CRC status taken or received CRC status taken is negative.
14	R/W	0x0	M_ACD_INT Auto Command Done When set, it means auto stop command(CMD12) completed.
13	R/W	0x0	M_DSE_BC_INT Data Start Error When set during receiving data, it means that host controller found a error start bit. When set during transmitting data, it means that busy signal is cleared.
12	R/W	0x0	M_CB_IW_INT Command Busy and Illegal Write
11	R/W	0x0	M_FU_FO_INT FIFO Underrun/Overflow
10	R/W	0x0	M_DSTO_VSD_INT Data Starvation Timeout/V1.8 Switch Done
9	R/W	0x0	M_DTO_BDS_INT Data Timeout/Boot Data Start
8	R/W	0x0	M_RTO_BACK_INT Response Timeout/Boot ACK Received

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7	R/W	0x0	M_DCE_INT Data CRC Error When set during receiving data, it means that the received data have data CRC error. When set during transmitting data, it means that the received CRC status taken is negative.
6	R/W	0x0	M_RCE_INT Response CRC Error
5	R/W	0x0	M_DRR_INT Data Receive Request When set, it means that there are enough data in FIFO during receiving data.
4	R/W	0x0	M_DTR_INT Data Transmit Request When set, it means that there are enough space in FIFO during transmitting data.
3	R/W	0x0	M_DTC_INT Data Transfer Complete
2	R/W	0x0	M_CC_INT Command Complete
1	R/W	0x0	M_RE_INT Response Error When set, Transmit Bit error or End Bit error or CMD Index error may occurs.
0	/	/	/

4.3.5.15. SMHC Raw Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0038			**Register Name: SMHC_RINTSTS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W1C	0x0	CARD_REMOVAL Card Removed This is write-1-to-clear bits.
30	R/W1C	0x0	CARD_INSERT Card Inserted This is write-1-to-clear bits.
29:17	/	/	/
16	R/W1C	0x0	SDIOI_INT SDIO Interrupt This is write-1-to-clear bits.
15	R/W1C	0x0	DEE Data End-bit Error When set during receiving data, it means that host controller does not receive valid data end bit.

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			When set during transmitting data, it means that host controller does not receive CRC status taken. This is write-1-to-clear bits.
14	R/W1C	0x0	ACD Auto Command Done When set, it means auto stop command(CMD12) completed. This is write-1-to-clear bits.
13	R/W1C	0x0	DSE_BC Data Start Error When set during receiving data, it means that host controller found a error start bit. When set during transmitting data, it means that busy signal is cleared. This is write-1-to-clear bits.
12	R/W1C	0x0	CB_IW Command Busy and Illegal Write This is write-1-to-clear bits.
11	R/W1C	0x0	FU_FO FIFO Underrun/Overflow This is write-1-to-clear bits.
10	R/W1C	0x0	DSTO_VSD Data Starvation Timeout/V1.8 Switch Done This is write-1-to-clear bits.
9	R/W1C	0x0	DTO_BDS Data Timeout/Boot Data Start This is write-1-to-clear bits.
8	R/W1C	0x0	RTO_BACK Response Timeout/Boot ACK Received This is write-1-to-clear bits.
7	R/W1C	0x0	DCE Data CRC Error When set during receiving data, it means that the received data have data CRC error. When set during transmitting data, it means that the received CRC status taken is negative. This is write-1-to-clear bits.
6	R/W1C	0x0	RCE Response CRC Error This is write-1-to-clear bits.
5	R/W1C	0x0	DRR Data Receive Request When set, it means that there are enough data in FIFO during receiving data. This is write-1-to-clear bits.
4	R/W1C	0x0	DTR Data Transmit Request

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			When set, it means that there are enough space in FIFO during transmitting data. This is write-1-to-clear bits.
3	R/W1C	0x0	DTC Data Transfer Complete This is write-1-to-clear bits.
2	R/W1C	0x0	CC Command Complete This is write-1-to-clear bits.
1	R/W1C	0x0	RE Response Error When set, Transmit Bit error or End Bit error or CMD Index error may occurs. This is write-1-to-clear bits.
0	/	/	/

4.3.5.16. SMHC Status Register(Default Value: 0x0000_0006)

Offset: 0x003C			Register Name: SMHC_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	DMA_REQ DMA Request DMA request signal state
30:26	/	/	/
25:17	R	0x0	FIFO_LEVEL FIFO Level Number of filled locations in FIFO
16:11	R	0x0	RESP_IDX Response Index Index of previous response, including any auto-stop sent by controller
10	R	0x0	FSM_BUSY Data FSM Busy Data transmit or receive state-machine is busy
9	R	0x0	CARD_BUSY Card data busy Inverted version of DATA[0] 0: card data not busy 1: card data busy
8	R	0x0	CARD_PRESENT Data[3] status level of DATA[3], checks whether card is present 0: card not present 1: card present
7:4	R	0x0	FSM_STA

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			Command FSM States 0000: Idle 0001: Send init sequence 0010: TX CMD start bit 0011: TX CMD TX bit 0100: TX CMD index + argument 0101: TX CMD CRC7 0110: TX CMD end bit 0111: RX response start bit 1000: RX response IRQ response 1001: RX response TX bit 1010: RX response CMD index 1011: RX response data 1100: RX response CRC7 1101: RX response end bit 1110: CMD path wait NCC 1111: Wait; CMD-to-response turnaround
3	R	0x0	FIFO_FULL FIFO Full 1: FIFO full 0: FIFO not full
2	R	0x1	FIFO_EMPTY FIFO Empty 1: FIFO Empty 0: FIFO not Empty
1	R	0x1	FIFO_TX_LEVEL FIFO TX Water Level Flag 0: FIFO didn’t reach transmit trigger level 1: FIFO reached transmit trigger level
0	R	0x0	FIFO_RX_LEVEL FIFO TX Water Level Flag 0: FIFO didn’t reach receive trigger level 1: FIFO reached receive trigger level

4.3.5.17. SMHC FIFO Water Level Register(Default Value: 0x000F_0000)

Offset: 0x0040			**Register Name: SMHC_FIFOTH**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x0	BSIZE_OF_TRANS Burst Size of Multiple Transaction 000: 1 transfers 001: 4 010: 8

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			011: 16 Others: Reserved Should be programmed same as DMA controller multiple transaction size. The units for transfers are the DWORD. A single transfer would be signaled based on this value. Value should be sub-multiple of (RX_TL + 1) and (FIFO_DEPTH - TX_TL) FIFO_DEPTH = 256 FIFO_SIZE = 256 * 32 = 1K Recommended: MSize = 16, TX_TL = 240, RX_TL = 15
27:24	/	/	/
23:16	R/W	0xF	RX_TL RX Trigger Level 0x0~0xFE: RX Trigger Level is 0~254 0xFF: Reserved FIFO threshold when FIFO request host to receive data from FIFO. When FIFO data level is greater than this value, DMA is request is raised if DMA enabled, or RX interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. Recommended: 15 (means greater than 15)
15:8	/	/	/
7:0	R/W	0x0	TX_TL TX Trigger Level 0x1~0xFF: TX Trigger Level is 1~255 0x0: no trigger FIFO threshold when FIFO requests host to transmit data to FIFO. When FIFO data level is less than or equal to this value, DMA TX request is raised if DMA enabled, or TX request interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. Recommended: 240(means less than or equal to 240)

4.3.5.18. SMHC Function Select Register(Default Value: 0x0000_0000)

Offset: 0x0044			**Register Name: SMHC_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	ABT_RDATA Abort Read Data

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			0: Ignored 1: After suspend command is issued during read-transfer, software polls card to find when suspend happened. Once suspend occurs, software sets bit to reset data state-machine, which is waiting for next block of data. Used in SDIO card suspends sequence. This bit is auto-cleared once controller reset to idle state.
1	R/W	0x0	READ_WAIT Read Wait 0: Clear SDIO read wait 1: Assert SDIO read wait
0	R/W	0x0	HOST_SEND_MMC_IRQRESQ Host Send MMC IRQ Response 0: Ignored 1: Send auto IRQ response When host is waiting MMC card interrupt response, setting this bit will make controller cancel wait state and return to idle state, at which time, controller will receive IRQ response sent by itself. This bit is auto-cleared after response is sent.

4.3.5.19. SMHC Transferred Byte Count Register 0 (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: SMHC_TBC0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	TBC0 Transferred Count 0 Number of bytes transferred between card and internal FIFO. The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

4.3.5.20. SMHC Transferred Byte Count Register 1 (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: SMHC_TBC1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	TBC1 Transferred Count 1 Number of bytes transferred between Host/DMA memory and internal FIFO. The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

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4.3.5.21. SMHC CRC Status Detect Control Register(Default Value: 0x0000_0003)

Offset: 0x0054			Register Name: SMHC_CSDC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	CRC_DET_PARA 110: HS400 speed mode 011: Other speed mode

4.3.5.22. SMHC Auto Command 12 Argument Register (Default Value: 0x0000_FFFF)

Offset: 0x0058			Register Name: SMHC_A12A
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xffff	SD_A12A. SD_A12A set the argument of command 12 automatically send by controller

4.3.5.23. SMHC New Timing Set Register (Default Value: 0x8171_0000)

Offset: 0x005C			Register Name: SMHC_NTSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	MODE_SELEC 0: Old mode of Sample/Output Timing 1: New mode of Sample/Output Timing Default value : 1
30:25	/	/	/
24	R/W	0x1	CMD_DAT_RX_PHASE_CLR During update clock operation, clear command line's and data lines' input phase. 0: Disable 1: Enable
23	/	/	/
22	R/W	0x1	DAT_CRC_STATUS_RX_PHASE_CLR Before receive CRC status, clear data lines' input phase. 0: Disable 1: Enable
21	R/W	0x1	DAT_TRANS_RX_PHASE_CLR Before transfer data, clear data lines' input phase. 0: Disable 1: Enable
20	R/W	0x1	DAT_RECV_RX_PHASE_CLR Before receive data, clear data lines' input phase clear

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			0: Disable 1: Enable
19:17	/	/	/
16	R/W	0x1	CMD_SEND_RX_PHASE_CLR Before send command, command rx phase clear 0: Disable 1: Enable
15:10	/	/	/
9:8	R/W	0x0	DAT_SAMPLE_TIMING_PHASE 00: Sample timing phase offset 90^0 01: Sample timing phase offset 180^0 10: Sample timing phase offset 270^0 11: Ignore Default value: 00
7:6	/	/	/
5:4	R/W	0x0	CMD_SAMPLE_TIMING_PHASE 00: Sample timing phase offset 90^0 01: Sample timing phase offset 180^0 10: Sample timing phase offset 270^0 11: Ignore Default value: 00
3:0	/	/	/

NOTE

This register is reserved for SMHC2, but valid for other SMHCs.

4.3.5.24. SMHC Auto Command 12 Argument Register (Default Value: 0x0000_FFFF)

Offset: 0x0058			Register Name: SMHC_A12A
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xffff	SD_A12A. SD_A12A set the argument of command 12 automatically send by controller

4.3.5.25. SMHC EMCE Control Register (Default Value: 0x0200_0000)

Offset: 0x0064			Register Name: SMHC_EMCE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x200	SEC_SZ Sector Size of EMCE.
15:8	/	/	/
7	R/W	0x0	BM_BLK_SZ

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			The size of bitmap-block size. 0: 512 Byte 1: 4096 Byte
6	R/W	0x0	BM_EN 0: Disable bitmap. 1: Enable bitmap. This bit is valid when EMCE is enable and use DMA transfer. If this bit is cleared, all data blocks associated with one write/read command will be encrypted/decrypted. If this bit is set, the data will be divided into many bitmap-blocks aligned to BM_BLK_SZ. The bitmap-blocks are associated with the bits of SMHC_EMCE_BMn register, and will be or will not be encrypted/decrypted determined by these bitmap bits. SMHC can support the last bitmap-block is not aligned to BM_BLK_SZ.
5	/	/	/
4	R/W	0x0	EMCE_ENCR 0:disabled encrypt and decrypt.Encrypt and decrypt will be bypassed in EMCE 1:enable encrypt and decrypt This bit is only available when EMCE_ENB is 1.
3:2	/	/	/
1	R/W	0x0	AC_MD Access Mode 0: Sector mode. The data address to access device is in sector(512 bytes) units. SMHC_CMDARG is a 32bit sector(512 bytes) address. 1: Byte mode. The data address to access device is in bytes units. SMHC_CMDARG is a 32bit byte address.
0	R/W	0x0	EMCE_ENB EMCE Enable 0: EMCE is disabled.EMCE will be bypass by host controller. 1: EMCE is enabled. The data of current command shall go through EMCE.Encrypt or decrypt is decided by EMCE_ENCR. The type and configuration of encryption algorithm are determined by EMCE's initial process, and out of this specification.

NOTE

This register is valid only for SMHC2.

4.3.5.26. SMHC EMCE Debug Register (Default Value: 0x0000_0000)

Offset: 0x0068	Register Name: SMHC_EMCE_DBG

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Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	EMCE_FIFO_LVL EMCE FIFO level in byte When transmitting data, it shows the number of data in FIFO which received from EMCE , then send from SMHC to device. When receiving dat, it shows the number of data in FIFO which is read from device, then send to EMCE.
15:2	/	/	/
13:4	R	0x0	BM_BLK_CNT Bitmap-block couter This field counts the number of bitmap-block for each write/read command. It is cleared when lunch a new command.
3	/	/	/
2	R	0x0	BM_BLK_BYPASS 1: Current bitmap-block is bypassed, and will not be encrypted/decrypted. 0: Current will be encrypted/decrypted. This bit is valid only when EMCE_ENB is 1 and EMCE_ENCR is 0.
1	R	0x0	EMCE_FIFO_UN When this bit is set, EMCE FIFO is underrun.
0	R	0x0	EMCE_FIFO_OV When this bit is set, EMCE FIFO is overflow.

NOTE

This register is valid only for SMHC2.

4.3.5.27. SMHC Hardware Reset Register (Default Value: 0x0000_0001)

Offset: 0x78			Register Name: SMHC_HWRST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x1	HW_RST. 1: Active mode 0: Reset These bits cause the cards to enter pre-idle state, which requires them to be re-initialized.

4.3.5.28. SMHC DMAC Control Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: SMHC_DMAC
Bit	**Read/Write**	**Default/Hex**	**Description**
31	W	0x0	DES_LOAD_CTRL When DMAC fetches a descriptor, if the valid bit of a descriptor is not set,

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			DMAC FSM will go to the suspend state. Setting this bit will make DMAC re-fetch descriptor again and do the transfer normally.
30:11	/	/	/
10:8	R	0x0	Reserved
7	R/W	0x0	IDMAC_ENB IDMAC Enable. When set, the IDMAC is enabled. DE is read/write.
6:2	R/W	0x0	Reserved
1	R/W	0x0	FIX_BUST_CTRL Fixed Burst. Controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations.
0	R/W	0x0	IDMAC_RST DMA Reset. When set, the DMA Controller resets all its internal registers. SWR is read/write. It is automatically cleared after 1 clock cycle.

4.3.5.29. SMHC Descriptor List Base Address Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: SMHC_DLBA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DES_BASE_ADDR Start of Descriptor List. Contains the base address of the First Descriptor. The LSB bits [1:0] are ignored and taken as all-zero by the IDMAC internally. Hence these LSB bits are read-only.

4.3.5.30. SMHC DMAC Status Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: SMHC_IDST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16:13	R	0x0	Reserved
12:10	R	0x0	DMAC_ERR_STA Error Bits. Indicates the type of error that caused a Bus Error. Valid only with Fatal Bus Error bit (IDSTS[2]) set. This field does not generate an interrupt. 001: Host Abort received during transmission 010: Host Abort received during reception Others: Reserved EB is read-only.
9	R/W1C	0x0	ABN_INT_SUM

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			Abnormal Interrupt Summary. Logical OR of the following: IDSTS[2]: Fatal Bus Interrupt IDSTS[4]: Descriptor Unavailable bit Interrupt IDSTS[5]: Card Error Summary Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes AIS to be set is cleared. Writing a 1 clears this bit.
8	R/W1C	0x0	NOR_INT_SUM Normal Interrupt Summary. Logical OR of the following: IDSTS[0]: Transmit Interrupt IDSTS[1]: Receive Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes NIS to be set is cleared. Writing a 1 clears this bit.
7:6	/	/	/
5	R/W1C	0x0	ERR_FLAG_SUM Card Error Summary. Indicates the status of the transaction to/from the card; also present in RINTSTS. Indicates the logical OR of the following bits: EBE: End Bit Error RTO: Response Timeout/Boot ACK Timeout RCRC: Response CRC SBE: Start Bit Error DRTO: Data Read Timeout/BDS timeout DCRC: Data CRC for Receive RE: Response Error Writing a 1 clears this bit.
4	R/W1C	0x0	DES_UNAVL_INT Descriptor Unavailable Interrupt. This bit is set when the descriptor is unavailable due to OWN bit = 0 (DES0[31] =0). Writing a 1 clears this bit.
3	/	/	/
2	R/W1C	0x0	FATAL_BERR_INT Fatal Bus Error Interrupt. Indicates that a Bus Error occurred (IDSTS[12:10]). When this bit is set, the DMA disables all its bus accesses. Writing a 1 clears this bit.
1	R/W1C	0x0	RX_INT Receive Interrupt. Indicates the completion of data reception for a descriptor. Writing a 1 clears this bit.
0	R/W1C	0x0	TX_INT Transmit Interrupt. Indicates that data transmission is finished for a descriptor. Writing a '1'

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			clears this bit.

4.3.5.31. SMHC DMAC Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: SMHC_IDIE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	Reserved
8	R/W	0x0	Reserved
7:6	/	/	/
5	R/W	0x0	ERR_SUM_INT_ENB Card Error summary Interrupt Enable. When set, it enables the Card Interrupt summary.
4	R/W	0x0	DES_UNAVL_INT_ENB Descriptor Unavailable Interrupt. When set along with Abnormal Interrupt Summary Enable, the Descriptor Unavailable interrupt is enabled.
3	/	/	/
2	R/W	0x0	FERR_INT_ENB Fatal Bus Error Enable. When set with Abnormal Interrupt Summary Enable, the Fatal Bus Error Interrupt is enabled. When reset, Fatal Bus Error Enable Interrupt is disabled.
1	R/W	0x0	RX_INT_ENB Receive Interrupt Enable. When set with Normal Interrupt Summary Enable, Receive Interrupt is enabled. When reset, Receive Interrupt is disabled.
0	R/W	0x0	TX_INT_ENB Transmit Interrupt Enable. When set with Normal Interrupt Summary Enable, Transmit Interrupt is enabled. When reset, Transmit Interrupt is disabled.

4.3.5.32. SMHC Card Threshold Control Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: SMHC_THLD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	CARD_RD_THLD Card Read Threshold Size
15:3	/	/	/
2	R/W	0x0	CARD_WR_THLD_ENB (only for SMHC2) Card Write Threshold Enable(HS400) 0: Card write threshold disable 1: Card write threshold enabled

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			Host controller initiates write transfer only if card threshold amount of data is available in transmit FIFO
1	R/W	0x0	BCIG (only for SMHC2) Busy Clear Interrupt Generation 0: Busy Clear Interrupt disabled 1: Busy Clear Interrupt Enabled The application can disable this feature if it does not want to wait for a Busy Clear Interrupt.
0	R/W	0x0	CARD_RD_THLD_ENB Card Read Threshold Enable 0: Card Read Threshold Disable 1: Card Read Threshold Enable Host controller initiates Read Transfer only if CARD_RD_THLD amount of space is available in receive FIFO.

4.3.5.33. SMHC eMMC4.5 DDR Start Bit Detection Control Register (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: SMHC_EDSD
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HS400_MD_EN(for SMHC2 only) HS400 Mode Enable 0: Disable 1: Enable It is required to set this bit to '1' before initiating any data transfer CMD in HS400 mode.
30:1	/	/	/
0	R/W	0x0	HALF_START_BIT Control for start bit detection mechanism inside mstorage based on duration of start bit. For eMMC 4.5, start bit can be: 0: Full cycle 1: Less than one full cycle Set HALF_START_BIT=1 for eMMC 4.5 and above; set to 0 for SD applications.

4.3.5.34. SMHC Response CRC Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: SMHC_RESP_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:0	R	0x0	RESP_CRC Response CRC Response CRC from device.

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NOTE

This register is reserved for SMHC2, but valid for other SMHCs.

4.3.5.35. SMHC Data7 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: SMHC_DAT7_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT7_CRC Data[7] CRC CRC in data[7] from device. In 8bit DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bit DDR mode,it is not used. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is reserved for SMHC2, but valid for other SMHCs.

4.3.5.36. SMHC Data6 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: SMHC_DAT6_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT6_CRC Data[6] CRC CRC in data[6] from device. In 8bit DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bit DDR mode,it is not used. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is reserved for SMHC2, but valid for other SMHCs.

4.3.5.37. SMHC Data5 CRC Register (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: SMHC_DAT5_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT5_CRC

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			Data[5] CRC CRC in data[5] from device. In 8bit DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bit DDR mode,it is not used. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is reserved for SMHC2, but valid for other SMHCs.

4.3.5.38. SMHC Data4 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: SMHC_DAT4_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT4_CRC Data[4] CRC CRC in data[4] from device. In 8 bit DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bit DDR mode, the higher 16 bits indicate the CRC of odd data, and the lower 16 bits indicate the CRC of even data. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is reserved for SMHC2, but valid for other SMHCs.

4.3.5.39. SMHC Data3 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: SMHC_DAT3_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT3_CRC Data[3] CRC CRC in data[3] from device. In 8 bit DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bit DDR mode, the higher 16 bits indicate the CRC of odd data, and the lower 16 bits indicate the CRC of even data. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is reserved for SMHC2, but valid for other SMHCs.

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4.3.5.40. SMHC Data2 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: SMHC_DAT2_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT2_CRC Data[2] CRC CRC in data[2] from device. In 8 bit DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bit DDR mode, the higher 16 bits indicate the CRC of odd data, and the lower 16 bits indicate the CRC of even data. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is reserved for SMHC2, but valid for other SMHCs.

4.3.5.41. SMHC Data1 CRC Register (Default Value: 0x0000_0000)

Offset: 0x012C			Register Name: SMHC_DAT1_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT1_CRC Data[1] CRC CRC in data[1] from device. In 8 bit DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bit DDR mode, the higher 16 bits indicate the CRC of odd data, and the lower 16 bits indicate the CRC of even data. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is reserved for SMHC2, but valid for other SMHCs.

4.3.5.42. SMHC Data0 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: SMHC_DAT0_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT0_CRC Data[0] CRC CRC in data[0] from device.

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			In 8 bit DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bit DDR mode, the higher 16 bits indicate the CRC of odd data, and the lower 16 bits indicate the CRC of even data. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is reserved for SMHC2, but valid for other SMHCs.

4.3.5.43. SMHC CRC Status Register (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: SMHC_CRC_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R	0x0	CRC_STA CRC Status CRC status from device in write operation Positive CRC status token: 3'b010 Negative CRC status token: 3'b101

NOTE

This register is reserved for SMHC2, but valid for other SMHCs.

4.3.5.44. SMHC Drive Delay Control Register (Default Value: 0x0001_0000)

Offset: 0x0140			Register Name: SMHC_DRV_DL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	DAT_DRV_PH_SEL Data Drive Phase Select 0: Data drive phase offset is 90^0 at SDR mode, 45^0 at DDR mode, 90^0 at HS400 mode. 1: Data drive phase offset is 180^0 at SDR mode, 90^0 at DDR mode, 0^0 at HS400 mode.
16	R/W	0x1	CMD_DRV_PH_SEL Command Drive Phase Select 0: Command drive phase offset is 90^0 at SDR mode, 45^0 at DDR mode, 90^0 at HS400 mode. 1: Command drive phase offset is 180^0 at SDR mode, 90^0 at DDR mode, 0^0 at HS400 mode.
15:0	/	/	/

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4.3.5.45. SMHC Sample Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0144			Register Name: SMHC_SAMP_DL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	SAMP_DL_CAL_START Sample Delay Calibration Start When set, start sample delay chain calibration.
14	R	0x0	SAMP_DL_CAL_DONE Sample Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in SAMP_DL.
13:8	R	0x20	SAMP_DL Sample Delay It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of card clock nearly. Generally, it is necessary to do drive delay calibration when card clock is changed. This bit is valid only when SAMP_DL_CAL_DONE is set.
7	R/W	0x0	SAMP_DL_SW_EN Sample Delay Software Enable When set, enable sample delay specified at SAMP_DL_SW
6	/	/	/
5:0	R/W	0x0	SAMP_DL_SW Sample Delay Software The relative delay between clock line and command line, data lines. It can be determined according to the value of SAMP_DL, the cycle of card clock and device's input timing requirement.

4.3.5.46. SMHC Data Strobe Delay Control Register(Default Value: 0x0000_2000)

Offset: 0x0148			Register Name: SMHC_DS_DL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	DS_DL_CAL_START Data Strobe Delay Calibration Start When set, start sample delay chain calibration.
14	R	0x0	DS_DL_CAL_DONE Data Strobe Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in DS_DL.

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13:8	R	0x20	DS_DL Data Strobe Delay It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of SMHC's clock nearly. This bit is valid only when SAMP_DL_CAL_DONE is set.
7	R/W	0x0	DS_DL_SW_EN Sample Delay Software Enable
6	/	/	/
5:0	R/W	0x0	DS_DL_SW Data Strobe Delay Software

NOTE

This register is for SMHC2 only.

4.3.5.47. SMHC EMCE Bitmap Register n (Default Value: 0x0000_0000)

Offset: 0x0150+0x04*n(n=0~31)			Register Name: SMHC_EMCE_BMn
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	BM_n(n=0~31) From LSB to MSB of SMHC_EMCE_BMn, each bit associates with one bitmap-block. 0: The associated bitmap-block will be bypassed in EMCE. 1: The associated bitmap-block will be encrypted/decrypted in EMCE. The total bits of all bitmap registers are 32*32=1024. The size of bitmap-block is determined by SMHC_EMCE BM_BLK_SZ, it may be 512 Byte or 4096 Byte. The maximum data size indicated by all 32 bitmap registers is 512K Byte or 4M Byte. In other words, the maximum data size of one multi-block write/read command is limited to 512K Byte or 4M Byte.

NOTE

This register is for SMHC2 only.

4.3.5.48. SMHC FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: SMHC_FIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX/RX_FIFO Data FIFO

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Chapter 5 Image

This section describes the image input of H6 V200:

- CSI

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5.1. CSI

5.1.1. Overview

The CMOS Sensor Interface(CSI) Controller is an image or video input control module which can receive image or video data over digital camera(DC)interface,BT.656 interface.The controller can store the data in memory directly.There is also a built-in Camera Control Interface(CCI) modules can be used for external device control.

The CSI includes the following feature:

CSI

- Supports 8/10-bit DC interface
- Supports BT656 interface
- Supports ITU-R BT.656 time-multiplexed format
- Supports image crop function
- Maximum still capture resolution for parallel interface to 5M
- Maximum video capture resolution for parallel interface to 1080P@30fps
- Maximum pixel clock for parallel to 148.5MHz

CCI

- Compatible with I2C transmission in 7 bit slave ID + 1 bit R/W
- Automatic transmission
- 0/8/16/32 bits register address supported
- 8/16/32 bits data supported
- 64 bytes-FIFO input CCI data supported
- Synchronized with CSI signal and delay trigger supported
- Repeated transmission with sync signal supported

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5.1.2. Block Diagram

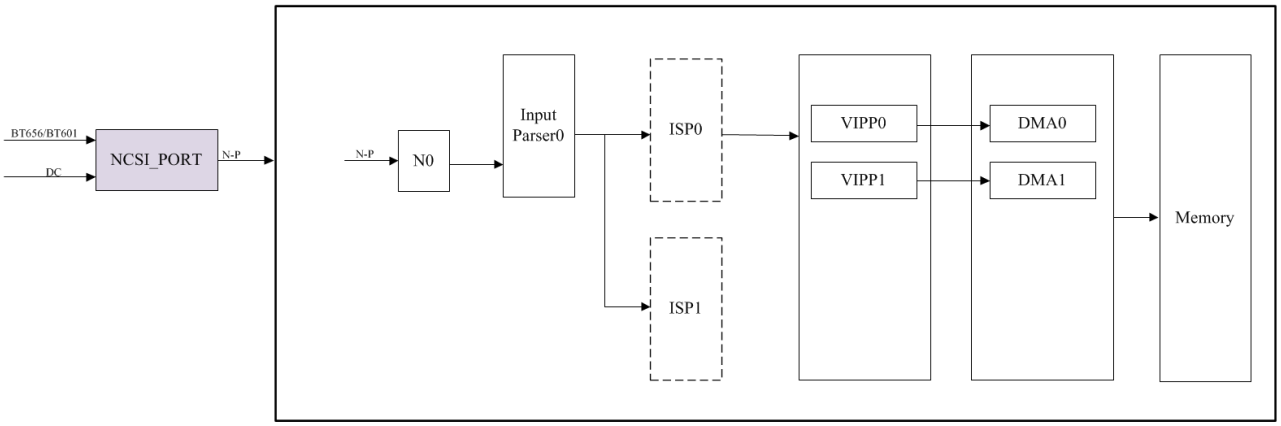


Figure 5-1. CSI Block Diagram

The CSI is consists of Input Parser, Video Input Post Process(VIPP) and DMA Control.In addition,the controller has 1 Input Parser, 2 VIPP and 2 DMA. ISP0 and ISP1 are empty.

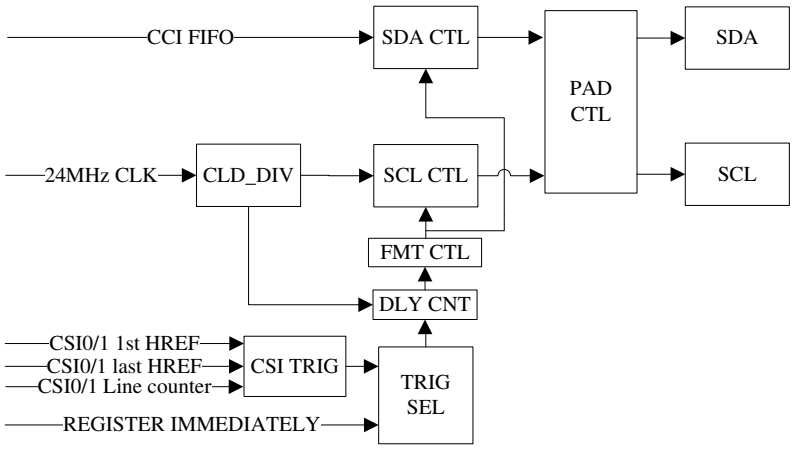


Figure 5-2. CCI Block Diagram

5.1.3. Operations and Functional Descriptions

5.1.3.1. External Signals

Table 5-1. CSI External Signals

Pin Name	Function Description	Type
CSI_MCLK	Master Clock for External Device	O
CSI_PCLK	Pixel Clock	I
CSI_VSYNC	Vertical SYNC Signal	I
CSI_HSYNC	Horizontal SYNC Signal	I

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CSI_D0	Video Input Data0	I
CSI_D1	Video Input Data1	I
CSI_D2	Video Input Data2	I
CSI_D3	Video Input Data3	I
CSI_D4	Video Input Data4	I
CSI_D5	Video Input Data5	I
CSI_D6	Video Input Data6	I
CSI_D7	Video Input Data7	I
CSI_D8	Video Input Data8	I
CSI_D9	Video Input Data9	I
CSI_SCK	CCI Control Clock	O
CSI_SDA	CCI Control Data	I/O

5.1.3.2. Typical Application

CSI module has one input port and two DMA which means it can support one port input and two video streams output to memory simultaneously at most. This make the applications very flexible.

CSI supports following input case:

- 1 parallel DC input
- 1 BT656 input interleaved 2-channel

5.1.3.3. CSI FIFO Distribution

Table 5-2. CSI FIFO Distribution

Interface	**YUYV422 Interleaved/Raw**			**MIPI Interface**		
Input format	YUV422		Raw	YUV422		Raw
Output format	Planar	UV combined	Raw/RGB /PRGB	Planar	UV combined	Raw/RGB /PRGB
CH0_FIFO0	Y	Y	All pixels data	Y	Y	All pixels data
CH0_FIFO1	Cb (U)	CbCr (UV)	-	Cb (U)	CbCr (UV)	-
CH0_FIFO2	Cr (V)	-	-	Cr (V)	-	-

Interface	**BT656 Interface**	**BT1120 Interface**
Input format	YUV422	YUV422

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Output format	Planar	UV combined	Planar	UV combined
CH0_FIFO0	Y	Y	Y	Y
CH0_FIFO1	Cb (U)	CbCr (UV)	Cb (U)	CbCr (UV)
CH0_FIFO2	Cr (V)	-	Cr (V)	-
CH1_FIFO0	Y	Y	Y	Y
CH1_FIFO1	Cb (U)	CbCr (UV)	Cb (U)	CbCr (UV)
CH1_FIFO2	Cr (V)	-	Cr (V)	-
CH2_FIFO0	Y	Y	Y	Y
CH2_FIFO1	Cb (U)	CbCr (UV)	Cb (U)	CbCr (UV)
CH2_FIFO2	Cr (V)	-	Cr (V)	-
CH3_FIFO0	Y	Y	Y	Y
CH3_FIFO1	Cb (U)	CbCr (UV)	Cb (U)	CbCr (UV)
CH3_FIFO2	Cr (V)	-	Cr (V)	-

5.1.3.4. Pixel Format Arrangement

RAW-10:

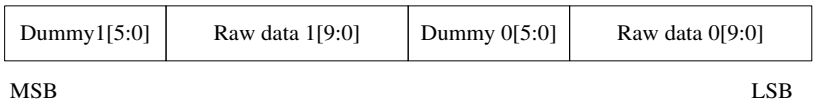


Figure 5-3. RAW-10 Format

RAW-12:

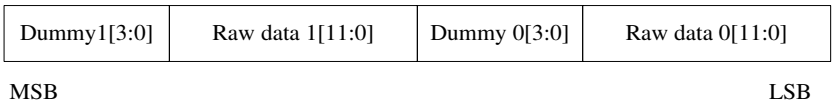


Figure 5-4. RAW-12 Format

YUV-10:

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Dummy1[5:0]	Y1[9:0]	Dummy 0[5:0]	Y 0[9:0]

MSB LSB

Figure 5-5. Y of YUV-10 Format

Dummy1[5:0]	V/U 0[9:0]	Dummy 0[5:0]	U/V 0[9:0]

MSB LSB

Figure 5-6. UV Combined of YUV-10 Format

RGB888:

B1[7:0]	R0[7:0]	G0[7:0]	B0[7:0]
G2[7:0]	B2[7:0]	R1[7:0]	G1[7:0]
R3[7:0]	G3[7:0]	B3[7:0]	R2[7:0]

MSB

Figure 5-7. RGB888 Format

PRGB888:

PAD[7:0]	R0[7:0]	G0[7:0]	B0[7:0]

MSB LSB

Figure 5-8. PRGB888 Format

RGB565:

R1[4:0]	G1[5:0]	B1[4:0]	R0[4:0]	G0[5:0]	B0[4:0]

MSB LSB

Figure 5-9. RGB565 Format

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5.1.3.5. CSI Timing

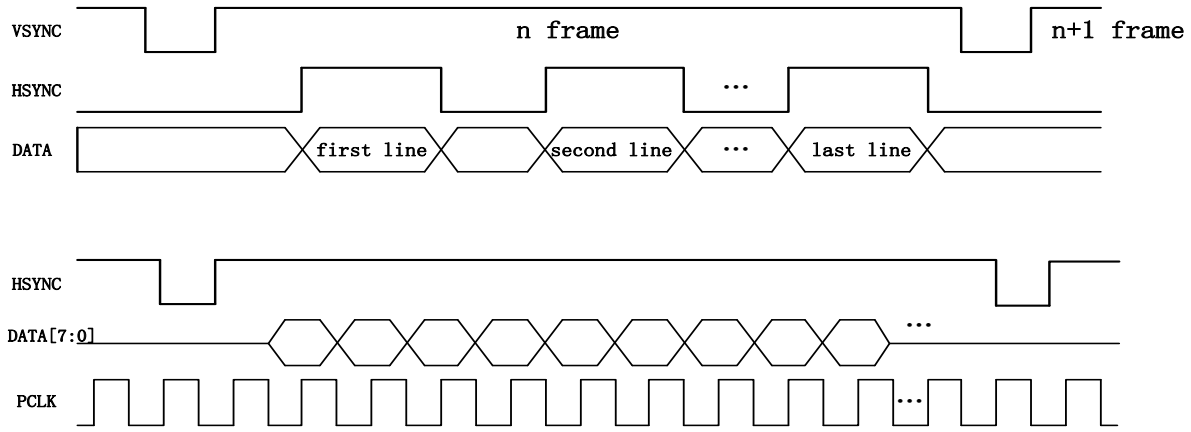


Figure 5-10. 8bit CMOS Sensor Interface Timing

(clock rising edge sample.vsync valid = positive,hsycn valid = positive)

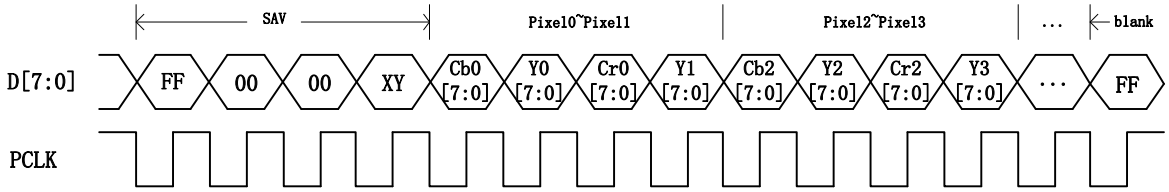


Figure 5-11. 8-bit YCbCr4:2:2 with Embedded Syncs(BT656) Timing

5.1.3.6. Bit Definition

Table 5-3. CCIR656 Header Code

Data Bit	First Word(0xFF)	Second Word(0x00)	Third Word(0x00)	Fourth Word
CS D[9] (MSB)	1	0	0	1
CS D[8]	1	0	0	F
CS D[7]	1	0	0	V
CS D[6]	1	0	0	H
CS D[5]	1	0	0	P3
CS D[4]	1	0	0	P2
CS D[3]	1	0	0	P1
CS D[2]	1	0	0	P0
CS D[1]	x	x	x	x
CS D[0]	x	x	x	x

NOTE

For compatibility with 8-bit interface, CS D[1] and CS D[0] are not defined.

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Table 5-4. CCIR656 Header Data Bit Definition

Decode	F	V	H	P3	P2	P1	P0
Field 1 start of active video (SAV)	0	0	0	0	0	0	0
Field 1 end of active video (EAV)	0	0	1	1	1	0	1
Field 1 SAV (digital blanking)	0	1	0	1	0	1	1
Field 1 EAV (digital blanking)	0	1	1	0	1	1	0
Field 2 SAV	1	0	0	0	1	1	1
Field 2 EAV	1	0	1	1	0	1	0
Field 2 SAV (digital blanking)	1	1	0	1	1	0	0
Field 2 EAV (digital blanking)	1	1	1	0	0	0	1

5.1.3.7. Offset Definition

Offset in horizontal and vertical can be added when receiving image. Unit is pixel.
For YUV422 format, pixel unit is a YU/YV combination.
For YUV420 format, pixel unit is a YU/YV combination in YC line, and only a Y in Y line.
For Bayer and RAW format, pixel unit is a R/G/B single component.
For RGB565, pixel unit is 2 bytes of RGB565 package.
For RGB888, pixel unit is 3 bytes of RGB combination.

5.1.3.8. Camera Communication Interface

The CCI module supports master mode I2C-compatible single read and write access to camera and related devices.
It reads a series of packet from FIFO (accessed by registers) and transmit with the format defined in specific register(or packet data).
In compact mode, format register define the slave ID, R/W flag, register address width(0/8/16/32…bit), data width(8/16/32…bit) and access counter.
In complete mode, all data and format will be loaded from memory packet.
The access counter should be set to N(N> 0), and it will read N packets from FIFO. The total bytes should not exceed 64 for FIFO input mode.

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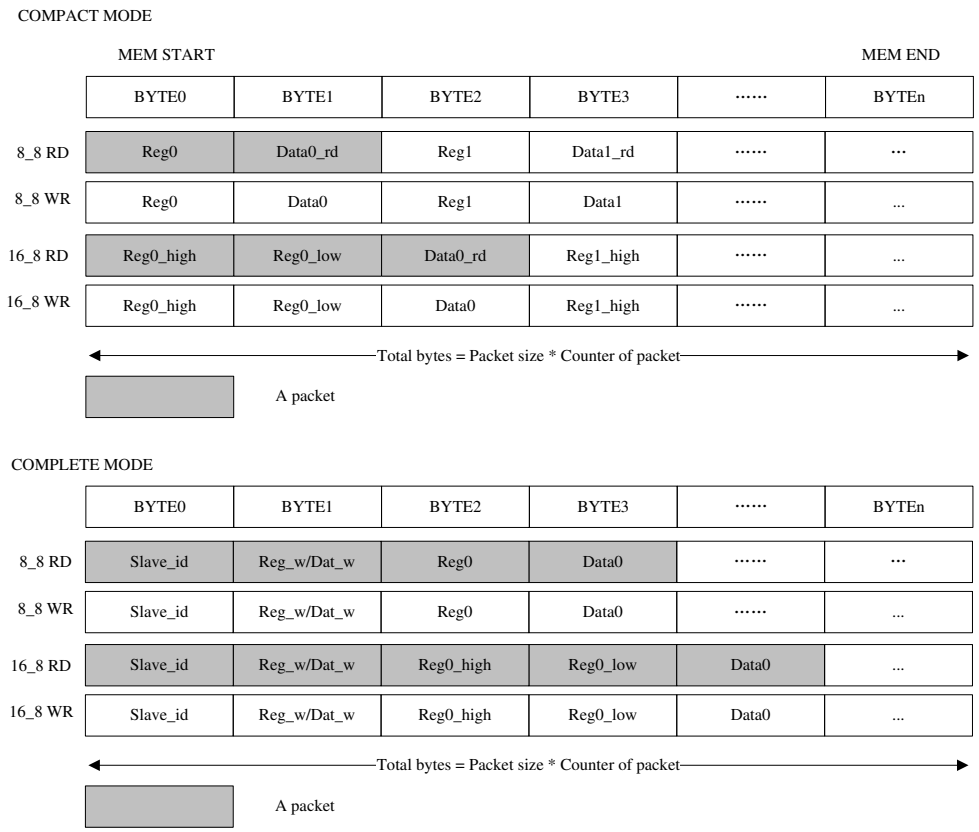


Figure 5-12. R/W Sequence in Compact/Complete Mode

A packet has several bytes filled with register address and data(if in complete mode, slave id and width should be filled too) as the I2C access sequence defined. That is, the low address byte will be transmitted/received first. Bytes will be sent in write access, while some address will be written back with the data received in read access.

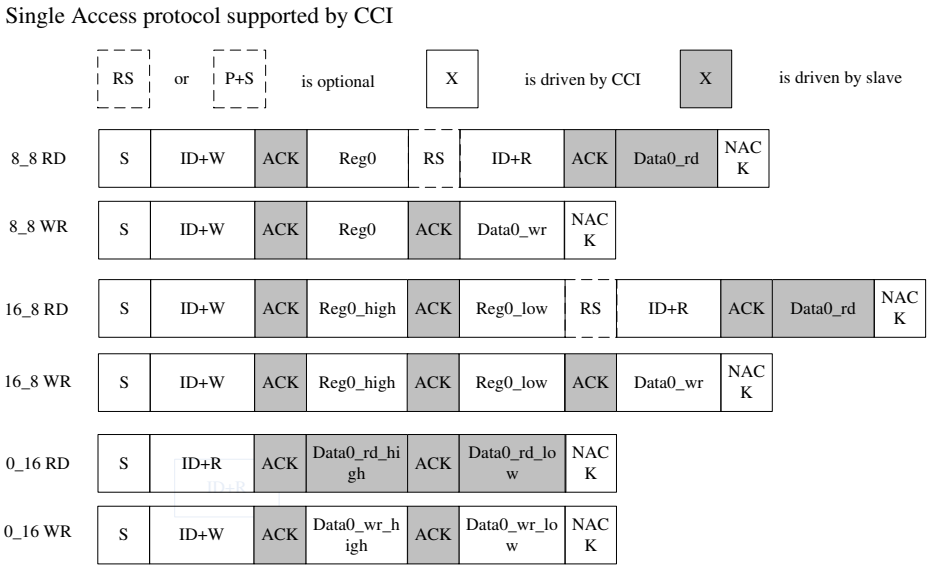


Figure 5-13. Single R/W Process of the CCI Protocol

After set the execution bit, the module will do the transmission automatically and return the result of success or fail. If any access fails, the whole transmission will be stopped and returns the number when it fails in the access counter.

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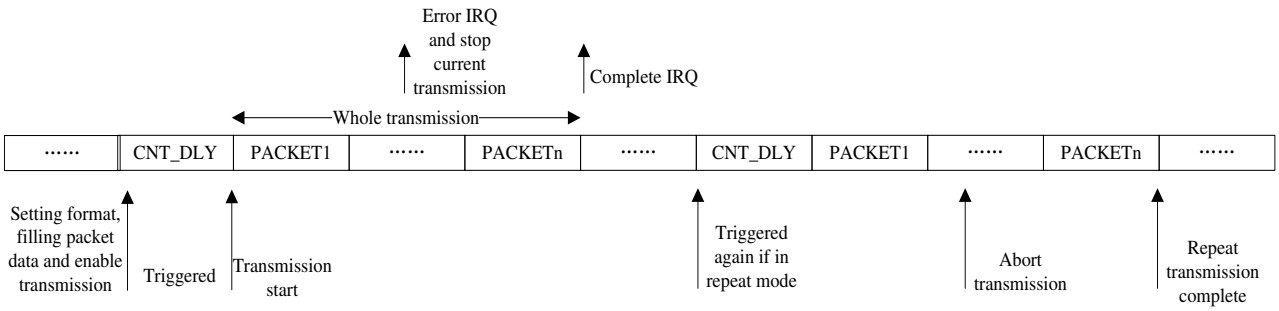


Figure 5-14. CCI Transmission Control

5.1.4. Register list

Module Name	Base Address
CSI_BASE	0x06620000
CSI_TOP	0x06620000
CSI_PARSER	0x06621000
CSI_DMA0	0x06623000
CSI_DMA1	0x06623100
CSI_CCI0	0x0662E000

CSI TOP register list:

Register Name	Offset	Register name
CSI_TOP_EN_REG	0x0000	CSI TOP Enable Register
CSI_PTN_GEN_EN_REG	0x0004	CSI Pattern Generation Enable Register
CSI_PTN_CTRL_REG	0x0008	CSI Pattern Control Register
/	0x000C~0x001C	Reserved
CSI_PTN_LEN_REG	0x0020	CSI Pattern Generation Length Register
CSI_PTN_ADDR_REG	0x0024	CSI Pattern Generation Address Register
CSI_PTN_ISP_SIZE_REG	0x0028	CSI Pattern ISP Size Register
	0x0028~0x0030	Reserved
CSI_ISP0_INPUT0_SEL_REG	0x0034	CSI ISP0 Input0 Select Register
CSI_ISP0_INPUT1_SEL_REG	0x0038	CSI ISP0 Input1 Select Register
	0x003C~0x0040	
CSI_ISP1_INPUT0_SEL_REG	0x0040	CSI ISP1 Input0 Select Register
CSI_ISP1_INPUT1_SEL_REG	0x0044	CSI ISP1 Input1 Select Register
/	0x0048~0x005C	Reserved
CSI_VIPP0_INPUT_SEL_REG	0x0060	CSI VIPP0 Input Select Register
CSI_VIPP1_INPUT_SEL_REG	0x0064	CSI VIPP1 Input Select Register

PARSER register list:

Register Name	Offset	Register name

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PRS_EN_REG	0x0000	Parser Enable Register
PRS_NCSI_IF_CFG_REG	0x0004	Parser NCSI Interface Configuration Register
PRS_MCSI_IF_CFG_REG	0x0008	Parser MCSI Interface Configuration Register
PRS_CAP_REG	0x000C	Parser Capture Register
PRS_SIGNAL_STA_REG	0x0010	Parser Signal Status Register
/	0x0018~0x0020	Reserved
PRS_C0_INFMT_REG	0x0024	Parser Channel_0 Input Format Register
PRS_C0_OUTPUT_HSIZE_REG	0x0028	Parser Channel_0 Output Horizontal Size Register
PRS_C0_OUTPUT_VSIZE_REG	0x002C	Parser Channel_0 Output Vertical Size Register
PRS_C0_INPUT_PARA0_REG	0x0030	Parser Channel_0 Input Parameter0 Register
PRS_C0_INPUT_PARA3_REG	0x003C	Parser Channel_0 Input Parameter3 Register
PRS_C0_INT_EN_REG	0x0040	Parser Channel_0 Interrupt Enable Register
PRS_C0_INT_STA_REG	0x0044	Parser Channel_0 Interrupt Status Register
/	0x0048~0x0120	Reserved
PRS_C1_INFMT_REG	0x0124	Parser Channel_1 Input Format Register
PRS_C1_OUTPUT_HSIZE_REG	0x0128	Parser Channel_1 Output Horizontal Size Register
PRS_C1_OUTPUT_VSIZE_REG	0x012C	Parser Channel_1 Output Vertical Size Register
PRS_C1_INPUT_PARA0_REG	0x0130	Parser Channel_1 Input Parameter0 Register
PRS_C1_INPUT_PARA3_REG	0x013C	Parser Channel_1 Input Parameter3 Register
PRS_C1_INT_EN_REG	0x0140	Parser Channel_1 Interrupt Enable Register
PRS_C1_INT_STA_REG	0x0144	Parser Channel_1 Interrupt Status Register
/	0x0148~0x04FC	Reserved
PRS_NCSI_RX_SIGNAL0_DLY_ADJ_REG	0x0500	Parser NCSI RX Signal0 Delay Adjust Register
PRS_NCSI_RX_SIGNAL3_DLY_ADJ_REG	0x050C	Parser NCSI RX Signal3 Delay Adjust Register
PRS_NCSI_RX_SIGNAL4_DLY_ADJ_REG	0x0510	Parser NCSI RX Signal4 Delay Adjust Register
PRS_NCSI_RX_SIGNAL5_DLY_ADJ_REG	0x0514	Parser NCSI RX Signal5 Delay Adjust Register
PRS_NCSI_RX_SIGNAL6_DLY_ADJ_REG	0x0518	Parser NCSI RX Signal6 Delay Adjust Register

DMA0/1 register list:

CSI_DMA_EN_REG	0x0000	CSI DMA Enable Register
CSI_DMA_CFG_REG	0x0004	CSI DMA Configuration Register
/	0x0008	Reserved
/	0x000C	Reserved
CSI_DMA_HSIZE_REG	0x0010	CSI DMA Horizontal Size Register
CSI_DMA_VSIZE_REG	0x0014	CSI DMA Vertical Size Register
/	0x0018	Reserved
/	0x001C	Reserved
CSI_DMA_F0_BUFA_REG	0x0020	CSI DMA FIFO 0 Output Buffer-A Address Register
/	0x0024	Reserved
CSI_DMA_F1_BUFA_REG	0x0028	CSI DMA FIFO 1 Output Buffer-A Address Register
/	0x002C	Reserved
CSI_DMA_F2_BUFA_REG	0x0030	CSI DMA FIFO 2 Output Buffer-A Address Register

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/	0x0034	Reserved
CSI_DMA_BUF_LEN_REG	0x0038	CSI DMA Buffer Length Register
CSI_DMA_FLIP_SIZE_REG	0x003C	CSI DMA Flip Size Register
/	0x0040~0x0048	Reserved
CSI_DMA_INT_EN_REG	0x0050	CSI DMA Interrupt Enable Register
CSI_DMA_INT_STA_REG	0x0054	CSI DMA Interrupt Status Register
CSI_DMA_LINE_CNT_REG	0x0058	CSI DMA LINE COUNTER Register
/	0x005C	Reserved
CSI_DMA_FRM_CLK_CNT_REG	0x0060	CSI DMA Frame Clock Counter Register
CSI_DMA_PCLK_STAT_REG	0x0070	CSI DMA PCLK Statistic Register

CCI0 register list:

CCI_CTRL	0x0000	CCI Control Register
CCI_CFG	0x0004	CCI Transmission Configuration Register
CCI_FMT	0x0008	CCI Packet Format Register
CCI_BUS_CTRL	0x000C	CCI Bus Control Register
/	0x0010	Reserved
CCI_INT_CTRL	0x0014	CCI Interrupt Control Register
CCI_LC_TRIG	0x0018	CCI Line Counter Trigger Register
/	0x001C~0x00FC	Reserved
CCI_FIFO_ACC	0x0100~0x013C	CCI FIFO Access Register
/	0x0140~0x01FC	Reserved
CCI_RSV_REG	0x0200~0x0220	CCI Reserved Register

5.1.5. Register Description

5.1.5.1. CSI TOP Enable Register(Default Value: 0x0000_0000)

Offset: 0x0000			**Register Name: CSI_TOP_EN_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	R/W	0x0	Reserved
0	R/W	0x0	CSI_TOP_EN 0: Reset and disable the CSI module 1: Enable the CSI module

5.1.5.2. CSI Pattern Generation Enable Register(Default Value: 0x0000_0000)

Offset: 0x0004			**Register Name: CSI_PTN_GEN_EN_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/

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23:16	R/W	0x0	PTN_CYCLE Pattern generating cycle counter. The pattern in dram will be generated in cycles of PTN_CYCLE+1.
15:5	/	/	/
4	R/WAC	0x0	PTN_START CSI Pattern Generating Start 0: Finish other: Start Software write this bit to“1” to start pattern generating from DRAM. When finished, the hardware will clear this bit to“0” automatically. Generating cycles depends on PTN_CYCLE.
3:1	/	/	/
0	R/W	0x0	PTN_GEN_EN Pattern Generation Enable

5.1.5.3. CSI Pattern Control Register(Default Value: 0x0000_000F)

Offset: 0x0008			**Register Name: CSI_PTN_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	PTN_PORT_SEL Pattern Generator output port selection 00:reserved 01:reserved 10:NCSI0 11:reserved
23:22	/	/	/
21:20	R/W	0x0	PTN_GEN_DATA_WIDTH 00:8-bit 01:10-bit 10:reserved 11:reserved
19:16	R/W	0x0	PTN_MODE Pattern mode selection 0000:reserved 0001:reserved 0010:reserved 0011:reserved 0100:NCSI YUV 8 bits width 0101:reserved 0110:reserved 0111:reserved 1000:BT656 8 bits width 1001:reserved

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			1010:reserved 1011:reserved 1100:reserved 1101:reserved 1110:reserved 1111:reserved
15:10	/	/	/
9:8	R/W	0x0	PTN_GEN_CLK_DIV Packet generator clock divider
7:0	R/W	0xF	PTN_GEN_DLY Clocks delayed before pattern generating start.

5.1.5.4. CSI Pattern Generation Length Register(Default Value:0x0000_0000)

Offset: 0x0020			Register Name: CSI_PTN_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	PTN_LEN The pattern length in byte when generating pattern.

5.1.5.5. CSI Pattern Generation Address Register(Default Value:0x0000_0000)

Offset: 0x0024			Register Name: CSI_PTN_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	PTN_ADDR The pattern DRAM address when generating pattern.

5.1.5.6. CSI Pattern ISP Size Register(Default Value:0x0000_0000)

Offset: 0x0028			Register Name: CSI_PTN_ISP_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	Height Vertical size,only valid for ISP mode pattern generation.
15:13	/	/	/
12:0	R/W	0x0	Width Horizontal size,only valid for ISP mode pattern generation.

5.1.5.7. CSI ISP0 Input0 Select Register(Default Value:0x0000_0000)

Offset :0x0030	Register Name: CSI_ISP0_INPUT0_SEL_REG

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Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2:0	R/W	0x0	ISP0 Input0 Select 000: input from Parser0 CH0 others: reserved

5.1.5.8. CSI ISP0 Input1 Select Register(Default Value:0x0000_0000)

Offset :0x0034			Register Name: CSI_ISP0_INPUT1_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	ISP0 Input1 Select 000: input from Parser0 CH1 others: reserved

5.1.5.9. CSI ISP1 Input0 Select Register(Default Value:0x0000_0001)

Offset :0x0040			Register Name: CSI_ISP1_INPUT0_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x1	ISP1 Input0 Select 001: input from Parser0 CH0 010: input from Parser0 CH1 others: reserved

5.1.5.10. CSI ISP1 Input1 Select Register(Default Value:0x0000_0000)

Offset :0x0044			Register Name: CSI_ISP1_INPUT1_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	ISP1 Input1 Select 000: input from Parser0 CH1 others: reserved

5.1.5.11. CSI VIPP0 Input Select Register(Default Value:0x0000_0000)

Offset :0x0060			Register Name: CSI_SCL0_INPUT_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	VIPP0 Input Select

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			000: input from ISP0 CH0 001: input from ISP1 CH0 others: reserved

5.1.5.12. CSI VIPP1 Input Select Register(Default Value:0x0000_0000)

Offset :0x0064			Register Name: CSI_SCL1_INPUT_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	VIPP1 Input Select 000: input from ISP0 CH0 001: input from ISP1 CH0 010: input from ISP0 CH1 011: input from ISP1 CH1 others: reserved

5.1.5.13. Parser Enable Register(Default Value:0x0000_0000)

Offset: 0x0000			Register Name: PRS_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	NCSI_EN 0: Reset and disable the NCSI module 1: Enable the NCSI module
15	R/W	0x0	PCLK_EN 0:Gate pclk input 1:Enable pclk input
14:1	/	/	/
1	R/W	0x0	PRS_MODE 0: NCSI 1: MCSI
0	R/W	0x0	PRS_EN 0: Reset and disable the parser module 1: Enable the parser module

5.1.5.14. Parser NCSI Interface Configuration Register(Default Value:0x0105_0080)

Offset: 0x0004			Register Name: PRS_NCSI_IF_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x1	FIELD_DT_PCLK_SHIFT Only for vsync detected field mode,the odd field permitted pclk shift = 4*

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			FIELD_DT_PCLK_SHIFT
23:22	/	/	/
21	R/W	0x0	SRC_TYPE Source type 0: Progressed 1: Interlaced
20	/	/	/
19	R/W	0x0	FIELD For YUV HV timing, Field polarity 0: negative(field=0 indicate odd, field=1 indicate even) 1: positive(field=1 indicate odd, field=0 indicate even) For BT656 timing, Field sequence 0: Normal sequence (field 0 first) 1: Inverse sequence (field 1 first)
18	R/W	0x1	VREF_POL Vref polarity 0: negative 1: positive This register is not apply to CCIR656 interface.
17	R/W	0x0	HERF_POL Href polarity 0: negative 1: positive This register is not apply to CCIR656 interface.
16	R/W	0x1	CLK_POL Data clock type 0: active in rising edge 1: active in falling edge
15:14	R/W	0x0	Field_DT_MODE（only valid when CSI_IF is YUV and source type is interlaced） 00:by both field and vsync 01:by field 10:by vsync 11:reserved
13	R/W	0x0	DDR_SAMPLE_ MODE_EN 0:disable 1:enable
12:11	R/W	0x0	SEQ_8PLUS2 When select IF_DATA_WIDTH to be 8+2bit, odd/even pixel byte at CSI-D[11:4] will be rearranged to D[11:2]+2'b0 at the actual CSI data bus according to these sequences: 00: 6'bx+D[9:8], D[7:0] 01: D[9:2], 6'bx+D[1:0] 10: D[7:0], D[9:8]+6'bx 11: D[7:0], 6'bx+D[9:8]
10:8	R/W	0x0	IF_DATA_WIDTH

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			000: 8-bit data bus 001: 10-bit data bus 010: 12-bit data bus 011: 8+2-bit data bus 100: 2x8-bit data bus Others: Reserved
7:6	R/W	0x2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU
5	R/W	0x0	OUTPUT_MODE 0:field mode 1:frame mode
4:0	R/W	0x0	CSI_IF YUV(separate syncs): 00000: YUYV422 Interleaved or RAW (All data in one data bus) 00001: reserved 00010: Reserved 00011: Reserved CCIR656(embedded syncs): 00100: BT656 1 channel 00101: reserved 00110: Reserved 00111: Reserved 01100: BT656 2 channels (All data interleaved in one data bus) 01101: reserved 01110: reserved 01111:reserved Others: Reserved

5.1.5.15. Parser MCSI Interface Configuration Register(Default Value:0x0000_0080)

Offset: 0x0008			Register Name: PRS_MCSI_IF_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/

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7:6	R/W	0X2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU
5	R/W	0x0	OUTPUT_MODE 0:field mode 1:frame mode
4:0	/	/	/

5.1.5.16. Parser Capture Register(Default Value:0x0000_0000)

Offset: 0x000C			Register Name: PRS_CAP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:10	R/W	0x0	CH1_CAP_MASK Vsync number masked before capture.
9	R/W	0x0	CH1_VCAP_ON Video capture control: Capture the video image data stream on channel 1. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
8	RC/W	0x0	CH1_SCAP_ON Still capture control: Capture a single still image frame on channel 1. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self clearing and always reads as a 0.
7:6	/	/	/
5:2	R/W	0x0	CH0_CAP_MASK Vsync number masked before capture.
1	R/W	0x0	CH0_VCAP_ON Video capture control: Capture the video image data stream on channel 0. 0: Disable video capture

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			If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
0	R/W	0x0	CH0_SCAP_ON Still capture control: Capture a single still image frame on channel 0. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self clearing and always reads as a 0.

5.1.5.17. Parser Signal Status Register(Default Value:0x0000_0000)

Offset: 0x0010			Register Name: PRS_SIGNAL_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R	0x0	PCLK_STA Indicates the pclk status 0:low 1:high
23:0	R	0x0	DATA_STA Indicates the Dn status(n=0~9),MSB for D9,LSB for D0 0:low 1:high

5.1.5.18. Parser Channel_0 Input Format Register(Default Value:0x0000_0003)

Offset: 0x0024			Register Name: PRS_CH0_INFMT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

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5.1.5.19. Parser Channel_0 Output Horizontal Size Register(Default Value:0x0500_0000)

Offset: 0x0028			Register Name: PRS_CH0_OUTPUT_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

5.1.5.20. Parser Channel_0 Output Vertical Size Register(Default Value:0x01E0_0000)

Offset: 0x002C			Register Name: PRS_CH0_OUTPUT_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x1E0	VER_LEN Valid line number of a frame.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

5.1.5.21. Parser Channel_0 Input Parameter0 Register(Default Value:0x0000_0000)

Offset: 0x0030			Register Name: PRS_CH0_INPUT_PARA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE 0:Progress 1:Interlace

5.1.5.22. Parser Channel_0 Input Parameter3 Register(Default Value:0x0000_0000)

Offset: 0x003C			Register Name: PRS_CH0_INPUT_PARA3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_Y(Unit is line)
15:14	/	/	/
13:0	R	0x0	INPUT_X(Unit is byte)

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5.1.5.23. Parser Channel_0 Interrupt Enable Register(Default Value:0x0000_0000)

Offset: 0x0040			Register Name: PRS_CH0_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN 0:disable 1:enable
0	R/W	0x0	INPUT_PARA0_INT_EN 0:disable 1:enable

5.1.5.24. Parser Channel_0 Interrupt Status Register(Default Value:0x0000_0000)

Offset: 0x0044			Register Name: PRS_CH0_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W1C	0x0	MUL_ ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update,this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register,parser input parameter2 register or parser input parameter3 register update,this flag set to 1. Write 1 to clear.

5.1.5.25. Parser Channel_1 Input Format Register(Default Value:0x0000_0003)

Offset: 0x0124			Register Name: PRS_CH1_INFMT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

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5.1.5.26. Parser Channel_1 Output Horizontal Size Register(Default Value:0x0500_0000)

Offset: 0x0128			Register Name: PRS_CH1_OUTPUT_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

5.1.5.27. Parser Channel_1 Output Vertical Size Register(Default Value:0x01E0_0000)

Offset: 0x012C			Register Name: PRS_CH1_OUTPUT_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x1E0	VER_LEN Valid line number of a frame.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. Data is valid from this line.

5.1.5.28. Parser Channel_1 Input Parameter0 Register(Default Value:0x0000_0000)

Offset: 0x0130			Register Name: PRS_CH1_INPUT_PARA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE 0:Progress 1:Interlace

5.1.5.29. Parser Channel_1 Input Parameter3 Register(Default Value:0x0000_0000)

Offset: 0x013C			Register Name: PRS_CH1_INPUT_PARA3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_X

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5.1.5.30. Parser Channel_1 Interrupt Enable Register(Default Value:0x0000_0000)

Offset: 0x0140			Register Name: PRS_CH1_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN 0:disable 1:enable
0	R/W	0x0	INPUT_PARA0_INT_EN 0:disable 1:enable

5.1.5.31. Parser Channel_1 Interrupt Status Register(Default Value:0x0000_0000)

Offset: 0x0144			Register Name: PRS_CH1_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W1C	0x0	MUL_ ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update,this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register,parser input parameter2 register or parser input parameter3 register update,this flag set to 1. Write 1 to clear.

5.1.5.32. Parser NCSI RX Signal0 Delay Adjust Register(Default Value:0x0000_0000)

Offset: 0x0500			Register Name: PRS_NCSI_RX_SIGNAL0_DLY_ADJ_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x0	Vsync_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	Hsync_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	Pclk_dly 32 Step for adjust, 1 step = 0.2ns

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5.1.5.33. Parser NCSI RX Signal3 Delay Adjust Register(Default Value:0x0000_0000)

Offset: 0x050C			Register Name: PRS_NCSI_RX_SIGNAL3_DLY_ADJ_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x0	reserved
23:21	/	/	/
20:16	R/W	0x0	reserved
15:13	/	/	/
12:8	R/W	0x0	reserved
7:5	/	/	/
4:0	R/W	0x0	reserved

5.1.5.34. Parser NCSI RX Signal4 Delay Adjust Register(Default Value:0x0000_0000)

Offset: 0x0510			Register Name: PRS_NCSI_RX_SIGNAL4_DLY_ADJ_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x0	reserved
23:21	/	/	/
20:16	R/W	0x0	reserved
15:13	/	/	/
12:8	R/W	0x0	D9_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D8_dly 32 Step for adjust, 1 step = 0.2ns

5.1.5.35. Parser NCSI RX Signal5 Delay Adjust Register(Default Value:0x0000_0000)

Offset: 0x0514			Register Name: PRS_NCSI_RX_SIGNAL5_DLY_ADJ_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x0	D7_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D6_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D5_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/

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4:0	R/W	0x0	D4_dly 32 Step for adjust, 1 step = 0.2ns

5.1.5.36. Parser NCSI RX Signal6 Delay Adjust Register(Default Value:0x0000_0000)

Offset: 0x0518			Register Name: PRS_NCSI_RX_SIGNAL6_DLY_ADJ_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x0	D3_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D2_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D1_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D0_dly 32 Step for adjust, 1 step = 0.2ns

5.1.5.37. CSI DMA Enable Register(Default Value:0x0000_0000)

Offset:0x0000			Register Name: CSI_DMA_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	CLK_CNT_SPL Sampling time for clk counter per frame,when the CLK_CNT_EN is set to 1. 0: Sampling clock counter every frame done 1: Sampling clock counter every vsync
1	R/W	0x0	CLK_CNT_EN clk count per frame enable
0	R/W	0x0	DMA_EN 0: Disable 1: Enable

5.1.5.38. CSI DMA Configuration Register(Default Value:0x0000_0000)

Offset: 0x0004			Register Name: CSI_DMA_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	PAD_VAL Padding value when OUTPUT_FMT is prgb888

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			0x00~0xff
23:20	/	/	/
19:16	R/W	0x0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: field-raw-8 0001: field-raw-10 0010: reserved 0011: reserved 0100: field-rgb565 0101: field-rgb888 0110: field-prgb888 0111: reserved 1000: frame-raw-8 1001: frame-raw-10 1010: reserved 1011: reserved 1100: frame-rgb565 1101: frame-rgb888 1110: frame-prgb888 1111: reserved When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined(UV sequence) 0101: field planar YCbCr 420 UV combined(UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111: frame planar YCbCr 422 UV combined(UV sequence) 1000: filed planar YCbCr 422 UV combined(VU sequence) 1001: field planar YCbCr 420 UV combined(VU sequence) 1010: frame planar YCbCr 420 UV combined(VU sequence) 1011: frame planar YCbCr 422 UV combined(VU sequence) 1100: field planar YCbCr 422 10bit UV combined(UV sequence) 1101: field planar YCbCr 420 10bit UV combined(UV sequence) 1110: field planar YCbCr 422 10bit UV combined(VU sequence) 1111: field planar YCbCr 420 10bit UV combined(VU sequence) When the input format is set YUV420 0000: Reserved 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: reserved

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			0100: reserved 0101: field planar YCbCr 420 UV combined(UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111~1000: reserved 1001: field planar YCbCr 420 UV combined(VU sequence) 1010: frame planar YCbCr 420 UV combined(VU sequence) 1011~1100: reserved 1101: field planar YCbCr 420 10bit UV combined(UV sequence) 1110: reserved 1111: field planar YCbCr 420 10bit UV combined(VU sequence) Others: reserved
15:14	/	/	/
13	R/W	0x0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0:Disable 1:Enable
12	R/W	0x0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0:Disable 1:Enable
11:10	R/W	0x0	FIELD_SEL Field selection. 00: capturing with field 1. 01: capturing with field 2. 10: capturing with either field. 11: reserved
9:8	/	/	/
7:6	R/W	0x0	FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames
5:2	/	/	/
1:0	R/W	0x0	MIN_SDR_WR_SIZE Minimum size of SDRAM block write 0: 256 bytes (if hflip is enable, always select 256 bytes) 1: 512 bytes 2: 1k bytes 3: 2k bytes

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5.1.5.39. CSI DMA Horizontal Size Register(Default Value:0x0500_0000)

Offset: 0x0010			Register Name: CSI_DMA_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

5.1.5.40. CSI DMA Vertical Size Register(Default Value:0x01E0_0000)

Offset: 0x0014			Register Name: CSI_DMA_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x1E0	VER_LEN Valid line number of a frame.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

5.1.5.41. CSI DMA FIFO 0 Output Buffer-A Address Register(Default Value:0x0000_0000)

Offset: 0x0020			Register Name: CSI_DMA_F0_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	F0_BUFA FIFO 0 output buffer-A address

5.1.5.42. CSI DMA FIFO 1 Output Buffer-A Address Register(Default Value:0x0000_0000)

Offset: 0x0028			Register Name: CSI_DMA_F1_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	F1_BUFA FIFO 1 output buffer-A address

5.1.5.43. CSI DMA FIFO 2 Output Buffer-A Address Register(Default Value:0x0000_0000)

Offset: 0x0030			Register Name: CSI_DMA_F2_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:0	R/W	0x0	F2_BUFA FIFO 2 output buffer-A address

5.1.5.44. CSI DMA Buffer Length Register(Default Value:0x0140_0280)

Offset: 0x0038			Register Name: CSI_DMA_BUF_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	0x140	BUF_LEN_C Buffer length of chroma C in a line. Unit is byte.
15:14	/	/	/
13:0	R/W	0x280	BUF_LEN Buffer length of luminance Y in a line. Unit is byte.

5.1.5.45. CSI DMA Flip Size Register(Default Value:0x01E0_0280)

Offset: 0x003C			Register Name: CSI_DMA_FLIP_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x1E0	VER_LEN Vertical line number when in VFLIP mode. Unit is line.
15:13	/	/	/
12:0	R/W	0x280	VALID_LEN Valid components of a line when in HFLIP mode. Unit is pixel.

5.1.5.46. CSI DMA Interrupt Enable Register(Default Value:0x0000_0000)

Offset: 0x0050			Register Name: CSI_DMA_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
6	R/W	0x0	HB_OF_INT_EN Hblank FIFO overflow The bit is set when 3 FIFOs still overflow after the hblank.
5	R/W	0x0	LC_INT_EN Line counter flag The bit is set when the specific line has been written to dram every

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			frame.The line number is set in the line counter register.
4	R/W	0x0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
3	R/W	0x0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.
2	R/W	0x0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
1	R/W	0x0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is wrote to buffer as long as video capture remains enabled.
0	R/W	0x0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been wrote to buffer. For video capture, the bit is set when the last frame has been wrote to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

5.1.5.47. CSI DMA Interrupt Status Register(Default Value:0x0000_0000)

Offset: 0X0054			Register Name: CSI_DMA_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W1C	0x0	VS_PD vsync flag
6	R/W1C	0x0	HB_OF_PD Hblank FIFO overflow
5	R/W1C	0x0	LC_PD Line counter flag
4	R/W1C	0x0	FIFO2_OF_PD FIFO 2 overflow
3	R/W1C	0x0	FIFO1_OF_PD FIFO 1 overflow
2	R/W1C	0x0	FIFO0_OF_PD FIFO 0 overflow
1	R/W1C	0x0	FD_PD

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			Frame done
0	R/W1C	0x0	CD_PD Capture done

5.1.5.48. CSI DMA Line Counter Register(Default Value:0x0000_0000)

Offset: 0x0058			Register Name: CSI_DMA_LINE_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	LINE_CNT_NUM The LINE_CNT_NUM is set by user,when internal line counter reach the set value,the LC_PD will set.

5.1.5.49. CSI DMA Frame Clock Counter Register(Default Value:0x0000_0000)

Offset: 0x0060			Register Name: CSI_DMA_FRM_CLK_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R	0x0	FRM_CLK_CNT Counter value between every frame. For instant hardware frame rate statics. The internal counter is added by one every 12MHz clock cycle. When frame done or vsync comes, the internal counter value is sampled to FRM_CLK_CNT, and cleared to 0.

5.1.5.50. CSI DMA PCLK Statistic Register(Default Value:0x0000_7FFF)

Offset: 0x0070			Register Name: CSI_DMA_PCLK_STAT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:16	R	0x0	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for each line. Update at every vsync or framedone.
15	/	/	/
14:0	R	0x7FFF	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.

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5.1.5.51. CCI Control Register(Default Value:0x0000_0000)

Offset: 0x0000			Register Name: CCI_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SINGLE_TRAN 0: Transmission idle 1: Start single transmission Automatically cleared to '0' when finished. Abort current transmission immediately if changing from '1' to '0'. If slave not respond for the expected status over the time defined by TIMEOUT, current transmission will stop. PACKET_CNT will return the sequence number when transmission fail. All format setting and data will be loaded from registers and FIFO when transmission start.
30	R/W	0x0	REPEAT_TRAN 0: transmission idle 1: repeated transmission When this bit is set to 1, transmission repeats when trigger signal (such as VSYNC/ VCAP done) repeats. If changing this bit from '1' to '0' during transmission, the current transmission will be guaranteed then stop.
29	R/W	0x0	RESTART_MODE 0: RESTART 1: STOP+START Define the CCI action after sending register address.
28	R/W	0x0	READ_TRAN_MODE 0: send slave_id+W 1: do not send slave_id+W Setting this bit to 1 if reading from a slave which register width is equal to 0.
27:24	R	0x0	TRAN_RESULT 000: OK 001: FAIL Other: Reserved
23:16	R	/	CCI_STA 0x00: bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK received 0x58: Data byte received in master mode, ACK not received

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			0x01: Timeout when sending 9th SCL clk Other: Reserved
15:2	/	/	/
1	R/W	0x0	SOFT_RESET 0: normal 1: reset
0	R/W	0x0	CCI_EN 0: Module disable 1: Module enable

5.1.5.52. CCI Transmission Configuration Register(Default Value:0x1000_0000)

Offset: 0x0004			**Register Name: CCI_CFG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x10	TIMEOUT_N When sending the 9th clock, assert fail signal when slave device did not response after **N*F_{SCL}** cycles. And software must do a reset to CCI module and send a stop condition to slave.
23:16	R/W	0x0	INTERVAL Define the interval between each packet in 40*F_{SCL} cycles. 0~255
15	R/W	0x0	PACKET_MODE Select where to load slave id / data width 0: Compact mode 1: Complete mode In compact mode, slave id/register width / data width will be loaded from CCI_FMT register, only address and data read from memory. In complete mode, they will be loaded from packet memory.
14:7	/	/	/
6:4	R/W	0x0	TRIG_MODE Transmit mode 000: Immediately, no trigger 001: Reserved 010: CSI0 int trigger 011: CSI1 int trigger
3:0	R/W	0x0	CSI_TRIG CSI Int trig signal select 0000: First HREF start 0001: Last HREF done 0010: Line counter trigger other: Reserved

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5.1.5.53. CCI Packet Format Register(Default Value:0x0011_0001)

Offset: 0x0008			Register Name: CCI_FMT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	R/W	0x0	SLV_ID 7bit address
24	R/W	0x0	CMD 0: write 1: read
23:20	R/W	0x1	ADDR_BYTE How many bytes be sent as address 0~15
19:16	R/W	0x1	DATA_BYTE How many bytes be sent/received as data 1~15 Normally use ADDR_DATA with 0_2, 1_1, 1_2, 2_1, 2_2 access mode. If DATA bytes is 0, transmission will not start. In complete mode, the ADDR_BYTE and DATA_BYTE is defined in a byte's high/low 4bit.
15:0	R/W	0x1	PACKET_CNT FIFO data be transmitted as PACKET_CNT packets in current format. Total bytes not exceed 32bytes.

5.1.5.54. CCI Bus Control Register(Default Value:0x0000_25C0)

Offset: 0x000C			Register Name: CCI_BUS_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	DLY_CYC 0~65535 F_{SCL} cycles between each transmission
15	R/W	0x0	DLY_TRIG 0: disable 1: execute transmission after internal counter delay when triggered
14:12	R/W	0x2	CLK_N CCI bus sampling clock F0=24MHz/2^CLK_N
11:8	R/W	0x5	CLK_M CCI output SCL frequency is F_{SCL}=F1/10=(F0/(CLK_M+1))/10
7	R	0x1	SCL_STA SCL current status
6	R	0x1	SDA_STA SDA current status
5	R/W	0x0	SCL_PEN SCL PAD enable
4	R/W	0x0	SDA_PEN SDA PAD enable
3	R/W	0x0	SCL_MOV

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			SCL manual output value
2	R/W	0x0	SDA_MOV SDA manual output value
1	R/W	0x0	SCL_MOE SCL manual output en
0	R/W	0x0	SDA_MOE SDA manual output en

5.1.5.55. CCI Interrupt Control Register(Default Value:0x0000_0000)

Offset: 0x0014			Register Name: CCI_INT_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	S_TRAN_ERR_INT_EN
16	R/W	0x0	S_TRAN_COM_INT_EN
15:2	/	/	/
1	R/W1C	0x0	S_TRAN_ERR_PD
0	R/W1C	0x0	S_TRAN_COM_PD

5.1.5.56. CCI Line Counter Trigger Control Register(Default Value:0x0000_0000)

Offset: 0x0018			Register Name: CCI_LC_TRIG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	LN_CNT 0~8191: line counter send trigger when 1st~8192th line is received.

5.1.5.57. CCI FIFO Access Register(Default Value:0x0000_0000)

Offset: 0x0100~0x013C			Register Name: CCI_FIFO_ACC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DATA_FIFO From 0x100 to 0x13C, CCI data fifo is 64bytes, used in fifo input mode. CCI transmission read/write data from/to fifo in byte.

5.1.5.58. CCI Reserved Register(Default Value:0x0000_0000)

Offset: 0x0200~0x0220			Register Name: CCI_RSV_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	From 0x200 to 0x220 address, normal TWI registers are copied here. All

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			transmission will be act like hardware controlling these registers. And don't change them in transmission.

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Chapter 6 Display

This chapter describes the H6 V200 display system from following perspectives:

- DE
- TCON TV
- TCON LCD
- TV Encoder
- HDMI

The following figure shows the block diagram of display system:

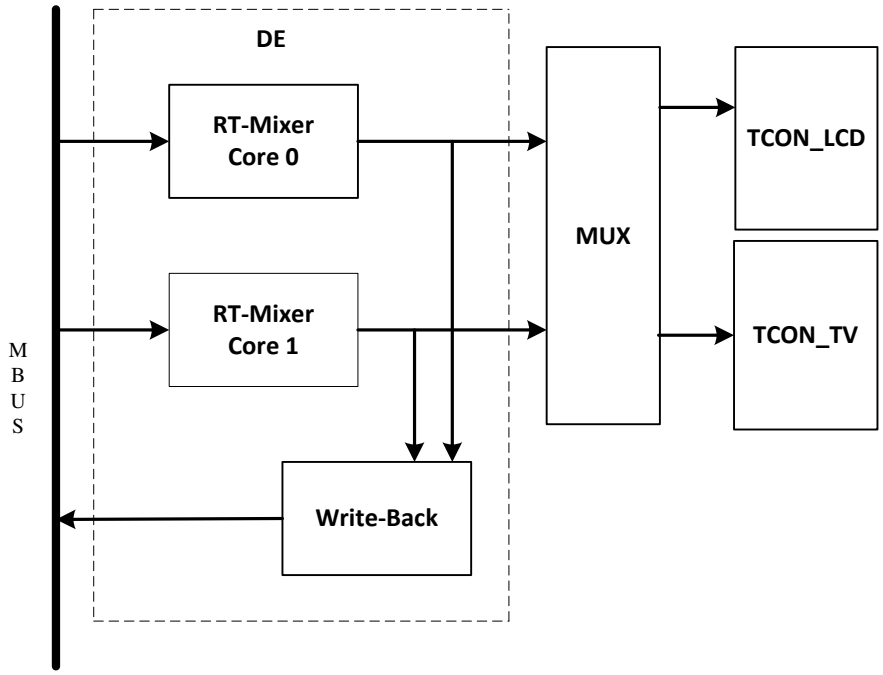


Figure 6-1. Display System Block Diagram

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6.1. DE

6.1.1. Overview

The Display Engine3.0(DE3.0) is a hardware composer to transfer image layers from a local bus or a video buffer to the TCON interface. The DE3.0 supports four overlay windows to blend, and supports image post-processing in the video channel.

Features:

- Output size up to 4096x4096
- Supports four alpha blending channels for main display, two channels for aux display
- Supports four overlay layers in each channel, and has a independent scaler
- Supports potter-duff compatible blending operation
- Supports AFBC buffer in main display
- Supports input format semi-planar of YUV422/YUV420/YUV411/P010/P210 and planar of YUV422/YUV420/YUV411, ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/RGB565
- Supports Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data
- Supports 10-bit processing path for HDR video
- Supports HDR-to-SDR and HLG-to-HDR conversion for HDR video and SDR-to-HDR conversion for SDR UI
- Supports SmartColor 3.0 for excellent display experience
  - Supports high quality video scaler with edge pattern detection
  - Adaptive detail/edge enhancement
  - Adaptive color enhancement
  - Adaptive contrast enhancement and fresh tone rectify
  - Adaptive de-noising with image quality assessment and block detector function
- Supports 3-D de-interlacer with low angle interpolation
- Supports write back for high efficient dual display and miracast

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6.2. TCON TV

6.2.1. Overview

The TCON_TV module is used for TV. The TCON_TV module includes the following features:

- Supports 10-bit pixeldepth YUV444, HV format output up to 4K@60Hz
- Supports 8-bit pixeldepth YUV444,HV format output up to 4K@60Hz

6.2.2. Block Diagram

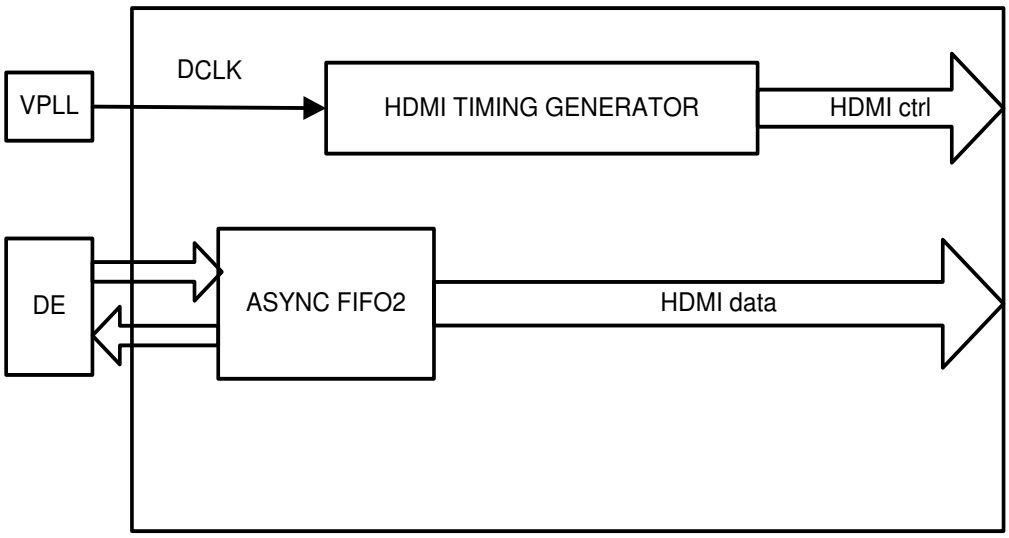


Figure 6-2. TCON TV Block Diagram

6.2.3. Operations and Functional Descriptions

6.2.3.1. Panel Interface

HV I/F is also known as Sync + DE mode, The HV_I/F is used to transfer signal to HDMI I/F.

Table 6-1. HV Panel Signals

Signal	Description	Type
Vsync	Vertical sync, indicates one new frame	O
Hsync	Horizontal sync, indicate one new scan line	O
DCLK	Dot clock, pixel data are sync by this clock	O

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LDE	LCD data enable	O
LD[29..0]	30Bit RGB/YUV output from input FIFO for panel	O

HV control signals are active low.

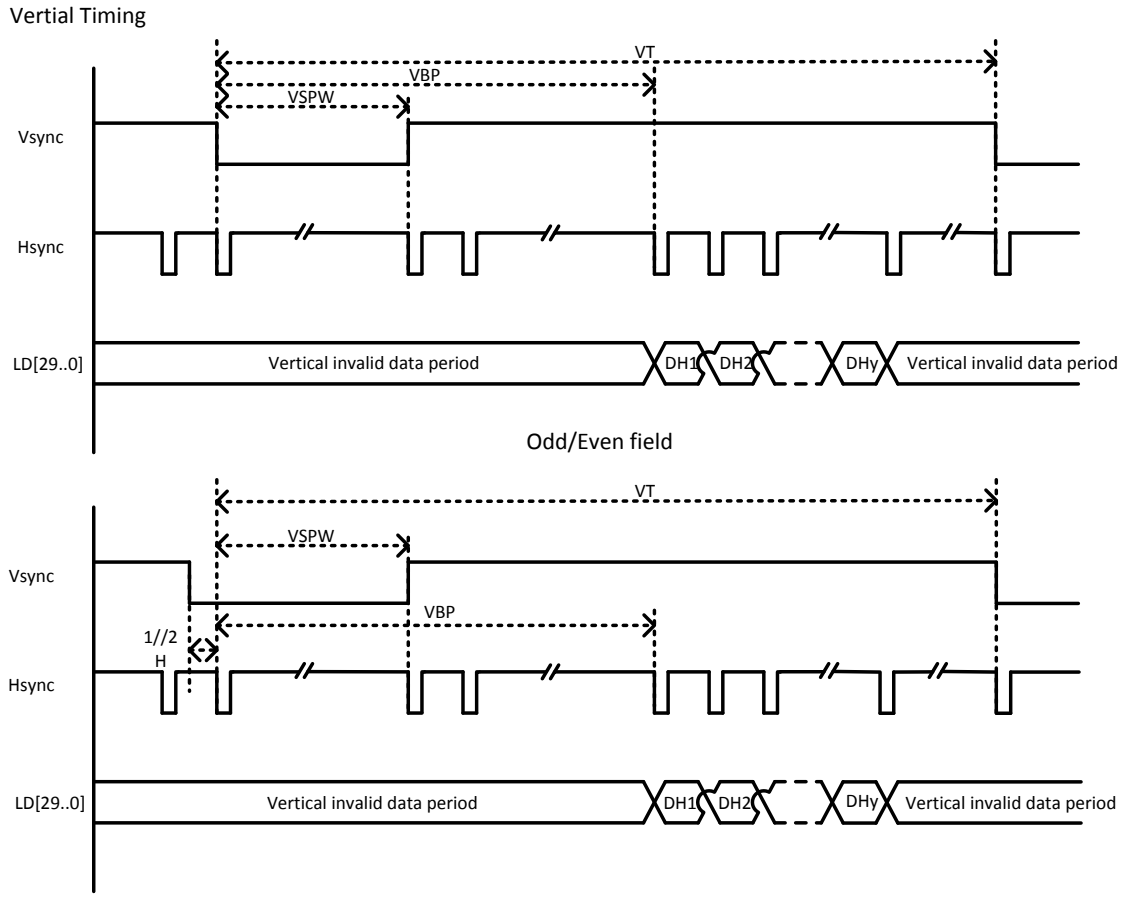


Figure 6-3. HV Interface Vertical Timing

6.2.3.2. CEU module

Function: This module enhance color data from DE .

R' = Rr*R + Rg*G + Rb*B
G' = Gr*R + Gg*G + Gb*B
B' = Br*R + Bg*G + Bb*B

NOTE

Rr, Rg, Rb, ,Gr, Gg, Gb, Br, Bg, Bb	**bool**	**0,1**
R, G, B	**u10**	**[0-1023]**

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R' have the range of [Rmin ,Rmax]
G' have the range of [Rmin ,Rmax]
B' have the range of [Rmin ,Rmax]

6.2.4. Register List

Module Name	Base Address
TCON_TV0	0x06515000

Register Name	Offset	Description
TV_GCTL_REG	0x000	TV Global Control Register
TV_GINT0_REG	0x004	TV Global Interrupt Register0
TV_GINT1_REG	0x008	TV Global Interrupt Register1
TV_CTL_REG	0x090	TV Control Register
TV_BASIC0_REG	0x094	TV Basic Timing Register0
TV_BASIC1_REG	0x098	TV Basic Timing Register1
TV_BASIC2_REG	0x09C	TV Basic Timing Register2
TV_BASIC3_REG	0x0A0	TV Basic Timing Register3
TV_BASIC4_REG	0x0A4	TV Basic Timing Register4
TV_BASIC5_REG	0x0A8	TV Basic Timing Register5
TV_IO_POL_REG	0x088	TV SYNC Signal Polarity Register
TV_IO_TRI_REG	0x08C	TV ISYNC Signal IO Control Register
TV_DEBUG_REG	0x0FC	TV Debug Register
TV_CEU_CTL_REG	0x100	TV CEU Control Register
TV_CEU_COEF_MUL_REG	0x110+N*0x04	TV CEU Coefficient Register0(N=0,1,2,4,5,6,8,9,10)
TV_CEU_COEF_RANG_REG	0x140+N*0x04	TV CEU Coefficient Register2(N=0,1,2)
TV_SAFE_PERIOD_REG	0x1F0	TV Safe Period Register
TV_FILL_CTL_REG	0x300	TV Fill Data Control Register
TV_FILL_BEGIN_REG	0x304+N*0x0C	TV Fill Data Begin Register(N=0,1,2)
TV_FILL_END_REG	0x308+N*0x0C	TV Fill Data End Register(N=0,1,2)
TV_FILL_DATA0_REG	0x30C+N*0x0C	TV Fill Data Value Register(N=0,1,2)
TV_DATA_IO_POL0_REG	0x330	TCON Data IO Polarity Control 0
TV_DATA_IO_POL1_REG	0x334	TCON Data IO Polarity Control 1
TV_DATA_ IO_TRI0_REG	0x338	TCON Data IO Enable Control 0
TV_DATA_ IO_TRI1_REG	0x33C	TCON Data IO Enable Control 1
TV_PIXELDEPTH_MODE_REG	0x340	TV Pixeldepth Mode Control Register

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6.2.5. Registers Description

6.2.5.1. TV_GCTL_REG(Default Value: 0x0000_0000)

Offset: 0x000			Register Name: TV_GCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TV_EN 0: disable 1: enable When it's disabled, the module will be reset to idle state.
30:0	/	/	/

6.2.5.2. TV_GINT0_REG(Default Value: 0x0000_0000)

Offset: 0x004			Register Name: TV_GINT0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	TV_VB_INT_EN 0: disable 1: enable
29	/	/	/
28	R/W	0x0	TV_LINE_INT_EN 0: disable 1: enable
27:15	/	/	/
14	R/W	0x0	TV_VB_INT_FLAG Asserted during vertical no-display period every frame. Write 0 to clear it.
13	/	/	/
12	R/W	0x0	TV_LINE_INT_FLAG trigger when SY1 match the current TV scan line Write 0 to clear it.
11:0	/	/	/

6.2.5.3. TV_GINT1_REG(Default Value: 0x0000_0000)

Offset: 0x008			Register Name: TV_GINT1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0x0	TV_Line_Int_Num scan line for TV line trigger(including inactive lines) Setting it for the specified line for trigger 1.

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			SY1 is writable only when LINE_TRG1 disable.

6.2.5.4. TV_SRC_CTL_REG(Default Value: 0x0000_0000)

Offset: 0x040			Register Name: TV0_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	TV_SRC_SEL 000: DE 001: Color Check 010: Grayscale Check 011: Black by White Check 100: Reserved 101: Reserved 111: Gridding Check

6.2.5.5. TV_CTL_REG(Default Value: 0x0000_0000)

Offset: 0x090			Register Name: TV_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TV_EN 0: disable 1: enable
30:9	/	/	/
8:4	R/W	0x0	START_DELAY This is for DE0 and DE1
3:2	/	/	/
1	R/W	0x0	TV_SRC_SEL 0: reserved 1: BLUE data The priority of this bit is higher than TV_SRC_SEL(bit[2:0]) in TV_SRC_CTL_REG.
0	/	/	/

6.2.5.6. TV_BASIC0_REG(Default Value: 0x0000_0000)

Offset: 0x094			Register Name: TV_BASIC0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	XI

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			source width is X+1
15:12	/	/	/
11:0	R/W	0x0	YI source height is Y+1

6.2.5.7. TV_BASIC1_REG(Default Value: 0x0000_0000)

Offset: 0x098			Register Name: TV_BASIC1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	LS_XO width is LS_XO+1
15:12	/	/	/
11:0	R/W	0x0	LS_YO width is LS_YO+1 this version LS_YO = TV_YI

6.2.5.8. TV_BASIC2_REG(Default Value: 0x0000_0000)

Offset: 0x09C			Register Name: TV_BASIC2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	TV_XO width is TV_XO+1
15:12	/	/	/
11:0	R/W	0x0	TV_YO height is TV_YO+1

6.2.5.9. TV_BASIC3_REG(Default Value: 0x0000_0000)

Offset: 0x0A0			Register Name: TV_BASIC3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	HT horizontal total time Thcycle = (HT+1) * Thdclk
15:12	/	/	/
11:0	R/W	0x0	HBP horizontal back porch Thbp = (HBP +1) * Thdclk

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6.2.5.10. TV_BASIC4_REG(Default Value: 0x0000_0000)

Offset: 0x0A4			Register Name: TV_BASIC4_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	VT horizontal total time (in HD line) Tvt = VT/2 * Th
15:12	/	/	/
11:0	R/W	0x0	VBP horizontal back porch (in HD line) Tvbp = (VBP +1) * Th

6.2.5.11. TV_BASIC5_REG(Default Value: 0x0000_0000)

Offset: 0x0A8			Register Name: TV_BASIC5_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x0	HSPW horizontal Sync Pulse Width (in dclk) Thspw = (HSPW+1) * Tdclk HT> (HSPW+1)
15:10	/	/	/
9:0	R/W	0x0	VSPW vertical Sync Pulse Width (in lines) Tvspw = (VSPW+1) * Th VT/2 > (VSPW+1)

6.2.5.12. TV_IO_POL_REG(Default Value: 0x0000_0000)

Offset: 0x088			Register Name: TV_IO_POL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	0x0	IO3_INV 0: not invert 1: invert
26	R/W	0x0	IO2_INV 0: not invert 1: invert
25	R/W	0x0	IO1_INV 0: not invert 1: invert
24	R/W	0x0	IO0_INV

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			0: not invert 1: invert
23:0	/	/	/

6.2.5.13. TV_IO_TRI_REG(Default Value: 0x0F00_0000)

Offset: 0x08C			Register Name: TV_IO_TRI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	0x1	IO3_OUTPUT_TRI_EN 1: disable 0: enable
26	R/W	0x1	IO2_OUTPUT_TRI_EN 1: disable 0: enable
25	R/W	0x1	IO1_OUTPUT_TRI_EN 1: disable 0: enable
24	R/W	0x1	IO0_OUTPUT_TRI_EN 1: disable 0: enable
23:0	/	/	/

6.2.5.14. TV_DEBUG_REG(Default Value: 0x0000_0000)

Offset: 0x0FC			Register Name: TV_DEBUG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	TV_FIFO_UNDER_FLOW
29	/	/	/
28	R	0x0	TV_FIELD_POLARITY 0: second field 1: first field
27:12	/	/	/
13	R/W	0x0	LINE_BUF_BYPASS 0: used 1: bypass
12	/	/	/
11:0	R	0x0	TV_CURRENT_LINE

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6.2.5.15. TV_CEU_CTL_REG(Default Value: 0x0000_0000)

Offset: 0x100			Register Name: TV_CEU_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CEU_EN 0: bypass 1: enable
30:0	/	/	/

6.2.5.16. TV_CEU_COEF_MUL_REG(Default Value: 0x0000_0000)

Offset: 0x110+N*0x04 (N=0,1,2,4,5,6,8,9,10)			Register Name: TV_CEU_COEF_MUL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	CEU_COEF_MUL_VALUE 1. CEU_Coef_Mul_Value only can be 0 or 1 2. REG Map: N=0: Rr N=1: Rg N=2: Rb N=4: Gr N=5: Gg N=6: Gb N=8: Br N=9: Bg N=10: Bb
7:0	/	/	/

6.2.5.17. TV_CEU_COEF_RANG_REG(Default Value: 0x0000_0000)

Offset: 0x140+N*0x04 (N=0,1,2)			Register Name: TV_CEU_COEF_RANG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x0	CEU_COEF_RANGE_MIN unsigned 10bit value, range of [0,1023]
15:10	/	/	/
9:0	R/W	0x0	CEU_COEF_RANGE_MAX unsigned 10bit value, range of [0,1023]

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6.2.5.18. TV_SAFE_PERIOD_REG(Default Value: 0x0000_0000)

Offset: 0x1F0			Register Name: TV_SAFE_PERIOD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	SAFE_PERIOD_FIFO_NUM
15:4	R/W	0x0	SAFE_PERIOD_LINE
3	/	/	/
2:0	R/W	0x0	SAFE_PERIOD_MODE 000: unsafe 001: safe 010: safe at line_buf_curr_num > safe_period_fifo_num 011: safe at 2 and safe at sync active 100: safe at line

6.2.5.19. TV_FILL_CTL_REG(Default Value: 0x0000_0000)

Offset: 0x300			Register Name: TV_FILL_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TV_FILL_EN 0: bypass 1: enable
30:0	/	/	/

6.2.5.20. TV_FILL_BEGIN_REG(Default Value: 0x0000_0000)

Offset: 0x304+N*0x0C (N=0,1,2)			Register Name: TV_FILL_BEGIN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	FILL_BEGIN

6.2.5.21. TV_FILL_END_REG(Default Value: 0x0000_0000)

Offset: 0x308+N*0x0C (N=0,1,2)			Register Name: TV_FILL_END_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	FILL_END

6.2.5.22. TV_FILL_DATA_REG(Default Value: 0x0000_0000)

Offset: 0x30C+N*0x0C (N=0,1,2)	Register Name: TV_FILL_DATA_REG

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Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:0	R/W	0x0	FILL_VALUE

6.2.5.23. TV_DATA_IO_POL0_REG(Default Value: 0x0000_0000)

Offset: 0x330			Register Name: TV_DATA_IO_POL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x0	R/CB_CHANNEL_DATA_INV[bit9:0] 0: normal polarity 1: invert the specify output
15:10	/	/	/
9:0	R/W	0x0	G/Y_CHANNEL_DATA_INV[bit9:0] 0: normal polarity 1: invert the specify output

6.2.5.24. TV_DATA_IO_POL1_REG(Default Value: 0x0000_0000)

Offset: 0x334			Register Name: TV_DATA_IO_POL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x0	B/CR_CHANNEL_DATA_INV 0: normal polarity 1: invert the specify output
15:0	/	/	/

6.2.5.25. TV_DATA_IO_TRI0_REG(Default Value: 0x03ff_03ff)

Offset: 0x338			Register Name: ADD_ TV_IO_TRI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x3ff	R/CB_CHANNEL_DATA_OUTPUT_TRI_EN 1: disable 0: enable Only high 6-bit is valid.
15:10	/	/	/
9:0	R/W	0x3ff	G/Y_CHANNEL_DATA_OUTPUT_TRI_EN 1: disable 0: enable Only high 6-bit is valid.

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6.2.5.26. TV_DATA_ IO_TRI1_REG(Default Value: 0x03ff_0000)

Offset: 0x33C			Register Name: ADD_ TV_IO_TRI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x3ff	B/CR_CHANNEL_DATA_OUTPUT_TRI_EN 1: disable 0: enable Only high 6-bit is valid.
15:0	/	/	/

6.2.5.27. TV_PIXELDEPTH_MODE_REG(Default Value: 0x0000_0000)

Offset: 0x340			Register Name: TV_PIXELDEPTH_MODE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	Colorbar Pixeldepth mode(Only valid for Colorbar output) 0: 8-bit mode 1: 10-bit mode

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6.3. TCON LCD

6.3.1. Overview

The TCON_LCD module is used for LCD. The TCON_LCD module includes the following features:

- Supports RGB interface with DE/SYNC mode, up to 1920x1080@60fps
- Supports serial RGB/dummy RGB interface, up to 800x480@60fps
- Supports i8080 interface, up to 800x480@60fps
- Supports CCIR656 interface for NTSC and PAL
- Supports RGB888, RGB666 and RGB565 with dither function
- Supports Gamma correction with R/G/B channel independence
- Supports color re-mapping
- Supports color enhance

6.3.2. Block Diagram

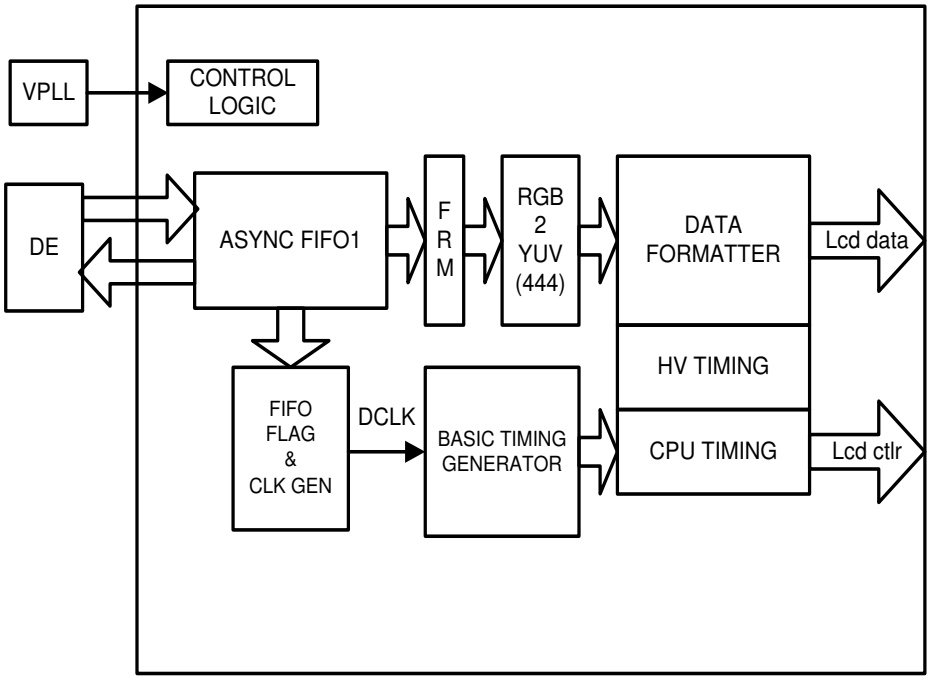


Figure 6-4.TCON_LCD Block Diagram

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6.3.3. Operations and Functional Descriptions

6.3.3.1. Panel Interface

6.3.3.1.1. HV_I/F(Sync+DE mode)

HV I/F is also known as Sync + DE mode, which is widely used in TFT LCD module for PMP/MP4 application.

Table 6-2. HV Panel Signals

Signal	Description	Type
Vsync	Vertical sync, indicates one new frame	O
Hsync	Horizontal sync, indicate one new scan line	O
DCLK	Dot clock, pixel data are sync by this clock	O
LDE	LCD data enable	O
LD[23..0]	24Bit RGB/YUV output from input FIFO for panel	O

The timing diagram of HV interface is as follows.

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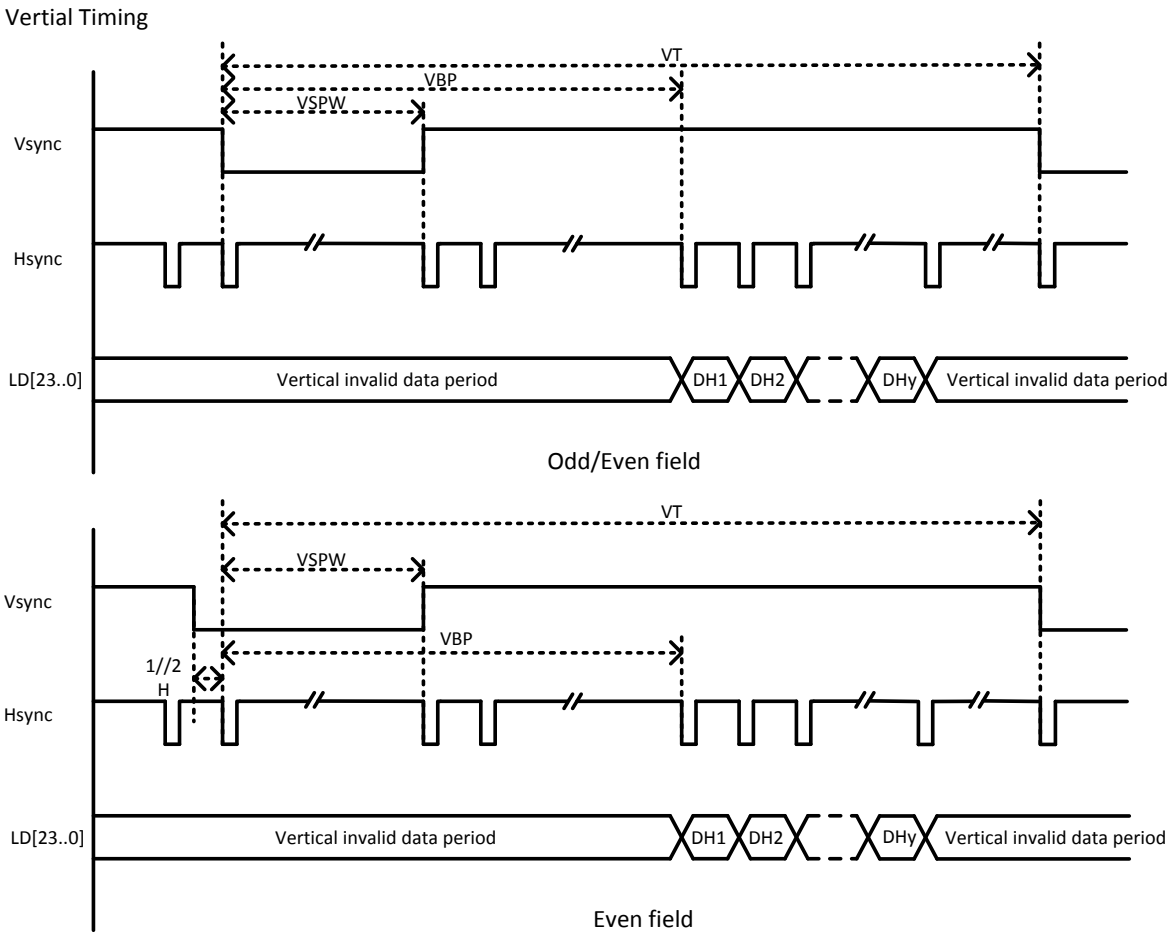


Figure 6-5.HV Interface Vertical Timing

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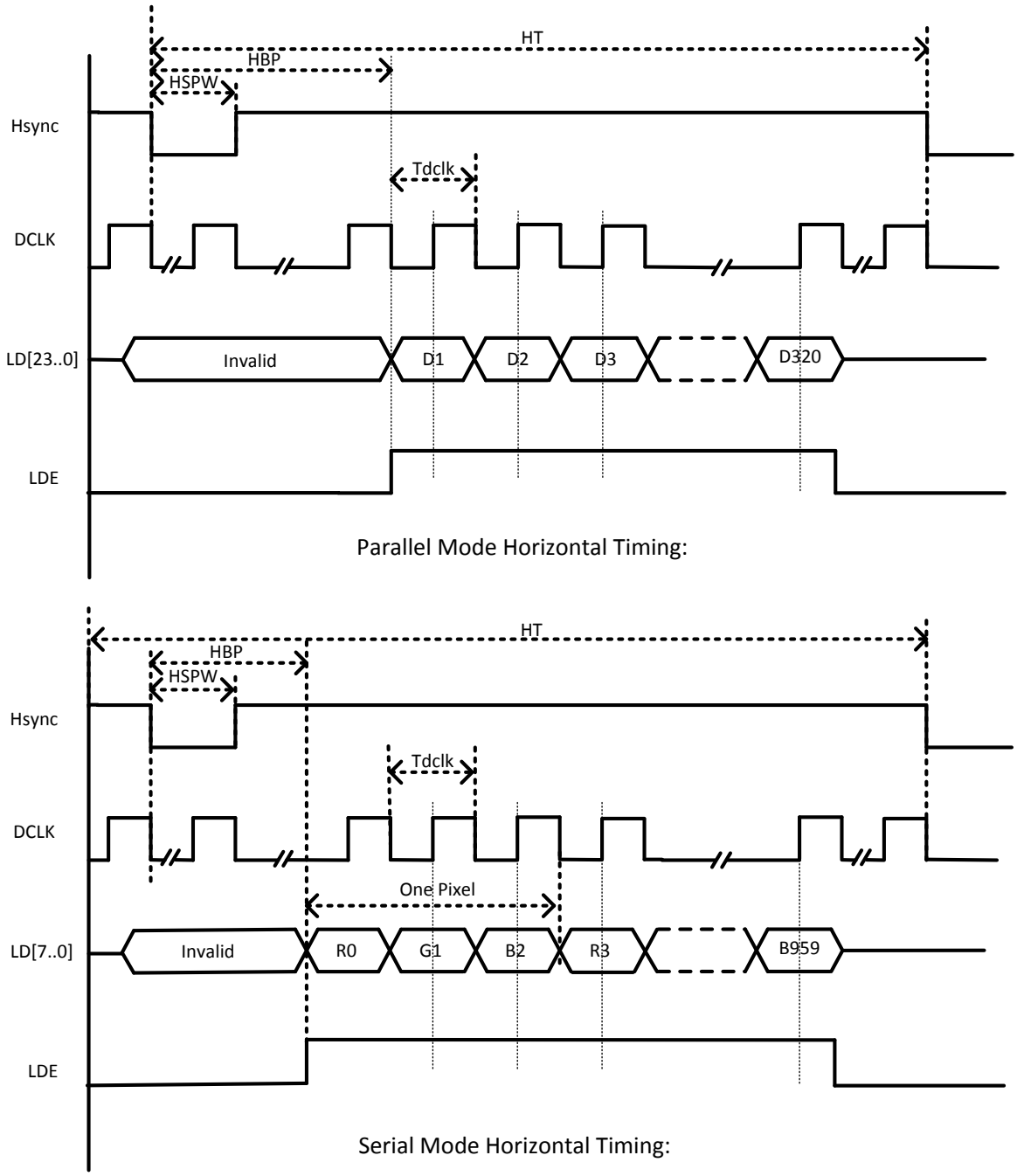


Figure 6-6.HV Interface Horizontal Timing

6.3.3.1.2. CCIR Output SAV/EAV Sync Signal

When in HV serial YUV output mode, its timing is CCIR656/601 compatible. SAV add right before active area every line; EAV add right after active area every line.

Its logic is:

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F = “0” for Field 1 F = “1” for Field 2

V = “1” during vertical blanking

H = “0” at SAV H = “1” at EAV

P3-P0 = protection bits

P3 = V ⊕H

P2 = F ⊕H

P1 = F ⊕V

P0 = F ⊕V ⊕H

Where ⊕represents the exclusive-OR function

The 4 byte SAV/EAV sequences are:

Table 6-3. EAV and SAV Sequence

	8-bit Data								**10-bit Data**	
	D9 (MSB)	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
preamble	1	1	1	1	1	1	1	1	1	1
	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0
Status word	1	F	V	H	P3	P2	P1	P0	0	0

6.3.3.1.3. CPU_I/F

CPU I/F LCD panel is most common interface for small size, low resolution LCD panels.

CPU control signals are active low.

Table 6-4. CPU Panel Signals

Main Signal	**Description**	**Type**
CS	Chip select, active low	O
WR	Write strobe, active low	O
RD	Read strobe, active low	O
A1	Address bit, controlled by "LCD_CPUI/F" BIT26/25	O
D[23..0]	Digital RGB output signal	I/O

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The following figure relationship between basic timing and CPU timing. WR is 180 degree delay of DCLK; CS is active when pixel data are valid; RD is always set to 1; A1 are set by "**Lcd_CPUI/F**".

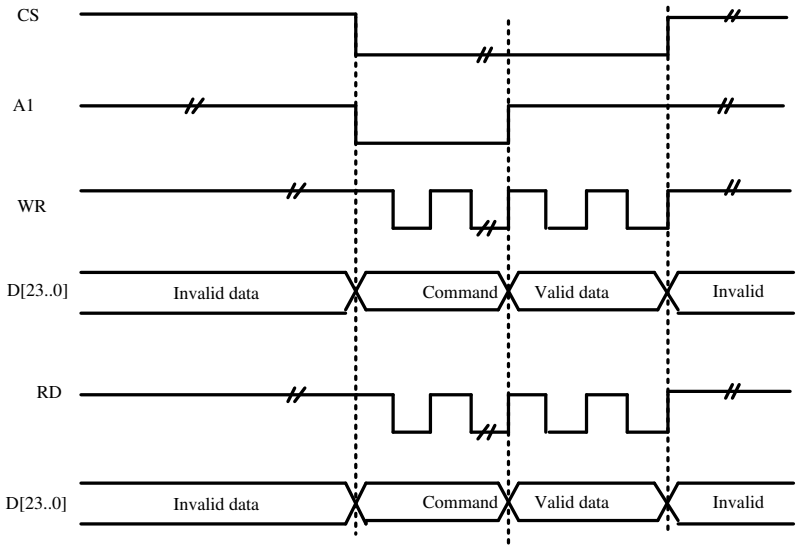


Figure 6-7. CPU Interface Timing

When CPU I/F is in IDLE state, it can generate WR/RD timing by setting "**Lcd_CPUI/F**". CS strobe is one DCLK width, WR/RD strobe is half DCLK width.

6.3.3.2. RGB Gamma Correction

Function: This module correct the RGB input data of DE.

A 256*8*3 Byte register file is used to store the gamma table. The following is the layout:

Table 6-5. RGB Gamma Correction Table

Offset	Value
0x400, 0x401, 0x402	{ B0[7:0], G0[7:0], R0[7:0] }
0x404,	{ B1[7:0], G1[7:0], R1[7:0] }
.....	.....
0x4FC	{ B255[7:0], G255[7:0], R255[7:0] }

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6.3.3.3. CEU module

Function: This module enhance color data from DE0 .

R' = Rr*R + Rg*G + Rb*B + Rc
G' = Gr*R + Gg*G + Gb*B +Gc
B' = Br*R + Bg*G + Bb*B + Bc

NOTE

Rr, Rg, Rb, ,Gr, Gg, Gb, Br, Bg, Bb	**s13**	**(-16,16)**
Rc, Gc, Bc	**s19**	**(-16384, 16384)**
R, G, B	**u8**	**[0-255]**

R' have the range of [Rmin ,Rmax]
G' have the range of [Rmin ,Rmax]
B' have the range of [Rmin ,Rmax]

6.3.3.4. CMAP Module

Function: This module map color data from DE.

Every 4 input pixels as an unit. an unit is divided into 12 bytes. Output byte can select one of those 12 bytes.Note that even line and odd line can be different, and output can be 12 bytes(4 pixels) or reduce to 6 bytes(2 pixels).

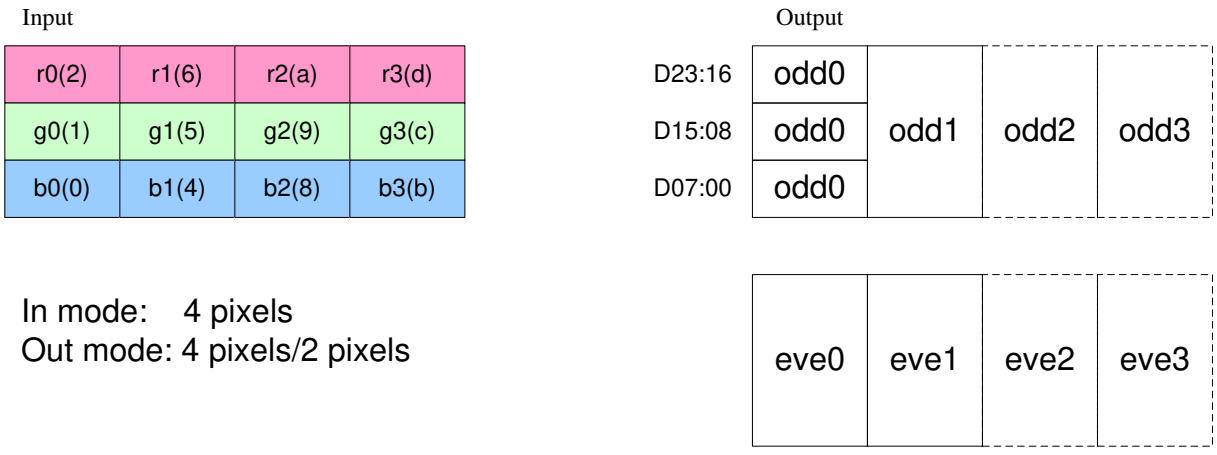


Figure 6-8. CMAP Module

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6.3.4. Register List

Module Name	Base Address
TCON_LCD0	0x06511000

Register Name	Offset	Description
LCD_GCTL_REG	0x000	LCD Global Control Register
LCD_GINT0_REG	0x004	LCD Global Interrupt Register0
LCD_GINT1_REG	0x008	LCD Global Interrupt Register1
LCD_FRM_CTL_REG	0x010	LCD FRM Control Register
LCD_FRM_SEED_REG	0x014+N*0x04	LCD FRM Seed Register(N=0,1,2,3,4,5)
LCD_FRM_TAB_REG	0x02C+N*0x04	LCD FRM Table Register(N=0,1,2,3)
LCD_3D_FIFO_REG	0x03C	LCD 3D FIFO Register
LCD_CTL_REG	0x040	LCD Control Register
LCD_DCLK_REG	0x044	LCD Data Clock Register
LCD_BASIC0_REG	0x048	LCD Basic Timing Register0
LCD_BASIC1_REG	0x04C	LCD Basic Timing Register1
LCD_BASIC2_REG	0x050	LCD Basic Timing Register2
LCD_BASIC3_REG	0x054	LCD Basic Timing Register3
LCD_HV_IF_REG	0x058	LCD HV Panel Interface Register
LCD_CPU_IF_REG	0x060	LCD CPU Panel Interface Register
LCD_CPU_WR_REG	0x064	LCD CPU Panel Write Data Register
LCD_CPU_RD0_REG	0x068	LCD CPU Panel Read Data Register0
LCD_CPU_RD1_REG	0x06C	LCD CPU Panel Read Data Register1
LCD_IO_POL_REG	0x088	LCD IO Polarity Register
LCD_IO_TRI_REG	0x08C	LCD IO Control Register
LCD_DEBUG_REG	0x0FC	LCD Debug Register
LCD_CEU_CTL_REG	0x100	LCD CEU Control Register
LCD_CEU_COEF_MUL_REG	0x110+N*0x04	LCD CEU Coefficient Register0(N=0,1,2,4,5,6,8,9,10)
LCD_CEU_COEF_ADD_REG	0x11C+N*0x10	LCD CEU Coefficient Register1(N=0,1,2)
LCD_CEU_COEF_RANG_REG	0x140+N*0x04	LCD CEU Coefficient Register2(N=0,1,2)
LCD_CPU_TRI0_REG	0x160	LCD CPU Panel Trigger Register0
LCD_CPU_TRI1_REG	0x164	LCD CPU Panel Trigger Register1
LCD_CPU_TRI2_REG	0x168	LCD CPU Panel Trigger Register2
LCD_CPU_TRI3_REG	0x16C	LCD CPU Panel Trigger Register3
LCD_CPU_TRI4_REG	0x170	LCD CPU Panel Trigger Register4
LCD_CPU_TRI5_REG	0x174	LCD CPU Panel Trigger Register5
LCD_CMAP_CTL_REG	0x180	LCD Color Map Control Register
LCD_CMAP_ODD0_REG	0x190	LCD Color Map Odd Line Register0
LCD_CMAP_ODD1_REG	0x194	LCD Color Map Odd Line Register1
LCD_CMAP_EVEN0_REG	0x198	LCD Color Map Even Line Register0
LCD_CMAP_EVEN1_REG	0x19C	LCD Color Map Even Line Register1

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LCD_SAFE_PERIOD_REG	0x1F0	LCD Safe Period Register
LCD_GAMMA_TABLE_REG	0x400-0x7FF	LCD Gamma Table Registers

6.3.5. Register Description

6.3.5.1. LCD_GCTL_REG(Default Value: 0x0000_0000)

Offset: 0x000			Register Name: LCD_GCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LCD_EN 0: disable 1: enable When it is disabled, the module will be reset to idle state.
30	R/W	0x0	LCD_GAMMA_EN 0: disable 1: enable
29:0	/	/	/

6.3.5.2. LCD_GINT0_REG(Default Value: 0x0000_0000)

Offset: 0x004			Register Name: LCD_GINT0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LCD_VB_INT_EN 0: disable 1: enable
30	/	/	/
29	R/W	0x0	LCD_LINE_INT_EN 0: disable 1: enable
28	/	/	/
27	R/W	0x0	LCD_TRI_FINISH_INT_EN 0: disable 1: enable
26:	R/W	0x0	LCD_TRI_COUNTER_INT_EN 0: disable 1: enable
25:16	/	/	/
15	R/W0C	0x0	LCD_VB_INT_FLAG Asserted during vertical no-display period every frame. Write 0 to clear it.
14	/	/	/
13	R/W0C	0x0	LCD_LINE_INT_FLAG

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			trigger when SY0 match the current LCD scan line Write 0 to clear it.
12	/	/	/
11	R/W0C	0x0	LCD_TRI_FINISH_INT_FLAG trigger when cpu trigger mode finish Write 0 to clear it.
10	R/W0C	0x0	LCD_TRI_COUNTER_INT_FLAG trigger when tri counter reach this value Write 0 to clear it.
9	R/W0C	0x0	LCD_TRI_UNDERFLOW_FLAG only used in dsi video mode, tri when sync by dsi but not finish Write 0 to clear it.
8:0	/	/	/

6.3.5.3. LCD_GINT1_REG(Default Value: 0x0000_0000)

Offset: 0x008			**Register Name: LCD_GINT1_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	LCD_LINE_INT_NUM scan line for LCD line trigger(including inactive lines) Setting it for the specified line for trigger0. SY0 is writable only when LINE_TRG0 disable.
15:0	/	/	/

6.3.5.4. LCD_FRM_CTL_REG(Default Value: 0x0000_0000)

Offset: 0x010			**Register Name: LCD_FRM_CTL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LCD_FRM_EN 0:disable 1:enable
30:7	/	/	/
6	R/W	0x0	LCD_FRM_MODE_R 0: 6bit frm output 1: 5bit frm output
5	R/W	0x0	LCD_FRM_MODE_G 0: 6bit frm output 1: 5bit frm output
4	R/W	0x0	LCD_FRM_MODE_B 0: 6bit frm output 1: 5bit frm output
3:2	/	/	/

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1:0	R/W	0x0	LCD_FRM_TEST 00: FRM 01: half 5/6bit, half FRM 10: half 8bit, half FRM 11: half 8bit, half 5/6bit

6.3.5.5. LCD_FRM_SEED_REG(Default Value: 0x0000_0000)

Offset: 0x014+N*0x04(N=0,1,2,3,4,5)			Register Name: LCD_FRM_SEED_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24:0	R/W	0x0	SEED_VALUE N=0: Pixel_Seed_R N=1: Pixel_Seed_G N=2: Pixel_Seed_B N=3: Line_Seed_R N=4: Line_Seed_G N=5: Line_Seed_B Avoid set it to 0

6.3.5.6. LCD_FRM_TAB_REG(Default Value: 0x0000_0000)

Offset: 0x02C+N*0x04(N=0,1,2,3)			Register Name: LCD_FRM_TAB_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	FRM_TABLE_VALUE

6.3.5.7. LCD_3D_FIFO_REG(Default Value: 0x0000_0000)

Offset: 0x03C			Register Name: LCD_3D_FIFO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	3D_FIFO_BIST_EN 0: disable 1: enable
30:14	/	/	/
13:4	R/W	0x0	3D_FIFO_HALF_LINE_SIZE The number of data in half line=3D_FIFO_HALF_LINE_SIZE+1 only valid when 3D_FIFO_SETTING set as 2
3:2	/	/	/
1:0	R/W	0x0	3D_FIFO_SETTING 0: by pass 1: used as normal FIFO 2: used as 3D interlace FIFO

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			3: reserved

6.3.5.8. LCD_CTL_REG(Default Value: 0x0000_0000)

Offset: 0x040			Register Name: LCD_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LCD_EN 0: disable 1: enable It executes at the beginning of the first blank line of LCD timing.
30:29	/	/	/
28	R/W	0x0	LCD_WORK_MODE 0: normal 1: dynamic freq
27:26	/	/	/
25:24	R/W	0x0	LCD_IF 00: HV(Sync+DE) 01: 8080 I/F 1x:reservd
23	R/W	0x0	LCD_RB_SWAP 0: default 1: swap RED and BLUE data at FIFO1
22	R/W	0x0	LCD_TEST_VALUE 0:all 0s 1:all 1s
21	R/W	0x0	LCD_FIFO1_RST Write 1 and then 0 at this bit will reset FIFO 1 1 holding time must more than 1 DCLK
20	R/W	0x0	LCD_INTERLACE_EN 0:disable 1:enable This flag is valid only when LCD_EN == 1
19:9	/	/	/
8:4	R/W	0x0	LCD_START_DELAY STA delay Valid only when LCD_EN == 1
3	/	/	/
2:0	R/W	0x0	LCD_SRC_SEL 000: DE 001: Color Check 010: Grayscale Check 011: Black by White Check 100: Test Data all 0 101: Test Data all 1

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			111: Gridding Check

6.3.5.9. LCD_DCLK REG(Default Value: 0x0000_0000)

Offset: 0x044			Register Name: LCD_DCLK REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:28	R/W	0x0	LCD_DCLK_EN
			LCLK_EN[3:0] :LCD clock enable
			4'h0, 'h4,4'h6,4'ha7:dclk_en=0;dclk1_en=0;dclk2_en=0;dclkm2_en=0;
			4'h1: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 0;
			4'h2: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 1;
			4'h3: dclk_en = 1; dclk1_en = 1; dclk2_en = 0; dclkm2_en = 0;
			4'h5: dclk_en = 1; dclk1_en = 0; dclk2_en = 1; dclkm2_en = 0;
			4'h8,4'h9,4'ha,4'hb,4'hc,4'hd,4'he,4'hf:
			dclk_en = 1;
			dclk1_en = 1;
			dclk2_en = 1;
			dclkm2_en = 1;

27:7	/	/	/
6:0	R/W	0x0	LCD_DCLK_DIV Tdclk = Tsclk * DCLKDIV 1.if dclk1&dclk2 used, DCLKDIV >=6 2.if dclk only, DCLKDIV >=1

6.3.5.10. LCD_BASIC0_REG(Default Value: 0x0000_0000)

Offset: 0x048			Register Name: LCD_BASIC0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	X Panel width is X+1
15:12	/	/	/
11:0	R/W	0x0	Y Panel height is Y+1

6.3.5.11. LCD_BASIC1_REG(Default Value: 0x0000_0000)

Offset: 0x04C			Register Name: LCD_BASIC1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	HT Thcycle = (HT+1) * Tdclk

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			Computation 1) parallel:HT = X + BLANK Limitation: 1) parallel :HT >= (HBP +1) + (X+1) +2 2) serial 1: HT >= (HBP +1) + (X+1) *3+2 3) serial 2: HT >= (HBP +1) + (X+1) *3/2+2
15:12	/	/	/
11:0	R/W	0x0	HBP horizontal back porch (in dclk) Thbp = (HBP +1) * Tdclk

6.3.5.12. LCD_BASIC2_REG(Default Value: 0x0000_0000)

Offset: 0x050			Register Name: LCD_BASIC2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	VT TVT = (VT)/2 * Thsync VT/2 >= (VBP+1) + (Y+1) +2
15:12	/	/	/
11:0	R/W	0x0	VBP Tvbp = (VBP +1) * Thsync

6.3.5.13. LCD_BASIC3_REG(Default Value: 0x0000_0000)

Offset: 0x054			Register Name: LCD_BASIC3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x0	HSPW Thspw = (HSPW+1) * Tdclk HT> (HSPW+1)
15:10	/	/	/
9:0	R/W	0x0	VSPW Tvspw = (VSPW+1) * Thsync VT/2 > (VSPW+1)

6.3.5.14. LCD_HV_IF_REG(Default Value: 0x0000_0000)

Offset: 0x058			Register Name: LCD_HV_IF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	HV_MODE 0000: 24bit/1cycle parallel mode

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			1000: 8bit/3cycle RGB serial mode(RGB888) 1010: 8bit/4cycle Dummy RGB(DRGB) 1011: 8bit/4cycle RGB Dummy(RGBD) 1100: 8bit/2cycle YUV serial mode(CCIR656)
27:26	R/W	0x0	RGB888_ODD_ORDER serial RGB888 mode Output sequence at odd lines of the panel (line 1, 3, 5, 7…) 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B
25:24	R/W	0x0	RGB888_EVEN_ORDER serial RGB888 mode Output sequence at even lines of the panel (line 2, 4, 6, 8…) 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B
23:22	R/W	0x0	YUV_SM serial YUV mode Output sequence 2-pixel-pair of every scan line 00: YUYV 01: YVYU 10: UYVY 11: VYUY
21:20	R/W	0x0	YUV EAV/SAV F LINE DELAY 00:F toggle right after active video line 01:delay 2 line(CCIR PAL) 10:delay 3 line(CCIR NTSC) 11:reserved
19	R/W	0x0	CCIR_CSC_DIS 0: enable 1: disable Only valid when HV mode is “1100”, select ‘0’ LCD convert source from RGB to YUV
18:0	/	/	/

6.3.5.15. LCD_CPU_IF_REG(Default Value: 0x0000_0000)

Offset: 0x060			**Register Name: LCD_CPU_IF_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	CPU_MODE 0000: 18bit/256K mode 0010: 16bit mode0 0100: 16bit mode1

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			0110: 16bit mode2 1000: 16bit mode3 1010: 9bit mode 1100: 8bit 256K mode 1110: 8bit 65K mode xxx1: 24bit for DSI
27	/	/	/
26	R/W	0x0	DA pin A1 value in 8080 mode auto/flash states
25	R/W	0x0	CA pin A1 value in 8080 mode WR/RD execute
24	/	/	/
23	R	0x0	WR_FLAG 0:write operation is finishing 1:write operation is pending
22	R	0x0	RD_FLAG 0:read operation is finishing 1:read operation is pending
21:18	/	/	/
17	R/W	0x0	AUTO auto Transfer Mode: If it's 1, all the valid data during this frame are write to panel. This bit is sampled by Vsync
16	R/W	0x0	FLUSH direct transfer mode: If it's enabled, FIFO1 is regardless of the HV timing, pixels data keep being transferred unless the input FIFO was empty. Data output rate control by DCLK.
15:4	/	/	/
3	R/W	0x0	TRIGGER_FIFO_BIST_EN 0: disable 1: enable Entry addr is 0xFF8
2	R/W	0x0	TRIGGER_FIFO_EN 0:disable 1:enable
1	R/W1S	0x0	TRIGGER_START write '1' to start a frame flush, write'0' has no effect. This flag indicated frame flush is running. Sofeware must make sure write '1' only when this flag is '0'.
0	R/W	0x0	TRIGGER_EN 0: trigger mode disable 1: trigger mode enable

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6.3.5.16. LCD_CPU_WR_REG(Default Value: 0x0000_0000)

Offset: 0x064			Register Name: LCD_CPU_WR_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	W	0x0	DATA_WR data write on 8080 bus, launch a write operation on 8080 bus

6.3.5.17. LCD_CPU_RD0_REG(Default Value: 0x0000_0000)

Offset: 0x068			Register Name: LCD_CPU_RD0_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R	0x0	DATA_RD0 data read on 8080 bus, launch a new read operation on 8080 bus

6.3.5.18. LCD_CPU_RD1_REG(Default Value: 0x0000_0000)

Offset: 0x06C			Register Name: LCD_CPU_RD1_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R	0x0	DATA_RD1 data read on 8080 bus, without a new read operation on 8080 bus

6.3.5.19. LCD_IO_POL_REG(Default Value: 0x0000_0000)

Offset: 0x088			Register Name: LCD_IO_POL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	IO_OUTPUT_SEL 0: normal output 1: register output when set as '1', d[23:0], io0, io1,io3 sync to dclk
30:28	R/W	0x0	DCLK_SEL 000: used DCLK0(normal phase offset) 001: used DCLK1(1/3 phase offset) 010: used DCLK2(2/3 phase offset) 101: DCLK0/2 phase 0 100: DCLK0/2 phase 90 reserved
27	R/W	0x0	IO3_INV 0: not invert 1: invert

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26	R/W	0x0	IO2_ INV 0: not invert 1: invert
25	R/W	0x0	IO1_INV 0: not invert 1: invert
24	R/W	0x0	IO0_INV 0: not invert 1: invert
23:0	R/W	0x0	DATA_INV LCD output port D[23:0] polarity control, with independent bit control: 0s: normal polarity 1s: invert the specify output

6.3.5.20. LCD_IO_TRI_REG(Default Value: 0x0FFF_FFFF)

Offset: 0x08C			**Register Name: LCD_IO_TRI_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	RGB_ENDIAN 0: normal 1: bits_invert
27	R/W	0x1	IO3_OUTPUT_TRI_EN 1: disable 0: enable
26	R/W	0x1	IO2_OUTPUT_TRI_EN 1: disable 0: enable
25	R/W	0x1	IO1_OUTPUT_TRI_EN 1: disable 0: enable
24	R/W	0x1	IO0_OUTPUT_TRI_EN 1: disable 0: enable
23:0	R/W	0xFFFFFF	DATA_OUTPUT_TRI_EN LCD output port D[23:0] output enable, with independent bit control: 1s: disable 0s: enable

6.3.5.21. LCD_DEBUG_REG(Default Value: 0x0000_0000)

Offset: 0x0FC			**Register Name: LCD_DEBUG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**

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31	R/W	0x0	LCD_FIFO_UNDER_FLOW
30	/	/	/
29	R	0x0	LCD_FIELD_POLARITY 0: second field 1: first field
28	/	/	/
27:16	R	0x0	LCD_CURRENT_LINE
15:0	/	/	/

6.3.5.22. LCD_CEU_CTL_REG(Default Value: 0x0000_0000)

Offset: 0x100			Register Name: LCD_CEU_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CEU_EN 0: bypass 1: enable
30:0	/	/	/

6.3.5.23. LCD_CEU_COEF_MUL_REG(Default Value: 0x0000_0000)

Offset: 0x110+N*0x04(N=0,1,2,4,5,6,8,9,10)			Register Name: LCD_CEU_COEF_MUL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	CEU_COEF_MUL_VALUE signed 13bit value, range of (-16,16) N=0: Rr N=1: Rg N=2: Rb N=4: Gr N=5: Gg N=6: Gb N=8: Br N=9: Bg N=10: Bb

6.3.5.24. LCD_CEU_COEF_ADD_REG(Default Value: 0x0000_0000)

Offset: 0x11C+N*0x10(N=0,1,2)			Register Name: LCD_CEU_COEF_ADD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18:0	R/W	0x0	CEU_COEF_ADD_VALUE signed 19bit value, range of (-16384, 16384)

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			N=0: Rc N=1: Gc N=2: Bc

6.3.5.25. LCD_CEU_COEF_RANG_REG(Default Value: 0x0000_0000)

Offset: 0x140+N*0x04(N=0,1,2)			Register Name: LCD_CEU_COEF_RANG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	CEU_COEF_RANGE_MIN unsigned 8bit value, range of [0,255]
15:8	/	/	/
7:0	R/W	0x0	CEU_COEF_RANGE_MAX unsigned 8bit value, range of [0,255]

6.3.5.26. LCD_CPU_TRI0_REG(Default Value: 0x0000_0000)

Offset: 0x160			Register Name: LCD_CPU_TRI0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	BLOCK_SPACE should be set >20*pixel_cycle
15:12	/	/	/
11:0	R/W	0x0	BLOCK_SIZE

6.3.5.27. LCD_CPU_TRI1_REG(Default Value: 0x0000_0000)

Offset: 0x164			Register Name: LCD_CPU_TRI1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R	0x0	BLOCK_CURRENT_NUM
15:0	R/W	0x0	BLOCK_NUM

6.3.5.28. LCD_CPU_TRI2_REG(Default Value: 0x0000_0000)

Offset: 0x168			Register Name: LCD_CPU_TRI2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x20	START_DELAY Tdly = (Start_Delay +1) * be_clk*8
15	R/W	0x0	TRANS_START_MODE 0: ecc_fifo+tri_fifo 1: tri_fifo

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14:13	R/W	0x0	SYNC_MODE 0x: auto 10: 0 11: 1
12:0	R/W	0x0	TRANS_START_SET Usual set as the length of a line

6.3.5.29. LCD_CPU_TRI3_REG(Default Value: 0x0000_0000)

Offset: 0x16C			Register Name: LCD_CPU_TRI3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R/W	0x0	TRI_INT_MODE 00: disable 01: counter mode 10: te rising mode 11: te falling mode when set as 01, Tri_Counter_Int occur in cycle of (Count_N+1)×(Count_M+1)×4 dclk. when set as 10 or 11, io0 is map as TE input.
27:24	/	/	/
23:8	R/W	0x0	COUNTER_N
7:0	R/W	0x0	COUNTER_M

6.3.5.30. LCD_CPU_TRI4_REG(Default Value: 0x0000_0000)

Offset: 0x170			Register Name: LCD_CPU_TRI4_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	PLUG_MODE_EN 0: disable 1:enable
27:25	/	/	/
24	R/W	0x0	A1 Valid in first Block
23:0	R/W	0x0	D23-D0 Valid in first Block

6.3.5.31. LCD_CPU_TRI5_REG(Default Value: 0x0000_0000)

Offset: 0x174			Register Name: LCD_CPU_TRI5_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:25	/	/	/
24	R/W	0x0	A1 Valid in Block except first
23:0	R/W	0x0	D23-D0 Valid in Block except first

6.3.5.32. LCD_CMAP_CTL_REG(Default Value: 0x0000_0000)

Offset: 0x180			Register Name: LCD_CMAP_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	COLOR_MAP_EN 0: bypass 1: enable This module only work when X is divided by 4
30:1	/	/	/
0	R/W	0x0	OUT_FORMAT 0: 4 pixel output mode: Out0 -> Out1 -> Out2 -> Out3 1: 2 pixel output mode: Out0 -> Out1

6.3.5.33. LCD_CMAP_ODD0_REG(Default Value: 0x0000_0000)

Offset: 0x190			Register Name: LCD_CMAP_ODD0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_ODD1
15:0	R/W	0x0	OUT_ODD0 bit15-12: Reservd bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0x0: in_b0 0x1: in_g0 0x2: in_r0 0x3: reservd 0x4: in_b1 0x5: in_g1 0x6: in_r1 0x7: reservd 0x8: in_b2 0x9: in_g2 0xa: in_r2 0xb: reservd 0xc: in_b3 0xd: in_g3

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			0xe: in_r3 0xf: reservd

6.3.5.34. LCD_CMAP_ODD1_REG(Default Value: 0x0000_0000)

Offset: 0x194			Register Name: LCD_CMAP_ODD1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_ODD3
15:0	R/W	0x0	OUT_ODD2

6.3.5.35. LCD_CMAP_EVEN0_REG(Default Value: 0x0000_0000)

Offset: 0x198			Register Name: LCD_CMAP_EVEN0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_EVEN1
15:0	R/W	0x0	OUT_EVEN0

6.3.5.36. LCD_CMAP_EVEN1_REG(Default Value: 0x0000_0000)

Offset: 0x19C			Register Name: LCD_CMAP_ EVEN1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_EVEN3
15:0	R/W	0x0	OUT_EVEN2

6.3.5.37. LCD_SAFE_PERIOD_REG(Default Value: 0x0000_0000)

Offset: 0x1F0			Register Name: LCD_SAFE_PERIOD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	SAFE_PERIOD_FIFO_NUM
15:4	R/W	0x0	SAFE_PERIOD_LINE
3	/	/	/
2:0	R/W	0x0	SAFE_PERIOD_MODE 000: unsafe 001: safe 010: safe at ecc_fifo_curr_num > safe_period_fifo_num 011: safe at 2 and safe at sync active 100: safe at line

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6.4. TV Encoder

6.4.1. Overview

- System resources are controlled by ATE
- Supports CCIR656 and Serial YUV interface
- 1 CVBS out, Support NTSC and PAL
- Plug status auto detecting

6.4.2. Block Diagram

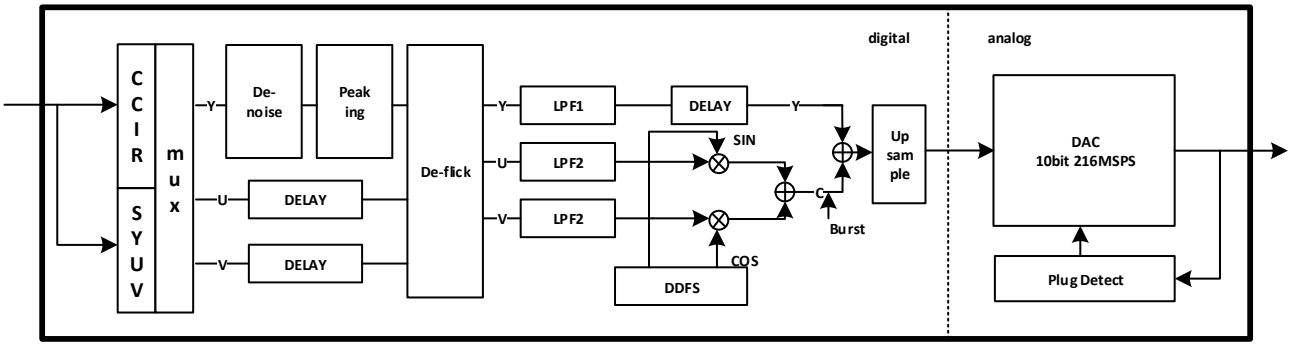


Figure 6-9. TV Encoder Block Diagram

6.4.3. Operations and Functional Descriptions

6.4.3.1. Typical Performance

Table 6-6. TV Encoder Typical Performance

No.	Test Item	Test Signal	Test Condition	Index Requirement	Unit	Typ
1	Video output level	Cbar75（75% color bar）or CCITT033.ts L35 Matrx625.mpg，L28	Peak-to-peak (p-p)	1000±30	mV	1000
			Luminance level	700±20	mV	700
			Horizontal synchronization level	300±10	mV	300
			Color synchronization level	300±10	mV	300

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2	Luminance non-linear	CCIR 17 or CCITT033.TS，L35 or Matrx625.Trp，L36 Matrx625.mpg，L28	1st order	100≤±4	%	100
			2nd order	100≤±4	%	97.6
			3rd order	100≤±4	%	99.8
			4th order	100≤±4	%	99.0
			5th order	100≤±4	%	98.7
3	Luminance gain		Δτ	100≤±5	%	102.0
4	Bright delay		Δ t	≤30	nS	3.0
5	K coefficient		K-2T	≤3	%	0.5
			K-PB	≤3	%	0.2
6	Short time distortion		The proportion of Upper/Lower punches	20	%	8.0
			Up/Down time	300	nS	197.5
7	Chroma noise ratio AM/PM	CCITT033.TS，L25 or Matrx625.Trp，L178	AM	≥50	dB	70
			PM	≥50	dB	60
8	Differential Gain(DG)	Modulated five-step wave or CCITT033 L612 Matrx625.mpg，L58	dG	≤±3	%	0.80
9	Differential Phase(DP)		dP	≤±3°	0	0.80
10	SNR(S/N)	CCITT033，L44 Matrx625.mpg，L 229	Non-weighting	≥52	dB	56
			Weighting	≥56	dB	60
11	Chroma non-linear	CCIR 331 or Matrx625.Trp，L84	Color gain error	≤±3	%	2.0
			Color phase error	≤±3°	0	0.0
			Color and Luminance intermodulation	≤±5	%	0.0
12	Amplitude-frequency characteristics	CCIR 18 or Matrx625.Trp，L105 Matrx625.mpg，L105	0.5MHz	≤±0.5	dB	0.10
			1.0MHz	≤±0.5	dB	0.10
			2.0MHz	≤±0.5	dB	0.15
			4.0MHz	≤±0.5	dB	0.15
			4.8MHz	≤±1	dB	0.20
			5.8MHz	-3～0.5	dB	0.20
13	Line synchronizationfront-end dither	Arbitrarily video signal	Jitter	≤20nSp-p	nS	3
14	Line Phase of subcarrier		SCH Phase	≤±10	0	0.5

6.4.3.2. CCIR656 Interface

CCIR656 support 8 bits format. The video timing reference codes are as follows.

Table 6-7. CCIR656 Interface

Data bit number	First word(FF)	Second word(00)	Third word(00)	Forth word(XY)

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7(MSB)	1	0	0	1
6	1	0	0	F
5	1	0	0	V
4	1	0	0	H
3	1	0	0	P3
2	1	0	0	P2
1	1	0	0	P1
0(LSB)	1	0	0	P0

F = 0 during filed 1; = 1 during filed 2

V = 0 elsewhere; = 1 during filed blanking

H = 0 in SAV; = 1 in EAV

P0, P1, P2, P3: protection bits

TV Encoder required Parallel YUV data with DE signal and RESYNC signal. There is 2 modes to generate DE signal and RESYNC signal.

6.4.3.3. Serial YUV Interface

Internal H and V are generated the same as CCIR656 SYNC mode. YUV serial data format is as follows.

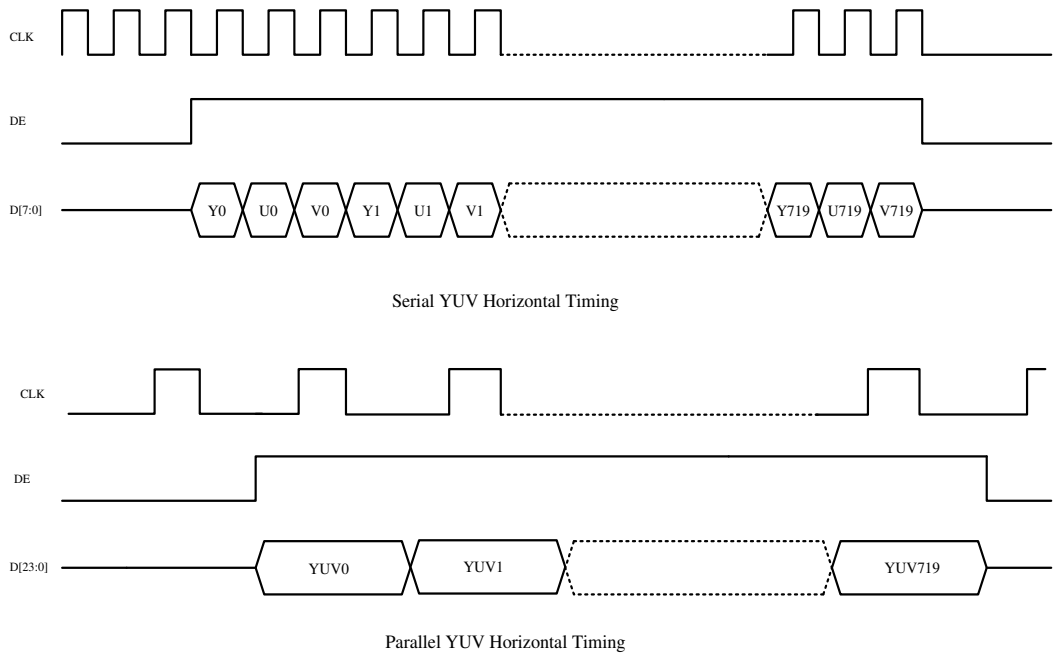
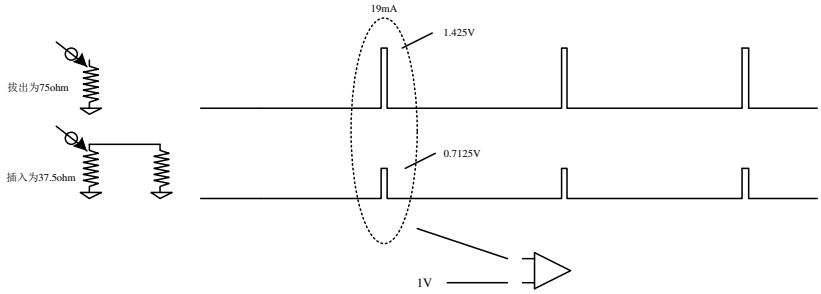


Figure 6-10. Serial YUV Interface

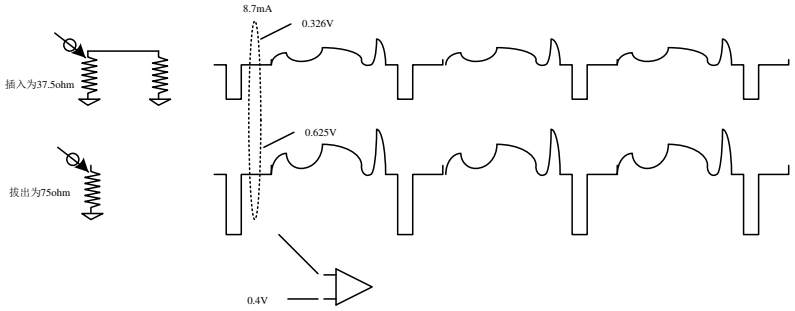
6.4.3.4. Plug Detect

DAC plug status detect block diagram is below.

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Plug detect at no CVBS output



Plug detect at CVBS output

Figure 6-11. DAC Plug Detect Block Diagram

6.4.4. Register List

Module Name	Base Address
ATE_TV Encoder	0x4000

Register Name	Offset	Description
TVE_CTL0	0x0000	TV Encoder Control 0 Register
TVE_CTL1	0x0002	TV Encoder Control 1 Register
TVE_MOD0	0x0004	TV Encoder Mode 0 Register
TVE_MOD1	0x0006	TV Encoder Mode 1 Register
TVE_DAC_CFG0	0x0008	TV Encoder DAC Configuration 0 Register
TVE_DAC_CFG1	0x000A	TV Encoder DAC Configuration 1 Register
TVE_YC_DELAY	0x000C	TV Encoder YC Delay Register
TVE_YC_FILTER	0x000E	TV Encoder YC Filter Register
TVE_BURST_FRQ0	0x0010	TV Encoder Burst Frequency 0 Register
TVE_BURST_FRQ1	0x0012	TV Encoder Burst Frequency 1 Register
TVE_FRONT_PORCH	0x0014	TV Encoder Front Porch Register
TVE_BACK_PORCH	0x0016	TV Encoder Back Porch Register
TVE_TOTAL_LINE	0x001C	TV Encoder Total Line Number Register
TVE_FIRST_ACTIVE	0x001E	TV Encoder First Active Line Register
TVE_BLACK_LEVEL	0x0020	TV Encoder Black Level Register

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TVE_BLANK_LEVEL	0x0022	TV Encoder Blank Level Register
TVE_PLUG_EN	0x0030	TV Encoder Plug Detect Enable Register
TVE_PLUG_IRQ_EN	0x0030	TV Encoder Plug Detect Interrupt Enable Register
TVE_PLUG_IRQ_STA	0x0034	TV Encoder Plug Detect Interrupt Status Register
TVE_PLUG_STA	0x0038	TV Encoder Plug Detect Status Register
TVE_PLUG_DEBOUNCE	0x0040	TV Encoder Plug Detect De-Bounce Register
TVE_PLUG_PULSE_LEVEL	0x00F4	TV Encoder Plug Detect Pulse Level Register
TVE_PLUG_PULSE_START	0x00F8	TV Encoder Plug Detect Pulse Start Register
TVE_PLUG_PULSE_PERIOD	0x00FA	TV Encoder Auto Detect Pulse Period Register
TVE_IF_CTL	0x1000	TV Encoder Interface Control Register
TVE_IF_TIM0	0x1008	TV Encoder Interface Timing 0 Register
TVE_IF_TIM1	0x100A	TV Encoder Interface Timing 1 Register
TVE_IF_TIM2	0x100C	TV Encoder Interface Timing 2 Register
TVE_IF_TIM3	0x100E	TV Encoder Interface Timing 3 Register
TVE_IF_SYNC0	0x1010	TV Encoder Interface SYNC 0 Register
TVE_IF_SYNC1	0x1012	TV Encoder Interface SYNC 1 Register
TVE_IF_SYNC2	0x1014	TV Encoder Interface SYNC 2 Register
TVE_IF_TIM4	0x1016	TV Encoder Interface Timing 4 Register
TVE_IF_STATUS	0x1018	TV Encoder Interface Status Register

6.4.5. Register Description

6.4.5.1. TV Encoder Control 0 Register(Default Value:0x0000)

Offset: 0x0000			**Register Name: TVE_CTL0**
Bit	**Read/Write**	**Default/Hex**	**Description**
15:14	/	/	/
13:10	R/W	0x0	Reserved
9	R/W	0x0	Reserved
8	R/W	0x0	Reserved
7:1	/	/	/
0	R/W	0x0	EN TV Encoder enable, default disable, write 1 to take it out of the reset state

6.4.5.2. TV Encoder Control 1 Register(Default Value:0x0000)

Offset: 0x0002			**Register Name: TVE_CTL1**
Bit	**Read/Write**	**Default/Hex**	**Description**
15	R/W	0x0	CLK_DISABLE TV Encoder clock gate disable 1: disable

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			0: enable
14:0	/	/	/

6.4.5.3. TV Encoder Mode 0 Register(Default Value:0x0000)

Offset: 0x0004			Register Name: TVE_MOD0
Bit	**Read/Write**	**Default/Hex**	**Description**
15:10	/	/	/
9	R/W	0x0	COLOR_BAR_TYPE Color Bar Type 0: NTSC: 75/7.5/75/7.5 PAL: 100/0/75/0 1: NTSC: 100/7.5/100/7.5 PAL: 100/0/100/0
8	R/W	0x0	COLOR_BAR_MOD Color Bar Mode Standard Color bar input selection This bit selects whether the Video Encoder video data input is replaced by an internal standard color bar generator or not. 0: The Video Encoder input is coming from the Display Engineer 1: The Video Encoder input is coming from an internal standard color bar generator.
7:1	/	/	/
0	R/W	0x0	TV_MOD TV Mode Select 0: NTSC 1: PAL Changing this register value will cause some relative register setting to relative value.

6.4.5.4. TV Encoder Mode 1 Register(Default Value:0x0000)

Offset: 0x0006			Register Name: TVE_MOD1
Bit	**Read/Write**	**Default/Hex**	**Description**
15:13	/	/	/
12	R/W	0x0	DAC_TEST_MOD 0: TV mode, DAC using tvclk 1: DAC test mode， DAC using AHB clock
11:5	/	/	/
4	R/W	0x0	C_SEQ Cb/Cr sequence for 422 mode

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			0: Cb first 1: Cr first
3	R/W	0x0	C_MODE Chroma Mode 0: 444 1: 422
2:0	/	/	/

6.4.5.5. TV Encoder DAC Configuration 0 Register(Default Value:0x12A0)

Offset: 0x0008			Register Name: TVE_DAC_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
15:1	/	/	Reserved
0	R/W	0x0	DAC_EN DAC Enable 0:disable 1:enable

6.4.5.6. TV Encoder DAC Configuration 1 Register(Default Value:0x4300)

Offset: 0x000A			Register Name: TVE_DAC_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	/	/	Reserved

6.4.5.7. TV Encoder YC Delay Register(Default Value:0x0004)

Offset: 0x000C			Register Name: TVE_YC_DELAY
Bit	**Read/Write**	**Default/Hex**	**Description**
15	/	/	/
14:12	R/W	0x0	Y_DELAY
11	/	/	/
10:8	R/W	0x0	C_DELAY
7:3	/	/	/
2:0	R/W	/	Reserved

6.4.5.8. TV Encoder YC Filter Register(Default Value:0x0003)

Offset: 0x000E			Register Name: TVE_YC_FILTER
Bit	**Read/Write**	**Default/Hex**	**Description**
15	R/W	0x0	Luma filter lti enable

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			0:disable Luma filter lti 1:enable Luma filter lti
14	/	/	/
13:12	R/W	0x0	upsample for dac Out up sample 0:27M 1:54M 2:108M 3:216M
11	/	/	/
10	R/W	0x0	Filters_Select 0: enable new peaking filter 1: enable new reduction filter
9:8	R/W	0x0	New luminance peaking filter selection
7:5	/	/	/
4	R/W	0x0	C_FIELD1_BP Chroma Filter Stage 1 0 : Chroma Filter stage 1 Enable 1: Chroma Filter stage 1 bypass
3	R/W	0x0	C_FIELD2_BP Chroma Filter Stage 2 Bypass 0 : Chroma Filter stage 2 Enable 1: Chroma Filter stage 2 bypass
2	R/W	0x0	C_FILTER3_BP Chroma Filter Stage 3 Bypass 0 : Chroma Filter stage 3 Enable 1: Chroma Filter stage 3 bypass
1	R/W	0x1	Y_FIELD_BP Luma Filter Bypass 0: Luma Filter enable 1: Luma Filter bypass
0	R/W	0x1	NOTCH_EN Notch Enable Luma notch filter on/off selection This bit selects if the luma notch filter is operating or bypassed. 0: The luma notch filter is bypassed 1: The luma notch filter is operating

6.4.5.9. TV Encoder Burst Frequency 0 Register(Default Value:0x7C1F)

Offset: 0x0010			**Register Name: TVE_BURST_FRQ0**
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x7c1f	BURST_FRQ_15_0 Specify the ratio between the color burst frequency. 32 bit unsigned

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			fraction. Default value is h21f07c1f, which is compatible with NTSC specs. 3.5795455MHz (X'21F07C1F'): NTSC-M, NTSC-J 4.43361875 MHz(X'2A098ACB'): PAL-B, D, G, H,I, N 3.582056 MHz (X'21F69446'):PAL-N(Argentina) 3.579611 MHz (X'21E6EFE3'): PAL-M

6.4.5.10. TV Encoder Burst Frequency 0 Register(Default Value:0x7C1F)

Offset: 0x0010			Register Name: TVE_BURST_FRQ0
Bit	**Read/Write**	**Default/Hex**	**Description**
15	R/W	0x7c1f	BURST_FRQ_15_0 Specify the ratio between the color burst frequency. 32 bit unsigned fraction. Default value is h21f07c1f, which is compatible with NTSC specs. 3.5795455MHz (X'21F07C1F'): NTSC-M, NTSC-J 4.43361875 MHz(X'2A098ACB'): PAL-B, D, G, H,I, N 3.582056 MHz (X'21F69446'):PAL-N(Argentina) 3.579611 MHz (X'21E6EFE3'): PAL-M

6.4.5.11. TV Encoder Burst Frequency 1 Register(Default Value:0x21F0)

Offset: 0x0012			Register Name: TVE_BURST_FRQ1
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x21F0	BURST_FRQ_31_16 Specify the ratio between the color burst frequency. 32 bit unsigned fraction. Default value is h21f07c1f, which is compatible with NTSC specs. 3.5795455MHz (X'21F07C1F'): NTSC-M, NTSC-J 4.43361875 MHz(X'2A098ACB'): PAL-B, D, G, H,I, N 3.582056 MHz (X'21F69446'):PAL-N(Argentina) 3.579611 MHz (X'21E6EFE3'): PAL-M

6.4.5.12. TV Encoder Front Porch Register(Default Value:0x0020)

Offset: 0x0014			Register Name: TVE_FRONT_PORCH
Bit	**Read/Write**	**Default/Hex**	**Description**
15:12	/	/	/
11:0	R/W	0x20	FRONT_PORCH Front Porch must be even specify the width of the front porch in encoder clock cycles. 6 bit unsigned even integer. Allowed range is 10 to 62. Default value is 32.

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6.4.5.13. TV Encoder Back Porch Register(Default Value:0x0076)

Offset: 0x0016			Register Name: TVE_BACK_PORCH
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:0	R/W	0x76	BACK_PORCH Back Porch Specify the width of the back porch in encoder clock cycles. Min value is (burst_width+breeze_way+17). 8 bit unsigned integer. Default value is 118

6.4.5.14. TV Encoder Total Line Number Register(Default Value:0x020D)

Offset: 0x001C			Register Name: TVE_TOTAL_LINE
Bit	**Read/Write**	**Default/Hex**	**Description**
15:11	/	/	/
10:0	R/W	0x20D	NUM_LINES Number Lines Specify the total number of lines in a video frame. 11 bit unsigned integer. Allowed range is 0 to 2048. Default value is 525. For interlaced video: When NTSC, and FirstVideoLine is greater than 20, then NumLines is restricted to be greater than 2*(FirstVideoLine+18). When NTSC, and FirstVideoLine is not greater than 20, then NumLines is restricted to be greater than 77. When PAL, and FirstVideoLine is greater than 22, then NumLines is restricted to be greater than 2*(FirstVideoLine+18). When PAL, and FirstVideoLine is not greater than 22, then NumLines is restricted to be greater than 81. If NumLines is even, then it is restricted to be divisible by 4. If NumLines is odd, then it is restricted to be divisible by 4 with a remainder of 1.

6.4.5.15. TV Encoder First Active Line Register(Default Value:0x0016)

Offset: 0x001E			Register Name: TVE_FIRST_ACTIVE
Bit	**Read/Write**	**Default/Hex**	**Description**
15:8	/	/	/
7:0	R/W	0x16	FIRST_VIDEO_LINE First Video Line Specify the index of the first line in a field/frame to have active video. 8 bit unsigned integer. For interlaced video: When VSync5=B‘0’, FirstVideoLine is restricted to be greater than 7. When VSync5=B‘1’, FirstVideoLine is restricted to be greater than 9. Default value is 21.

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6.4.5.16. TV Encoder Black Level Register(Default Value:0x011A)

Offset: 0x0020			Register Name: TVE_BLACK_LEVEL
Bit	**Read/Write**	**Default/Hex**	**Description**
15:10	/	/	/
9:0	R/W	0x11a	BLACK_LEVEL Black Level Specify the black level setting. 10 bit unsigned integer. Allowed range is 240 to 1023. Default value is 282

6.4.5.17. TV Encoder Blank Level Register(Default Value:0x00F0)

Offset: 0x0022			Register Name: TVE_BLANK_LEVEL
Bit	**Read/Write**	**Default/Hex**	**Description**
15:10	/	/	/
9:0	R/W	0x0f0	BLANK_LEVEL Blank Level Specify the blank level setting for active lines. 10 bit unsigned integer. Allowed range 0 to 1023. Default value is hexF0(dec240).

6.4.5.18. TV Encoder Plug Detect Enable Register(Default Value:0x0000)

Offset: 0x0030			Register Name: TVE_PLUG_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
15:1	/	/	/
0	R/W	0x0	AUTO_DET_EN Auto Detection Enable

6.4.5.19. TV Encoder Plug Detect Interrupt Enable Register(Default Value:0x0000)

Offset: 0x0032			Register Name: TVE_PLUG_IRQ_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
15:1	/	/	/
0	R/W	0x0	AUTO_DET_IRQ_EN Auto Detection Interrupt Enable

6.4.5.20. TV Encoder Plug Detect Interrupt Status Register(Default Value:0x0000)

Offset: 0x0034			Register Name: TVE_PLUG_IRQ_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
15:1	/	/	/

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0	R/W	0x0	AUTO_DET_IRQ_STA Auto detection interrupt active flag, write 1 to inactive DAC0 auto detection interrupt.

6.4.5.21. TV Encoder Plug Detect Status Register(Default Value:0x0000)

Offset: 0x0038			Register Name: TVE_PLUG_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
15:1	/	/	/
0	R/W	0x0	AUTO_DET_STA DAC Status 00: Unconnected 01: Connected 11: Short to ground 10: Reserved

6.4.5.22. TV Encoder Plug Detect Debounce Register(Default Value:0x0000)

Offset: 0x0040			Register Name: TVE_PLUG_DEBOUNCE
Bit	**Read/Write**	**Default/Hex**	**Description**
15:4	/	/	/
3:0	R/W	0x0	DAC_DE_BNC DAC debounce times

6.4.5.23. TV Encoder Plug Detect Pulse Level Register(Default Value:0x0000)

Offset: 0x00F4			Register Name: TVE_PLUG_PULSE_LEVEL
Bit	**Read/Write**	**Default/Hex**	**Description**
15:10	/	/	/
9:0	R/W	0x0	DETECT_PULSE_LEVEL Use for DAC data input at auto detect pluse

6.4.5.24. TV Encoder Plug Detect Pulse Start Register(Default Value:0x0000)

Offset: 0x00F8			Register Name: TVE_PLUG_PULSE_START
Bit	**Read/Write**	**Default/Hex**	**Description**
15	/	/	/
14:0	R/W	0x0	DETECT_PULSE_START

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6.4.5.25. TV Encoder Auto Detect Pulse Period Register(Default Value:0x0000)

Offset: 0x00FA			Register Name: TVE_PLUG_PULSE_PERIOD
Bit	**Read/Write**	**Default/Hex**	**Description**
15	/	/	/
14:0	R/W	0x0	DETECT_PULSE_PERIOD Use 32K clock

6.4.5.26. TV Encoder Interface Control Register(Default Value:0x0000)

Offset: 0x1000			Register Name: TVE_IF_CTL0
Bit	**Read/Write**	**Default/Hex**	**Description**
15:13	/	/	/
12	R/W	0x0	PROGRESSIVE_MODE 0: interlaced 1: progressive
11:10	/	/	/
9:8	R/W	0x0	SYUV_INPUT_FORMAT 000: YUV 001: YVU 010: UYV 011: UVY 100: VYU 101: VUY Others: reserved
6	/	/	/
5:4	R/W	0x0	CCIR656_INPUT_FORMAT 00: YUYV 01: YVYU 10: UYVY 11: VYUY
3:2	/	/	/
1:0	R/W	0x0	INTERFACE_SEL 0 : CCIR656 input interface 1 : Serial YUV input interface

6.4.5.27. TV Encoder Interface Timing 0 Register(Default Value:0x0000)

Offset: 0x1008			Register Name: TVE_IF_TIM0
Bit	**Read/Write**	**Default/Hex**	**Description**
15:9	/	/	/
8:0	R/W	0x0	HBP horizontal back porch

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			T_{hbp} = HBP×T_{clk}

6.4.5.28. TV Encoder Interface Timing 1 Register(Default Value:0x0000)

Offset: 0x100A			Register Name: TVE_IF_TIM1
Bit	**Read/Write**	**Default/Hex**	**Description**
15:12	/	/	/
11:0	R/W	0x0	HACT Horizontal active cycle T_{hact} = H_HACT×T_{clk}

6.4.5.29. TV Encoder Interface Timing 2 Register(Default Value:0x0000)

Offset: 0x100C			Register Name: TVE_IF_TIM2
Bit	**Read/Write**	**Default/Hex**	**Description**
15:9	/	/	/
8:0	R/W	0x0	VBP_ODD Vertical back porch in line T_{hbp} = VBP×T_h

6.4.5.30. TV Encoder Interface Timing 3 Register(Default Value:0x0000)

Offset: 0x100E			Register Name: TVE_IF_TIM3
Bit	**Read/Write**	**Default/Hex**	**Description**
15:10	/	/	/
9:0	R/W	0x0	VACT Vertical active in line T_{hact} = VACT×T_h

6.4.5.31. TV Encoder Interface SYNC 0 Register(Default Value:0x0000)

Offset: 0x1010			Register Name: TVE_IF_SYNC0
Bit	**Read/Write**	**Default/Hex**	**Description**
15	R/W	0x0	INPUT_BYPASS_TO_DAC 0: normal 1: D[7:0] - DAC[7:0], HSYNC - DAC[8], VSYNC-DAC[9]
14:10	/	/	/
9	R/W	0x0	V_OUTPUT 0: VSYNC IO normal mode, as input 1: internal V signal output to VSYNC IO
8	R/W	0x0	H_OUTPUT

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			0: HSYNC IO normal mode, as input 1: internal H signal output to HSYNC IO
7	/	/	/
6	R/W	0x0	/
5	R/W	0x0	V_SEL 0 : internal V signal from sync CCIR reference codes 1 : internal V signal from sync IO generator Node that internal DE signal is generate from internal V and H signal
4	R/W	0x0	H_SEL 0 : internal H signal from sync CCIR reference codes 1 : internal H signal from sync IO generator that internal DE signal is generated from internal V and H signal
3	/	/	/
2	R/W	0x0	CLOCK_POLARITY 0: latch data from clock falling edge 1: latch data from clock rising edge
1	R/W	0x0	VSYNC_POLARITY 0: active 0 1: active 1
0	R/W	0x0	HSYNC_POLARITY 0: active 0 1: active 1

6.4.5.32. TV Encoder Interface SYNC 1 Register(Default Value:0x0000)

Offset: 0x1012			**Register Name: TVE_IF_SYNC1**
Bit	**Read/Write**	**Default/Hex**	**Description**
15:3	/	/	/
2:0	R/W	0x0	RESYNC_INTERVAL_TIME 000 : Disable 001 : once at start 010 : every 4 vsync 011 : every 8 vsync 100 : every 16 vsync Others : Disable

6.4.5.33. TV Encoder Interface SYNC 2 Register(Default Value:0x0000)

Offset: 0x1014			**Register Name: TVE_IF_SYNC2**
Bit	**Read/Write**	**Default/Hex**	**Description**
15:12	R/W	0x0	RESYNC_DELAY_LINE
11:0	R/W	0x0	RESYNC_DELAY_PIXLE Count by dclk

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6.4.5.34. TV Encoder Interface Timing 4 Register(Default Value:0x0000)

Offset: 0x1016			Register Name: TVE_IF_TIM4
Bit	**Read/Write**	**Default/Hex**	**Description**
15:9	/	/	/
8:0	R/W	0x0	VBP_EVEN Vertical back porch in line $T_{hbp} = VBP \times T_h$

6.4.5.35. TV Encoder Interface Status Register(Default Value:0x0000)

Offset: 0x1018			Register Name: TVE_IF_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
15	R	0x0	DE_STATUS Internal DE signal status
14	R	0x0	F_STATUS Internal F signal status
13	R	0x0	V_STATUS Internal V signal status
12	R	0x0	H_STATUS Internal H signal status
11	R	0x0	CCIR_P_ERROR If CCIR code P3-P0 is not equal to H V F XOR result, this bit is set'1', write '1' to clear this bit.
10	/	/	/
9:0	R	0x0	H_LINE_NUM Indecate total H signal cycle number in a Frame time.

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6.5. HDMI

6.5.1. Overview

Features:

- HDCP1.4/2.2 support
- DDC and SCDC support
- Integrated CEC hardware engine
- Video Support
  - 2D Video : 4K/1080P/1080I/720P/576P/480P/576I/480I, up to 4K@60fps
  - 3D Video : 4K/1080P/720P/576P/480P, up to 4K@30fps
  - Supports RGB/YUV444/YUV422/YUV420 output
  - Color depth: 8/10Bit
  - HDR10: compliant with CTA-861.3 and SMPTE ST 2048
- Audio Support
  - Uncompressed audio formats: IEC60958 L-PCM audio samples, up to 192kHz
  - Compressed audio formats: IEC61937 compressed audio, up to 1536kHz

6.5.2. Block Diagram

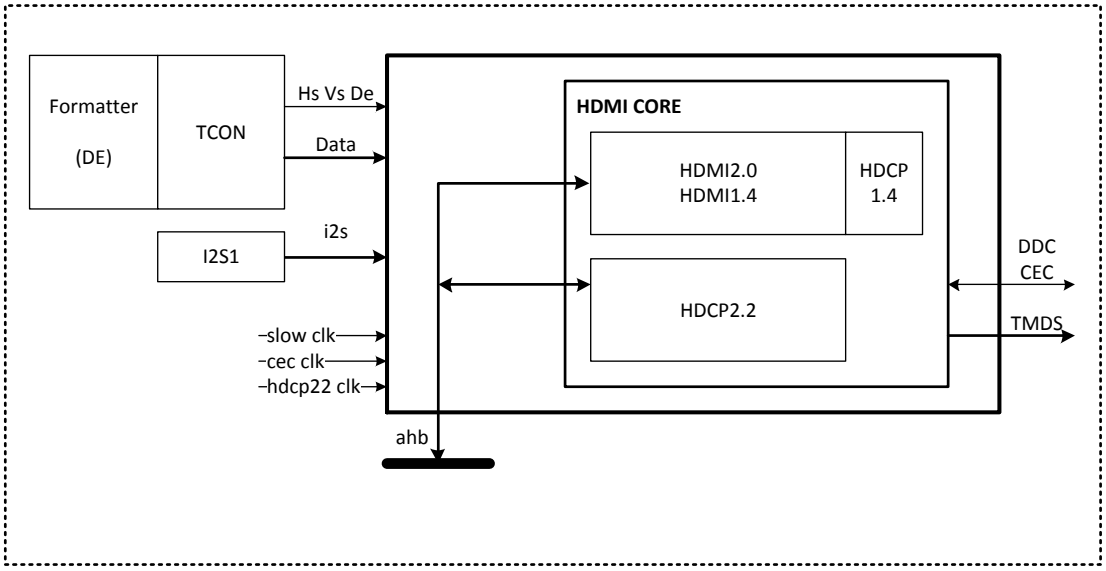


Figure 6-12. HDMI Block Diagram

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Chapter 7 Audio

This chapter describes the H6 V200 audio, including:

- Audio HUB
- I2S/PCM
- One Wire Audio(OWA)
- DMIC
- Audio Codec

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7.1. Audio HUB

7.1.1. Overview

The Audio HUB(AHUB) defines an audio subsystem to support various types of audio protocols and function modules. To provide a flexible audio streaming environment, it is essential to implement a versatile audio fabric to connect audio modules independently and simultaneously.

The Audio HUB is a crossbar switch matrix connecting various audio modules such as I2S/PCM, DAM(Digital Audio MIXER) etc. Audio HUB is attached to the APB bus and is programmable through the bus.

Features:

- Concurrent switching between audio clients
  - The audio client are I2S/PCM, DAM and APBIF.
  - A TX client can talk to multiple RX clients simultaneously.
  - A RX client can only talk to one TX clients.
- Scalable MxN crossbar switch, where
  - M is the number of TX clients
  - N is the number of RX clients
- Supports three 64*32bit TX streams FIFO and three 128*32bit RX streams FIFO for APB DMA operations.
- Supports two DAM, one I2S/PCM for Audio Codec and one I2S/PCM for HDMI.

7.1.2. Block Diagram

Figure 7-1 shows the block diagram of the Audio HUB. Audio HUB I2S/PCM1 connects to HDMI, Audio HUB I2S/PCM3 connects to Audio Codec, for the package of H6 V200 processor, the pins of Audio HUB I2S/PCM1 and I2S/PCM3 are not fetches out.

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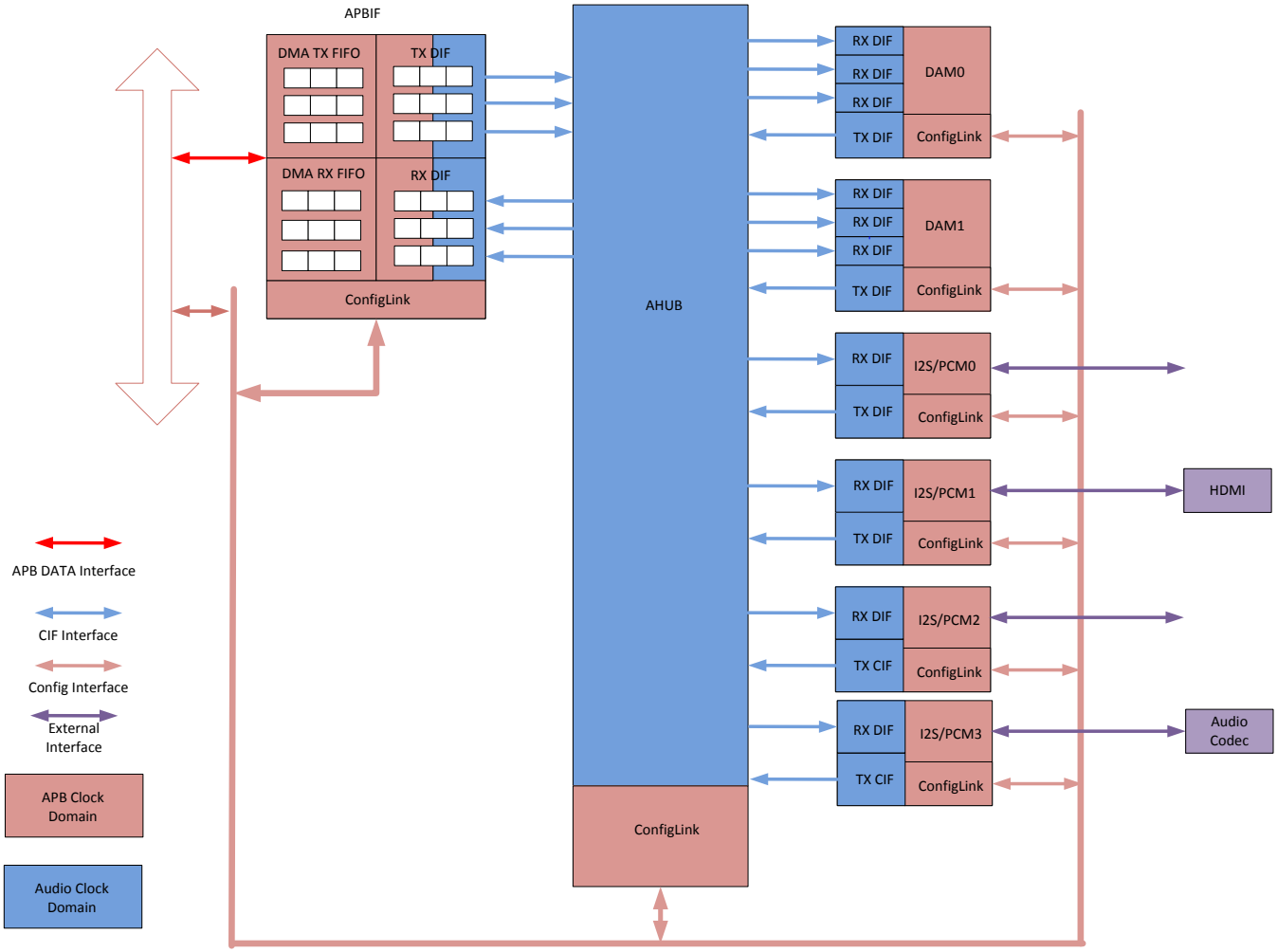


Figure 7-1. Audio HUB Block Diagram

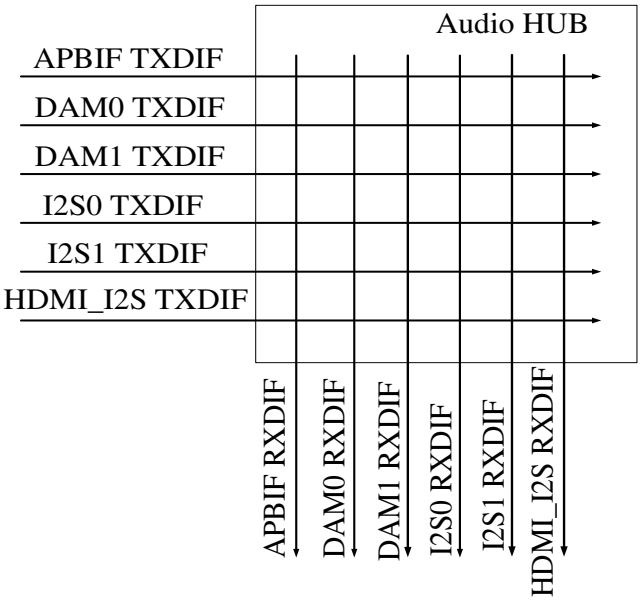


Figure 7-2. Audio HUB Crossbar Switch and Clients

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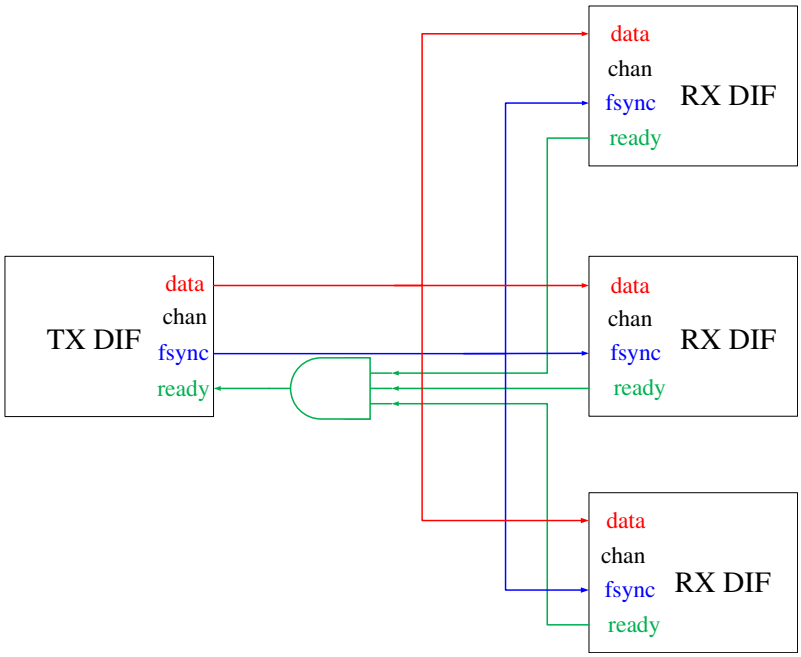


Figure 7-3. Signal Exchange between TX and RX Clients

An AHUB session has four signals to transmit audio data from a TX client to RX client. The fsync signal is asserted when a new frame starts. A frame consists of samples from multiple channels, the chan signal is asserted when a new channel starts. When a RX client asserts the ready signal, it should be ready to receive data.

7.1.3. Operations and Functional Descriptions

7.1.3.1. External Signals

The following table describes the external signals of Audio HUB.

Table 7-1. Audio HUB External Signals

Signal	Description	Type
H_PCM0_MCLK	Audio HUB I2S/PCM 0 Master Clock	O
H_PCM0_CLK	Audio HUB I2S/PCM 0 Sample Rate Serial Clock	I/O
H_PCM0_SYNC	Audio HUB I2S/PCM 0 Sample Rate Left and Right Channel Select Clock/Sync	I/O
H_PCM0_DIN	Audio HUB I2S/PCM 0 Serial Data Input	I
H_PCM0_CLK	Audio HUB I2S/PCM 0 Serial Data Output	O
H_PCM2_MCLK	Audio HUB I2S/PCM 2 Master Clock	O
H_PCM2_CLK	Audio HUB I2S/PCM 2 Sample Rate Serial Clock	I/O
H_PCM2_SYNC	Audio HUB I2S/PCM 2 Sample Rate Left and Right Channel Select Clock/Sync	I/O
H_PCM2_DIN	Audio HUB I2S/PCM 2 Serial Data Input	I
H_PCM2_CLK	Audio HUB I2S/PCM 2 Serial Data Output	O

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7.1.3.2. Clock Sources

Audio HUB System controller uses the APB CLK and AUDIO_PLL. The APB CLK is the system clock and the Audio PLL is the protocol clock. Table 7-2 describes the clock sources for Audio HUB system. Users can see Clock Controller Unit(CCU) for clock setting, configuration and gating information.

Table 7-2. Audio HUB Clock Sources

Clock Sources	Description
APB CLK	from the System CLK
AUDIO_PLL	24.576MHz or 22.5792MHz generated by AUDIO_PLL to produce 48kHz or 44.1kHz serial frequency.

7.1.3.3. I2S/PCM Transmit Format

The Audio HUB consists of four I2S/PCM, one I2S/PCM for HDMI ,one I2S/PCM for Audio Codec and two DAM(Digital Audio MIXER). The I2S/PCM supports standard I2S mode, Left-justified I2S mode, Right-justified I2S mode, PCM mode and TDM mode. Software can select one of them in which the I2S/PCM works by setting the I2S/PCM Control Register. From Figure 7-4 to Figure 7-8 describe the waveforms for LRCK(SYNC), BCLK(CLK) and SDO(DOUT), SDI(DIN).

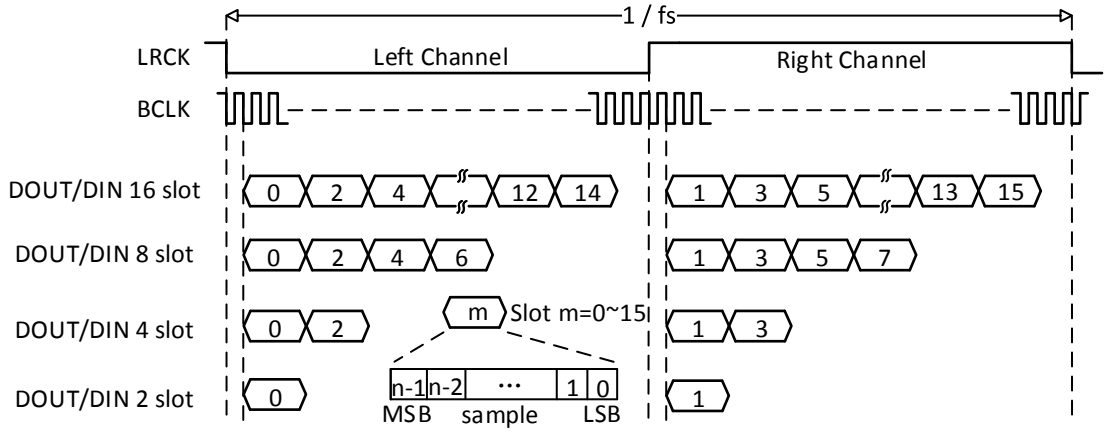
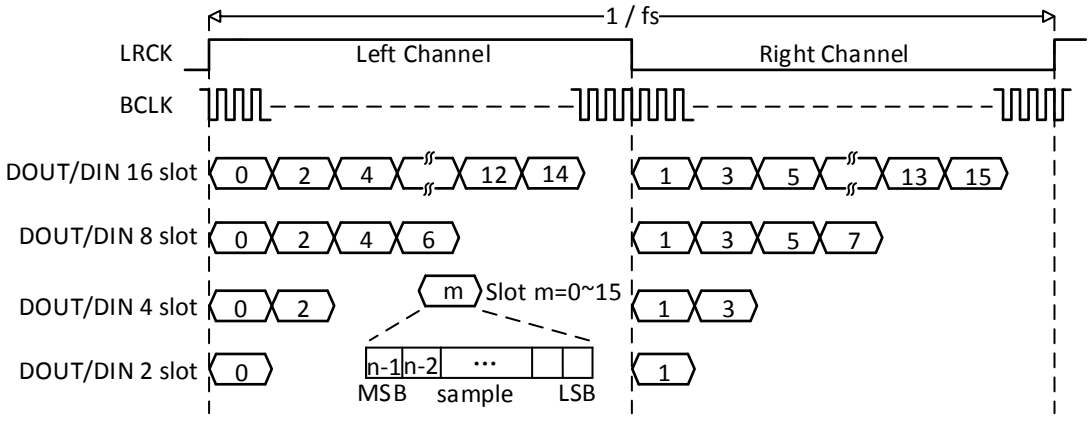


Figure 7-4. Timing Diagram for Standard I2S/TDM-I2S Mode



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Figure 7-5. Timing Diagram for Left-justified/TDM-Left Mode

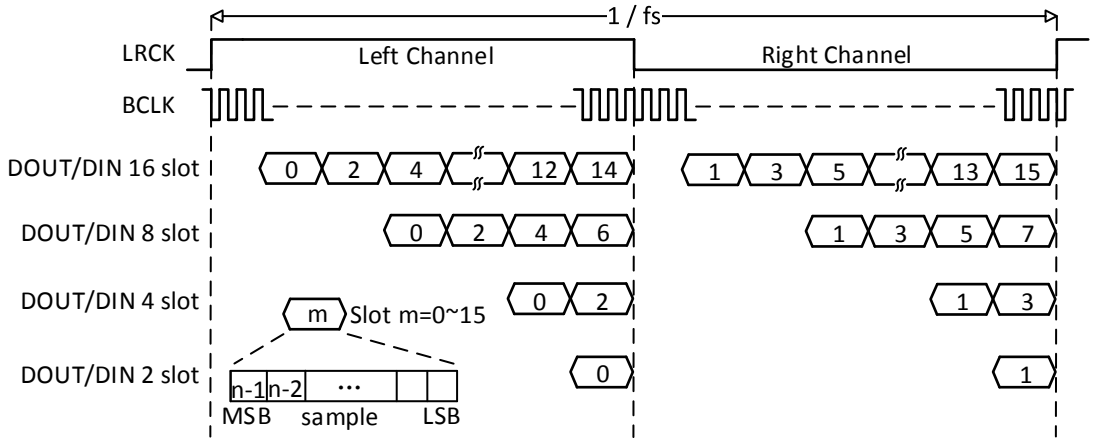


Figure 7-6. Timing Diagram for Right-justified/TDM-Right Mode

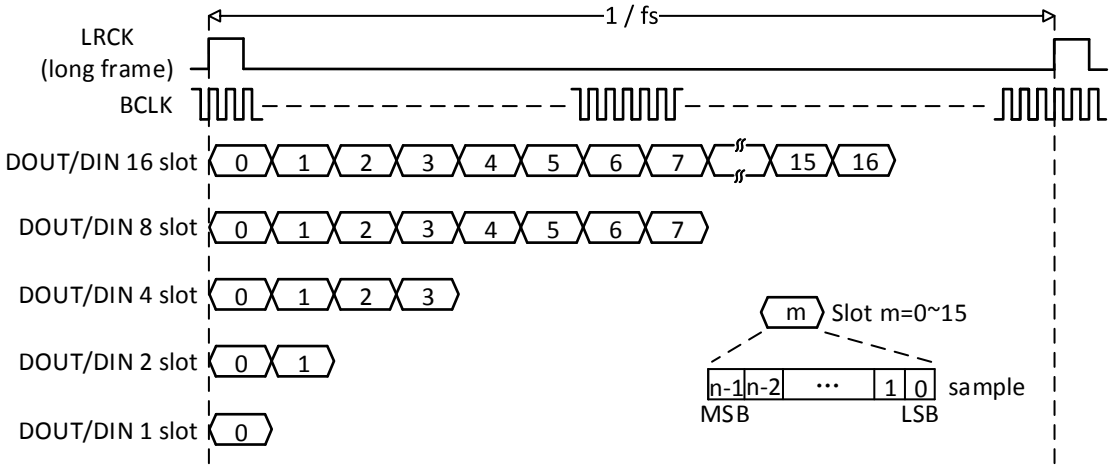


Figure 7-7. Timing Diagram for PCM Mode (long frame)

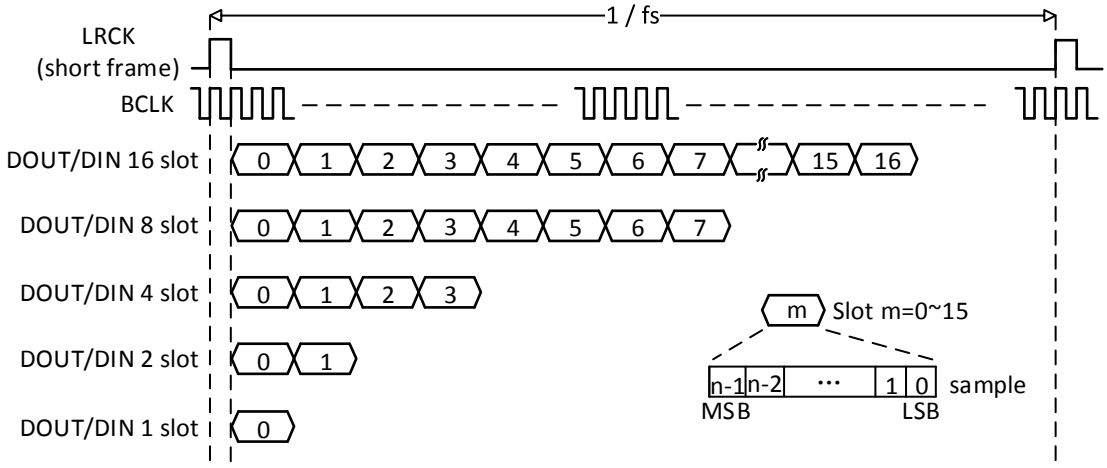


Figure 7-8. Timing Diagram for PCM Mode (short frame)

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7.1.4. Operation Modes

The software operation of the AHUB has eight steps: system setup, TXDIF Initial and Enable, RXDIF Initial and Enable, I2SnInitial and Enable, DAM Initial and Enable, DMA setup, AHUB disable and Check Record_buffer. Eight steps are described in detail in the following sections.

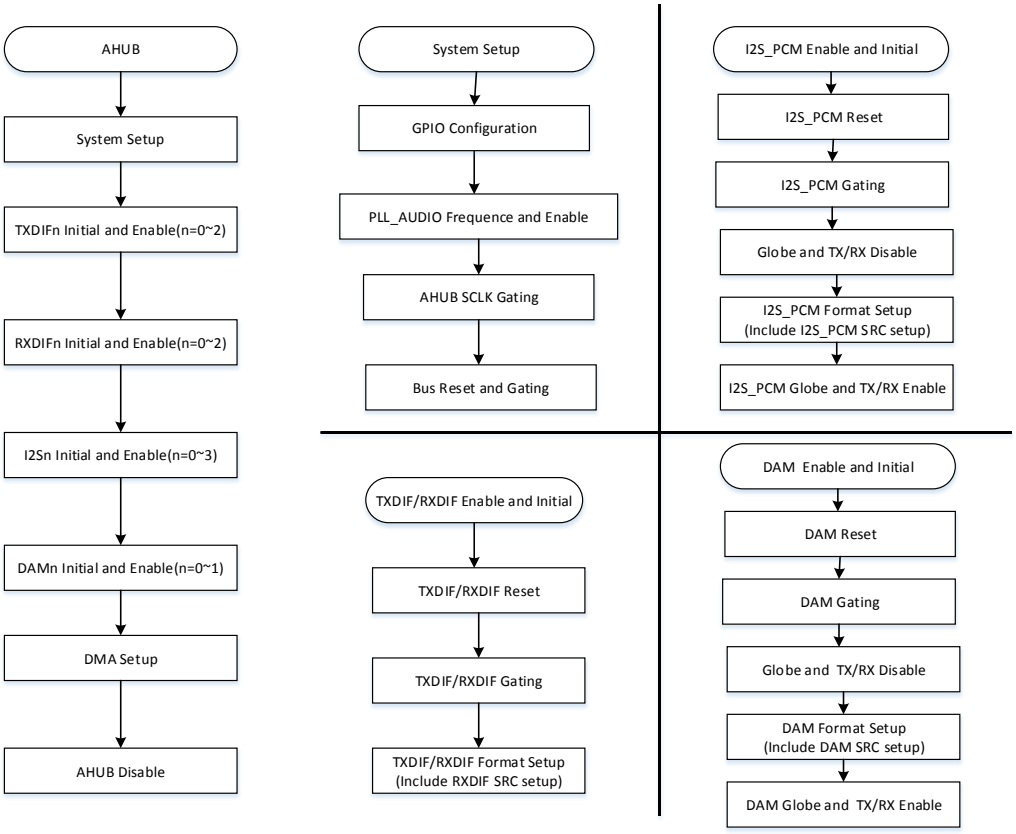


Figure 7-9. AUDIO HUB Operation Flow

7.1.4.1. System Setup

In the system setup, the first step is properly programming the GPIO. When the streaming pass by the I2S, and because I2S/PCM port is a multiplex pin. You can find the function in the pin multiplex specification.

Follow the clock source for Audio HUB. Choose 24.576MHz or 22.5792MHz. At first, set up the frequency of **PLL_AUDIO** in the **PLL_AUDIO_CTRL_REG**, and disable the **PLL_ENABLE** bit of **PLL_AUDIO_CTRL_REG**. Then, enable the **PLL_ENABLE** bit of **PLL_AUDIO_CTRL_REG**, Clear the **AUDIO_HUB Clock Register** and the **AUDI0_HUB Bus Gating Reset Register**. Then open the **Audio HUB SCLK_GATING** by writing 1 to **AUDIO_HUB Clock Register**[31], and open the Bus reset and gating by writing 1 to **AUDI0_HUB Bus Gating Reset Register**[0]/ **Reset Register**[16].

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7.1.4.2. TXDIF/RXDIF Initialization

Firstly, Reset and open the gating clock of the TXDIFn(n=0~2) by writing 1 to the **AHUB Reset**[31:29] and **AHUB Gating**[31:29]. When the TXDIF is used, the corresponding bit will be set . Secondly, Set up the format of the TXDIF, including TX_width, chan_num, txim and txtl. You can setup the format by writing value to **TXn_Control** and **TXn FIFO Control**.

RXDIF Initialization is similar to TXDIF. Firstly, Reset and Open the gating clock of the RXDIFn(n=0~2) by writing 1 to the **AHUB Reset**[27:25] and **AHUB Gating**[27:25]. When the TXDIF is used, the corresponding bit will be set. Secondly, Set up the format of the RXDIF, including RX_width, chan_num, rxom , rxtl and rx_src. You can setup the format by writing value to **RXn_Control** and **RXn FIFO Control**. And Setup the rx_src by writing value to **RXn Contact Select Register**. When the TXDIF contact to this RXDIF, the corresponding bit will be set.

7.1.4.3. I2S Initialization and DAM Initialization

Firstly, Reset and open the gating clock of the I2Sn(n=0~3) by writing 1 to the **AHUB Reset**[23:20] and **AHUB Gating**[23:20]. When the I2S is used, the corresponding bit will be set. Secondly, You should close the **globe enable bit**(I2Sn_CTRL[0]),disable **TX and RX bit**(I2Sn_CTRL[2:1]). Thirdly, you can setup the I2S/PCM of mater and slave. And choose the contact object to setup **I2Sn_RXDIF_CONT**. The configuration can be referred to the protocol of I2S/PCM. Thirdly, you can set up the translation mode, the sample resolution, the wide of slot, the channel slot number and so on. And then, Setup the **globe enable**, **TX enable** and **RX enable**.

DAM Initialization is similar to I2S. Firstly, Reset and open the gating clock of the DAMn(n=0~1) by writing 1 to the **AHUB Reset**[15:14] and **AHUB Gating**[15:14]. When the DAM is used, the corresponding bit will be set. Secondly, you can setup the DAM of **RXn_chan_num**(n=0~2) and **TX_chan_num**. And choose the contact object to setup **DAM_RXDIFn_SRC**(n=0~2). Thirdly, you can set up the RXn(n=0~2) and the TX channel in the DAM,and the channel volume. Please refer to the specification for more details.

7.1.4.4. DMA Setup

The Audio HUB supports two methods to transfer the data. The most common way is DMA, the setup of DMA can be found in the DMA specification. In this module, you just enable the DRQ and open the streaming start.

7.1.4.5. AHUB Disable

At last, you must disable the Audio HUB by writing 0x0 to the **AHUB_RST Register**.

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7.1.5. Typical Application

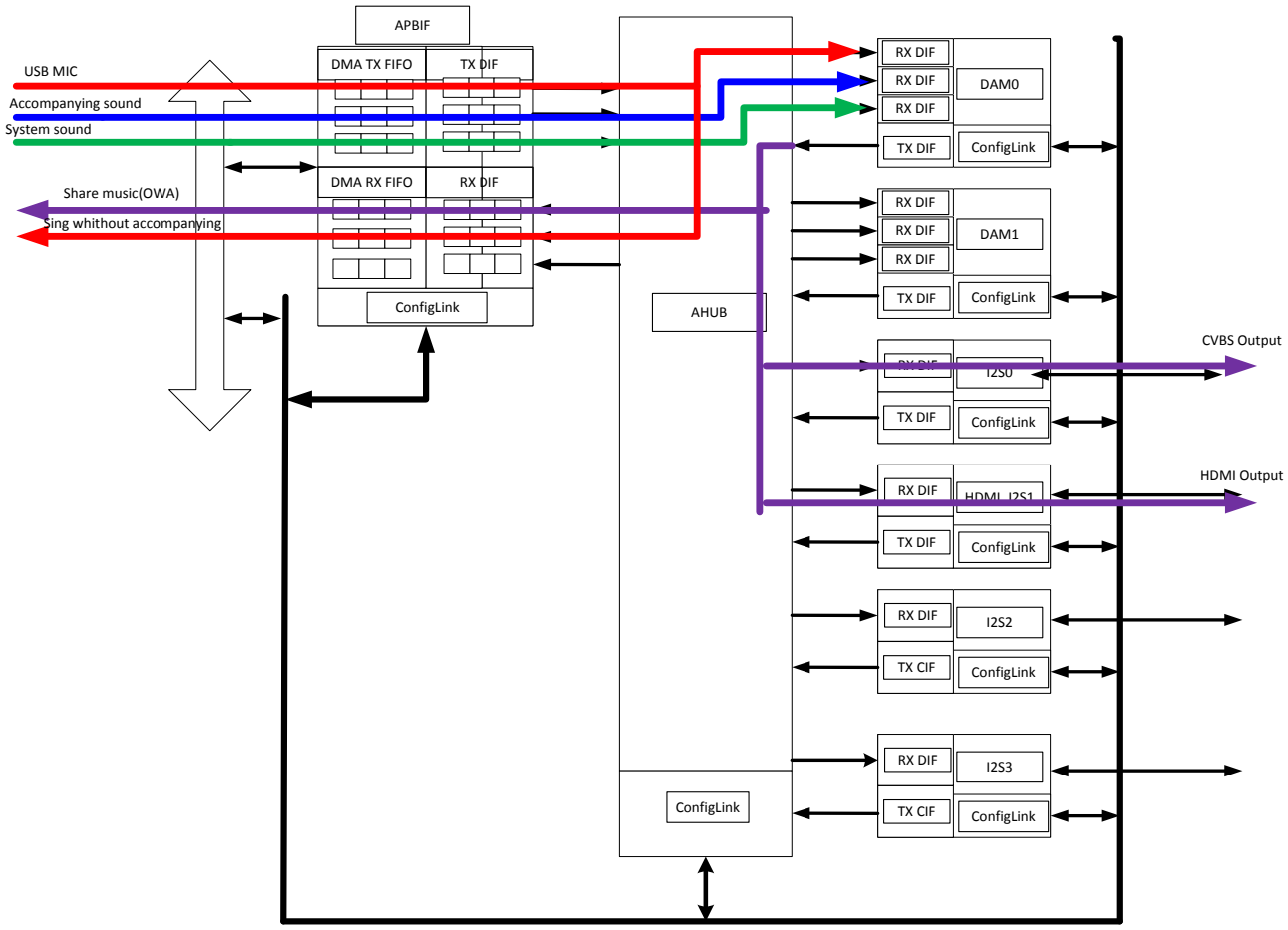


Figure 7-10.USB MIC Karaoke Date Streaming

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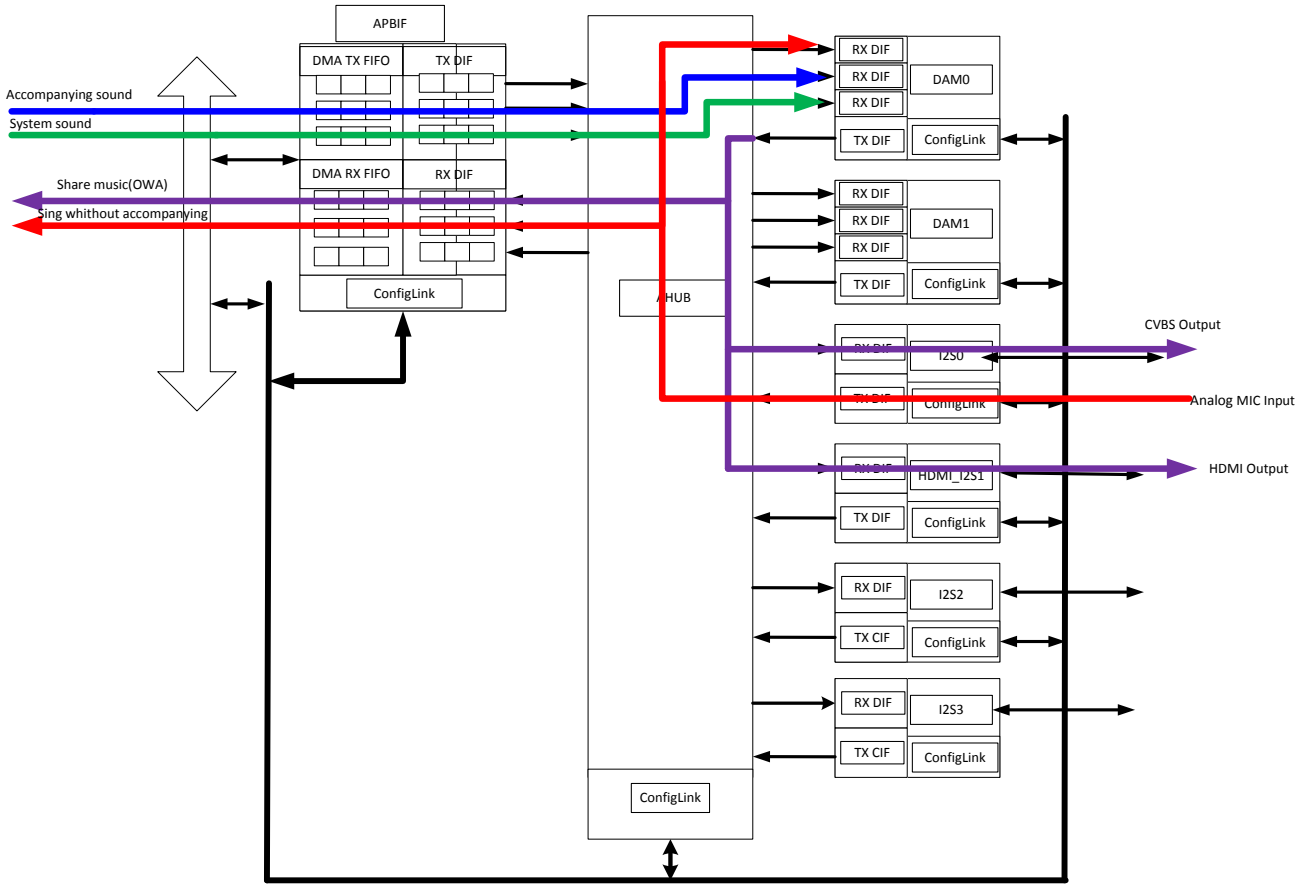


Figure 7-11.Analog MIC Karaoke Date Streaming

7.1.6. Register List

Module Name	Base Address
AHUB	0x05097000

Register Name	Offset	Description
AHUB_CTL	0x0000	AHUB Control
AHUB_RST	0x0008	AHUB Reset
AHUB_GAT	0x000C	AHUB Gating
APBIF_TXn_CTRL	0x0010+n*0x0030(n=0~2)	APBIF TXn Control
APBIF_TXnIRQ_CTRL	0x0014+n*0x0030(n=0~2)	APBIF TXn DMA & Interrupt Control
APBIF_TXnIRQ_STS	0x0018+n*0x0030(n=0~2)	AHUB APBIF TXn DMA & Interrupt Status
APBIF_TXnFIFO_CTRL	0x0020+n*0x0030(n=0~2)	AHUB APBIF TXn FIFO Control
APBIF_TXnFIFO_STS	0x0024+n*0x0030(n=0~2)	APBIF TXn FIFO Status
APBIF_TXnFIFO	0x0030+n*0x0030(n=0~2)	APBIF TXn FIFO
APBIF_TXnFIFO_CNT	0x0034+n*0x0030(n=0~2)	APBIF TXn FIFO Counter
APBIF_RXn_CTRL	0x0100+n*0x0030(n=0~2)	APBIF RXn Control

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APBIF_RXnIRQ_CTRL	0x0104+n*0x0030(n=0~2)	APBIF RXn DMA & Interrupt Control
APBIF_RXnIRQ_STS	0x0108+n*0x0030(n=0~2)	APBIF RXn DMA & Interrupt Status
APBIF_RXnFIFO_CTRL	0x0110+n*0x0030(n=0~2)	APBIF RXn FIFO Control
APBIF_RXnFIFO_STS	0x0114+n*0x0030(n=0~2)	APBIF RX0 FIFO Status
APBIF_RXn_CONT	0x0118+n*0x0030(n=0~2)	APBIF RXn Contact Select
APBIF_RXnFIFO	0x0120+n*0x0030(n=0~2)	APBIF RXn FIFO
APBIF_RXnFIFO_CNT	0x0124+n*0x0030(n=0~2)	APBIF RXn FIFO Counter
I2Sn_CTRL	0x0200+n*0x0100(n=0~3)	I2Sn Control
I2Sn_FMT0	0x0204+n*0x0100(n=0~3)	I2Sn Format 0
I2Sn_FMT1	0x0208+n*0x0100(n=0~3)	I2Sn Format 1
I2Sn_CLKD	0x020C+n*0x0100(n=0~3)	I2Sn Clock Divide
I2Sn_RXDIF_CONT	0x0220+n*0x0100(n=0~3)	I2Sn RXDIF Contact Select
I2Sn_CHCFG	0x0224+n*0x0100(n=0~3)	I2Sn Channel Configuration
I2Sn_IRQ_CTRL	0x0228+n*0x0100(n = 0~3)	I2Sn DMA & Interrupt Control
I2Sn_IRQ_STS	0x022C+n*0x0100(n = 0~3)	I2Sn DMA & Interrupt Status
I2Sn_SDOUTm_SLOTCTR	0x0230+n*0x0100+m*0x0010 (n=0~3)(m=0~3)	I2Sn Output Slot Control
I2Sn_SDOUTmCHMAP0	0x0234+n*0x0100+m*0x0010 (n=0~3)(m=0~3)	I2Sn SDOUTm Channel Mapping 0
I2Sn_SDOUTmCHMAP1	0x0238+n*0x0100+m*0x0010 (n=0~3)(m=0~3)	I2Sn SDOUTm Channel Mapping 1
I2Sn_SDIN_SLOTCTR	0x0270+n*0x0100(n=0~3)	I2Sn Input Slot Control
I2Sn_SDINCHMAP0	0x0274+n*0x0100(n=0~3)	I2Sn SDIN Channel Mapping 0
I2Sn_SDINCHMAP1	0x0278+n*0x0100(n=0~3)	I2Sn SDIN Channel Mapping 1
DAMn_CTRL	0x0A00+n*0x0080(n=0,1)	DAM Control
DAMn_RX0_SRC	0x0A10+n*0x0080(n=0,1)	DAM RXDIF0 Source Select
DAMn_RX1_SRC	0x0A14+n*0x0080(n=0,1)	DAM RXDIF1 Source Select
DAMn_RX2_SRC	0x0A18+n*0x0080(n=0,1)	DAM RXDIF2 Source Select
DAMn_MIX_CTRL0	0x0A30+n*0x0080(n=0,1)	DAM MIX Control 0
DAMn_MIX_CTRL1	0x0A34+n*0x0080(n=0,1)	DAM MIX Control 1
DAMn_MIX_CTRL2	0x0A38+n*0x0080(n=0,1)	DAM MIX Control 2
DAMn_MIX_CTRL3	0x0A3C+n*0x0080(n=0,1)	DAM MIX Control 3
DAMn_MIX_CTRL4	0x0A40+n*0x0080(n=0,1)	DAM MIX Control 4
DAMn_MIX_CTRL5	0x0A44+n*0x0080(n=0,1)	DAM MIX Control 5
DAMn_MIX_CTRL6	0x0A48+n*0x0080(n=0,1)	DAM MIX Control 6
DAMn_MIX_CTRL7	0x0A4C+n*0x0080(n=0,1)	DAM MIX Control 7
DAMn_GAIN_CTRL0	0x0A50+n*0x0080(n=0,1)	DAM GAIN Control 0
DAMn_GAIN_CTRL1	0x0A54+n*0x0080(n=0,1)	DAM GAIN Control 1
DAMn_GAIN_CTRL2	0x0A58+n*0x0080(n=0,1)	DAM GAIN Control 2
DAMn_GAIN_CTRL3	0x0A5C+n*0x0080(n=0,1)	DAM GAIN Control 3
DAMn_GAIN_CTRL4	0x0A60+n*0x0080(n=0,1)	DAM GAIN Control 4
DAMn_GAIN_CTRL5	0x0A64+n*0x0080(n=0,1)	DAM GAIN Control 5
DAMn_GAIN_CTRL6	0x0A68+n*0x0080(n=0,1)	DAM GAIN Control 6
DAMn_GAIN_CTRL7	0x0A6C+n*0x0080(n=0,1)	DAM GAIN Control 7

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7.1.7. Register Description

7.1.7.1. AHUB Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: AHUB_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/W	0x0	HDMI_SRC_SELECT 0:From I2S/PCM(0x050910000) 1:From Audio HUB HDMI(I2S1)
3:0	/	/	/

7.1.7.2. AHUB Reset Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: AHUB_ RST
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	APBIF_TXDIF0_RST 0: Assert 1: De-assert
30	R/W	0x0	APBIF_TXDIF1_RST 0: Assert 1: De-assert
29	R/W	0x0	APBIF_TXDIF2_RST 0: Assert 1: De-assert
28	/	/	/
27	R/W	0x0	APBIF_RXDIF0_RST 0: Assert 1: De-assert
26	R/W	0x0	APBIF_RXDIF1_RST 0: Assert 1: De-assert
25	R/W	0x0	APBIF_RXDIF2_RST 0: Assert 1: De-assert
24	/	/	/
23	R/W	0x0	I2S0_RST 0: Assert 1: De-assert
22	R/W	0x0	I2S1_RST 0: Assert

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			1: De-assert
21	R/W	0x0	I2S2_RST 0: Assert 1: De-assert
20	R/W	0x0	I2S3_RST 0: Assert 1: De-assert
19:16	/	/	/
15	R/W	0x0	DAM0_RST 0: Assert 1: De-assert
14	R/W	0x0	DAM1_RST 0: Assert 1: De-assert
13:0	/	/	/

7.1.7.3. AHUB Clock Gating Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: AHUB_GAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	APBIF_TXDIF0_GAT 0: Clock is OFF 1: Clock is ON
30	R/W	0x0	APBIF_TXDIF1_GAT 0: Clock is OFF 1: Clock is ON
29	R/W	0x0	APBIF_TXDIF2_GAT 0: Clock is OFF 1: Clock is ON
28	/	/	/
27	R/W	0x0	APBIF_RXDIF0_GAT 0: Clock is OFF 1: Clock is ON
26	R/W	0x0	APBIF_RXDIF1_GAT 0: Clock is OFF 1: Clock is ON
25	R/W	0x0	APBIF_RXDIF2_GAT 0: Clock is OFF 1: Clock is ON
24	/	/	/
23	R/W	0x0	I2S0_GAT 0: Clock is OFF 1: Clock is ON
22	R/W	0x0	I2S1_GAT

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			0: Clock is OFF 1: Clock is ON
21	R/W	0x0	I2S2_GAT 0: Clock is OFF 1: Clock is ON
20	R/W	0x0	I2S3_GAT 0: Clock is OFF 1: Clock is ON
19:16	/	/	/
15	R/W	0x0	DAM0_GAT 0: Clock is OFF 1: Clock is ON
14	R/W	0x0	DAM1_GAT 0: Clock is OFF 1: Clock is ON
13:0	/	/	/

7.1.7.4. AHUB APBIF TXn Control Register (Default Value: 0x0000_0100)

Offset: 0x0010+n*0x0030(n= 0~2)			Register Name: APBIF_TXn_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18:16	R/W	0x0	TXn_SR TX Sample Resolution 000:Reserved 001:8-bit 010:12-bit 011:16-bit 100:20-bit 101:24-bit 110:28-bit 111:32-bit
15:12	/	/	/
11:8	R/W	0x1	TXn_CHAN_NUM TX Channel Number which between CPU/DMA and FIFO 0000: 1 Channel 0001: 2 Channel ... 1110: 15 Channel 1111: 16 Channel
7:5	/	/	/
4	R/W	0x0	TXn_START APBIF TX Streaming Start
3:0	/	/	/

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7.1.7.5. AHUB APBIF TXn DMA & Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0014+n*0x0030(n = 0~2)			Register Name: APBIF_TXnIRQ_CTRL
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	TXn_DRQ TX FIFO Empty DRQ Enable 0: Disable 1: Enable
2	/	/	/
1	R/W	0x0	TXnOI_EN TX FIFO Overrun Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	TXnEI_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable

7.1.7.6. AHUB APBIF TXn DMA & Interrupt Status Register (Default Value: 0x0000_0001)

Offset: 0x0018+n*0x0030(n = 0~2)			Register Name: APBIF_TXnIRQ_STS
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	/	/	/
1	R/W1C	0x0	TXnO_INT TXFIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: TXFIFO Overrun Pending Interrupt Write ‘1’ to clear this interrupt.
0	R/W1C	0x1	TXnE_INT TXFIFO Empty pending Interrupt 0: No pending IRQ 1: TXFIFO Empty Pending Interrupt When Data in TXFIFO are Less than TX Trigger Level Write ‘1’ to clear this Interrupt or automatic clear if Interrupt condition fails

7.1.7.7. AHUB APBIF TXn FIFO Control Register (Default Value: 0x0000_0200)

Offset: 0x0020+n*0x0030(n = 0~2)	Register Name: APBIF_TXnFIFO_CTRL

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Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W1C	0x0	FTXn Write '1' to flush TX FIFO, self clear to '0'.
11:10	/	/	/
9:4	R/W	0x20	TXnTL TX FIFO Empty Trigger Level Interrupt and DMA request trigger level for TXFIFO normal condition Trigger Level = TXnTL
3:1	/	/	/
0	R/W	0x0	TXnIM TX FIFO Input Mode(Mode 0, 1) 0: Valid data at the MSB of TXFIFO register 1: Valid data at the LSB of TXFIFO register Example for 20-bits transmitted audio sample: Mode0: FIFO_I[31:0]={APB_WDATA[31:12], 12'h0} Mode1: FIFO_I[31:0]={APB_WDATA[19:0], 12'h0}

7.1.7.8. AHUB APBIF TXn FIFO Status Register (Default Value: 0x0000_0140)

Offset: 0x0024+n*0x0030(n = 0~2)			Register Name: APBIF_TXnFIFO_STS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R	0x1	TXnE TXFIFO Empty 0: No Room for New Sample in TXFIFO 1: More than One Room for New Sample in TXFIFO (>= 1 Word)
7	/	/	/
6:0	R	0x40	TXnE_CNT TXFIFO Empty Space Word Counter

7.1.7.9. AHUB APBIF TXn FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0030+n*0x0030(n = 0~2)			Register Name: APBIF_TXnFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	W	0x0	TXn_DATA TX Sample Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.

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7.1.7.10. AHUB APBIF TXn FIFO Counter Register (Default Value: 0x0000_0000)

Offset: 0x0034+n*0x0030(n = 0~2)			Register Name: APBIF_TXnFIFO_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TXn_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should counter on base of this initial value.

7.1.7.11. AHUB APBIF RXn Control Register (Default Value: 0x0000_0100)

Offset: 0x0100+n*0x0030(n = 0~2)			Register Name: APBIF_RXn_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18:16	R/W	0x0	RXn_SR RX Sample Resolution 000:Reserved 001:8-bit 010:12-bit 011:16-bit 100:20-bit 101:24-bit 110:28-bit 111:32-bit
15:12	/	/	/
11:8	R/W	0x1	RXn_CHAN_NUM TX Channel Number which between CPU/DMA and FIFO 0: 1 Channel 1: 2 Channel ... 14: 15 Channel 15: 16 Channel
7:5	/	/	/
4	R/W	0x0	RXn_START APBIF RX Streaming Start
3:0	/	/	/

7.1.7.12. AHUB APBIF RXn DMA & Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0104+n*0x0030(n = 0~2)	Register Name: APBIF_RXnIRQ_CTRL

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Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	RXn_DRQ RX FIFO Data Available DRQ Enable 0: Disable 1: Enable When set to '1', RXFIFO DMA Request line is asserted if Data is available in RXFIFO.
2	R/W	0x0	RXnUI_EN RX FIFO Under run Interrupt Enable 0: Disable 1: Enable
1	/	/	/
0	R/W	0x0	RXnAI_EN RX FIFO Data Available Interrupt Enable 0: Disable 1: Enable

7.1.7.13. AHUB APBIF RXn DMA & Interrupt Status Register (Default Value: 0x0000_0001)

Offset: 0x0108+n*0x0030(n = 0~2)			Register Name: APBIF_RXnIRQ_STS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W1C	0x0	RXnU_INT RX FIFO Underrun Pending Interrupt 0: No Pending Interrupt 1: RXFIFO Underrun Pending Interrupt Write '1' to clear this interrupt.
1	/	/	/
0	R/W1C	0x0	RXnA_INT RX FIFO Data Available Pending Interrupt 0: No Pending IRQ 1: TX FIFO Data Available Pending Interrupt When Data in RX FIFO are more than RX Trigger Level Write '1' to clear this Interrupt or Automatic clear if Interrupt condition fails

7.1.7.14. AHUB APBIF RXn FIFO Control Register (Default Value: 0x0000_0400)

Offset: 0x0110+n*0x0030(n = 0~2)			Register Name: APBIF_RXnFIFO_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12	R/W1C	0x0	FRXn

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			Write ‘1’ to flush RX FIFO, self clear to ‘0’.
11	/	/	/
10:4	R/W	0x40	RXnTL RX FIFO Empty Trigger Level Interrupt and DMA request trigger level for RXFIFO normal condition Trigger Level = RXnTL
3:2	/	/	/
1:0	R/W	0x0	RXnOM RX FIFO Output Mode(Mode 0, 1,2,3) 00: Expanding ‘0’ at LSB of RX FIFO register 01: Expanding received sample sign bit at MSB of RX FIFO register. 10: Truncating received samples at high half-word of RX FIFO register and low half-word of RX FIFO register is filled by ‘0’. 11: Truncating received samples at low half-word of RX FIFO register and high half-word of RX FIFO register is expanded by its sign bit. Example for 20-bits received audio sample: Mode 0: APB_RDATA[31:0] = {FIFO_O[31:12], 12’h0}. Mode 1: APB_RDATA[31:0] = {12{FIFO_O[31]}, FIFO_O[31:12]}. Mode 2: APB_RDATA[31:0] = {FIFO_O[31:16], 16’h0}. Mode 3: APB_RDATA[31:0] = {16{FIFO_O[31]}, FIFO_O[31:16]}.

7.1.7.15. AHUB APBIF RXn FIFO Status Register (Default Value: 0x0000_0100)

Offset: 0x0114+n*0x0030(n = 0~ 2)			Register Name: APBIF_RXnFIFO_STS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R	0x1	RXnA RX FIFO Available 0: No available data in RX FIFO 1: More than One Sample in RX FIFO (>= 1 Word)
7:0	R	0x0	RXnA_CNT RX FIFO Available Sample Word Counter

7.1.7.16. AHUB APBIF RXn Contact Select Register (Default Value: 0x0000_0000)

Offset: 0x0118+n*0x0030(n = 0~ 2)			Register Name: APBIF_RXn_CONT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	0x0	RXn_CONTACT_RXDIF Bit[31]:APBIF_TXDIF0 Bit[30]:APBIF_TXDIF1 Bit[29]:APBIF_TXDIF2 Bit[28]:Reserved Bit[27]:I2S0_TXDIF

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			Bit[26]:I2S1_TXDIF(HDMI) Bit[25]:I2S2_TXDIF Bit[24]:Reserved Bit[23]:I2S3_TXDIF Bit[22~20]:Reserved Bit[19]:DAM0_TXDIF Bit[18~16]:Reserved Bit[15]:DAM1_TXDIF Bit[14~0]:Reserved When the TXDIF Contact to this RXDIF, the corresponding bit will be set.
11:0	/	/	/

7.1.7.17. AHUB APBIF RXn FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0120+n*0x0030(n = 0~2)			Register Name: APBIF_RXnFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	RXn_DATA RX Sample Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

7.1.7.18. AHUB APBIF RXn FIFO Counter Register (Default Value: 0x0000_0000)

Offset: 0x0124+n*0x0030(n = 0~2)			Register Name: APBIF_RXnFIFO_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RXn_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is write into RXFIFO by function module, the RX sample counter register increases by one. The RX sample counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should counter on base of this initial value.

7.1.7.19. AHUB I2Sn Control Register (Default Value: 0x0004_0000)

Offset: 0x0200+n*0x0100(n = 0~3)			Register Name: I2Sn_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0x1	BCLK/LRCK Direction 0:Input 1:Output
17:12	/	/	/

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11	R/W	0x0	SDO3_EN 0:Disable, Hi-Z state 1:Enable
10	R/W	0x0	SDO2_EN 0:Disable, Hi-Z state 1:Enable
9	R/W	0x0	SDO1_EN 0:Disable, Hi-Z state 1:Enable
8	R/W	0x0	SDO0_EN 0:Disable, Hi-Z state 1:Enable
7	/	/	/
6	R/W	0x0	OUT Mute 0: Normal transfer 1: Force DOUT to output 0
5:4	R/W	0x0	MODE_SEL Mode Selection 00: PCM mode(offset 0: DSP_B; offset 1: DSP_A) 01: Left mode(offset 0: L-J Mode; offset 1: I2S mode) 10: Right-Justified mode 11: Reserved
3	R/W	0x0	LOOPBACK Loop back test 0: Normal mode 1: Loopback test When set '1', connecting the SDO0 with the SDI
2	R/W	0x0	TXEN Transmitter Block Enable 0: Disable 1: Enable
1	R/W	0x0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0x0	GEN Globe Enable A disable on this bit overrides any other block or channel enables. 0: Disable 1: Enable

7.1.7.20. AHUB I2Sn Format Register 0(Default Value: 0x0000_0033)

Offset: 0x0204+n*0x0100(n = 0~3)	Register Name: I2Sn_FMT0

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Bit	Read/Write	Default/Hex	Description
31	/	/	/
30	R/W	0x0	LRCK_WIDTH (Only apply in PCM mode) LRCK width 0: LRCK = 1 BCLK width (short frame) 1: LRCK = 2 BCLK width (long frame)
29:20	/	/	/
19	R/W	0x0	LRCK_POLARITY When apply in I2S/Left-Justified/Right-Justified mode: 0: Left channel when LRCK is low 1: Left channel when LRCK is high When apply in PCM mode: 0: PCM LRCK asserted at the negative edge 1: PCM LRCK asserted at the positive edge
18	/	/	/
17:8	R/W	0x0	LRCK_PERIOD It is used to program the number of BCLKs per channel of sample frame. This value is interpreted as follow: PCM Mode: Number of BCLKs within (Left + Right) channel width. I2S/Left-Justified/Right-Justified Mode: Number of BCLKs within each individual channel width(Left or Right) For example: N = 7 : 8 BCLKs width ... N = 1023 : 1024 BCLKs width
7	R/W	0x0	BCLK_POLARITY 0: Normal mode, negative edge drive and positive edge sample 1: Invert mode, positive edge drive and negative edge sample
6:4	R/W	0x3	SR Sample Resolution 000: Reserved 001: 8-bit 010: 12-bit 011: 16-bit 100: 20-bit 101: 24-bit 110: 28-bit 111: 32-bit
3	R/W	0x0	EDGE_TRANSFER 0: SDO drive data and SDI sample data at the different BCLK edge 1: SDO drive data and SDI sample data at the sample BCLK edge BCLK_PLARITY = 0, use negative edge BCLK_PLARITY = 1, use positive edge
2:0	R/W	0x3	SW Slot Width Select

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			000: Reserved 001: 8-bit 010: 12-bit 011: 16-bit 100: 20-bit 101: 24-bit 110: 28-bit 111: 32-bit

7.1.7.21. AHUB I2Sn Format Register 1(Default Value: 0x0000_0030)

Offset: 0x0208+n*0x0100(n = 0~3)			Register Name: I2Sn_FMT1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	RX MLS MSB/LSB First Select 0: MSB First 1: LSB First
6	R/W	0x0	TX MLS MSB/LSB First Select 0: MSB First 1: LSB First
5:4	R/W	0x3	SEXT Sign Extend in slot [sample resolution < width] 00: Zeros or audio gain padding at LSB position 01: Sign extension at MSB position 10: Reserved 11: Transfer 0 after each sample in each slot
3:2	R/W	0x0	RX_PDM PCM Data Mode 00: Linear PCM 01: reserved 10: 8-bit u-law 11: 8-bit A-law
1:0	R/W	0x0	TX_PDM PCM Data Mode 00: Linear PCM 01: reserved 10: 8-bit u-law 11: 8-bit A-law

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7.1.7.22. AHUB I2Sn Clock Divide Register (Default Value: 0x0000_0000)

Offset: 0x020C+n*0x0100(n = 0~3)			Register Name: I2Sn_CLKD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	MCLKO_EN 0: Disable MCLK Output 1: Enable MCLK Output
7:4	R/W	0x0	BCLKDIV BCLK Divide Ratio from PLL_Audio 0000: reserved 0001: Divide by 1 0010: Divide by 2 0011: Divide by 4 0100: Divide by 6 0101: Divide by 8 0110: Divide by 12 0111: Divide by 16 1000: Divide by 24 1001: Divide by 32 1010: Divide by 48 1011: Divide by 64 1100: Divide by 96 1101: Divide by 128 1110: Divide by 176 1111: Divide by 192
3:0	R/W	0x0	MCLKDIV MCLK Divide Ratio from PLL_Audio 0000: reserved 0001: Divide by 1 0010: Divide by 2 0011: Divide by 4 0100: Divide by 6 0101: Divide by 8 0110: Divide by 12 0111: Divide by 16 1000: Divide by 24 1001: Divide by 32 1010: Divide by 48 1011: Divide by 64 1100: Divide by 96 1101: Divide by 128 1110: Divide by 176 1111: Divide by 192

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7.1.7.23. AHUB I2Sn RXDIF Contact Select Register (Default Value: 0x0000_0000)

Offset: 0x0220+n*0x0100(n = 0~3)			Register Name: I2Sn_RXDIF_CONT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	0x0	RXn_CONTACT_RXDIF Bit[31]:APBIF_TXDIF0 Bit[30]:APBIF_TXDIF1 Bit[29]:APBIF_TXDIF2 Bit[28]:Reserved Bit[27]:I2S0_TXDIF Bit[26]:I2S1_TXDIF(HDMI) Bit[25]:I2S2_TXDIF Bit[24]:Reserved Bit[23]:I2S3_TXDIF Bit[22]:Reserved Bit[21]:Reserved Bit[20]:Reserved Bit[19]:DAM0_TXDIF Bit[18]:Reserved Bit[17]:Reserved Bit[16]:Reserved Bit[15]:DAM1_TXDIF Bit[14]:Reserved Bit[13]:Reserved Bit[12]:Reserved When the TXDIF Contact to this RXDIF, the corresponding bit will be set.
11:0	/	/	/

7.1.7.24. AHUB I2Sn Channel Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0224+n*0x0100(n = 0~3)			Register Name: I2Sn_CHCFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	TX_SLOT_HIZ 0:Normal Mode for the Last Half Cycle of BCLK in the Slot 1:Turn to Hi-Z State for the Last Half Cycle of BCLK in the Slot
8	R/W	0x0	TX_STATE 0: Transfer Level 0 When Not Transferring Slot 1:Turn to Hi-Z State(TDM) When Not Transferring Slot
7:4	R/W	0x0	RX_CHAN_NUM RX Channel/Slot Number which between AHUB and I2Sn 0000: 1 channel or slot … 0111: 8 channels or slots

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			1000: 9 channels or slots … 1111: 16 channels or slots
3:0	R/W	0x0	TX_CHAN_NUM TX Channel/Slot Number which between AHUB and I2Sn 0000: 1 channel or slot … 0111: 8 channels or slots 1000: 9 channels or slots … 1111: 16 channels or slots

7.1.7.25. AHUB I2Sn DMA & Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0228+n*0x0100(n = 0~3)			Register Name: I2Sn_IRQ_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	RXnOI_EN RX FIFO Overrun Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	TXnUI_EN TX FIFO Under run Interrupt Enable 0: Disable 1: Enable

7.1.7.26. AHUB I2Sn DMA & Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x022C+n*0x0100(n = 0~3)			Register Name: I2Sn_IRQ_STS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1C	0x0	RXnO_INT RX FIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: RXFIFO Overrun Pending Interrupt Write ‘1’ to clear this interrupt
0	R/W1C	0x0	TXnU_INT TX FIFO Underrun Pending Interrupt 0: No Pending Interrupt 1: TXFIFO Underrun Pending Interrupt Write ‘1’ to clear this interrupt

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7.1.7.27. AHUB I2Sn Output SLOT Control Register (Default Value: 0x0000_0000)

Offset: 0x0230+n*0x0100+m*0x0010 (n=0~3)(m=0~3)			Register Name: I2Sn_SDOUTm_SLOTCTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x0	SDOUTm_OFFSET SDOUT offset tune, SDOUT data offset to LRCK 0: no offset n: data is offset by n BCLKs to LRCK
19:16	R/W	0x0	SDOUTm_SLOT_NUM SDOUT slot number select for each output 0000: 1 Slots ... 0111: 8 Slots 1000: 9 Slots ... 1111: 16 Slots
15:0	R/W	0x0	SDOUTm_SLOT_EN SDOUT slot enable, bit[15:0] refer to slot[15:0]. When one or more slot(s) is(are) disable, the affected slot(s) is(are) set to disable state 0: Disable 1: Enable

7.1.7.28. AHUB SDOUTm Channel Mapping Register 0(Default Value: 0x7654_3210)

Offset: 0x0234+n*0x0100+m*0x0010 (n=0~3)(m=0~3)			Register Name: I2Sn_SDOUTmCHMAP0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x7	SDOUTm_SLOT7_MAP SDOUT Slot7 Mapping 0000: 1st channel data ... 1111: 16th channel data
27:24	R/W	0x6	SDOUTm_SLOT6_MAP SDOUT Slot6 Mapping 0000: 1st channel data ... 1111: 16th channel data
23:20	R/W	0x5	SDOUTm_SLOT5_MAP SDOUT Slot5 Mapping 0000: 1st channel data ... 1111: 16th channel data

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19:16	R/W	0x4	SDOUTm_SLOT4_MAP SDOUT Slot4 Mapping 0000: 1st channel data ... 1111: 16th channel data
15:12	R/W	0x3	SDOUTm_SLOT3_MAP SDOUT Slot3 Mapping 0000: 1st channel data ... 1111: 16th channel data
11:8	R/W	0x2	SDOUTm_SLOT2_MAP SDOUT Slot2 Mapping 0000: 1st channel data ... 1111: 16th channel data
7:4	R/W	0x1	SDOUTm_SLOT1_MAP SDOUT Slot1 Mapping 0000: 1st channel data ... 1111: 16th channel data
3:0	R/W	0x0	SDOUTm_SLOT0_MAP SDOUT Slot0 Mapping 0000: 1st channel data ... 1111: 16th channel data

7.1.7.29. AHUB SDOUTm Channel Mapping Register 1(Default Value: 0xFEDC_BA98)

Offset: 0x0238+n*0x0100+m*0x0010 (n=0~3)(m=0~3)			**Register Name: I2Sn_SDOUTmCHMAP1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0xF	SDOUTm_SLOT15_MAP SDOUT Slot15 Mapping 0000: 1st channel data ... 1111: 16th channel data
27:24	R/W	0xE	SDOUTm_SLOT14_MAP SDOUT Slot14 Mapping 0000: 1st channel data ... 1111: 16th channel data
23:20	R/W	0xD	SDOUTm_SLOT13_MAP SDOUT Slot13 Mapping 0000: 1st channel data

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			... 1111: 16th channel data
19:16	R/W	0xC	SDOUTm_SLOT12_MAP SDOUT Slot12 Mapping 0000: 1st channel data ... 1111: 16th channel data
15:12	R/W	0xB	SDOUTm_SLOT11_MAP SDOUT Slot11 Mapping 0000: 1st channel data ... 1111: 16th channel data
11:8	R/W	0xA	SDOUTm_SLOT10_MAP SDOUT Slot10 Mapping 0000: 1st channel data ... 1111: 16th channel data
7:4	R/W	0x9	SDOUTm_SLOT9_MAP SDOUT Slot9 Mapping 0000: 1st channel data ... 1111: 16th channel data
3:0	R/W	0x8	SDOUTm_SLOT8_MAP SDOUT Slot8 Mapping 0000: 1st channel data ... 1111: 16th channel data

7.1.7.30. AHUB I2Sn Input Slot Control Register (Default Value: 0x0000_0000)

Offset: 0x0270+n*0x0100(n=0~3)			Register Name: I2Sn_SDIN_SLOTCTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x0	SDIN_OFFSET SDIN offset tune, SDIN data offset to LRCK 0: no offset n: data is offset by n BCLKs to LRCK
19:16	R/W	0x0	SDIN_SLOT_NUM SDIN Slot number Select for each output 0000: 1 Slots ... 0111: 8 Slots 1000: 9 Slots ...

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			1111: 16 Slots
15:0	/	/	/

7.1.7.31. AHUB SDIN Channel Mapping Register 0(Default Value: 0x7654_3210)

Offset: 0x0274+n*0x0100(n=0~3)			Register Name: I2Sn_SDINCHMAP0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x7	SDIN_SLOT7_MAP SDIN Slot7 Mapping 0000: 1st channel data ... 1111: 16th channel data
27:24	R/W	0x6	SDIN_SLOT6_MAP SDIN Slot6 Mapping 0000: 1st channel data ... 1111: 16th channel data
23:20	R/W	0x5	SDIN_SLOT5_MAP SDIN Slot5 Mapping 0000: 1st channel data ... 1111: 16th channel data
19:16	R/W	0x4	SDIN_SLOT4_MAP SDIN Slot4 Mapping 0000: 1st channel data ... 1111: 16th channel data
15:12	R/W	0x3	SDIN_SLOT3_MAP SDIN Slot3 Mapping 0000: 1st channel data ... 1111: 16th channel data
11:8	R/W	0x2	SDIN_SLOT2_MAP SDIN Slot2 Mapping 0000: 1st channel data ... 1111: 16th channel data
7:4	R/W	0x1	SDIN_SLOT1_MAP SDIN Slot1 Mapping 0000: 1st channel data ... 1111: 16th channel data
3:0	R/W	0x0	SDIN_SLOT0_MAP SDIN Slot0 Mapping

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			0000: 1st channel data ... 1111: 16th channel data

7.1.7.32. AHUB SDIN Channel Mapping Register 1(Default Value: 0xFEDC_BA98)

Offset: 0x0278+n*0x0100(n=0~3)			Register Name: I2Sn_SDINCHMAP1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0xF	SDIN_SLOT15_MAP SDIN Slot15 Mapping 0000: 1st channel data ... 1111: 16th channel data
27:24	R/W	0xE	SDIN_SLOT14_MAP SDIN Slot14 Mapping 0000: 1st channel data ... 1111: 16th channel data
23:20	R/W	0xD	SDIN_SLOT13_MAP SDIN Slot13 Mapping 0: 1st channel data ... 15: 16th channel data
19:16	R/W	0xC	SDIN_SLOT12_MAP SDIN Slot12 Mapping 0000: 1st channel data ... 1111: 16th channel data
15:12	R/W	0xB	SDIN_SLOT11_MAP SDIN Slot11 Mapping 0000: 1st channel data ... 1111: 16th channel data
11:8	R/W	0xA	SDIN_SLOT10_MAP SDIN Slot10 Mapping 0000: 1st channel data ... 1111: 16th channel data
7:4	R/W	0x9	SDIN_SLOT9_MAP SDIN Slot9 Mapping 0000: 1st channel data ... 1111: 16th channel data
3:0	R/W	0x8	SDIN_SLOT8_MAP

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			SDIN Slot8 Mapping 0000: 1st channel data ... 1111: 16th channel data

7.1.7.33. AHUB DAM Control Register (Default Value: 0x0000_0000)

Offset: 0x0A00 + n*0x0080(n=0,1)			Register Name: DAM_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x0	RX2_NUM RX2 Channel Num
23:20	R/W	0x0	RX1_NUM RX1 Channel Num
19:16	R/W	0x0	RX0_NUM RX0 Channel Num
15:12	/	/	/
11:8	R/W	0x0	TX Channel Num
7	/	/	/
6	R/W	0x0	RX2EN Receiver Enable 0: Disable 1: Enable
5	R/W	0x0	RX1EN Receiver Enable 0: Disable 1: Enable
4	R/W	0x0	RX0EN Receiver Enable 0: Disable 1: Enable
3:1	/	/	/
0	R/W	0x0	TXEN Transmitter Enable 0: Disable 1: Enable

7.1.7.34. AHUB DAM RXDIF0 Source Select (Default Value: 0x0000_0000)

Offset: 0x0A10 + n*0x0080(n=0,1)			Register Name: DAM_RX0_SRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	0x0	RXn_CONTACT_RXDIF Bit[31]:APBIF_TXDIF0

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			Bit[30]:APBIF_TXDIF1 Bit[29]:APBIF_TXDIF2 Bit[28]:Reserved Bit[27]:I2S0_TXDIF Bit[26]:I2S1_TXDIF(HDMI) Bit[25]:I2S2_TXDIF Bit[24]:Reserved Bit[23]:I2S3_TXDIF Bit[22]:Reserved Bit[21]:Reserved Bit[20]:Reserved Bit[19]:DAM0_TXDIF0 Bit[18]:Reserved Bit[17]:Reserved Bit[16]:Reserved Bit[15]:DAM1_TXDIF0 Bit[14]:Reserved Bit[13]:Reserved Bit[12]:Reserved When the TXDIF Contact to this RXDIF, the corresponding bit will be set.
11:0	/	/	/

7.1.7.35. AHUB DAM RXDIF1 Source Select (Default Value: 0x0000_0000)

Offset: 0x0A14 + n*0x0080(n=0,1)			Register Name: DAM_RX1_SRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	0x0	RXn_CONTACT_RXDIF Bit[31]:APBIF_TXDIF0 Bit[30]:APBIF_TXDIF1 Bit[29]:APBIF_TXDIF2 Bit[28]:Reserved Bit[27]:I2S0_TXDIF Bit[26]:I2S1_TXDIF(HDMI) Bit[25]:I2S2_TXDIF Bit[24]:Reserved Bit[23]:I2S3_TXDIF Bit[22]:Reserved Bit[21]:Reserved Bit[20]:Reserved Bit[19]:DAM0_TXDIF0 Bit[18]:Reserved Bit[17]:Reserved Bit[16]:Reserved Bit[15]:DAM1_TXDIF0

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			Bit[14]:Reserved Bit[13]:Reserved Bit[12]:Reserved When the TXDIF Contact to this RXDIF, the corresponding bit will be set.
11:0	/	/	/

7.1.7.36. AHUB DAM RXDIF2 Source Select (Default Value: 0x0000_0000)

Offset: 0x0A18 + n*0x0080(n=0,1)			Register Name: DAM_RX2_SRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	0x0	RXn_CONTACT_RXDIF Bit[31]:APBIF_TXDIF0 Bit[30]:APBIF_TXDIF1 Bit[29]:APBIF_TXDIF2 Bit[28]:Reserved Bit[27]:I2S0_TXDIF Bit[26]:I2S1_TXDIF(HDMI) Bit[25]:I2S2_TXDIF Bit[24]:Reserved Bit[23]:I2S3_TXDIF Bit[22]:Reserved Bit[21]:Reserved Bit[20]:Reserved Bit[19]:DAM0_TXDIF0 Bit[18]:Reserved Bit[17]:Reserved Bit[16]:Reserved Bit[15]:DAM1_TXDIF0 Bit[14]:Reserved Bit[13]:Reserved Bit[12]:Reserved When the TXDIF Contact to this RXDIF, the corresponding bit will be set.
11:0	/	/	/

7.1.7.37. AHUB DAM MIX Control 0(Default Value: 0x0111_0000)

Offset: 0x0A30 + n*0x0080(n=0,1)			Register Name: DAM_MIX_CTRL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x1	TXCH1_MIX_RXCH2 RX2 Channel NUM to TXDIF Channel 1 N: TXDIF Channel 1 MIX RX2 Channel N
23:20	R/W	0x1	TXCH1_MIX_RXCH1

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			RX1 Channel NUM to TXDIF Channel 1 N: TXDIF Channel 1 MIX RX1 Channel N
19:16	R/W	0x1	TXCH1_MIX_RXCH0 RX0 Channel NUM to TXDIF Channel 1 N: TXDIF Channel 1 MIX RX0 Channel N
15:12	/	/	
11:8	R/W	0x0	TXCH0_MIX_RXCH2 RX2 Channel NUM to TXDIF Channel 0 N: TXDIF Channel 0 MIX RX2 Channel N
7:4	R/W	0x0	TXCH0_MIX_RXCH1 RX1 Channel NUM to TXDIF Channel 0 N: TXDIF Channel 0 MIX RX1 Channel N
3:0	R/W	0x0	TXCH0_MIX_RXCH0 RX0 Channel NUM to TXDIF Channel 0 N: TXDIF Channel 0 MIX RX0 Channel N

7.1.7.38. AHUB DAM MIX Control 1(Default Value: 0x0333_0222)

Offset: 0x0A34 + n*0x0080(n=0,1)			Register Name: DAM_MIX_CTRL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x3	TXCH3_MIX_RXCH2 RX2 Channel NUM to TXDIF Channel 3 N: TXDIF Channel 3 MIX RX2 Channel N
23:20	R/W	0x3	TXCH3_MIX_RXCH1 RX1 Channel NUM to TXDIF Channel 3 N: TXDIF Channel 3 MIX RX1 Channel N
19:16	R/W	0x3	TXCH3_MIX_RXCH0 RX0 Channel NUM to TXDIF Channel 3 N: TXDIF Channel 3 MIX RX0 Channel N
15:12	/	/	/
11:8	R/W	0x2	TXCH2_MIX_RXCH2 RX2 Channel NUM to TXDIF Channel 2 N: TXDIF Channel 2 MIX RX2 Channel N
7:4	R/W	0x2	TXCH2_MIX_RXCH1 RX1 Channel NUM to TXDIF Channel 2 N: TXDIF Channel 2 MIX RX1 Channel N
3:0	R/W	0x2	TXCH2_MIX_RXCH0 RX0 Channel NUM to TXDIF Channel 2 N: TXDIF Channel 2 MIX RX0 Channel N

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7.1.7.39. AHUB DAM MIX Control 2(Default Value: 0x0555_0444)

Offset: 0x0A38 + n*0x0080(n=0,1)			Register Name: DAM_MIX_CTRL2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x5	TXCH5_MIX_RXCH2 RX2 Channel NUM to TXDIF Channel 5 N: TXDIF Channel 5 MIX RX2 Channel N
23:20	R/W	0x5	TXCH5_MIX_RXCH1 RX1 Channel NUM to TXDIF Channel 5 N: TXDIF Channel 5 MIX RX1 Channel N
19:16	R/W	0x5	TXCH5_MIX_RXCH0 RX0 Channel NUM to TXDIF Channel 5 N: TXDIF Channel 5 MIX RX0 Channel N
15:12	/	/	/
11:8	R/W	0x4	TXCH4_MIX_RXCH2 RX2 Channel NUM to TXDIF Channel 4 N: TXDIF Channel 4 MIX RX2 Channel N
7:4	R/W	0x4	TXCH4_MIX_RXCH1 RX1 Channel NUM to TXDIF Channel 4 N: TXDIF Channel 2 MIX RX1 Channel N
3:0	R/W	0x4	TXCH4_MIX_RXCH0 RX0 Channel NUM to TXDIF Channel 4 N: TXDIF Channel 4 MIX RX0 Channel N

7.1.7.40. AHUB DAM MIX Control 3(Default Value: 0x0777_0666)

Offset: 0x0A3C + n*0x0080(n=0,1)			Register Name: DAM_MIX_CTRL3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x7	TXCH7_MIX_RXCH2 RX2 Channel NUM to TXDIF Channel 7 N: TXDIF Channel 7 MIX RX2 Channel N
23:20	R/W	0x7	TXCH7_MIX_RXCH1 RX1 Channel NUM to TXDIF Channel 7 N: TXDIF Channel 7 MIX RX1 Channel N
19:16	R/W	0x7	TXCH7_MIX_RXCH0 RX0 Channel NUM to TXDIF Channel 7 N: TXDIF Channel 7 MIX RX0 Channel N
15:12	/	/	/
11:8	R/W	0x6	TXCH6_MIX_RXCH2 RX2 Channel NUM to TXDIF Channel 6 N: TXDIF Channel 6 MIX RX2 Channel N
7:4	R/W	0x6	TXCH6_MIX_RXCH1

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			RX1 Channel NUM to TXDIF Channel 6 N: TXDIF Channel 6 MIX RX1 Channel N
3:0	R/W	0x6	TXCH6_MIX_RXCH0 RX0 Channel NUM to TXDIF Channel 6 N: TXDIF Channel 6 MIX RX0 Channel N

7.1.7.41. AHUB DAM MIX Control 4(Default Value: 0x0999_0888)

Offset: 0x0A40 + n*0x0080(n=0,1)			Register Name: DAM_MIX_CTRL4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x9	TXCH9_MIX_RXCH2 RX2 Channel NUM to TXDIF Channel 9 N: TXDIF Channel 9 MIX RX2 Channel N
23:20	R/W	0x9	TXCH9_MIX_RXCH1 RX1 Channel NUM to TXDIF Channel 9 N: TXDIF Channel 9 MIX RX1 Channel N
19:16	R/W	0x9	TXCH9_MIX_RXCH0 RX0 Channel NUM to TXDIF Channel 9 N: TXDIF Channel 9 MIX RX0 Channel N
15:12	/	/	/
11:8	R/W	0x8	TXCH8_MIX_RXCH2 RX2 Channel NUM to TXDIF Channel 8 N: TXDIF Channel 8 MIX RX2 Channel N
7:4	R/W	0x8	TXCH8_MIX_RXCH1 RX1 Channel NUM to TXDIF Channel 8 N: TXDIF Channel 8 MIX RX1 Channel N
3:0	R/W	0x8	TXCH8_MIX_RXCH0 RX0 Channel NUM to TXDIF Channel 8 N: TXDIF Channel 8 MIX RX0 Channel N

7.1.7.42. AHUB DAM MIX Control 5(Default Value: 0x0BBB_0AAA)

Offset: 0x0A44 + n*0x0080(n=0,1)			Register Name: DAM_MIX_CTRL5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0xB	TXCHB_MIX_RXCH2 RX2 Channel NUM to TXDIF Channel B N: TXDIF Channel B MIX RX2 Channel N
23:20	R/W	0xB	TXCHB_MIX_RXCH1 RX1 Channel NUM to TXDIF Channel B N: TXDIF Channel B MIX RX1 Channel N
19:16	R/W	0xB	TXCHB_MIX_RXCH0

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			RX0 Channel NUM to TXDIF Channel B N: TXDIF Channel B MIX RX0 Channel N
15:12	/	/	/
11:8	R/W	0xA	TXCHA_MIX_RXCH2 RX2 Channel NUM to TXDIF Channel A N: TXDIF Channel A MIX RX2 Channel N
7:4	R/W	0xA	TXCHA_MIX_RXCH1 RX1 Channel NUM to TXDIF Channel A N: TXDIF Channel A MIX RX1 Channel N
3:0	R/W	0xA	TXCHA_MIX_RXCH0 RX0 Channel NUM to TXDIF Channel A N: TXDIF Channel A MIX RX0 Channel N

7.1.7.43. AHUB DAM MIX Control 6(Default Value: 0x0DDD_0CCC)

Offset: 0x0A48 + n*0x0080(n=0,1)			Register Name: DAM_MIX_CTRL6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0xD	TXCHD_MIX_RXCH2 RX2 Channel NUM to TXDIF Channel D N: TXDIF Channel D MIX RX2 Channel N
23:20	R/W	0xD	TXCHD_MIX_RXCH1 RX1 Channel NUM to TXDIF Channel D N: TXDIF Channel D MIX RX1 Channel N
19:16	R/W	0xD	TXCHD_MIX_RXCH0 RX0 Channel NUM to TXDIF Channel D N: TXDIF Channel D MIX RX0 Channel N
15:12	/	/	/
11:8	R/W	0xC	TXCHC_MIX_RXCH2 RX2 Channel NUM to TXDIF Channel C N: TXDIF Channel C MIX RX2 Channel N
7:4	R/W	0xC	TXCHC_MIX_RXCH1 RX1 Channel NUM to TXDIF Channel C N: TXDIF Channel C MIX RX1 Channel N
3:0	R/W	0xC	TXCHC_MIX_RXCH0 RX0 Channel NUM to TXDIF Channel C N: TXDIF Channel C MIX RX0 Channel N

7.1.7.44. AHUB DAM MIX Control 7(Default Value: 0x0FFF_0EEE)

Offset: 0x0A4C + n*0x0080(n=0,1)			Register Name: DAM_MIX_CTRL7
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/

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27:24	R/W	0xF	TXCHF_MIX_RXCH2 RX2 Channel NUM to TXDIF Channel F N: TXDIF Channel F MIX RX2 Channel N
23:20	R/W	0xF	TXCHF_MIX_RXCH1 RX1 Channel NUM to TXDIF Channel F N: TXDIF Channel F MIX RX1 Channel N
19:16	R/W	0xF	TXCHF_MIX_RXCH0 RX0 Channel NUM to TXDIF Channel F N: TXDIF Channel F MIX RX0 Channel N
15:12	/	/	/
11:8	R/W	0xE	TXCHE_MIX_RXCH2 RX2 Channel NUM to TXDIF Channel E N: TXDIF Channel E MIX RX2 Channel N
7:4	R/W	0xE	TXCHE_MIX_RXCH1 RX1 Channel NUM to TXDIF Channel E N: TXDIF Channel E MIX RX1 Channel N
3:0	R/W	0xE	TXCHE_MIX_RXCH0 RX0 Channel NUM to TXDIF Channel E N: TXDIF Channel E MIX RX0 Channel N

7.1.7.45. AHUB DAM Volume Control 0(Default Value: 0x0111_0111)

Offset: 0x0A50 + n*0x0080(n=0,1)			Register Name: DAM_VOL_CTRL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x1	TXCH1_GAIN_RXCH2 RX2 Channel NUM to TXDIF Channel 1 Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
23:20	R/W	0x1	TXCH1_GAIN_RXCH1 RX1 Channel NUM to TXDIF Channel 1 Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
19:16	R/W	0x1	TXCH1_GAIN_RXCH0 RX0 Channel NUM to TXDIF Channel 1 Gain 0000: Mute 0001: 0dB 0010: -6dB

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			0100:-12dB Others: Reserved
15:12	/	/	/
11:8	R/W	0x1	TXCH0_GAIN_RXCH2 RX2 Channel NUM to TXDIF Channel 0 Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
7:4	R/W	0x1	TXCH0_GAIN_RXCH1 RX1 Channel NUM to TXDIF Channel 0 Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
3:0	R/W	0x1	TXCH0_GAIN_RXCH0 RX0 Channel NUM to TXDIF Channel 0 Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved

7.1.7.46. AHUB DAM Volume Control 1(Default Value: 0x0111_0111)

Offset: 0x0A54 + n*0x0080(n=0,1)			**Register Name: DAM_VOL_CTRL1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x1	TXCH3_GAIN_RXCH2 RX2 Channel NUM to TXDIF Channel 3 Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
23:20	R/W	0x1	TXCH3_GAIN_RXCH1 RX1 Channel NUM to TXDIF Channel 3 Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved

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19:16	R/W	0x1	TXCH3_GAIN_RXCH0 RX0 Channel NUM to TXDIF Channel 3 Gain 0000: Mute 0001: 0dB 0010: -6dB 0100: -12dB Others: Reserved
15:12	/	/	/
11:8	R/W	0x1	TXCH2_GAIN_RXCH2 RX2 Channel NUM to TXDIF Channel 2 Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
7:4	R/W	0x1	TXCH2_GAIN_RXCH1 RX1 Channel NUM to TXDIF Channel 2 Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
3:0	R/W	0x1	TXCH2_GAIN_RXCH0 RX0 Channel NUM to TXDIF Channel 2 Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved

7.1.7.47. AHUB DAM Volume Control 2(Default Value: 0x0111_0111)

Offset: 0x0A58 + n*0x0080(n=0,1)			**Register Name: DAM_VOL_CTRL2**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x1	TXCH5_GAIN_RXCH2 RX2 Channel NUM to TXDIF Channel 5 Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
23:20	R/W	0x1	TXCH5_GAIN_RXCH1 RX1 Channel NUM to TXDIF Channel 5 Gain

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			0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
19:16	R/W	0x1	TXCH5_GAIN_RXCH0 RX0 Channel NUM to TXDIF Channel 5 Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
15:12	/	/	/
11:8	R/W	0x1	TXCH4_GAIN_RXCH2 RX2 Channel NUM to TXDIF Channel 4 Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
7:4	R/W	0x1	TXCH4_GAIN_RXCH1 RX1 Channel NUM to TXDIF Channel 4 Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
3:0	R/W	0x1	TXCH4_GAIN_RXCH0 RX0 Channel NUM to TXDIF Channel 4 Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved

7.1.7.48. AHUB DAM Volume Control 3(Default Value: 0x0111_0111)

Offset: 0x0A5C + n*0x0080(n=0,1)			Register Name: DAM_VOL_CTRL3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x1	TXCH7_GAIN_RXCH2 RX2 Channel NUM to TXDIF Channel 7 Gain 0000: Mute 0001: 0dB

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			0010: -6dB 0100:-12dB Others: Reserved
23:20	R/W	0x1	TXCH7_GAIN_RXCH1 RX1 Channel NUM to TXDIF Channel 7 Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
19:16	R/W	0x1	TXCH7_GAIN_RXCH0 RX0 Channel NUM to TXDIF Channel 7 Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
15:12	/	/	/
11:8	R/W	0x1	TXCH6_GAIN_RXCH2 RX2 Channel NUM to TXDIF Channel 6 Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
7:4	R/W	0x1	TXCH6_GAIN_RXCH1 RX1 Channel NUM to TXDIF Channel 6 Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
3:0	R/W	0x1	TXCH6_GAIN_RXCH0 RX0 Channel NUM to TXDIF Channel 6 Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved

7.1.7.49. AHUB DAM Volume Control 4(Default Value: 0x0111_0111)

Offset: 0x0A60 + n*0x0080(n=0,1)			**Register Name: DAM_VOL_CTRL4**
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:28	/	/	/
27:24	R/W	0x1	TXCH9_GAIN_RXCH2 RX2 Channel NUM to TXDIF Channel 9 Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
23:20	R/W	0x1	TXCH9_GAIN_RXCH1 RX1 Channel NUM to TXDIF Channel 9 Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
19:16	R/W	0x1	TXCH9_GAIN_RXCH0 RX0 Channel NUM to TXDIF Channel 9 Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
15:12	/	/	/
11:8	R/W	0x1	TXCH8_GAIN_RXCH2 RX2 Channel NUM to TXDIF Channel 8 Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
7:4	R/W	0x1	TXCH8_GAIN_RXCH1 RX1 Channel NUM to TXDIF Channel 8 Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
3:0	R/W	0x1	TXCH8_GAIN_RXCH0 RX0 Channel NUM to TXDIF Channel 8 Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved

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7.1.7.50. AHUB DAM Volume Control 5(Default Value: 0x0111_0111)

Offset: 0x0A64 + n*0x0080(n=0,1)			Register Name: DAM_VOL_CTRL5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x1	TXCHB_GAIN_RXCH2 RX2 Channel NUM to TXDIF Channel B Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
23:20	R/W	0x1	TXCHB_GAIN_RXCH1 RX1 Channel NUM to TXDIF Channel B Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
19:16	R/W	0x1	TXCHB_GAIN_RXCH0 RX0 Channel NUM to TXDIF Channel B Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
15:12	/	/	/
11:8	R/W	0x1	TXCHA_GAIN_RXCH2 RX2 Channel NUM to TXDIF Channel A Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
7:4	R/W	0x1	TXCHA_GAIN_RXCH1 RX1 Channel NUM to TXDIF Channel A Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
3:0	R/W	0x1	TXCHA_GAIN_RXCH0 RX0 Channel NUM to TXDIF Channel A Gain 0000: Mute 0001: 0dB

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			0010: -6dB 0100:-12dB Others: Reserved

7.1.7.51. AHUB DAM Volume Control 6(Default Value: 0x0111_0111)

Offset: 0x0A68 + n*0x0080(n=0,1)			Register Name: DAM_VOL_CTRL6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x1	TXCHD_GAIN_RXCH2 RX2 Channel NUM to TXDIF Channel D Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
23:20	R/W	0x1	TXCHD_GAIN_RXCH1 RX1 Channel NUM to TXDIF Channel D Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
19:16	R/W	0x1	TXCHD_GAIN_RXCH0 RX0 Channel NUM to TXDIF Channel D Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
15:12	/	/	/
11:8	R/W	0x1	TXCHC_GAIN_RXCH2 RX2 Channel NUM to TXDIF Channel C Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
7:4	R/W	0x1	TXCHC_GAIN_RXCH1 RX1 Channel NUM to TXDIF Channel C Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB

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			Others: Reserved
3:0	R/W	0x1	TXCHC_GAIN_RXCH0 RX0 Channel NUM to TXDIF Channel C Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved

7.1.7.52. AHUB DAM Volume Control 7(Default Value: 0x0111_0111)

Offset: 0x0A6C + n*0x0080(n=0,1)			Register Name: DAM_VOL_CTRL7
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x1	TXCHF_GAIN_RXCH2 RX2 Channel NUM to TXDIF Channel F Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
23:20	R/W	0x1	TXCHF_GAIN_RXCH1 RX1 Channel NUM to TXDIF Channel F Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
19:16	R/W	0x1	TXCHF_GAIN_RXCH0 RX0 Channel NUM to TXDIF Channel F Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
15:12	/	/	/
11:8	R/W	0x1	TXCHE_GAIN_RXCH2 RX2 Channel NUM to TXDIF Channel E Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
7:4	R/W	0x1	TXCHE_GAIN_RXCH1

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			RX1 Channel NUM to TXDIF Channel E Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved
3:0	R/W	0x1	TXCHE_GAIN_RXCH0 RX0 Channel NUM to TXDIF Channel E Gain 0000: Mute 0001: 0dB 0010: -6dB 0100:-12dB Others: Reserved

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7.2. I2S/PCM

7.2.1. Overview

The I2S/PCM Controller is designed to transfer streaming audio-data between the system memory and the codec chip. The controller supports standard I2S format, Left-justified Mode format, Right-justified Mode format, PCM Mode format and TDM Mode format.

Features:

- Compliant with standard Philips Inter-IC sound (I2S) bus specification
- Compliant with Left-justified, Right-justified, PCM mode, and TDM (Time Division Multiplexing) format
- Supports full-duplex synchronous work mode
- Supports Master/Slave mode
- Supports adjustable interface voltage
- Supports clock up to 24.576MHz
- Supports adjustable audio sample resolution from 8-bit to 32-bit
- Supports up to 16 channel(fs = 48kHz) which has adjustable width from 8-bit to 32-bit
- Supports sample rate from 8kHz to 384kHz(CHAN = 2)
- Supports 8-bit u-law and 8-bit A-law companded sample
- One 128 depth x 32-bit width TXFIFO for data transmit, one 64 depth x 32-bit width RXFIFO for data receive
- Support programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Programmable FIFO thresholds
- Interrupt and DMA Support
- Supports loop back mode for test

7.2.2. Block Diagram

The block diagram of I2S/PCM interface is shown below.

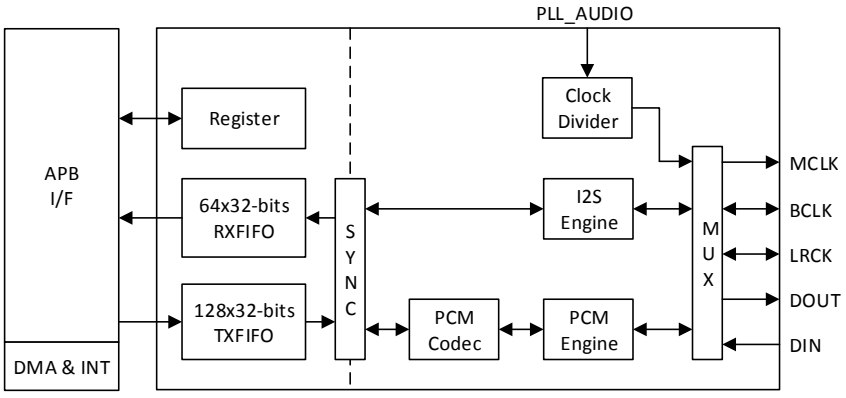


Figure 7-12. I2S/PCM Interface System Block Diagram

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7.2.3. Operations and Functional Descriptions

7.2.3.1. External Signals

Table 7-3 describes the external signals of I2S/PCM interface. SYNC and CLK are bidirectional I/O, when I2S/PCM interface is configured as Master device, SYNC and CLK is output pin; when I2S/PCM interface is configured as slave device, SYNC and CLK is input pin. MCLK is an output pin for external device. DOUT is always the serial data output pin, and DIN is the serial data input. For information about General Purpose I/O port, see Port Controller(CPUX-PORT).

Table 7-3. I2S/PCM External Signals

Signal Name	Description	Type
PCM0_MCLK	I2S/PCM 0 Master Clock	O
PCM0_CLK	I2S/PCM 0 Sample Rate Serial Clock	I/O
PCM0_SYNC	I2S/PCM 0 Sample Rate Left and Right Channel Select Clock/Sync	I/O
PCM0_DIN	I2S/PCM 0 Serial Data Input	I
PCM0_DOUT	I2S/PCM 0 Serial Data Output	O
PCM2_MCLK	I2S/PCM 2 Master Clock	O
PCM2_CLK	I2S/PCM 2 Sample Rate Serial Clock	I/O
PCM2_SYNC	I2S/PCM 2 Sample Rate Left and Right Channel Select Clock/Sync	I/O
PCM2_DIN	I2S/PCM 2 Serial Data Input	I
PCM2_DOUT	I2S/PCM 2 Serial Data Output	O

7.2.3.2. Clock Sources

Table 7-4 describes the clock sources for I2S/PCM. Users can see **Chapter 3.3.CCU** for clock setting, configuration and gating information.

Table 7-4. I2S/PCM Clock Sources

Clock Name	Description
PLL_AUDIO	24.576 MHz or 22.5792 MHz generated by PLL_AUDIO to produce 48 kHz or 44.1 kHz serial frequency

7.2.3.3. Timing Diagram

The I2S/PCM supports standard I2S mode,Left-justified I2S mode,Right-justified I2S mode,PCM mode and TDM mode. Software can select any modes by setting the **I2S/PCM Control Register**.Figure 7-13 to Figure 7-17 describe the waveforms for LRCK,BCLK and DOUT,DIN.

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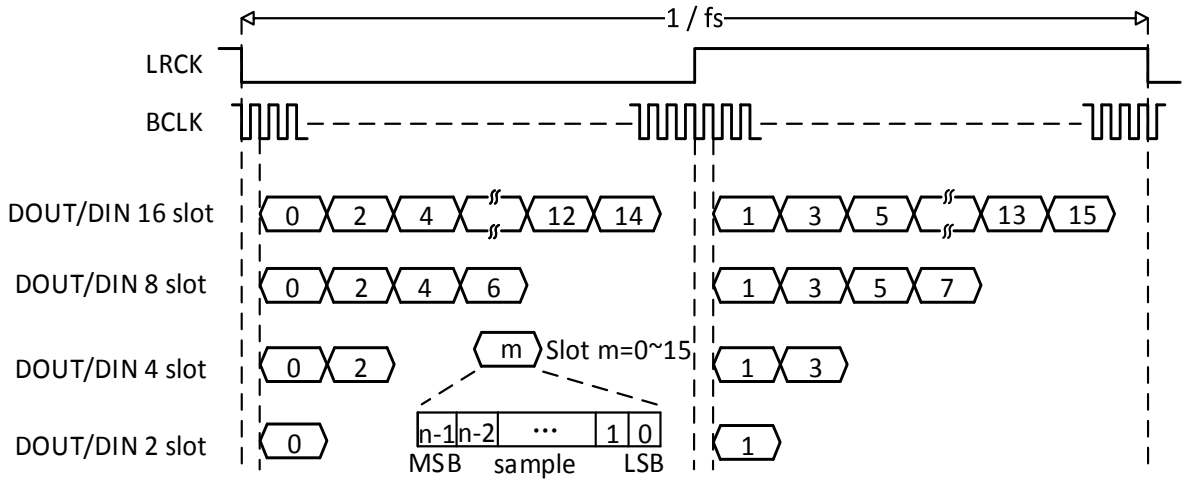


Figure 7-13. I2S/TDM-I2S Mode Timing

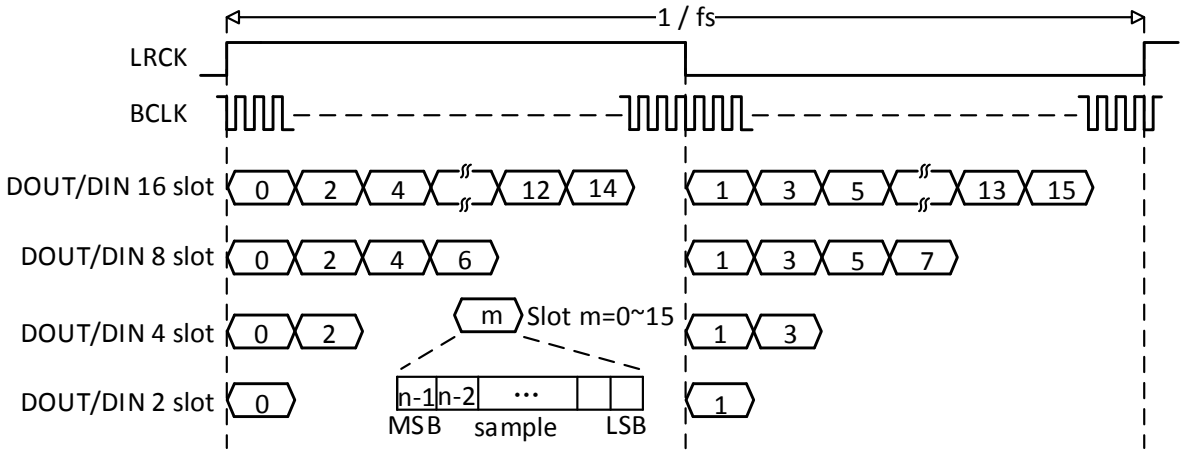


Figure 7-14. Left-Justified/TDM-Left Mode Timing

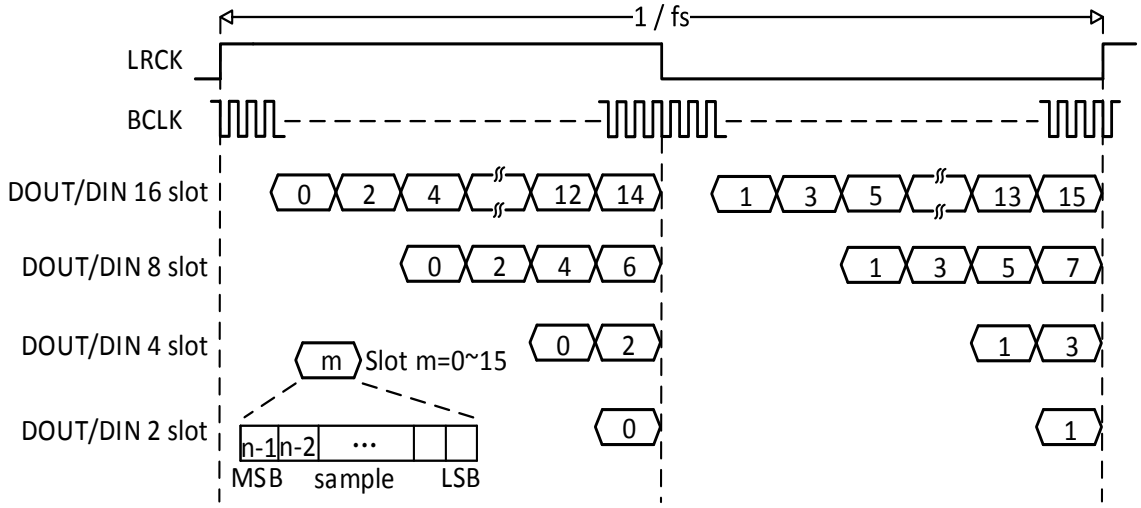


Figure 7-15. Right-Justified/TDM-Right Mode Timing

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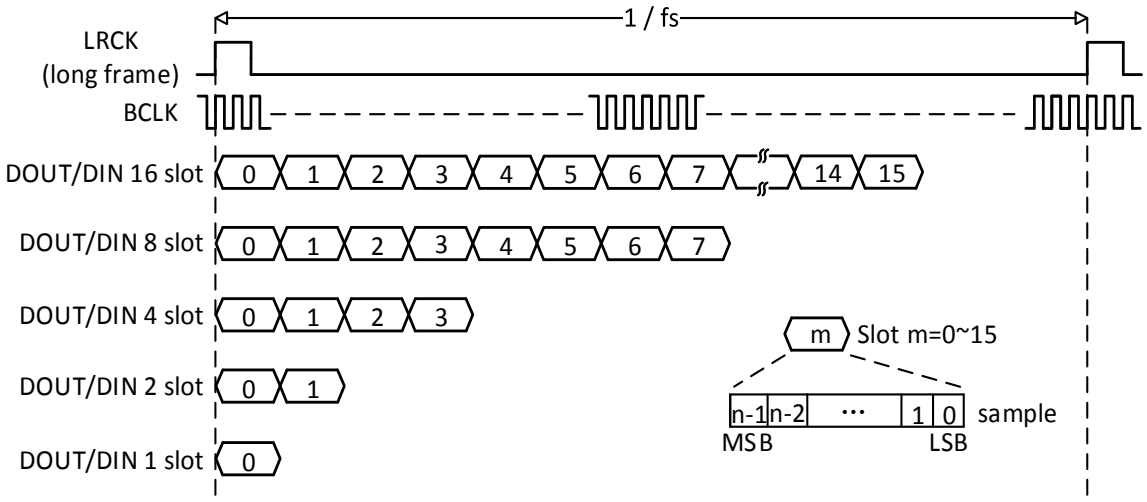


Figure 7-16. PCM Mode Timing (long frame)

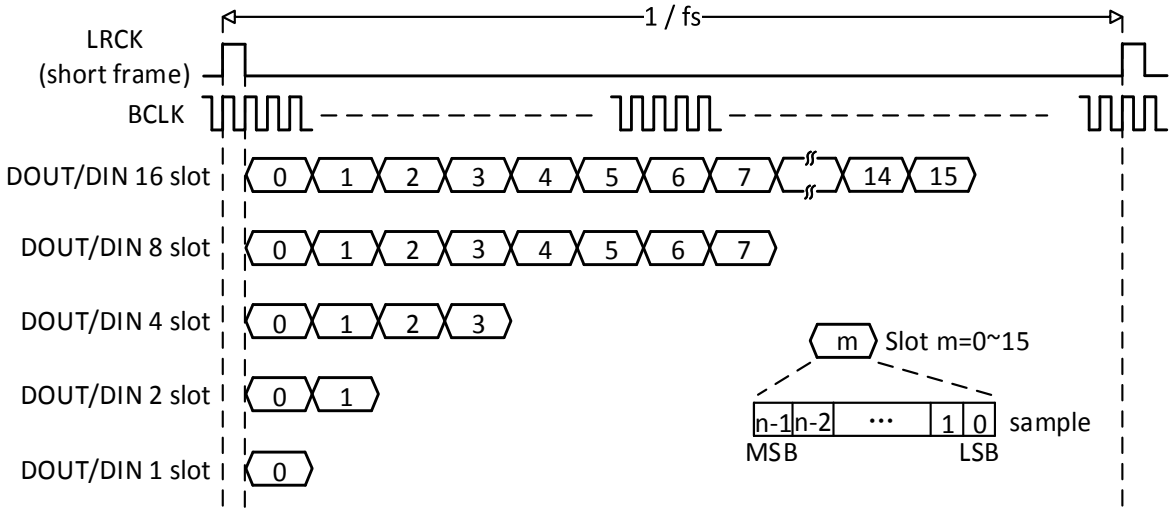


Figure 7-17. PCM Mode Timing (short frame)

7.2.3.4. Operation Modes

The software operation of the I2S/PCM is divided into five steps: system setup, I2S/PCM initialization, the channel setup, DMA setup and Enable/Disable module. These five steps are described in detail in the following sections.

(1). System setup and I2S/PCM initialization

The clock source for the I2S/PCM should be followed. At first you must disable the PLL_AUDIO through the **PLL_ENABLE** bit of **PLL_AUDIO_CTRL_REG** in the CCU. The second step, you must set up the frequency of the PLL_AUDIO in the **PLL_AUDIO_CTRL_REG**. After that, you must open the I2S/PCM gating through the **I2S/PCM_CLK_REG** when you checkout that the LOCK bit of **PLL_AUDIO_CTRL_REG** becomes to 1. At last, you must reset and open the I2S/PCM bus gating in the **CCU_I2S_BGR_REG**.

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After the system setup, the register of I2S/PCM can be setup. At first, you should initialization the I2S/PCM. You should close the **Globe Enable** bit(I2S/PCM_CTL[0]) , **Transmitter Block Enable** bit(I2S/PCM_CTL[2]) and **Receiver Block Enable** bit(I2S/PCM_CTL[1]) by writing 0 to it. After that, you must clear the TX/RX FIFO by writing 0 to the bit[25:24] of **I2S/PCM_FCTL**. At last, you can clear the TX FIFO and RX FIFO counter by writing 0 to **I2S/PCM_TXCNT** and **I2S/PCM_RXCNT**.

(2). Channel setup and DMA setup

First, you can setup the I2S/PCM of mater and slave. The configuration can be referred to the protocol of I2S/PCM. Then, you can set up the translation mode, the sample resolution, the wide of slot, the channel slot number and the trigger level and so on. The setup of register can be found in the specification.

The I2S/PCM supports two methods to transfer the data. The most common way is DMA, the setup of DMA can be found in the **DMA**. In this module, you just enable the DRQ.

(3). Enable and Disable I2S/PCM

To enable the function, you can enable TX/RX by writing **the I2S/PCM_CT**L[2:1]. After that, you must enable I2S/PCM by writing the **Globe Enable** bit to 1 in the I2S/PCM_CTL. Write the **Globe Enable** to 0 to disable I2S/PCM.

7.2.4. Register List

Module Name	Base Address
I2S/PCM0	0x05090000
I2S/PCM1(used for HDMI)	0x05091000
I2S/PCM2	0x05092000
I2S/PCM3(used for Audio Codec)	0x0508F000

Register Name	Offset	Description
I2S/PCM_CTL	0x0000	I2S/PCM Control Register
I2S/PCM_FMT0	0x0004	I2S/PCM Format Register 0
I2S/PCM_FMT1	0x0008	I2S/PCM Format Register 1
I2S/PCM_ISTA	0x000C	I2S/PCM Interrupt Status Register
I2S/PCM_RXFIFO	0x0010	I2S/PCM RXFIFO Register
I2S/PCM_FCTL	0x0014	I2S/PCM FIFO Control Register
I2S/PCM_FSTA	0x0018	I2S/PCM FIFO Status Register
I2S/PCM_INT	0x001C	I2S/PCM DMA & Interrupt Control Register
I2S/PCM_TXFIFO	0x0020	I2S/PCM TXFIFO Register
I2S/PCM_CLKD	0x0024	I2S/PCM Clock Divide Register
I2S/PCM_TXCNT	0x0028	I2S/PCM TX Sample Counter Register
I2S/PCM_RXCNT	0x002C	I2S/PCM RX Sample Counter Register

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I2S/PCM_CHCFG	0x0030	I2S/PCM Channel Configuration Register
I2S/PCM_TXCHCFG	0x0034	I2S/PCM TX Channel Configuration Register
I2S/PCM_TXCHMAP0	0x0044	I2S/PCM TX Channel Mapping Register0
I2S/PCM_TXCHMAP1	0x0048	I2S/PCM TX Channel Mapping Register1
I2S/PCM_RXCHSEL	0x0064	I2S/PCM RX Channel Select Register
I2S/PCM_RXCHMAP0	0x0068	I2S/PCM RX Channel Mapping Register0
I2S/PCM_RXCHMAP1	0x006C	I2S/PCM RX Channel Mapping Register1

7.2.5. Register Description

7.2.5.1. I2S/PCM Control Register(Default Value: 0x0006_0000)

Offset: 0x0000			Register Name: I2S/PCM_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0x1	BCLK_OUT 0: Input 1: Output
17	R/W	0x1	LRCK_OUT 0: Input 1: Output
16:9	/	/	/
8	R/W	0x0	DOUT_EN 0: Disable, Hi-Z State 1: Enable
7	/	/	/
6	R/W	0x0	OUT_MUTE 0: Normal Transfer 1: Force DOUT to Output 0
5:4	R/W	0x0	MODE_SEL Mode Selection 00: PCM Mode (offset 0: Long Frame; offset 1: Short Frame) 01: Left Mode (offset 0: LJ Mode; offset 1: I2S Mode) 10: Right-Justified Mode 11: Reserved
3	R/W	0x0	LOOP Loop Back Test 0: Normal Mode 1: Loop Back Test When Set ‘1’ , Connecting the DOUT with the DIN.
2	R/W	0x0	TXEN Transmitter Block Enable 0: Disable

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			1: Enable
1	R/W	0x0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0x0	GEN Globe Enable A disable on this bit overrides any other block or channel enables. 0: Disable 1: Enable

7.2.5.2. I2S/PCM Format Register 0(Default Value: 0x0000_0033)

Offset: 0x0004			Register Name: I2S/PCM_FMT0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	LRCK_WIDTH (Only Apply in PCM Mode) LRCK Width 0: LRCK = 1 BCLK Width (Short Frame) 1: LRCK = 2 BCLK Width (Long Frame)
29:20	/	/	/
19	R/W	0x0	LRCK_POLARITY When Apply in I2S / Left-Justified / Right-Justified Mode: 0: Left Channel When LRCK is Low 1: Left Channel When LRCK is High When Apply in PCM Mode: 0: PCM LRCK Asserted at the Negative Edge 1: PCM LRCK Asserted at the Positive Edge
18	/	/	/
17:8	R/W	0x0	LRCK_PERIOD It is used to program the number of BCLKs per channel of sample frame. This value is interpreted as follow: PCM Mode: Number of BCLKs within (Left + Right) channel width. I2S / Left-Justified / Right-Justified Mode: Number of BCLKs within each individual channel width (Left or Right) . N+1 For example: N = 7: 8 BCLKs width … N = 1023: 1024 BCLKs width
7	R/W	0x0	BCLK_POLARITY 0: Normal Mode, DOUT Drive Data at Negative Edge 1: Invert Mode, DOUT Drive Data at Positive Edge
6:4	R/W	0x3	SR

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			Sample Resolution 000: Reserved 001: 8-bit 010: 12-bit 011: 16-bit 100: 20-bit 101: 24-bit 110: 28-bit 111: 32-bit
3	R/W	0x0	EDGE_TRANSFER 0: DOUT Drive Data and DIN Sample Data at the Different BCLK Edge 1: DOUT Drive Data and DIN Sample Data at the Same BCLK Edge BCLK_POLARITY = 0, EDGE_TRANSFER = 0, DIN Sample Data at Positive Edge; BCLK_POLARITY = 0, EDGE_TRANSFER = 1, DIN Sample Data at Negative Edge; BCLK_POLARITY = 1, EDGE_TRANSFER = 0, DIN Sample Data at Negative Edge; BCLK_POLARITY = 1, EDGE_TRANSFER = 1, DIN Sample Data at Positive Edge.
2:0	R/W	0x3	SW Slot Width Select 000: Reserved 001: 8-bit 010: 12-bit 011: 16-bit 100: 20-bit 101: 24-bit 110: 28-bit 111: 32-bit

7.2.5.3. I2S/PCM Format Register 1(Default Value: 0x0000_0030)

Offset: 0x0008			**Register Name: I2S/PCM_FMT1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	RX MLS MSB/LSB First Select 0: MSB First 1: LSB First
6	R/W	0x0	TX MLS MSB/LSB First Select 0: MSB First 1: LSB First

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5:4	R/W	0x3	SEXT Sign Extend in Slot [Sample Resolution < Slot Width] 00: Zeros or Audio Gain Padding at LSB Position 01: Sign Extension at MSB Position 10: Reserved 11: Transfer 0 after each Sample in each Slot
3:2	R/W	0x0	RX_PDM PCM Data Mode 00: Linear PCM 01: Reserved 10: 8-bit u-law 11: 8-bit A-law
1:0	R/W	0x0	TX_PDM PCM Data Mode 00: Linear PCM 01: Reserved 10: 8-bits u-law 11: 8-bits A-law

7.2.5.4. I2S/PCM Interrupt Status Register(Default Value: 0x0000_0010)

Offset: 0x000C			Register Name: I2S/PCM_ISTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W1C	0x0	TXU_INT TXFIFO Underrun Pending Interrupt 0: No Pending Interrupt 1: TXFIFO Underrun Pending Interrupt Write ‘1’ to clear this interrupt.
5	R/W1C	0x0	TXO_INT TXFIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: TXFIFO Overrun Pending Interrupt Write ‘1’ to clear this interrupt.
4	R/W1C	0x1	TXE_INT TXFIFO Empty Pending Interrupt 0: No Pending IRQ 1: TXFIFO Empty Pending Interrupt When Data in TXFIFO are Less than TX Trigger Level Write ‘1’ to clear this interrupt or automatic clear if interrupt condition fails.
3	/	/	/
2	R/W1C	0x0	RXU_INT RXFIFO Underrun Pending Interrupt

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			0: No Pending Interrupt 1: RXFIFO Underrun Pending Interrupt Write '1' to clear this interrupt.
1	R/W1C	0x0	RXO_INT RXFIFO Overrun Pending Interrupt 0: No Pending IRQ 1: RXFIFO Overrun Pending IRQ Write '1' to clear this interrupt.
0	R/W1C	0x0	RXA_INT RXFIFO Data Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ When Data in RXFIFO are More than RX Trigger Level Write '1' to clear this interrupt or automatic clear if interrupt condition fails.

7.2.5.5. I2S/PCM RXFIFO Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: I2S/PCM_RXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	RX_DATA RX Sample Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

7.2.5.6. I2S/PCM FIFO Control Register(Default Value: 0x0004_00F0)

Offset: 0x0014			Register Name: I2S/PCM_FCTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HUB_EN Audio Hub Enable 0 : Disable 1 : Enable
30:26	/	/	/
25	R/W1C	0x0	FTX Write '1' to flush TXFIFO, self clear to '0'.
24	R/W1C	0x0	FRX Write '1' to flush RXFIFO, self clear to '0'.
23:19	/	/	/
18:12	R/W	0x40	TXTL TXFIFO Empty Trigger Level Interrupt and DMA request trigger level for TXFIFO normal condition. Trigger Level = TXTL

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11:10	/	/	/
9:4	R/W	0xF	RXTL RXFIFO Trigger Level Interrupt and DMA request trigger level for RXFIFO normal condition. Trigger Level = RXTL + 1
3	/	/	/
2	R/W	0x0	TXIM TXFIFO Input Mode (Mode 0, 1) 0: Valid data at the MSB of TXFIFO register 1: Valid data at the LSB of TXFIFO register Example for 20-bit Transmitted Audio Sample: Mode 0: TXFIFO[31:0] = {APB_WDATA[31:12], 12'h0} Mode 1: TXFIFO[31:0] = {APB_WDATA[19:0], 12'h0}
1:0	R/W	0x0	RXOM RXFIFO Output Mode (Mode 0, 1, 2, 3) 00: Expanding '0' at LSB of RXFIFO register 01: Expanding received sample sign bit at MSB of RXFIFO register 10: Truncating received samples at high half-word of RXFIFO register and low half-word of RXFIFO register is filled by '0' 11: Truncating received samples at low half-word of RXFIFO register and high half-word of RXFIFO register is expanded by its sign bit Example for 20-bit Received Audio Sample: Mode 0: APB_RDATA[31:0] = {RXFIFO[31:12], 12'h0} Mode 1: APB_RDATA[31:0] = {12{RXFIFO[31]}, RXFIFO[31:12]} Mode 2: APB_RDATA [31:0] = {RXFIFO[31:16], 16'h0} Mode 3: APB_RDATA[31:0] = {16{RXFIFO[31], RXFIFO[31:16]}

7.2.5.7. I2S/PCM FIFO Status Register(Default Value: 0x1080_0000)

Offset: 0x0018			Register Name: I2S/PCM_FSTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R	0x1	TXE TXFIFO Empty 0: No Room for New Sample in TXFIFO 1: More than One Room for New Sample in TXFIFO (>= 1 Word)
27:24	/	/	/
23:16	R	0x80	TXE_CNT TXFIFO Empty Space Word Counter
15:9	/	/	/
8	R	0x0	RXA RXFIFO Available 0: No Available Data in RXFIFO 1: More than One Sample in RXFIFO (>= 1 Word)

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7	/	/	/
6:0	R	0x0	RXA_CNT RXFIFO Available Sample Word Counter

7.2.5.8. I2S/PCM DMA & Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: I2S/PCM_INT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TX_DRQ TXFIFO Empty DRQ Enable 0: Disable 1: Enable
6	R/W	0x0	TXUI_EN TXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TXOI_EN TXFIFO Overrun Interrupt Enable 0: Disable 1: Enable When set to '1', an interrupt happens when writing new audio data if TXFIFO is full.
4	R/W	0x0	TXEI_EN TXFIFO Empty Interrupt Enable 0: Disable 1: Enable
3	R/W	0x0	RX_DRQ RXFIFO Data Available DRQ Enable 0: Disable 1: Enable When set to '1', RXFIFO DMA request line is asserted if data is available in RXFIFO.
2	R/W	0x0	RXUI_EN RXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	RXOI_EN RXFIFO Overrun Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RXAI_EN RXFIFO Data Available Interrupt Enable 0: Disable

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			1: Enable

7.2.5.9. I2S/PCM TXFIFO Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: I2S/PCM_TXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	W	0x0	TX_DATA TX Sample Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.

7.2.5.10. I2S/PCM Clock Divide Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: I2S/PCM_CLKD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	MCLKO_EN 0: Disable MCLK Output 1: Enable MCLK Output **NOTE** **Whether in Slave or Master mode, when this bit is set to '1', MCLK should be output.**
7:4	R/W	0x0	BCLKDIV BCLK Divide Ratio from PLL_AUDIO 0000: Reserved 0001: Divide by 1 0010: Divide by 2 0011: Divide by 4 0100: Divide by 6 0101: Divide by 8 0110: Divide by 12 0111: Divide by 16 1000: Divide by 24 1001: Divide by 32 1010: Divide by 48 1011: Divide by 64 1100: Divide by 96 1101: Divide by 128 1110: Divide by 176 1111: Divide by 192
3:0	R/W	0x0	MCLKDIV

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			MCLK Divide Ratio from PLL_AUDIO 0000: Reserved 0001: Divide by 1 0010: Divide by 2 0011: Divide by 4 0100: Divide by 6 0101: Divide by 8 0110: Divide by 12 0111: Divide by 16 1000: Divide by 24 1001: Divide by 32 1010: Divide by 48 1011: Divide by 64 1100: Divide by 96 1101: Divide by 128 1110: Divide by 176 1111: Divide by 192

7.2.5.11. I2S/PCM TX Counter Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: I2S/PCM_TXCNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this initial value.

7.2.5.12. I2S/PCM RX Counter Register(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: I2S/PCM_RXCNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this initial value.

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7.2.5.13. I2S/PCM Channel Configuration Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: I2S/PCM_CHCFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	TX_SLOT_HIZ 0: Normal mode for the last half cycle of BCLK in the Slot 1: Turn to Hi-Z State for the last half cycle of BCLK in the Slot
8	R/W	0x0	TX_STATE 0: Transfer level 0 When Not Transferring Slot 1: Turn to Hi-Z State (TDM) When Not Transferring Slot
7:4	R/W	0x0	RX_SLOT_NUM RX Channel/Slot number between CPU/DMA and RXFIFO 0000: 1 Channel or Slot ... 0111: 8 Channels or Slots 1000: 9 Channels or Slots ... 1111:16 Channels or Slots
3:0	R/W	0x0	TX_SLOT_NUM TX Channel/Slot number between CPU/DMA and TXFIFO 0000: 1 Channel or Slot ... 0111: 8 Channels or Slots 1000: 9 Channels or Slots ... 1111:16 Channels or Slots

7.2.5.14. I2S/PCM TX Channel Select Register(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: I2S/PCM_TXCHSEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x0	TX_OFFSET TX offset Tune, TX Data offset to LRCK 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	TX_CHSEL TX Channel (Slot) number select for each output 0000: 1 Channel / Slot … 0111: 8 Channels / Slots 1000: 9 Channels / Slots ...

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			1111: 16 Channels / Slots
15:0	R/W	0x0	TX_CHEN TX Channel (Slot) Enable, bit[15:0] refer to Slot [15:0]. When one or more Slot(s) is(are) disabled, the affected Slot(s) is(are) set to the disable state. 0: Disable 1: Enable

7.2.5.15. I2S/PCM TX Channel Mapping Register 0(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: I2S/PCM_TXCHMAP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	TX_CH15_MAP TX Channel 15 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
27:24	R/W	0x0	TX_CH14_MAP TX Channel 14 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th sample
23:20	R/W	0x0	TX_CH13_MAP TX Channel 13 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
19:16	R/W	0x0	TX_CH12_MAP TX Channel 12 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample

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15:12	R/W	0x0	TX_CH11_MAP TX Channel 11 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th sample
11:8	R/W	0x0	TX_CH10_MAP TX Channel 10 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
7:4	R/W	0x0	TX_CH9_MAP TX Channel 9 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
3:0	R/W	0x0	TX_CH8_MAP TX Channel 8 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample

7.2.5.16. I2S/PCM TX Channel Mapping Register 1(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: I2S/PCM_TXCHMAP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	TX_CH7_MAP TX Channel 7 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ...

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			1111: 16th Sample
27:24	R/W	0x0	TX_CH6_MAP TX Channel 6 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
23:20	R/W	0x0	TX_CH5_MAP TX Channel 5 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
19:16	R/W	0x0	TX_CH4_MAP TX Channel 4 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
15:12	R/W	0x0	TX_CH3_MAP TX Channel 3 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
11:8	R/W	0x0	TX_CH2_MAP TX Channel 2 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
7:4	R/W	0x0	TX_CH1_MAP TX Channel 1 Mapping 0000: 1st Sample ...

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			0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
3:0	R/W	0x0	TX_CH0_MAP TX Channel 0 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample

7.2.5.17. I2S/PCM RX Channel Select Register(Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: I2S/PCM_RXCHSEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x0	RX_OFFSET RX offset Tune, RX Data offset to LRCK 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	RX_CHSEL RX Channel (Slot) Number Select for Input 0000: 1 Channel / Slot ... 0111: 8 Channels / Slots 1000: 9 Channels / Slots ... 1111: 16 Channels / Slots
15:0	/	/	/

7.2.5.18. I2S/PCM RX Channel Mapping Register0(Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: I2S/PCM_RXCHMAP0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	RX_CH15_MAP RX Channel 15 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ...

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			1111: 16th Sample
27:24	R/W	0x0	RX_CH14_MAP RX Channel 14 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
23:20	R/W	0x0	RX_CH13_MAP RX Channel 13 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
19:16	R/W	0x0	RX_CH12_MAP RX Channel 12 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
15:12	R/W	0x0	RX_CH11_MAP RX Channel 11 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
11:8	R/W	0x0	RX_CH10_MAP RX Channel 10 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
7:4	R/W	0x0	RX_CH9_MAP RX Channel 9 Mapping 0000: 1st Sample ...

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			0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
3:0	R/W	0x0	RX_CH8_MAP RX Channel 8 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample

7.2.5.19. I2S/PCM RX Channel Mapping Register 1(Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: I2S/PCM_RXCHMAP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	RX_CH7_MAP RX Channel 7 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
27:24	R/W	0x0	RX_CH6_MAP RX Channel 6 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
23:20	R/W	0x0	RX_CH5_MAP RX Channel 5 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
19:16	R/W	0x0	RX_CH4_MAP RX Channel 4 Mapping 0000: 1st Sample

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			... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
15:12	R/W	0x0	RX_CH3_MAP RX Channel 3 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
11:8	R/W	0x0	RX_CH2_MAP RX Channel 2 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
7:4	R/W	0x0	RX_CH1_MAP RX Channel 1 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
3:0	R/W	0x0	RX_CH0_MAP RX Channel 0 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample

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7.3. One Wire Audio(OWA)

7.3.1. Overview

The OWA(One Wire Audio) provides a serial bus interface for audio data between system. This interface is widely used for consumer audio.

Features:

- IEC-60958 transmitter functionality
- Compliance with S/PDIF Interface
- Supports channel status insertion for the transmitter
- Supports channel status capture for the receiver
- Hardware parity generation on the transmitter
- Hardware parity checking on the receiver
- One 128×24bits TXFIFO and 64x24bits RXFIFO for audio data transfer
- Programmable FIFO thresholds
- Interrupt and DMA support
- Supports 16-bit,20-bit,24-bit data formats

7.3.2. Block Diagram

The OWA block diagram is shown below.

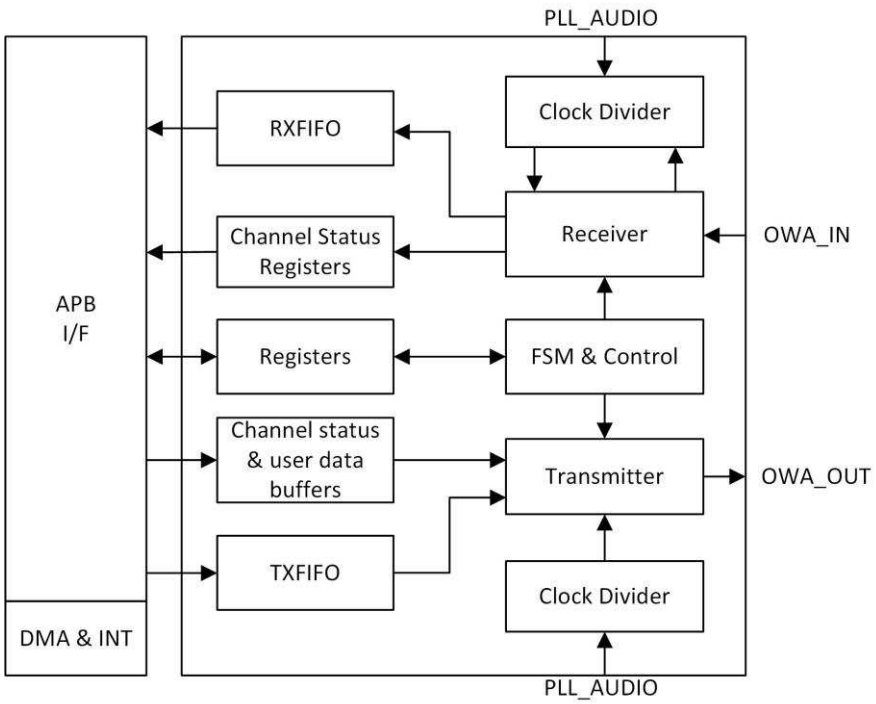


Figure 7-18. OWA Block Diagram

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7.3.3. Operations and Functional Descriptions

7.3.3.1. External Signals

OWA is a Biphase-Mark Encoding Digital Audio Transfer protocol. In this protocol, the CLK signal and data signals is transfer in the same line. Table 7-5 describes the external signals of OWA. OWA_DOUT is output pin for output CLK and DATA, and OWA_DIN is input pin for input CLK and DATA.

Table 7-5. OWA External Signals

Signal Name	Description	Type
OWA_OUT	OWA output	O
OWA_IN	OWA input	I
OWA_MCLK	OWA Master Clock	O

7.3.3.2. Clock Sources

Table 7-6 describes the clock sources for OWA. Users can see **Chapter 3.3.CCU** for clock setting, configuration and gating information.

Table 7-6. OWA Clock Sources

Clock Name	Description
PLL_AUDIO	24.576 MHz or 22.5792 MHz generated by PLL_AUDIO to produce 48 kHz or 44.1 kHz serial frequency

7.3.3.3. Biphase-Mark Code (BMC)

In OWA format, the digital signal is coded using the biphase-mark code (BMC). The clock, frame, and data are embedded in only one signal—the data pin. In the BMC system, each data bit is encoded into two logical states (00, 01, 10, or 11) at the pin.Figure 7-19 and Table 7-7 show how data is encoded to the BMC format.

As shown in Figure 7-19, the frequency of the clock is twice the data bit rate. In addition, the clock is always programmed to 128xfs, where fs is the sample rate. The device receiving in OWA format can recover the clock and frame information from the BMC signal.

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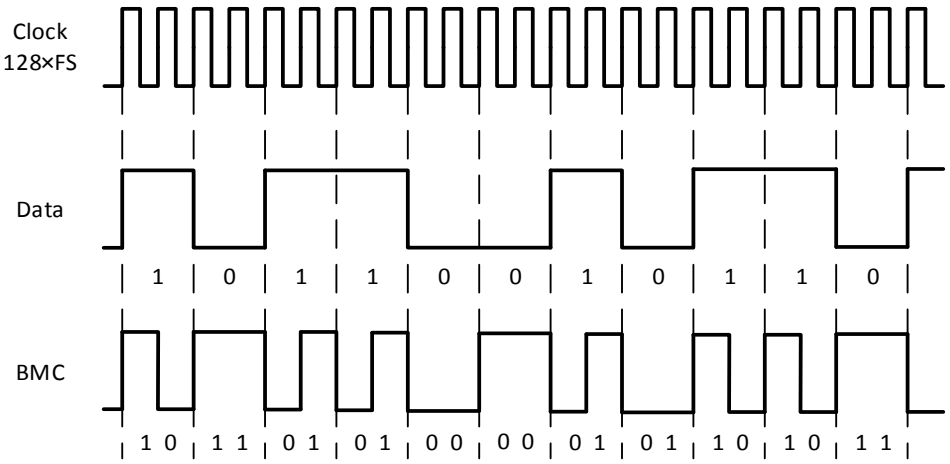


Figure 7-19. OWA Biphase-Mark Code

Table 7-7. Biphase-Mark Encoder

Data	Previous State	BMC
0	0	11
0	1	00
1	0	10
1	1	01

7.3.3.4. OWA Transmit Format

The OWA supports Digital Audio Data transfer out and receive in. And it supports full-duplex synchronous work mode. Software can set the work mode by the OWA Control Register.

Every audio sample transmitted in a subframe consists 32-bit, numbered from 0 to 31. Figure 7-20 shows a subframe.The OWA supports the transfer of digital audio data. And it supports full-duplex synchronous work mode.

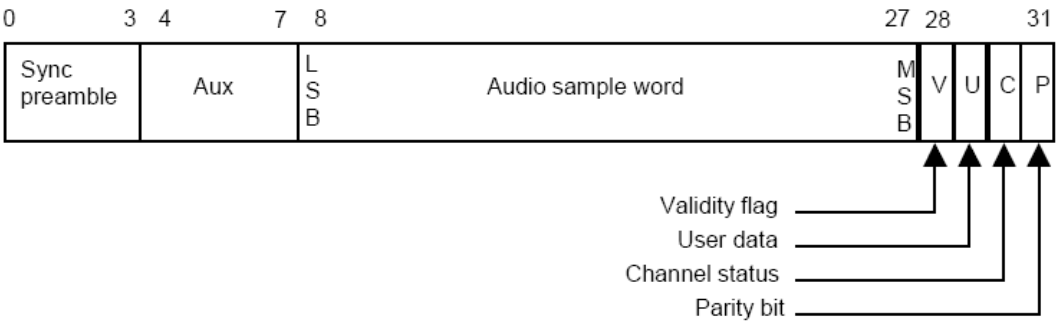


Figure 7-20. OWA Sub-Frame Format

Bit 0-3 carry one of the four permitted preambles to signify the type of audio sample in the current subframe. The preamble is not encoded in BMC format, and therefore the preamble code can contain more than two consecutive 0 or 1 logical states in a row. See Table 1-4.

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Bit 4-27 carry the audio sample word in linear 2s-complement representation. The most-significant

bit (MSB) is carried by bit 27. When a 24-bit coding range is used, the least-significant bit (LSB) is in bit 4. When a 20-bit coding range is used, bit 8-27 carry the audio sample word with the LSB in bit 8. bit 4-7 may be used for other applications and are designated auxiliary sample bits.

If the source provides fewer bits than the interface allows (either 20 or 24), the unused LSBs are set to logical 0. For a nonlinear PCM audio application or a data application, the main data field may carry any other information.

Bit 28 carries the validity bit (V) associated with the main data field in the subframe.

Bit 29 carries the user data channel (U) associated with the main data field in the subframe.

Bit 30 carries the channel status information (C) associated with the main data field in the subframe. The channel status indicates if the data in the subframe is digital audio or some other type of data.

Bit 31 carries a parity bit (P) such that bit 4-31 carry an even number of 1s and an even number of 0s (even parity). As shown in Table 7-8, the preambles (bit 0-3) are also defined with even parity.

Table 7-8. Preamble Codes

Preamble Code	Previous Logical State	Logical State	Description
B(or Z)	0	1110 1000	Start of a block and subframe 1
M(or X)	0	1110 0010	Subframe 1
W(or Y)	0	1110 0100	Subframe 2

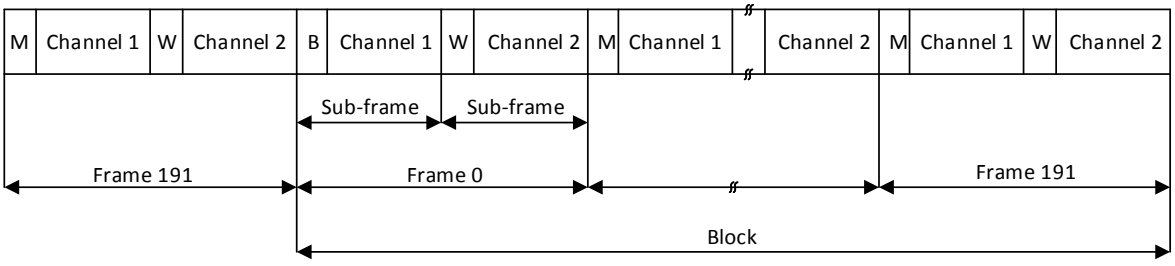


Figure 7-21. OWA Frame/Block Format

7.3.3.5. Operation Modes

The software operation of the OWA is divided into five steps: system setup, OWA initialization, the channel setup, DMA setup and enable/disable module. These five steps are described in detail in the following sections.

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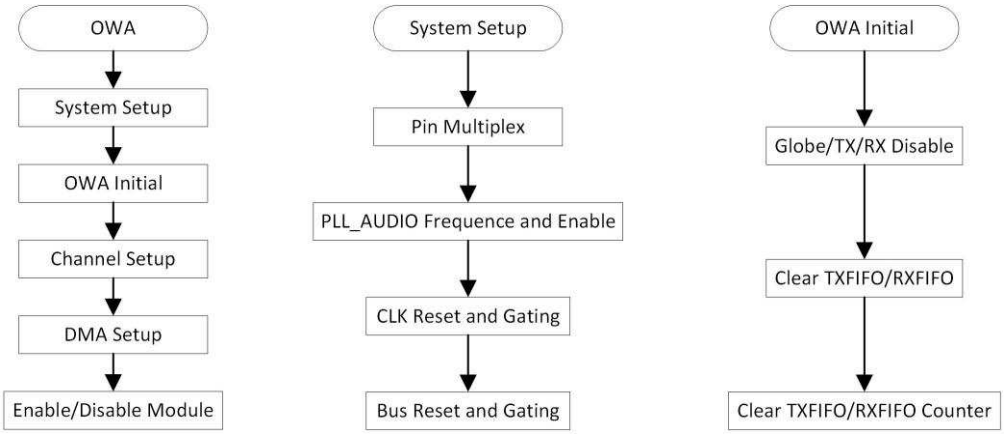


Figure 7-22. OWA Operation Flow

(1) System Setup and OWA Initialization

The first step in the OWA initialization is properly programming the GPIO. Because the OWA port is a multiplex pin. You can find the function in the **Port Controller**.

The clock source for the OWA should be followed. At first you must reset the audio PLL in the **CCU**. The second step, you must setup the frequency of the Audio PLL. After that, you must open the OWA gating. At last, you must open the OWA bus gating.

After the system setup, the register of OWA can be setup. At first, you should reset the OWA by writing 1 to **OWA_CTL**[0] and clear the TX/RX FIFO by writing 1 to **OWA_FCTL**[17:16]. After that you should enable the globe enable bit by writing 1 to **OWA_CTL**[1] and clear the interrupt and TX/RX counter by the **OWA_ISTA** and **OWA_TX_CNT**.

(2) Channel Setup and DMA Setup

The OWA support three methods to transfer the data. The most common way is DMA, the configuration of DMA can be found in the **DMA**. In this module, you just enable the DRQ.

(3) Enable and Disable OWA

To enable the function, you can enable TX by writing the **OWA_TX_CFIG**[31]. After that, you must enable OWA by writing the **GEN** bit to 1 in the **OWA_CTL** register. Writing the **GEN** bit to 0 disable process.

7.3.4. Register List

Module Name	Base Address
OWA	0x05093000

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Register Name	Offset	Description
OWA_GEN_CTL	0x0000	OWA General Control Register
OWA_TX_CFIG	0x0004	OWA TX Configuration Register
OWA_RX_CFIG	0x0008	OWA RX Configuration Register
OWA_ISTA	0x000C	OWA Interrupt Status Register
OWA_RXFIFO	0x0010	OWA RXFIFO Register
OWA_FCTL	0x0014	OWA FIFO Control Register
OWA_FSTA	0x0018	OWA FIFO Status Register
OWA_INT	0x001C	OWA Interrupt Control Register
OWA_TX_FIFO	0x0020	OWA TX FIFO Register
OWA_TX_CNT	0x0024	OWA TX Counter Register
OWA_RX_CNT	0x0028	OWA RX Counter Register
OWA_TX_CHSTA0	0x002C	OWA TX Channel Status Register0
OWA_TX_CHSTA1	0x0030	OWA TX Channel Status Register1
OWA_RXCHSTA0	0x0034	OWA RX Channel Status Register0
OWA_RXCHSTA1	0x0038	OWA RX Channel Status Register1

7.3.5. Register Description

7.3.5.1. OWA General Control Register (Default Value : 0x0000_0080)

Offset: 0x0000			Register Name: OWA_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:5	R/W	0x4	MCLKDIV MCLK Clock Divide Ratio MCLK Divide Ratio from PLL_AUDIO 00000: Divide by 128 00001: Divide by 2 00010: Divide by 4 00011: Divide by 6 00100: Divide by 8 00101: Divide by 10 00110: Divide by 12 00111: Divide by 14 01000: Divide by 16 01001: Divide by 18 01010: Divide by 20 01011: Divide by 22 01100: Divide by 24 …… 11111: Divide by 62
4	/	/	/

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3	R/W	0x0	MCLKEN MCLK Enable 0: Disable 1: Enable
2	R/W	0x0	LOOP Loop Back Test 0: Normal Mode 1: Loop Back Test When set '1', connecting the DOUT with the DIN.
1	R/W	0x0	GEN Global Enable A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable
0	R/W	0x0	RST Reset 0: Normal 1: Reset Self clear to 0.

7.3.5.2. OWA TX Configure Register (Default Value: 0x0000_00F0)

Offset: 0x0004			Register Name: OWA_TX_CFIG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TX_SINGLE_MODE Tx Single Channel Mode 0: Disable 1: Enable
30:18	/	/	/
17	R/W	0x0	ASS Audio Sample Select with TX FIFO Underrun When 0: Sending 0 1: Sending the last audio This bit is only valid in PCM mode
16	R/W	0x0	TX_AUDIO TX Data Type 0: Linear PCM (Valid bit of both sub-frame set to 0) 1: Non-audio(Valid bit of both sub-frame set to 1)
15:9	/	/	/
8:4	R/W	0xF	TX_RATIO TX Clock Divide Ratio Clock divide ratio = TX TATIO +1 Fs= PLL_AUDIO/[(TX_TATIO +1)*64*2]

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3:2	R/W	0x0	TX_SF TX Sample Format 00: 16 bits 01: 20 bits 10: 24 bits 11: Reserved
1	R/W	0x0	TX_CHM CHSTMODE 0: Channel status A&B set to 0 1: Channel status A&B generated form TX_CHSTA
0	R/W	0x0	TXEN 0: Disabled 1: Enabled

7.3.5.3. OWA RX Configure Register (Default Value: 0x0000_00F0)

Offset: 0x0008			Register Name: OWA_RX_CFIG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R	0x0	RX_LOCK_FLAG 0: Unlock 1: Lock
3	R/W	0x0	RX_CHST_SRC 0: RX_CH_STA Register Holds Status from Channel A 1: RX_CH_STA Register Holds Status from Channel B
2	/	/	/
1	R/W	0x0	CHST_CP Channel Status Capture 0: Idle or Capture End 1: Capture Channel Status Start When set to '1', the channel status information is capturing, the bit will clear to '0' after captured.
0	R/W	0x0	RXEN 0: Disabled 1: Enabled

7.3.5.4. OWA Interrupt Status Register (Default Value: 0x0000_0010)

Offset: 0x000C			Register Name: OWA_ISTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W1C	0x0	RX_LOCK_INT 0: No Pending IRQ

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			1: RX lock Pending Interrupt (RX_LOCK_FLAG 0→1) Write '1' to clear this interrupt.
17	R/W1C	0x0	RX_UNLOCK_INT RX Unlock Pending Interrupt 0: No Pending IRQ 1: RX Unlock Pending Interrupt (RX_LOCK_FLAG 1→0) Write '1' to clear this interrupt.
16	R/W1C	0x0	RX_PARERRI_INT RX Parity Error Pending Interrupt 0: No Pending IRQ 1: RX Parity Error Pending Interrupt Write '1' to clear this interrupt.
15:7	/	/	/
6	R/W	0x0	TXU_INT TX FIFO Underrun Pending Interrupt 0: No Pending IRQ 1: FIFO Underrun Pending Interrupt Writing "1" to clear this interrupt.
5	R/W	0x0	TXO_INT TX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending Interrupt Writing "1" to clear this interrupt.
4	R/W	0x1	TXE_INT TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt Writing "1" to clear this interrupt or automatically clear if the interrupt condition fails.
3:2	/	/	/
1	R/W1C	0x0	RXO_INT RXFIFO Overrun Pending Interrupt 0: RXFIFO Overrun Pending Write '1' to clear this interrupt.
0	R/W1C	0x0	RXA_INT RXFIFO Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.

7.3.5.5. OWA RX FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0010	Register Name: OWA_RXFIFO

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Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RX_DATA Host can get one sample by reading this register, the A channel data is first and then the B channel data.

7.3.5.6. OWA FIFO Control Register (Default Value: 0x0004_0200)

Offset: 0x0014			Register Name: OWA_FCTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HUB_EN Audio Hub Enable 0: Disable 1: Enable
30	R/W1C	0x0	FTX Write '1' to flush TXFIFO, self clear to '0'.
29	R/W1C	0x0	FRX Write '1' to flush RXFIFO, self clear to '0'.
28:20	/	/	/
19:12	R/W	0x40	TXTL TX FIFO empty Trigger Level Interrupt and DMA request trigger level for TX FIFO normal condition. Trigger Level = TXTL
11	/	/	/
10:4	R/W	0x20	RXTL RX FIFO Trigger Level Interrupt and DMA request trigger level for RX FIFO normal condition. Trigger Level = RXTL + 1
3	/	/	/
2	R/W	0x0	TXIM TXFIFO Input Mode(Mode0, 1) 0: Valid Data at the MSB of TXFIFO Register 1: Valid Data at the LSB of TXFIFO Register Example for 20-bits transmitted audio sample: Mode 0: TXFIFO[23:0] = {APB_WDATA[31:12], 4'h0} Mode 1: TXFIFO[23:0] = {APB_WDATA[19:0], 4'h0}
1:0	R/W	0x0	RXOM RXFIFO Output Mode(Mode 0,1,2,3) 00: Expanding '0' at LSB of RXFIFO Register 01: Expanding Received Sample Sign bit at MSB of RXFIFO Register 10: Truncating Received Samples at High Half-word of RXFIFO Register and Low Half-word of RXFIFO Register is filled by '0' 11: Truncating Received Samples at Low Half-word of RXFIFO Register and High Half-word of RXFIFO Register is Expanded by Its Sigh Bit Mode 0: APB_RDATA[31:0] = {RXFIFO[23:0], 8'h0}

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			Mode 1: APB_RDATA[31:0] = {8'RXFIFO[23], RXFIFO[23:0]} Mode 2: APB_RDATA[31:0] = {RXFIFO[23:8], 16'h0} Mode 3: APB_RDATA[31:0] ={16'RXFIFO[23], RXFIFO[23:8]}

7.3.5.7. OWA FIFO Status Register (Default Value: 0x8080_0000)

Offset: 0x0018			Register Name: OWA_FSTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x1	TXE TXFIFO Empty (Indicate TXFIFO is Not Full) 0: No Room for New Sample in TXFIFO 1: More than One Room for New Sample in TXFIFO (>=1 Word)
30:24	/	/	/
23:16	R	0x80	TXE_CNT TXFIFO Empty Space Word Counter
15	R	0x0	RXA RXFIFO Available 0: No Available Data in RXFIFO 1: More than One Sample in RXFIFO (>=1 Word)
14:7	/	/	/
6:0	R	0x0	RXA_CNT RXFIFO Available Sample Word Counter

7.3.5.8. OWA Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: OWA_INT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0x0	RX_LOCKI_EN RX LOCK Interrupt Enable 0: Disable 1: Enable
17	R/W	0x0	RX_UNLOCKI_EN RX UNLOCK Interrupt Enable 0: Disable 1: Enable
16	R/W	0x0	RX_PARERRI_EN RX PARITY ERORR Interrupt Enable 0: Disable 1: Enable
15:8	/	/	/
7	R/W	0x0	TX_DRQ TXFIFO Empty DRQ Enable

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			0: Disable 1: Enable
6	R/W	0x0	TXUI_EN TXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TXOI_EN TXFIFO Overrun Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	TXEI_EN TXFIFO Empty Interrupt Enable 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	RX_DRQ RXFIFO Data Available DRQ Enable When Set to '1', RXFIFO DMA Request is Asserted if Data is Available in RXFIFO. 0: Disable 1: Enable
1	R/W	0x0	RXOI_EN RXFIFO Overrun Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RXAI_EN RXFIFO Data Available Interrupt Enable 0: Disable 1: Enable

7.3.5.9. OWA TX FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: OWA_TXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	W	0x0	TX_DATA Transmitting A, B channel data should be written this register one by one. The A channel data is first and then the B channel data.

7.3.5.10. OWA TX Counter Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: OWA_TX_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX_CNT

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			TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial value at any time. After updated by the initial value, the counter register should count on base of this initial value.

7.3.5.11. OWA RX Counter Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: OWA_RX_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Codec, the RX sample counter register increases by one. The RX Counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this value.

7.3.5.12. OWA TX Channel Status Register0 (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: OWA_TX_CHSTA0
Bit	**Read/Write**	**Default/Hex**	**Description**
31: 30	/	/	/
29:28	R/W	0x0	CA Clock Accuracy 00: Level 2 01: Level 1 10: Level 3 11: Not matched
27:24	R/W	0x0	FREQ Sampling Frequency 0000: 44.1kHz 0001: Not indicated 0010: 48kHz 0011: 32kHz 0100: 22.05kHz 0101: Reserved 0110: 24kHz 0111: Reserved 1000: Reserved 1001: 768kHz 1010: 96kHz

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			1011: Reserved 1100:176.4kHz 1101: Reserved 1110: 192kHz 1111: Reserved
23:20	R/W	0x0	CN Channel Number
19:16	R/W	0x0	SN Source Number
15:8	R/W	0x0	CC Category Code Indicates the kind of equipment that generates the digital audio interface signal.
7:6	R/W	0x0	MODE Mode 00: Default Mode 01~11: Reserved
5:3	R/W	0x0	EMP Emphasis Additional format information For bit 1 = “0”, Linear PCM audio mode: 000: 2 audio channels without pre-emphasis 001: 2 audio channels with 50 μs / 15 μs pre-emphasis 010: Reserved (for 2 audio channels with pre-emphasis) 011: Reserved (for 2 audio channels with pre-emphasis) 100~111: Reserved For bit 1 = “1”, other than Linear PCM applications: 000: Default state 001~111: Reserved
2	R/W	0x0	CP Copyright 0: Copyright is asserted 1: No copyright is asserted
1	R/W	0x0	TYPE Audio Data Type 0: Linear PCM Samples 1: For none-linear PCM audio such as AC3, DTS, MPEG audio
0	R/W	0x0	PRO Application Type 0: Consumer Application 1: Professional Application This bit must be fixed to “0”

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7.3.5.13. OWA TX Channel Status Register1 (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: OWA_TX_CHSTA1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0x0	CGMS_A 00: Copying is permitted without restriction 01: One generation of copies may be made 10: Condition not be used 11: No copying is permitted
7:4	R/W	0x0	ORIG_FREQ Original Sampling Frequency 0000: Not indicated 0001: 192kHz 0010: 12kHz 0011: 176.4kHz 0100: Reserved 0101: 96kHz 0110: 8kHz 0111: 88.2kHz 1000: 16kHz 1001: 24kHz 1010: 11.025kHz 1011: 22.05kHz 1100: 32kHz 1101: 48kHz 1110: Reserved 1111: 44.1kHz
3:1	R/W	0x0	WL Sample Word Length For bit 0 = “0”: 000: Not indicated 001: 16 bits 010: 18 bits 100: 19 bits 101: 20 bits 110: 17 bits 111: Reserved For bit 0 = “1”: 000: Not indicated 001: 20 bits 010: 22 bits 100: 23 bits 101: 24 bits

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			110: 21 bits 111: Reserved
0	R/W	0x0	MWL Max Word Length 0: Maximum audio sample word length is 20 bits 1: Maximum audio sample word length is 24 bits

7.3.5.14. OWA RX Channel Status Register0 (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: OWA_RX_CHSTA0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R/W	0x0	CA Clock Accuracy 00: Level 2 01: Level 1 10: Level 3 11: Not Matched
27:24	R/W	0x0	FREQ Sampling Frequency 0000: 44.1kHz 0001: Not Indicated 0010: 48kHz 0011: 32kHz 0100: 22.05kHz 0101: Reserved 0110: 24kHz 0111: Reserved 1000: Reserved 1001: 768kHz 1010: 96kHz 1011: Reserved 1100:176.4kHz 1101: Reserved 1110: 192kHz 1111: Reserved
23:20	R/W	0x0	CN Channel Number
19:16	R/W	0x0	SN Source Number
15:8	R/W	0x0	CC Category Code Indicates the Kind of Equipment that Generates the digital audio interface Signal.

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7:6	R/W	0x0	MODE Mode 00: Default Mode 01~11: Reserved
5:3	R/W	0x0	EMP Emphasis Additional Format Information For bit 1 = '0', Linear PCM Audio Mode: 000: 2 Audio Channels without Pre-emphasis 001: 2 Audio Channels with 50 µs / 15 µs Pre-emphasis 010: Reserved (For 2 Audio Channels with Pre-emphasis) 011: Reserved (For 2 Audio Channels with Pre-emphasis) 100~111: Reserved For bit 1 = '1', Other than Linear PCM Applications: 000: Default State 001~111: Reserved
2	R/W	0x0	CP Copyright 0: Copyright is Asserted 1: No Copyright is Asserted
1	R/W	0x0	TYPE Audio Data Type 0: Linear PCM Samples 1: For None-linear PCM Audio Such as AC3, DTS, MPEG Audio
0	R/W	0x0	PRO Application Type 0: Consumer Application 1: Professional Application

7.3.5.15. OWA RX Channel Status Register1 (Default Value: 0x0000_0000)

Offset: 0x0038			**Register Name: OWA_RX_CHSTA1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0x0	CGMS_A 00: Copying is Permitted without Restriction 01: One Generation of Copies May Be Made 10: Condition Not Be Used 11: No Copying is Permitted
7:4	R/W	0x0	ORIG_FREQ Original Sampling Frequency 0000: Not Indicated 0001: 192kHz

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			0010: 12kHz 0011: 176.4kHz 0100: Reserved 0101: 96kHz 0110: 8kHz 0111: 88.2kHz 1000: 16kHz 1001: 24kHz 1010: 11.025kHz 1011: 22.05kHz 1100: 32kHz 1101: 48kHz 1110: Reserved 1111: 44.1kHz
3:1	R/W	0x0	WL Sample Word Length For bit 0 = '0': 000: Not Indicated 001: 16 bits 010: 18 bits 100: 19 bits 101: 20 bits 110: 17 bits 111: Reserved For bit 0 = '1': 000: Not Indicated 001: 20 bits 010: 22 bits 100: 23 bits 101: 24 bits 110: 21 bits 111: Reserved
0	R/W	0x0	MWL Max Word Length 0: Maximum Audio Sample Word Length is 20 bits 1: Maximum Audio Sample Word Length is 24 bits

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7.4. DMIC

7.4.1. Overview

DMIC Controller supports a 8-channels digital microphone interface, the DMIC controller can output 128fs or 64fs (fs= ADC sample rate).

The DMIC controller includes the following features:

- Supports up to 8 channels
- Supports sample rate from 8kHz to 48kHz

7.4.2. Block Diagram

Figure 7-23 shows a block diagram of the DMIC.

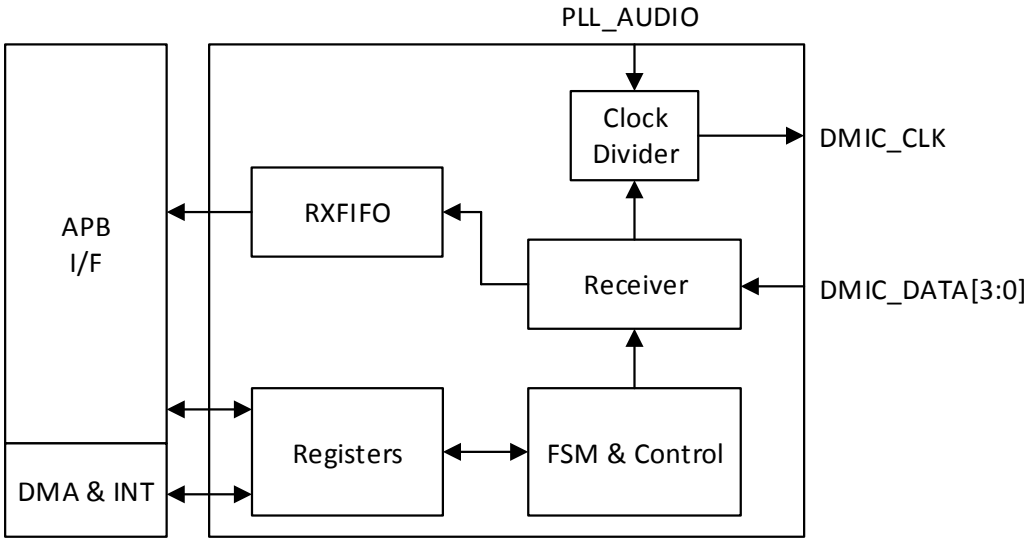


Figure 7-23. DMIC Block Diagram

7.4.3. Operations and Functional Descriptions

7.4.3.1. External Signals

Table 7-9 describes the external signals of DMIC.

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Table 7-9. DMIC External Signals

Signal	Description	Type
DMIC_CLK	Digital Microphone Clock Output	O
DMIC_DATA0	Digital Microphone Data Input	I
DMIC_DATA1	Digital Microphone Data Input	I
DMIC_DATA2	Digital Microphone Data Input	I
DMIC_DATA3	Digital Microphone Data Input	I

7.4.3.2. Clock Sources

Table 7-10 describes the clock source for DMIC. Users can see **Clock Controller Unit(CCU)** for clock setting, configuration and gating information.

Table 7-10. DMIC Clock Sources

Clock Sources	Description
PLL_AUDIO	24.576MHz or 22.5792MHz generated by PLL_AUDIO to produce 48kHz or 44.1kHz serial frequency.

7.4.3.3. Operation Mode

The software operation of the DMIC is divided into five steps: system setup, DMIC initialization, the channel setup, DMA setup and Enable/Disable module. Five steps are described in detail in the following sections.

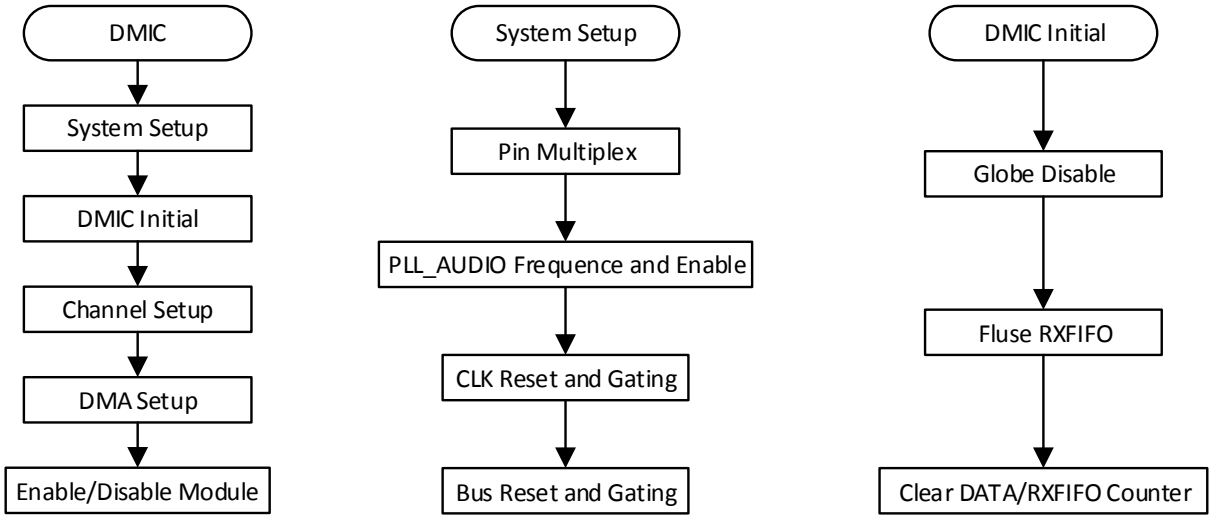


Figure 7-24. DMIC Operation Mode

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7.4.3.3.1. System Setup and DMIC Initialization

The first step in the system setup is properly programming the GPIO. Because the DMIC port is a multiplex pin. You can find the function in the pin multiplex specification.

The clock source for the DMIC should be followed. At first you must disable the PLL_AUDIO though the PLL_ENABLE bit of **PLL_AUDIO_CTRL_REG** in the CCU. The second step, you must set up the frequency of the PLL_AUDIO in the **PLL_AUDIO_CTRL_REG**. Then enable PLL_AUDIO. After that, you must open the DMIC gating through the **DMIC_CLK_REG** when you checkout that the LOCK bit of **PLL_AUDIO_CTRL_REG** becomes 1. At last, you must reset and open the DMIC bus gating in the CCU_DMIC_BGR_REG.

After the system setup, the register of DMIC can be setup. At first, you should initialize the DMIC. You should close the **globe enable bit**(DMIC_EN[8]) , **data channel enable bit**(DMIC_EN[7:0]) by writing 0 to it. After that, you must flush the RXFIFO by writing 1 to register **DMIC_RXFIFO_CTR**[31]. At last, you can clear the Data/RXFIFO counter by writing 1 to **DMIC_RXFIFO_STA,DMIC_CNT**.

7.4.3.3.2. Channel Setup and DMA Setup

You can set up the sample rate, the sample resolution, the over sample rate, the channel number, the RXFIFO output mode and the RXFIFO trigger level and so on. The setup of register can be found in the specification.

The DMIC supports two methods to transfer the data. The most common way is DMA, the setup of DMA can be found in the DMA specification. In this module, you just enable the DRQ.

7.4.3.3.3. Enable and Disable DMIC

To enable the function, you can enable **data channel enable bit**(DMIC_EN[7:0]) by writing 1 to it. After that, you must enable DMIC by writing the **Globe Enable bit** to 1 in the **DMIC_EN**[8]. Write the **Globe Enable** to 0 to disable DMIC.

7.4.4. Register List

Module Name	Base Address
DMIC	0x05095000

Register Name	Offset	Description
DMIC_EN	0x0000	DMIC Enable Control Register
DMIC_SR	0x0004	DMIC Sample Rate Register
DMIC_CTR	0x0008	DMIC Control Register
DMIC_ DATA	0x0010	DMIC DATA Register

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DMIC_INTC	0x0014	MIC Interrupt Control Register
DMIC_INTS	0x0018	DMIC Interrupt Status Register
DMIC_FIFO_CTR	0x001C	DMIC FIFO Control Register
DMIC_FIFO_STA	0x0020	DMIC FIFO Status Register
DMIC_CH_NUM	0x0024	DMIC Channel Numbers Register
DMIC_CH_MAP	0x0028	DMIC Channel Mapping Register
DMIC_CNT	0x002C	DMIC Counter Register
DATA0_DATA1_VOL_CTR	0x0030	DATA0 And DATA1 Volume Control Register
DATA2_DATA3_VOL_CTR	0x0034	DATA2 And DATA3 Volume Control Register
HPF_EN_CTR	0x0038	High Pass Filter Enable Control Register
HPF_COEF_REG	0x003C	High Pass Filter Coef Register
HPF_GAIN_REG	0x0040	High Pass Filter Gain Register

7.4.5. Register Description

7.4.5.1. DMIC Enable Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: DMIC_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	GLOBE_EN DMIC Globe Enabl 0: Disable 1: Enable
7	R/W	0x0	DATA3_CHR_EN DATA3 Right Channel 1 Enable 0: Disable 1: Enable
6	R/W	0x0	DATA3_CHL_EN DATA3 Left Channel Enable 0: Disable 1: Enable
5	R/W	0x0	DATA2_CHR_EN DATA2 Right Channel 1 Enable 0: Disable 1: Enable
4	R/W	0x0	DATA2_CHL_EN DATA2 Left Channel Enable 0: Disable 1: Enable
3	R/W	0x0	DATA1_CHR_EN DATA1 Right Channel 1 Enable 0: Disable

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			1: Enable
2	R/W	0x0	DATA1_CHL_EN DATA1 Left Channel Enable 0: Disable 1: Enable
1	R/W	0x0	DATA0_CHR_EN DATA0 Right Channel 1 Enable 0: Disable 1: Enable
0	R/W	0x0	DATA0_CHL_EN DATA0 Left Channel Enable 0: Disable 1: Enable

7.4.5.2. DMIC Sample Rate Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: DMIC_SR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	DMIC_SR Sample Rate of DMIC 000: 48 kHz 010: 24 kHz 100: 12 kHz 110: Reserved 001: 32 kHz 011: 16 kHz 101: 8 kHz 111: Reserved 44.1 kHz/22.05 kHz/11.025 kHz can be supported by Audio PLL Configure Bit.

7.4.5.3. DMIC Control Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: DMIC_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:9	R/W	0x0	DMICFDT DMICFIFO Delay Time for Writing Data after GLOBE_EN 00: 5ms 01: 10ms 10: 200ms 11: 30ms
8	R/W	0x0	DMICDFEN

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			DMIC FIFO Delay Function for Writing Data after GLOBE_EN 0: Disable 1: Enable
7	R/W	0x0	DATA3 Left Data and Right Data Sweep Enable 0: Disable 1: Enable
6	R/W	0x0	DATA2 Left Data and Right Data Sweep Enable 0: Disable 1: Enable
5	R/W	0x0	DATA1 Left Data and Right Data Sweep Enable 0: Disable 1: Enable
4	R/W	0x0	DATA0 Left Data and Right Data Sweep Enable 0: Disable 1: Enable
3:1	/	/	/
0	R/W	0x0	DMIC Oversample Rate 0: 128 (Support 8 kHz ~ 24 kHz) 1: 64 (Support 16 kHz ~ 48 kHz)

7.4.5.4. DMIC DATA Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: DMIC_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMIC_DATA

7.4.5.5. DMIC Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: DMIC_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	FIFO_DRQ_EN DMIC FIFO Data Available DRQ Enable 0: Disable 1: Enable
1	R/W	0x0	FIFO_OVERRUN_IRQ_EN DMIC FIFO Over Run IRQ Enable 0: Disable 1: Enable
0	R/W	0x0	DATA_IRQ_EN DMIC FIFO Data Available IRQ Enable 0: Disable 1: Enable

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7.4.5.6. DMIC Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: DMIC_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1C	0x0	FIFO_OVERRUN_IRQ_PENDING DMIC FIFO Over Run Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Writing '1' to clear this interrupt or automatically clear if interrupt condition fails
0	R/ W1C	0x0	FIFO_DATA_IRQ_PENDING DMIC FIFO Data Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ Writing '1' to clear this interrupt or automatically clear if interrupt condition fails.

7.4.5.7. DMIC FIFO Control Register (Default Value: 0x0000_0040)

Offset: 0x001C			Register Name: DMIC_FIFO_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W1C	0x0	DMIC_FIFO_FLUSH DMIC FIFO Flush Writing '1' to flush TX FIFO, self clear to '0'
30:10	/	/	/
9	R/W	0x0	FIFO_MODE RX FIFO Output Mode (Mode 0, 1) 0: Expanding '0' at LSB of TX FIFO register 1: Expanding received sample sign bit at MSB of TX FIFO register For 24-bit received audio sample: Mode 0: RXDATA[31:0] = {FIFO_O[23:0], 8'h0} Mode 1: Reserved For 16-bit received audio sample: Mode 0: RXDATA[31:0] = {FIFO_O[23:8], 16'h0} Mode 1: RXDATA[31:0] = {16{FIFO_O[23]}, FIFO_O[23:8]}
8	R/W	0x0	Sample_Resolution 0: 16 bit 1: 24 bit
7:0	R/W	0x40	FIFO_TRG_LEVEL

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			FIFO Trigger Level (TRLV[7:0]) Interrupt and DMA request trigger level for DMIC FIFO normal condition IRQ/DRQ Generated when WLEVEL > TRLV[7:0]) WLEVEL represents the number of valid samples in the DMIC FIFO

7.4.5.8. DMIC FIFO Status Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: DMIC_FIFO_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DMIC_DATA_CNT DMIC FIFO Available Sample Word Counter

7.4.5.9. DMIC Channel Numbers Register (Default Value: 0x0000_0001)

Offset: 0x0024			Register Name: DMIC_CH_NUM
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x1	DMIC_CH_NUM DMIC Enable Channel Numbers are (N+1)

7.4.5.10. DMIC Channel Mapping Register (Default Value: 0x7654_3210)

Offset: 0x0028			Register Name: DMIC_CH_MAP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x7	DMIC_CH7_MAP DMIC Channel 7 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
27:24	R/W	0x6	DMIC_CH6_MAP DMIC Channel 6 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel

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			0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
23:20	R/W	0x5	DMIC_CH5_MAP DMIC Channel 5 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
19:16	R/W	0x4	DMIC_CH4_MAP DMIC Channel 4 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
15:12	R/W	0x3	DMIC_CH3_MAP DMIC Channel 3 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
11:8	R/W	0x2	DMIC_CH2_MAP DMIC Channel 2 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
7:4	R/W	0x1	DMIC_CH1_MAP DMIC Channel 1 Mapping

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			0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
3:0	R/W	0x0	DMIC_CH0_MAP DMIC Channel0 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel

7.4.5.11. DMIC Counter Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: DMIC_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DMIC _CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value **NOTE** **It is used for Audio/ Video Synchronization**

7.4.5.12. DATA0 and DATA1 Volume Control Register (Default Value: 0xA0A0_A0A0)

Offset: 0x0030			Register Name: DATA0_DATA1_VOL_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0xA0	DATA1L_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ……..

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			0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ……. 0xFF: 71.25 dB
23:16	R/W	0xA0	DATA1R_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …….. 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ……. 0xFF: 71.25 dB
15:8	R/W	0xA0	DATA0L_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …….. 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ……. 0xFF: 71.25 dB
7:0	R/W	0xA0	DATA0R_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …….. 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ……. 0xFF: 71.25 dB

7.4.5.13. DATA2 and DATA3 Volume Control Register (Default Value: 0xA0A0_A0A0)

Offset: 0x0034			Register Name: DATA2_DATA3_VOL_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0xA0	DATA3L_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB

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			…….. 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB …….. 0xFF: 71.25 dB
23:16	R/W	0xA0	DATA3R_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …….. 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB …….. 0xFF: 71.25 dB
15:8	R/W	0xA0	DATA2L_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …….. 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB …….. 0xFF: 71.25 dB
7:0	R/W	0xA0	DATA2R_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …….. 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB …….. 0xFF: 71.25 dB

7.4.5.14. High Pass Filter Enable Control Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: HPF_EN_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	HPF_DATA3_CHR_EN DATA3 Right Channel Enable

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			0: Disable 1: Enable
6	R/W	0x0	HPF_DATA3_CHL_EN DATA3 Left Channel Enable 0: Disable 1: Enable
5	R/W	0x0	HPF_DATA2_CHR_EN DATA2 Right Channel Enable 0: Disable 1: Enable
4	R/W	0x0	HPF_DATA2_CHL_EN DATA2 Left Channel Enable 0: Disable 1: Enable
3	R/W	0x0	HPF_DATA1_CHR_EN DATA1 Right Channel Enable 0: Disable 1: Enable
2	R/W	0x0	HPF_DATA1_CHL_EN DATA1 Left Channel Enable 0: Disable 1: Enable
1	R/W	0x0	HPF_DATA0_CHR_EN DATA0 Right Channel Enable 0: Disable 1: Enable
0	R/W	0x0	HPF_DATA0_CHL_EN DATA0 Left Channel Enable 0: Disable 1: Enable

7.4.5.15. High Pass Filter Coef Register (Default Value: 0x00FF_AA45)

Offset: 0x003C			Register Name: HPF_COEF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x00FFAA45	High Pass Filter Coefficient

7.4.5.16. High Pass Filter Gain Register (Default Value: 0x00FF_D522)

Offset: 0x0040			Register Name: HPF_GAIN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x00FFD522	High Pass Filter Gain

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7.5. Audio Codec

7.5.1. Overview

- System resources are controlled by ATE
- Two audio digital-to-analog(DAC) channels
  - 100dB SNR@A-weight
  - Supports DAC Sample Rates from 8 kHz to 192 kHz
- Supports analog/digital volume control
- Two differential microphone inputs
- One lineout output with voltage ramp
- Two audio analog-to-digital(ADC) channels
  - 92dB SNR@A-weight
  - Supports ADC Sample Rates from 8kHz to 48kHz
- Supports Automatic Gain Control(AGC) adjusting the ADC recording output

7.5.2. Operations and Functional Descriptions

7.5.2.1. Typical Performance

Test Conditions:
VCC-IO= 3.3V, AVCC=2.8V, TA=25℃, 1kHz sinusoid signal, fs = 48kHz, Input PGA gain = 0dB, 20-bit audio data unless otherwise stated.

Items	Parameter	Test Conditions	Min	Typ	Max	Unit
DAC Path	DAC to LINEOUTL or LINEOUTR(R=10kΩ)					
	Fullscale	0dBFS 1kHz		0.8		Vrms
	SNR@A	0dB 1kHz		100		dB
	THD+N	0dB 1kHz		-80		dB
	Crosstalk	0dB 1kHz		75		dB
	Noise Floor	0data A-weighted		7		uVrms
ADC Path	MIC1 to ADC via ADC mixer					
	SNR@A	2.5Vpp 1kHz 0dB		92		dB
	THD+N	2.5Vpp 1kHz 0dB		-80		dB
	SNR@A	30mV 1kHz 24dB		81		dB
	THD+N	30mV 1kHz 24dB		-70		dB
	SNR@A	30mV 1kHz 30dB		81		dB
	THD+N	30mV 1kHz 30dB		-76		dB
	SNR@A	10mV 1kHz 42dB		73		dB
	THD+N	10mV 1kHz 42dB		-72		dB

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	Crosstalk			80		dB
	Noise Floor			7		uVrms
	MIC2 to ADC via ADC mixer					
	SNR@A	2.5Vpp 1kHz 0dB		92		dB
	THD+N	2.5Vpp 1kHz 0dB		-65		dB
	SNR@A	30mV 1kHz 24dB		81		
	THD+N	30mV 1kHz 24dB		-77		dB
	SNR@A	30mV 1kHz 30dB		83		dB
	THD+N	30mV 1kHz 30dB		-77		dB
	SNR@A	30mV 1kHz 42dB		73		dB
	THD+N	30mV 1kHz 42dB		-71		dB
	Crosstalk			80		dB
	Noise Floor			7		uVrms
AA path	MIC1 to LINEOUT via output mixer					
	Fullscale	2.5Vpp 1kHz 0dB		0.8		Vrms
	SNR@A	2.5Vpp 1kHz 0dB		92		dB
	THD+N	2.5Vpp 1kHz 0dB		80		dB
	CrossTalk			75		dB

7.5.2.2. Power Domain

The AC-AVCC provides power to ADC/DAC analog part. VDD-SYS provides power to ADC/DAC digital part and all the register.

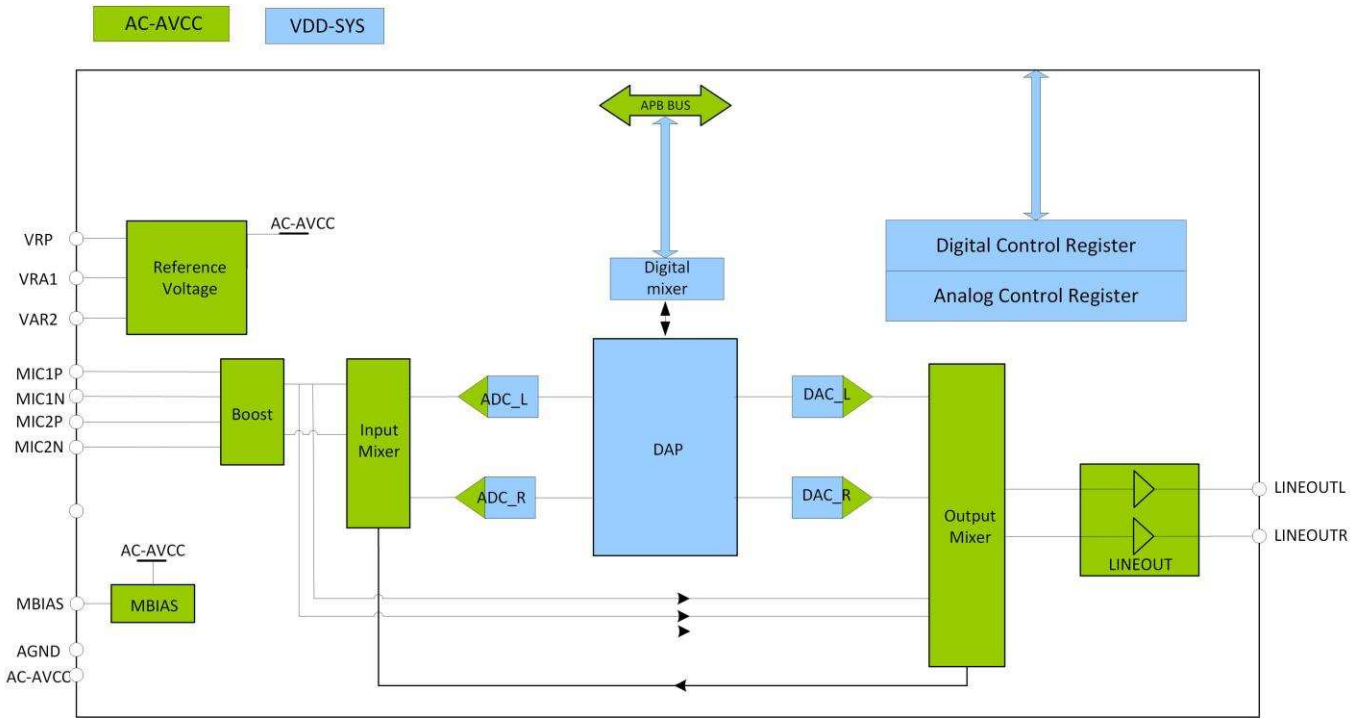


Figure 7-25. Audio Codec Power Domain

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7.5.2.3. Analog Data Path Diagram

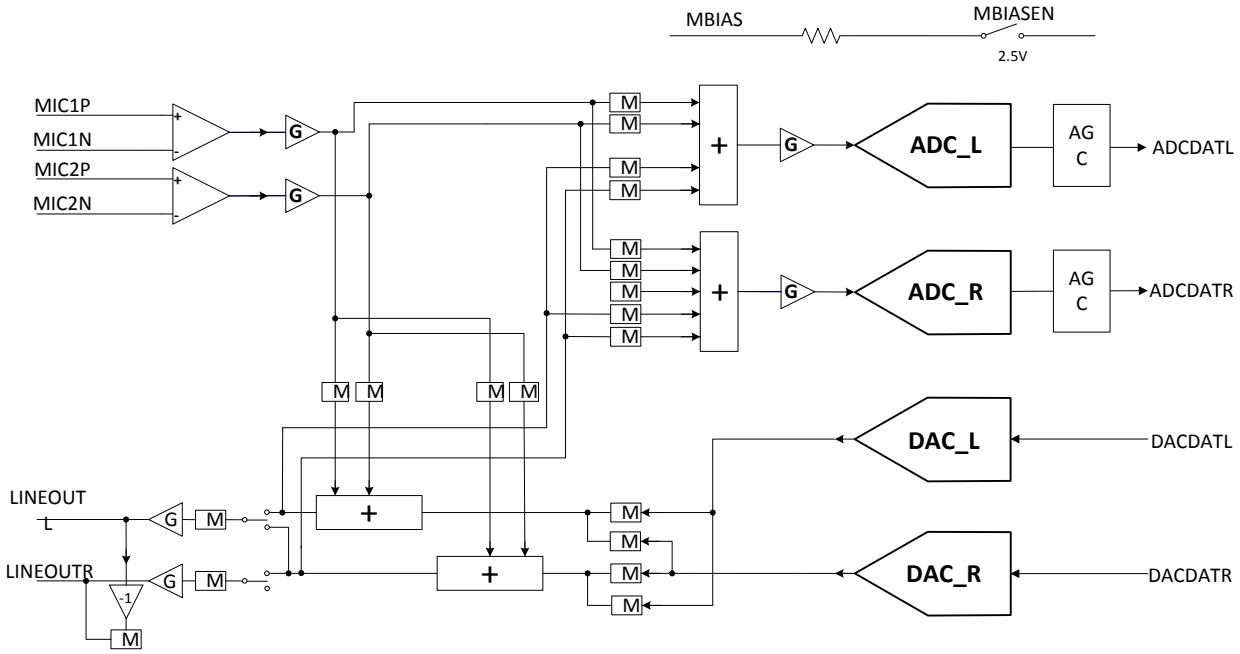


Figure 7-26. Analog Data Path Diagram

7.5.2.4. Digital Data Path Diagram

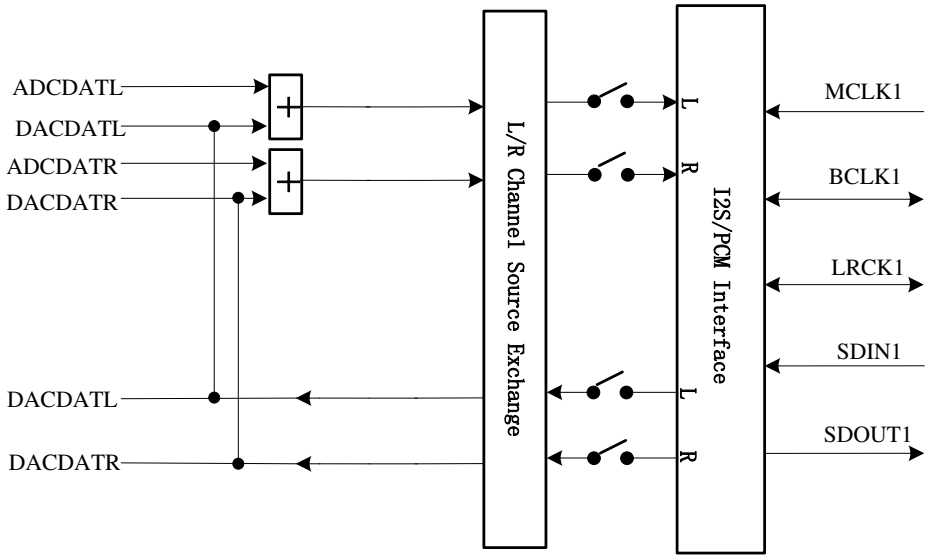


Figure 7-27. Digital Data Path Diagram

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7.5.2.5. Stereo ADC

The stereo ADC is used for recording stereo sound. The sample rate of the stereo ADC is independent of DAC sample rate. In order to save power, the left and right ADC can be powered down separately by setting AC_ADC_ACTRL register.

The volume control of the stereo ADC is set by AC_ADC_ACTRL register.

7.5.2.6. Stereo DAC

The stereo DAC can be configured to different sample rate by setting the register. In order to save power, the left and right DAC can be powered down separately by setting register AC_DAC_ACTRL.

7.5.2.7. Analog Mixer

The Codec supports two mixers for all function requirements: LINEOUT mixer and ADC record mixer.

7.5.2.8. Analog Input and Output

The Codec has two analog input ports: microphone input(MIC1,MIC2).

The Codec has one analog output port: LINEOUT output.

7.5.2.9. Microphone BIAS

The MBIAS output provides a low noise reference voltage suitable for biasing electrets type microphones and the associated external resistor biasing network.

7.5.2.10. Interrupt

The Audio Codec has one interrupt output and two interrupt sources.

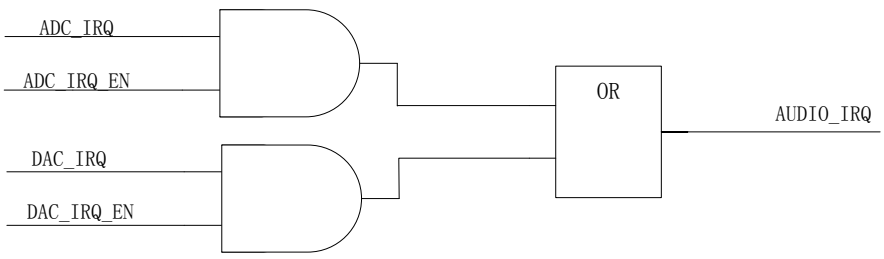


Figure 7-28. Interrupt System

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7.5.3. Register List

Module Name	Base Address
ATE_Audio Codec	0x2000

Register Name	Offset	Description
SYS_CLK_CTL	0x0000	System Clock Control Register
SYS_MOD_RST	0x0002	System Module Reset Control Register
SYS_SAMP_CTL	0x0004	System Sample Rate Control Register
AIF _CTL	0x0100	AIF Control Register
AIF _CLK	0x0102	AIF Clock Register
AIF _FMT0	0x0104	AIF Format 0 Register
AIF _FMT1	0x0108	AIF Format 1 Register
AIF _MIX_SRC	0x0114	AIF Digital Mixer Source Select Register
AIF _MIX_GAIN	0x0116	AIF Digital Mixer Gain Select Register
AIF _DACDAT_DVC	0x0118	AIF DACDAT Volume Control Register
AIF _ADCDAT_DVC	0x011A	AIF ADCDAT Volume Control Register
AC_DAC_DPC	0x0200	DAC Digital Part Control Register
AC_DAC_MIX_SRC	0x0202	DAC Digital Input Mixer Source Select Register
AC_DAC_MIX_GAIN	0x0204	DAC Digital Input Mixer Gain Select Register
DACA_OMIXER_CTRL	0x0220	DAC & Output Mixer Analog Control Register
OMIXER_SR	0x0222	Output Mixer Source Select Register
LINEOUT_CTRL	0x0224	Lineout Control Register
AC_ADC_DPC	0x0300	ADC Digital Part Control Register
MBIAS_CTRL	0x0310	MICBIAS Control Register
ADC_MIC_CTRL	0x0320	ADC & MIC Control Register
ADCMIXER_SR	0x0322	ADC Mixer Source Control Register
ANALOG_TUNING0	0x032A	Bias Control Register
ANALOG_TUNING	0x032C	Analog performance tuning Control Register
AC_AGC_SEL	0x0480	ADC DAP Function Selected Register
AC_ADC_DAPLCTRL	0x0500	ADC DAP Left Channel Control Register
AC_ADC_DAPRCTRL	0x0502	ADC DAP Right Channel Control Register
AC_ADC_DAPLSTA	0x0504	ADC DAP Left Status Register
AC_ADC_DAPRSTA	0x0506	ADC DAP Right Status Register
AC_ADC_DAPLTL	0x0508	ADC DAP Left Target Level Register
AC_ADC_DAPRTL	0x050A	ADC DAP Right Target Level Register
AC_ADC_DAPLHAC	0x050C	ADC DAP Left High Average Coef Register
AC_ADC_DAPLLAC	0x050E	ADC DAP Left Low Average Coef Register
AC_ADC_DAPRHAC	0x0510	ADC DAP Right High Average Coef Register
AC_ADC_DAPRLAC	0x0512	ADC DAP Right Low Average Coef Register
AC_ADC_DAPLDT	0x0514	ADC DAP Left Decay Time Register

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AC_ADC_DAPLAT	0x0516	ADC DAP Left Attack Time Register
AC_ADC_DAPRDT	0x0518	ADC DAP Right Decay Time Register
AC_ADC_DAPRAT	0x051A	ADC DAP Right Attack Time Register
AC_ADC_DAPNTH	0x051C	ADC DAP Noise Threshold Register
AC_ADC_DAPLHNAC	0x051E	ADC DAP Left Input Signal High Average Coef Register
AC_ADC_DAPLLNAC	0x0520	ADC DAP Left Input Signal Low Average Coef Register
AC_ADC_DAPRHNAC	0x0522	ADC DAP Right Input Signal High Average Coef Register
AC_ADC_DAPRLNAC	0x0524	ADC DAP Right Input Signal Low Average Coef Register
AC_DAPHHPFC	0x0526	ADC DAP High HPF Coef Register
AC_DAPLHPFC	0x0528	ADC DAP Low HPF Coef Register
AC_DAPOPT	0x052A	ADC DAP Optimum Register
AC_DAC_DAPCTRL	0x1000	DAC DAP Channel Control Register
AC_DRC_HHPFC	0x1002	DRC High HPF Coef Register
AC_DRC_LHPFC	0x1004	DRC Low HPF Coef Register
AC_DRC_CTRL	0x1006	DRC Control Register
AC_DRC_LPFHAT	0x1008	DRC Left Peak Filter High Attack Time Coef Register
AC_DRC_LPFLAT	0x100A	DRC Left Peak Filter Low Attack Time Coef Register
AC_DRC_RPFHAT	0x100C	DRC Right Peak Filter High Attack Time Coef Register
AC_DRC_RPFLAT	0x100E	DRC Peak Filter Low Attack Time Coef Register
AC_DRC_LPFHRT	0x1010	DRC Left Peak Filter High Release Time Coef Register
AC_DRC_LPFLRT	0x1012	DRC Left Peak Filter Low Release Time Coef Register
AC_DRC_RPFHRT	0x1014	DRC Right Peak filter High Release Time Coef Register
AC_DRC_RPFLRT	0x1016	DRC Right Peak filter Low Release Time Coef Register
AC_DRC_LRMSHAT	0x1018	DRC Left RMS Filter High Coef Register
AC_DRC_LRMSLAT	0x101A	DRC Left RMS Filter Low Coef Register
AC_DRC_RRMSHAT	0x101C	DRC Right RMS Filter High Coef Register
AC_DRC_RRMSLAT	0x101E	DRC Right RMS Filter Low Coef Register
AC_DRC_HCT	0x1020	DRC Compressor Threshold High Setting Register
AC_DRC_LCT	0x1022	DRC Compressor Threshold High Setting Register
AC_DRC_HKC	0x1024	DRC Compressor Slope High Setting Register
AC_DRC_LKC	0x1026	DRC Compressor Slope Low Setting Register
AC_DRC_HOPC	0x1028	DRC Compressor High Output at Compressor Threshold Register
AC_DRC_LOPC	0x102A	DRC Compressor Low Output at Compressor Threshold Register
AC_DRC_HLT	0x102C	DRC Limiter Theshold High Setting Register
AC_DRC_LLT	0x102E	DRC Limiter Theshold Low Setting Register
AC_DRC_HKl	0x1030	DRC Limiter Slope High Setting Register
AC_DRC_LKl	0x1032	DRC Limiter Slope Low Setting Register
AC_DRC_HOPL	0x1034	DRC Limiter High Output at Limiter Threshold
AC_DRC_LOPL	0x1036	DRC Limiter Low Output at Limiter Threshold
AC_DRC_HET	0x1038	DRC Expander Threshold High Setting Register
AC_DRC_LET	0x103A	DRC Expander Threshold Low Setting Register
AC_DRC_HKE	0x103C	DRC Expander Slope High Setting Register
AC_DRC_LKE	0x103E	DRC Expander Slope Low Setting Register
AC_DRC_HOPE	0x1040	DRC Expander High Output at Expander Threshold

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AC_DRC_LOPE	0x1042	DRC Expander Low Output at Expander Threshold
AC_DRC_HKN	0x1044	DRC Linear Slope High Setting Register
AC_DRC_LKN	0x1046	DRC Linear Slope Low Setting Register
AC_DRC_SFHAT	0x1048	DRC Smooth Filter Gain High Attack Time Coef Register
AC_DRC_SFLAT	0x104A	DRC Smooth Filter Gain Low Attack Time Coef Register
AC_DRC_SFHRT	0x104C	DRC Smooth Filter Gain High Release Time Coef Register
AC_DRC_SFLRT	0x104E	DRC Smooth Filter Gain Low Release Time Coef Register
AC_DRC_MXGHS	0x1050	DRC MAX Gain High Setting Register
AC_DRC_MXGLS	0x1052	DRC MAX Gain Low Setting Register
AC_DRC_MNGHS	0x1054	DRC MIN Gain High Setting Register
AC_DRC_MNGLS	0x1056	DRC MIN Gain Low Setting Register
AC_DRC_EPSHC	0x1058	DRC Expander Smooth Time High Coef Register
AC_DRC_EPSLC	0x105A	DRC Expander Smooth Time Low Coef Register
AC_DRC_HPFHGAIN	0x105E	DRC HPF Gain High Coef Register
AC_DRC_HPFLGAIN	0x1060	DRC HPF Gain Low Coef Register
AC_DRC_BISTCR	0x1100	DRC Bist Control Register
AC_DRC_BISTST	0x1102	DRC Bist Status Register

7.5.4. Register Description

7.5.4.1. System Clock Control Register(Default Value:0x0000)

Offset: 0x0000			**Register Name: SYS_CLK_CTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x0	Module clock enable control 0: Clock disable 1: Clock enable BIT15-AIF BIT14-Reserved BIT13-Reserved BIT12-Reserved BIT11-Reserved BIT10-Reserved BIT9-Reserved BIT8-Reserved BIT7-HPF & AGC BIT6-HPF & DRC BIT5-Reserved BIT4-Reserved BIT3-ADC Digital BIT2-DAC Digital BIT1-Reserved BIT0-Reserved

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7.5.4.2. System Module Reset Control Register(Default Value:0x0000)

Offset: 0x0002			Register Name: SYS_MOD_RST
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x0	Module Reset control 0: Reset asserted 1: Reset de-asserted BIT15-AIF BIT14-Reserved BIT13-Reserved BIT12-Reserved BIT11-Reserved BIT10-Reserved BIT9-Reserved BIT8-Reserved BIT7-HPF & AGC BIT6-HPF & DRC BIT5-Reserved BIT4-Reserved BIT3-ADC Digital BIT2-DAC Digital BIT1-Reserved BIT0-Reserved

7.5.4.3. System Sample Rate Control Register(Default Value:0x0000)

Offset: 0x0004			Register Name: SYS_SAMP_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
15:4	/	/	/
3:0	R/W	0x0	SYS_FS System Sample Rate Control 0000: 8kHz 0001: 11.025kHz 0010: 12kHz 0011: 16kHz 0100: 22.05kHz 0101: 24kHz 0110: 32kHz 0111: 44.1kHz 1000: 48kHz 1001: 96kHz

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			1010: 192kHz Other: Reserved

7.5.4.4. AIF Control Register(Default Value:0x0000)

Offset: 0x0100			Register Name: AIF _CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
15:4	/	/	/
3	R/W	0x0	SDO0_EN 0: Disable, Hi-Z state 1: Enable
2	R/W	0x0	TXEN Transmitter Block Enable 0: Disable 1: Enable
1	R/W	0x0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0x0	GEN Globe Enable A disable on this bit overrides any other block or channel enables. 0: Disable 1: Enable

7.5.4.5. AIF Clock Register(Default Value:0x0000)

Offset: 0x0102			Register Name: AIF_CLK
Bit	**Read/Write**	**Default/Hex**	**Description**
15	R/W	0x0	BCLK_OUT 0: input 1: output
14	R/W	0x0	LRCK_OUT 0: input 1: output
13:10	R/W	0x0	BCLKDIV BCLK Divide Ratio from PLL2 0: reserved 1: Divide by 1 2: Divide by 2 3: Divide by 4 4: Divide by 6 5: Divide by 8

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			6: Divide by 12 7: Divide by 16 8: Divide by 24 9: Divide by 32 10: Divide by 48 11: Divide by 64 12: Divide by 96 13: Divide by 128 14: Divide by 176 15: Divide by 192
9:0	R/W	0x0	LRCK_PERIOD It is used to program the number of BCLKs per channel of sample frame. This value is interpreted as follow: PCM mode: Number of BCLKs within (Left + Right) channel width I2S / Left-Justified / Right-Justified mode: Number of BCLKs within each individual channel width (Left or Right) N+1 For example: n = 7: 8 BCLK width … n = 1023: 1024 BCLKs width

7.5.4.6. AIF Format 0 Register(Default Value:0x0000)

Offset: 0x0104			Register Name: AIF_FMT0
Bit	**Read/Write**	**Default/Hex**	**Description**
15:14	R/W	0x0	MODE_SEL Mode Selection 00: PCM mode (offset 0: DSP_B; offset 1: DSP_A) 01: Left mode (offset 0: LJ mode; offset 1: I2S mode) 10: Right-Justified mode 11: Reserved
13:12	/	/	/
11:10	R/W	0x0	TXn_OFFSET TXn offset tune, TXn data offset to LRCK 0: no offset n: data is offset by n BCLKs to LRCK
9:8	R/W	0x0	RX_OFFSET RX offset tune, RX data offset to LRCK 0: no offset n: data is offset by n BCLKs to LRCK
7	/	/	/
6:4	R/W	0x0	SR Sample Resolution

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			000: Reserved 001: 8-bit 010: 12-bit 011: 16-bit 100: 20-bit 101: 24-bit 110: 28-bit 111: 32-bit
3:1	R/W	0x0	SW Slot Width Select 000: Reserved 001: 8-bit 010: 12-bit 011: 16-bit 100: 20-bit 101: 24-bit 110: 28-bit 111: 32-bit
0	R/W	0x0	LOOP Loop back test 0: Normal mode 1: Loop back test When set '1', connecting the SDO0 with the SDI

7.5.4.7. AIF Format 1 Register(Default Value:0x0300)

Offset: 0x0108			Register Name: AIF_FMT1
Bit	**Read/Write**	**Default/Hex**	**Description**
15	R/W	0x0	BCLK_POLARITY 0: normal mode, negative edge drive and positive edge sample 1: invert mode, positive edge drive and negative edge sample
14	R/W	0x0	LRCK_POLARITY When apply in I2S / Left-Justified / Right-Justified mode: 0: Left channel when LRCK is low 1: Left channel when LRCK is high When apply in PCM mode: 0: PCM LRCK asserted at the negative edge 1: PCM LRCK asserted at the positive edge
13	R/W	0x0	EDGE_TRANSFER 0: SDO drive data and SDI sample data at the different BCLK edge 1: SDO drive data and SDI sample data at the same BCLK edge BCLK_POLARITY = 0, use negative edge BCLK_POLARITY = 1, use positive edge
12	/	/	/

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11	R/W	0x0	RX MLS MSB / LSB First Select 0: MSB First 1: LSB First
10	R/W	0x0	TX MLS MSB / LSB First Select 0: MSB First 1: LSB First
9:8	R/W	0x3	SEXT Sign Extend in slot [sample resolution < slot width] 00: Zeros or audio gain padding at LSB position 01: Sign extension at MSB position 10: Reserved 11: Transfer 0 after each sample in each slot
7:5	/	/	/
4	R/W	0x0	LRCK_WIDTH (only apply in PCM mode) LRCK width 0: LRCK = 1 BCLK width (short frame) 1: LRCK = 2 BCLK width (long frame)
3:2	R/W	0x0	RX_PDM PCM Data Mode 00: Linear PCM 01: reserved 10: 8-bit u-law 11: 8-bit A-law
1:0	R/W	0x0	TX_PDM PCM Data Mode 00: Linear PCM 01: reserved 10: 8-bit u-law 11: 8-bit A-law

7.5.4.8. AIF Digital Mixer Source Select Register(Default Value:0x0000)

Offset: 0x0114			**Register Name: AIF_MIX_SRC**
Bit	**Read/Write**	**Default/Hex**	**Description**
15:14	/	/	/
13:12	R/W	0x0	AIF_MIXL_SRC AIF ADCDAT left channel mixer source select 0: Disable 1:Enable Bit13: AIF_DACDATL Bit12: ADCDATL
11:10	/	/	/

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9:8	R/W	0x0	AIF_MIXR_SRC AIF ADCDAT Right channel mixer source select 0: Disable 1:Enable Bit9: AIF_DACDATR Bit8: ADCR
7:0	/	/	/

7.5.4.9. AIF Digital Mixer Gain Select Register(Default Value:0x0000)

Offset: 0x0116			Register Name: AIF_MIX_GAIN
Bit	**Read/Write**	**Default/Hex**	**Description**
15:14	/	/	/
13:12	R/W	0x0	AIF_MIXL_SRC AIF ADCDAT left channel mixer gain control 0: 0dB 1: -6dB Bit13: AIF_ DACDATL Bit12: ADCDATL
11:10	/	/	/
9:8	R/W	0x0	AIF_MIXR_SRC AIF ADCDAT Right channel mixer gain control 0: 0dB 1: -6dB Bit9: AIF_ DACDATR Bit8: ADCR
7:0	/	/	/

7.5.4.10. AIF DACDAT Volume Control Register(Default Value:0xA0A0)

Offset: 0x0118			Register Name: AIF_DACDAT_DVC
Bit	**Read/Write**	**Default/Hex**	**Description**
15:8	R/W	0xA0	AIF_DACDAT_VOL_L AIF DACDAT left channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …… 0x9F: -0.75dB 0xA0: 0dB 0xA1: 0.75dB …… 0xFF:71.25dB

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7:0	R/W	0xA0	AIF_DACDAT_VOL_R AIF DACDAT Right channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …… 0x9F: -0.75dB 0xA0: 0dB 0xA1: 0.75dB …… 0xFF: 71.25dB

7.5.4.11. AIF ADCDAT Volume Control Register(Default Value:0xA0A0)

Offset: 0x011A			Register Name: AIF_ADCDAT_DVC
Bit	**Read/Write**	**Default/Hex**	**Description**
15:8	R/W	0xA0	AIF_ADCDAT_VOL_L AIF ADCDAT left channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …… 0x9F: -0.75dB 0xA0: 0dB 0xA1: 0.75dB …… 0xFF: 71.25dB
7:0	R/W	0xA0	AIF_ADCDAT_VOL_L AIF ADCDAT left channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …… 0x9F: -0.75dB 0xA0: 0dB 0xA1: 0.75dB …… 0xFF: 71.25dB

7.5.4.12. DAC Digital Part Control Register(Default Value:0x0000)

Offset: 0x0200			Register Name: AC_DAC_DPC
Bit	**Read/Write**	**Default/Hex**	**Description**

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15	R/W	0x0	ENDA. DAC Digital Part Enable 0: Disabe 1: Enable
14	R/W	0x0	ENHPF HPF Function Enable 0: Enable 1: Disable
13	R/W	0x0	DAFIR32 Enable 32-tap FIR filter 0: 64-tap 1: 32-tap
12	R/W	0x0	Reserved
11:8	R/W	0x0	MODQU Internal DAC Quantization Levels Levels=[7*(21+MODQU[3:0])]/128 Default levels=7*21/128=1.15
7:0	R/W	0x0	Reserved

7.5.4.13. DAC Digital Input Mixer Source Select Register(Default Value:0x0000)

Offset: 0x0202			Register Name: AC_DAC_MIX_SRC
Bit	**Read/Write**	**Default/Hex**	**Description**
15:14	/	/	/
13:12	R/W	0x0	DACL_MXR_SRC DAC left channel mixer source select 0: Disable 1:Enable Bit13: AIF_DACDATL Bit12: ADCL
11:10	/	/	/
9:8	R/W	0x0	DACR_MXR_SRC DAC right channel mixer source select 0: Disable 1:Enable Bit9: AIF_DACDATR Bit8: ADCR
7:0	/	/	/

7.5.4.14. DAC Digital Input Mixer Gain Select Register(Default Value:0x0000)

Offset: 0x0204			Register Name: AC_DAC_MIX_GAIN
Bit	**Read/Write**	**Default/Hex**	**Description**

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15:14	/	/	/
13:12	R/W	0x0	DACL_MXR_SRC DAC left channel mixer source select 0: 0dB 1: -6dB Bit13: AIF_DACDATL Bit12: ADCL
11:10	/	/	/
9:8	R/W	0x0	DACR_MXR_SRC DAC right channel mixer source select 0: 0dB 1: -6dB Bit9: AIF_DACDATR Bit8: ADCR
7:0	/	/	/

7.5.4.15. DAC & Output Mixer Analog Control Register(Default Value:0x0333)

Offset: 0x0220			**Register Name: DACA_OMIXER_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
15	R/W	0x0	DACAREN Internal DAC Analog Right channel Enable 0: Disable 1: Enable
14	R/W	0x0	DACALEN Internal DAC Analog Left channel Enable 0: Disable 1: Enable
13	R/W	0x0	RMIXEN Right analog output MIXer Enable 0: Disable 1: Enable
12	R/W	0x0	LMIXEN Left analog output MIXer Enable 0: Disable 1: Enable
11	/	/	/
10:8	R/W	0x3	Reserved
7	R/W	0x0	/
6:4	R/W	0x3	MIC1G, (volm1) MIC1 BOOST stage to L or R output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
3	/	/	/
2:0	R/W	0x3	MIC2G, (volm2)

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			MIC2 BOOST stage to L or R output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB

7.5.4.16. Output Mixer Source Select Register(Default Value:0x0000)

Offset: 0x0222			Register Name: OMIXER_SR
Bit	**Read/Write**	**Default/Hex**	**Description**
15	/	/	/
14:8	R/W	0x0	RMIXMUTE Right output MIXer MUTE control 0: Mute 1: On Bit14: MIC1 boost stage Bit13: MIC2 boost stage Bit12: Reserved Bit11: Reserved Bit10: Reserved Bit9: DACR Bit8: DACL
7	/	/	/
6:0	R/W	0x0	LMIXMUTE Left output MIXer MUTE control 0: Mute 1: On Bit6: MIC1 boost stage Bit5: MIC2 boost stage Bit4: Reserved Bit3: Reserved Bit2: Reserved Bit1: DACL Bit0: DACR

7.5.4.17. Lineout Control Register(Default Value:0x0120)

Offset: 0x0224			Register Name: LINEOUT_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
15	R/W	0x0	LINEOUTEN Right & Left LINEOUT Enable 0: disable 1: enable
14	R/W	0x0	Line-out Left Select 0: not select 1: selected

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13	R/W	0x0	Line-out Right Select 0: not select 1: selected
12	R/W	0x0	Left line-out source select 0: left output mixer 1: left output mixer + right output mixer
11	R/W	0x0	Right line-out source select 0: right output mixer 1: left line-out, for differential output
10	R/W	0x0	LINEOUT_SLOPE_SELECT LINEOUT slope select cosine or ramp 0: select cosine 1: select ramp
9:8	R/W	0x1	LINEOUT_SLOPE_LENGTH_CTRL, (slopelengthsel) LINEOUT Anti-pop slope time Control 00: 131ms 01: 262ms 10: 393ms 11:524ms
7:5	R/W	0x1	ANTI_POP_CTRL, (antipoplengthsel) LINEOUT Anti-pop time Control 000: 131ms 001: 262ms 010: 393ms 011:524ms 100:655ms 101: 786ms 110: 917ms 111: 1048ms
4:0	R/W	0x0	LINEOUTVOL Line-out Volume Control, Total 31 level, from 0dB to -48dB, 1.5dB/step, mute when 00000 & 00001

7.5.4.18. ADC Digital Part Control Register(Default Value:0x0000)

Offset: 0x0300			Register Name: AC_ADC_DPC
Bit	**Read/Write**	**Default/Hex**	**Description**
15	R/W	0x0	ENAD ADC Digital part enable 0: Disable 1: Enable
14	R/W	0x0	ENDM Digital microphone enable 0: Analog ADC mode

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			1: Digital microphone mode
13	R/W	0x0	ADFIR32 Enable 32-tap FIR filter 0: 64-tap 1: 32-tap
12:4	R/W	0x0	Reserved
3:2	R/W	0x0	ADOUT_DTS ADC Delay Time For transmitting data after ENAD 00:5ms 01:10ms 10:20ms 11:30ms
1	R/W	0x0	ADOUT_DLY ADC Delay Function enable for transmitting data after ENAD 0: Disable 1: Enable
0	R/W	0x0	Reserved

7.5.4.19. MICBIAS Control Register(Default Value:0x6100)

Offset: 0x0310			**Register Name: MBIAS_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
15	R/W	0x0	MMICBIASEN Master Microphone Bias enable 0: disable 1: enable
14	R/W	0x1	MMIC BIAS chopper enable 0: disable 1:enable
13:12	R/W	0x2	MMIC BIAS chopper clock select 00: 250kHz 01: 500kHz 10: 1MHz 11: 2MHz
11:10	R/W	0x0	/
9:8	R/W	0x1	MBIASSEL MMICBIAS voltage level select 00: 1.76V 01: 1.96V 10: 2.20V 11: 2.33V
7:0	R/W	0x0	/

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7.5.4.20. ADC & MIC Control Register(Default Value:0x0344)

Offset: 0x0320			Register Name: ADC_MIC_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
15	R/W	0x0	ADCREN ADC Right Channel Enable 0: Disable 1: Enable
14	R/W	0x0	ADCLEN ADC Left Channel Enable 0: Disable 1: Enable
13:11	R/W	0x0	/
10:8	R/W	0x3	ADCG ADC Input Gain Control From -4.5dB to 6dB, 1.5dB/step default is 0dB
7	R/W	0x0	MIC1AMPEN MIC1 Boost AMP Enable 0: Disable 1: Enable
5:4	R/W	0x4	MIC1BOOST MIC1 Boost AMP Gain Control 0dB when 000, 24dB to 42dB when 001 to 111, 3dB/step, default is 33dB
3	R/W	0x0	MIC2AMPEN MIC2 Boost AMP Enable 0: Disable 1: Enable
2:0	R/W	0x4	MIC2BOOST MIC2 Boost AMP Gain Control 0dB when 000, 24dB to 42dB when 001 to 111, 3dB/step, default is 33dB

7.5.4.21. ADC Mixer Source Control Register(Default Value:0x0000)

Offset: 0x0322			Register Name: ADCMIXER_SR
Bit	**Read/Write**	**Default/Hex**	**Description**
15	R/W	0x0	/
14:8	R/W	0x0	RADCMIXMUTE Right ADC Mixer Mute Control 0: Mute 1:On Bit 14: MIC1 Boost stage Bit 13: MIC2 Boost stage Bit 12: Reserved Bit 11: Reserved

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			Bit 10: Reserved Bit 9: Right output mixer Bit 8: Left output mixer
7	R/W	0x0	/
6:0	R/W	0x0	LADCMIXMUTE Left ADC Mixer Mute Control 0: Mute 1: Not mute Bit 6: MIC1 Boost stage Bit 5: MIC2 Boost stage Bit 4: Reserved Bit 3: Reserved Bit 2: Reserved Bit 1: Left output mixer Bit 0: Right output mixer

7.5.4.22. Bias Control Register(Default Value:0x8900)

Offset: 0x032A			**Register Name: ANALOG_TUNING0**
Bit	**Read/Write**	**Default/Hex**	**Description**
15	R/W	0x1	ALDOEN Analog LDO enable 0: disable 1: enable
14:12	R/W	0x0	/
11	R/W	0x1	DITHER ADC dither on/off control 0: dither off 1: dither on
10	/	/	/
9:8	R/W	0x1	DITHER_CLK_SELECT ADC dither clock select 00: ADC FS * (8/9), about 43kHz when FS=48kHz 01: ADC FS * (16/15), about 51kHz when FS=48kHz 10: ADC FS * (4/3), about 64kHz when FS=48kHz 11: ADC FS * (16/9), about 85kHz when FS=48kHz
7	R/W	0x0	LINEOUT_SPEED_SELECT LINEOUT setup speed control (for testing) 0: slow 1: fast
6	R/W	0x0	CURRENT_TEST_SELECT Internal current sink test enable (from MICIN1N pin) 0:Normal 1: For Debug

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5:0	/	/	/

7.5.4.23. Analog performance tuning Control Register(Default Value:0x5555)

Offset: 0x032C			Register Name: ANALOG_TUNING
Bit	**Read/Write**	**Default/Hex**	**Description**
15:14	R/W	0x1	OPDRV_OPCOM_CUR. OPDRV/OPCOM output stage current setting
13:12	R/W	0x1	OPADC1_BIAS_CUR. OPADC1 Bias Current Select
11:10	R/W	0x1	OPADC2_BIAS_CUR. OPADC2 Bias Current Select
9:8	R/W	0x1	OPAAF_BIAS_CUR. OPAAF in ADC Bias Current Select
7:6	R/W	0x1	OPMIC_BIAS_CUR OPMIC Bias Current Control
5:4	R/W	0x1	OPVR_BIAS_CUR. OPVR Bias Current Control
3:2	R/W	0x1	OPDAC_BIAS_CUR. OPDAC Bias Current Control
1:0	R/W	0x1	OPMIX_BIAS_CUR. OPMIX/OPLPF/OPDRV/OPCOM Bias Current Control

7.5.4.24. ADC DAP Function Selected Register(Default Value:0x0000)

Offset: 0x0480			Register Name: AC_AGC_SEL
Bit	**Read/Write**	**Default/Hex**	**Description**
15:2	/	/	/
1	R/W	0x0	/
0	R/W	0x0	AGC_SEL AGC Function selected Control 0: disable 1: enable

7.5.4.25. ADC DAP Left Channel Control Register(Default Value:0x0000)

Offset: 0x0500			Register Name: AC_ADC_DAPLCTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
15	/	/	/
14	R/W	0x0	Left AGC enable 0: disable

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			1: enable
13	R/W	0x0	Left HPF enable 0: disable 1: enable
12	R/W	0x0	Left Noise detect enable 0: disable 1: enable
11:10	R/W	0x0	Reserved
9:8	R/W	0x0	Left Hysteresis setting 00: 1dB 01: 2dB 10: 4dB 11: disable;
7:4	R/W	0x0	Left Noise debounce time 0000: disable 0001: 4/fs 0010: 8/fs ---------- 1111: 16*4096/fs $T=2^{(N+1)}/fs$, except N=0
3:0	R/W	0x0	Left Signal debounce time 0000: disable 0001: 4/fs 0010: 8/fs ---------- 1111: 16*4096/fs $T=2^{(N+1)}/fs$, except N=0

7.5.4.26. ADC DAP Right Channel Control Register(Default Value:0x0000)

Offset: 0x0502			**Register Name: AC_ADC_DAPRCTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
15	/	/	/
14	R/W	0x0	Right AGC enable 0: disable 1: enable
13	R/W	0x0	Right HPF enable 0: disable 1: enable
12	R/W	0x0	Right Noise detect enable 0: disable 1: enable
11:10	R/W	0x0	Reserved
9: 8	R/W	0x0	Right Hysteresis setting

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			00: 1dB 01: 2dB 10: 4dB 11: disable
7: 4	R/W	0x0	Right Noise debounce time 0000: disable 0001: 4/fs 0010: 8/fs ---------- 1111: 16*4096/fs $T=2^{(N+1)}/fs$,except N=0
3: 0	R/W	0x0	Right Signal debounce time 0000: disable 0001: 4/fs 0010: 8/fs ---------- 1111: 16*4096/fs $T=2^{(N+1)}/fs$, except N=0

7.5.4.27. ADC DAP Left Status Register(Default Value:0x0000)

Offset: 0x0504			Register Name: AC_ADC_DAPLSTA
Bit	**Read/Write**	**Default/Hex**	**Description**
15:10	R	0x0	Reserved
9	R	0x0	Left AGC saturation flag
8	R	0x0	Left AGC noise-threshold flag
7:0	R	0x0	Left Gain applied by AGC (7.1 format 2s complement(-20dB – 40dB), 0.5B/ step) 0x50: 40dB 0x4F: 39.5dB ---------- 0x00: 00dB 0xFF: -0.5dB

7.5.4.28. ADC DAP Right Status Register(Default Value:0x0000)

Offset: 0x0506			Register Name: AC_ADC_DAPRSTA
Bit	**Read/Write**	**Default/Hex**	**Description**
11:10	R	0x0	Reserved
9	R	0x0	Right AGC saturation flag
8	R	0x0	Right AGC noise-threshold flag
7:0	R	0x0	Right Gain applied by AGC (7.1 format 2s complement(-20dB – 40dB), 0.5dB /step)

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			0x50: 40dB 0x4F: 39.5dB ---------- 0x00: 00dB 0xFF: -0.5dB

7.5.4.29. ADC DAP Left Target Level Register(Default Value:0x2C28)

Offset: 0x0508			Register Name: AC_ADC_DAPLTL
Bit	**Read/Write**	**Default/Hex**	**Description**
15:14	/	/	/
13:8	R/W	0x2C(-20dB)	Left channel target level setting(-1dB -- -30dB).(6.0format 2s complement)
7:0	R/W	0x28(20dB)	Left channel max gain setting(0-40dB).(7.1format 2s complement)

7.5.4.30. ADC DAP Right Target Level Register(Default Value:0x2C28)

Offset: 0x050A			Register Name: AC_ADC_DAPRTL
Bit	**Read/Write**	**Default/Hex**	**Description**
15:14	/	/	/
13:8	R/W	0x2C (-20dB)	Right channel target level setting(-1dB -- -30dB).(6.0format 2s complement)
7:0	R/W	0x28 (20dB)	Right channel max gain setting (0-40dB). (7.1format 2s complement)

7.5.4.31. ADC DAP Left High Average Coef Register(Default Value:0x0005)

Offset: 0x050C			Register Name: AC_ADC_DAPLHAC
Bit	**Read/Write**	**Default/Hex**	**Description**
15:11	/	/	/
10:0	R/W	0x0005	Left channel output signal average level coefficient setting(the coefficient [reg06[10:0],reg07] is 3.24 format 2s complement)

7.5.4.32. ADC DAP Left Low Average Coef Register(Default Value:0x1EB8)

Offset: 0x050E			Register Name: AC_ADC_DAPLLAC
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x1EB8	Left channel output signal average level coefficient setting(the coefficient [reg07[10:0],reg08] is 3.24 format 2s complement)

7.5.4.33. ADC DAP Right High Average Coef Register(Default Value:0x0005)

Offset: 0x0510	Register Name: AC_ADC_DAPRHAC

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Bit	Read/Write	Default/Hex	Description
15:11	/	/	/
10:0	R/W	0x0005	Right channel output signal average level coefficient setting(the coefficient [reg08[10:0],reg09] is 3.24 format 2s complement)

7.5.4.34. ADC DAP Right Low Average Coef Register(Default Value:0x1EB8)

Offset: 0x0512			Register Name: AC_ADC_DAPRLAC
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x1EB8	Right channel output signal average level coefficient setting(the coefficient [reg08[10:0],reg09] is 3.24 format 2s complement)

7.5.4.35. ADC DAP Left Decay Time Register(Default Value:0x001F)

Offset: 0x0514			Register Name: AC_ADC_DAPLDT
Bit	**Read/Write**	**Default/Hex**	**Description**
15	/	/	/
14:0	R/W	0x001F (32x32fs)	Left decay time coefficient setting 0000: 1x32/fs 0001: 2x32/fs ---------- 7FFF: 2^{15} x32/fs T=(n+1)*32/fs When the gain increases, the actual gain will increase 0.5dB at every decay time.

7.5.4.36. ADC DAP Left Attack Time Register(Default Value:0x0000)

Offset: 0x0516			Register Name: AC_ADC_DAPLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
15	/	/	/
14:0	R/W	0x0000	Left attack time coefficient setting 0000: 1x32/fs 0001: 2x32/fs ---------- 7FFF: 2^{15} x32/fs T=(n+1)*32/fs When the gain decreases, the actual gain will decrease 0.5dB at every attack time.

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7.5.4.37. ADC DAP Right Decay Time Register(Default Value:0x001F)

Offset: 0x0518			Register Name: AC_ADC_DAPRDT
Bit	**Read/Write**	**Default/Hex**	**Description**
15	/	/	/
14:0	R/W	0x001F (32x32fs)	Right decay time coefficient setting 0000: 1x32/fs 0001: 2x32/fs ---------- 7FFF: 2^{15} x32/fs T=(n+1)*32/fs When the gain increases, the actual gain will increase 0.5dB at every decay time.

7.5.4.38. ADC DAP Right Attack Time Register(Default Value:0x0000)

Offset: 0x051A			Register Name: AC_ADC_DAPRAT
Bit	**Read/Write**	**Default/Hex**	**Description**
15	/	/	/
14:0	R/W	0x0000	Right attack time coefficient setting 0000: 1x32/fs 0001: 2x32/fs ---------- 7FFF: 2^{15} x32/fs T=(n+1)*32/fs When the gain decreases, the actual gain will decrease 0.5dB at every attack time.

7.5.4.39. ADC DAP Noise Threshold Register(Default Value:0x1E1E)

Offset: 0x051C			Register Name: AC_ADC_DAPNTH
Bit	**Read/Write**	**Default/Hex**	**Description**
15:13	/	/	/
12:8	R/W	0x1E(-90dB)	Left channel noise threshold setting. 0x00: -30dB 0x01: -32dB 0x02: -34dB ---------- 0x1D: -88dB 0x1E: -90dB 0x1F: -90dB(the same as 0x1E)
7:5	/	/	/
4:0	R/W	0x1E(-90dB)	Right channel noise threshold setting(-90 -- -30dB).

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			0x00: -30dB 0x01: -32dB 0x02: -34dB ---------- 0x1D: -88dB 0x1E: -90dB 0x1F: -90dB(the same as 0x1E)

7.5.4.40. ADC DAP Left Input Signal High Average Coef Register(Default Value:0x0005)

Offset: 0x051E			Register Name: AC_ADC_DAPLHNAC
Bit	**Read/Write**	**Default/Hex**	**Description**
15:11	/	/	/
10:0	R/W	0x0005	Left input signal average filter coefficient to check noise or not(the coefficient [reg0f[10:0],reg10] is 3.24 format 2s complement), always the same as the left output signal average filter's.

7.5.4.41. ADC DAP Left Input Signal Low Average Coef Register(Default Value:0x1EB8)

Offset: 0x0520			Register Name: AC_ADC_DAPLLNAC
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x1EB8	Left input signal average filter coefficient to check noise or not(the coefficient [reg0f[10:0],reg10] is 3.24 format 2s complement) always the same as the left output signal average filter's

7.5.4.42. ADC DAP Right Input Signal High Average Coef Register(Default Value:0x0005)

Offset: 0x0522			Register Name: AC_ADC_DAPRHNAC
Bit	**Read/Write**	**Default/Hex**	**Description**
15:11	/	/	/
10:0	R/W	0x0005	Right input signal average filter coefficient to check noise or not(the coefficient [reg11[10:0],reg12] is 3.24 format 2s complement), always the same as the right output signal average filter's

7.5.4.43. ADC DAP Right Input Signal Low Average Coef Register(Default Value:0x1EB8)

Offset: 0x0524			Register Name: AC_ADC_DAPRLNAC
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x1EB8	Right input signal average filter coefficient to check noise or not(the coefficient [reg11[10:0],reg12] is 3.24 format 2s complement), always the same as the right output signal average filter's

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7.5.4.44. ADC DAP High HPF Coef Register(Default Value:0x00FF)

Offset: 0x0526			Register Name: AC_DAPHHPFC
Bit	**Read/Write**	**Default/Hex**	**Description**
15:11	/	/	/
10:0	R/W	0x00FF	HPF coefficient setting(the coefficient [reg13[10:0],reg14] is 3.24 format 2s complement)

7.5.4.45. ADC DAP Low HPF Coef Register(Default Value:0xFAC1)

Offset: 0x0528			Register Name: AC_DAPLHPFC
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0xFAC1	HPF coefficient setting(the coefficient [reg13[10:0],reg14] is 3.24 format 2s complement)

7.5.4.46. ADC DAP Optimum Register(Default Value:0x0000)

Offset: 0x052A			Register Name: AC_DAPOPT
Bit	**Read/Write**	**Default/Hex**	**Description**
15:11	/	/	/
10	R/W	0x0	Left energy default value setting(include the input and output) 0: min 1: max
9:8	R/W	0x0	Left channel gain hystersis setting. The different between target level and the signal level must larger than the hystersis when the gain change. 00: 0.4375db 01: 0.9375db 10: 1.9375db 11: 3db
7:6	/	/	/
5	R/W	0x0	The input signal average filter coefficient setting 0: is the [reg0f[10:0], reg10] and [reg11[1:0], reg12]; 1: is the [reg06[10:0], reg07] and [reg08[1:0], reg09];
4	R/W	0x0	AGC output when the channel in noise state 0: output is zero 1: output is the input data
3	/	/	/
2	R/W	0x0	Right energy default value setting(include the input and output) 0: min 1: max

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1:0	R/W	0x0	Right channel gain hystersis setting. The different between target level and the signal level must larger than the hystersis when the gain change. 00: 0.4375db 01: 0.9375db 10: 1.9375db 11: 3db

7.5.4.47. DAC DAP Channel Control Register(Default Value:0x0000)

Offset: 0x1000			Register Name: AC_DAC_DAPCTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
15:3	/	/	/
2	R/W	0x0	DRC enable control 0: disable 1: enable
1	R/W	0x0	DRC Left channel HPF enable control 0: disable 1: enable
0	R/W	0x0	DRC Right channel HPF enable control 0: disable 1: enable

7.5.4.48. DRC High HPF Coef Register(Default Value:0x00FF)

Offset: 0x1002			Register Name: AC_DRC_HHPFC
Bit	**Read/Write**	**Default/Hex**	**Description**
15:11	/	/	/
10:0	R/W	0xFF	HPF coefficient setting and the data is 3.24 format.

7.5.4.49. DRC Low HPF Coef Register(Default Value:0xFAC1)

Offset: 0x1004			Register Name: AC_DRC_LHPFC
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0xFAC1	HPF coefficient setting and the data is 3.24 format.

7.5.4.50. DRC Control Register(Default Value:0x0080)

Offset: 0x1006			Register Name: AC_DRC_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
15	R	0x0	DRC delay buffer data output state when drc delay function is enble and the

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			drc funciton disable. After disable drc function and this bit go to 0, the user should write the drc delay function bit to 0; 0 : not complete 1 : is complete
14	/	/	/
13:8	R/W	0x0	Signal delay time setting 6'h00 : (8x1)fs 6'h01 : (8x2)fs 6'h02 : (8x3)fs ---------- 6'h2e : (8*47)fs 6'h2f : (8*48)fs 6'h30 -- 6'h3f : (8*48)fs Delay time = 8*(n+1)fs, n<6'h30; When the delay function is disable, the signal delay time is unused.
7	R/W	0x1	The delay buffer use or not when the drc disable and the drc buffer data output completely 0 : don't use the buffer 1 : use the buffer
6	R/W	0x0	DRC gain max limit enable 0 : disable 1 : enable
5	R/W	0x0	DRC gain min limit enable. when this fuction enable, it will overwrite the noise detect funciton. 0 : disable 1 : enable
4	R/W	0x0	Control the drc to detect noise when ET enable 0 : disable 1 : enable
3	R/W	0x0	Signal function Select 0 : RMS filter 1 : Peak filter When Signal function Select Peak filter, the RMS parameter is unused. (AC_DRC_LRMSHAT / AC_DRC_LRMSLAT / AC_DRC_LRMSHAT / AC_DRC_LRMSLAT) When Signal function Select RMS filter, the Peak filter parameter is unused.(AC_DRC_LPFHAT / AC_DRC_LPFLAT / AC_DRC_RPFHAT / AC_DRC_RPFLAT / AC_DRC_LPFHRT / AC_DRC_LPFLRT / AC_DRC_RPFHRT / AC_DRC_RPFLRT)
2	R/W	0x0	Delay function enable 0 : disable 1 : enable When the bit is 0, the Signal delay time is unused.
1	R/W	0x0	DRC LT enable 0 : disable

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			1 : enable When the bit is 0, Kl and OPL parameter is unused.
0	R/W	0x0	DRC ET enable 0 : disable 1 : enable When the bit is 0, Ke and OPE parameter is unused.

7.5.4.51. DRC Left Peak Filter High Attack Time Coef Register(Default Value:0x000B)

Offset: 0x1008			Register Name: AC_DRC_LPFHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
15:11	/	/	/
10:0	R/W	0x000B	The left peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

7.5.4.52. DRC Left Peak Filter Low Attack Time Coef Register(Default Value:0x77BF)

Offset: 0x100A			Register Name: AC_DRC_LPFLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x77BF	The left peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

7.5.4.53. DRC Right Peak Filter High Attack Time Coef Register(Default Value:0x000B)

Offset: 0x100C			Register Name: AC_DRC_RPFHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
15:11	/	/	/
10:0	R/W	0x000B	The left peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

7.5.4.54. DRC Peak Filter Low Attack Time Coef Register(Default Value:0x77BF)

Offset: 0x100E			Register Name: AC_DRC_RPFLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x77BF	The left peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

7.5.4.55. DRC Left Peak Filter High Release Time Coef Register(Default Value:0x00FF)

Offset: 0x1010	Register Name: AC_DRC_LPFHRT

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Bit	Read/Write	Default/Hex	Description
15:11	/	/	/
10:0	R/W	0x00FF	The left peak filter release time parameter setting, which determine by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

7.5.4.56. DRC Left Peak Filter Low Release Time Coef Register(Default Value:0xE1F8)

Offset: 0x1012			Register Name: AC_DRC_LPFLRT
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0xE1F8	The left peak filter release time parameter setting, which determine by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

7.5.4.57. DRC Right Peak filter High Release Time Coef Register(Default Value:0x00FF)

Offset: 0x1014			Register Name: AC_DRC_RPFHRT
Bit	Read/Write	Default/Hex	Description
15:11	/	/	/
10:0	R/W	0x00FF	The left peak filter attack time parameter setting, which determine by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

7.5.4.58. DRC Right Peak filter Low Release Time Coef Register(Default Value:0xE1F8)

Offset: 0x1016			Register Name: AC_DRC_RPFLRT
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0xE1F8	The left peak filter release time parameter setting, which determine by the equation that AT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

7.5.4.59. DRC Left RMS Filter High Coef Register(Default Value:0x0001)

Offset: 0x1018			Register Name: AC_DRC_LRMSHAT
Bit	Read/Write	Default/Hex	Description
15:11	/	/	/
10:0	R/W	0x0001	The left RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

7.5.4.60. DRC Left RMS Filter Low Coef Register(Default Value:0x2BAF)

Offset: 0x101A			Register Name: AC_DRC_LRMSLAT
Bit	Read/Write	Default/Hex	Description

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15:0	R/W	0x2BAF	The left RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

7.5.4.61. DRC Right RMS Filter High Coef Register(Default Value:0x0001)

Offset: 0x101C			Register Name: AC_DRC_RRMSHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
15:11	/	/	/
10:0	R/W	0x0001	The right RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

7.5.4.62. DRC Right RMS Filter Low Coef Register(Default Value:0x2BAF)

Offset: 0x101E			Register Name: AC_DRC_RRMSLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x2BAF	The right RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

7.5.4.63. DRC Compressor Threshold High Setting Register(Default Value:0x06A4)

Offset: 0x1020			Register Name: AC_DRC_HCT
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x06A4	The compressor threshold setting, which set by the equation that CTin = -CT/6.0206. The format is 8.24 (-40dB)

7.5.4.64. DRC Compressor Threshold High Setting Register(Default Value:0xD3C0)

Offset: 0x1022			Register Name: AC_DRC_LCT
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0xD3C0	The compressor threshold setting, which set by the equation that CTin = -CT/6.0206. The format is 8.24 (-40dB)

7.5.4.65. DRC Compressor Slope High Setting Register(Default Value:0x0800)

Offset: 0x1024			Register Name: AC_DRC_HKC
Bit	**Read/Write**	**Default/Hex**	**Description**
15:13	/	/	/
13:0	R/W	0x0800	The slope of the compressor which determine by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is interger. The format is 8.24. (2 : 1)

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7.5.4.66. DRC Compressor Slope Low Setting Register(Default Value:0x0000)

Offset: 0x1026			Register Name: AC_DRC_LKC
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x0000	The slope of the compressor which determine by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is interger. The format is 8.24. (2 : 1)

7.5.4.67. DRC Compressor High Output at Compressor Threshold Register(Default Value:0xF95B)

Offset: 0x1028			Register Name: AC_DRC_HOPC
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0xF95B	The output of the compressor which determine by the equation -OPC/6.0206 The format is 8.24 (-40dB)

7.5.4.68. DRC Compressor Low Output at Compressor Threshold Register(Default Value:0x2C3F)

Offset: 0x102A			Register Name: AC_DRC_LOPC
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x2C3F	The output of the compressor which determine by the equation OPC/6.0206 The format is 8.24 (-40dB)

7.5.4.69. DRC Limiter Threshold High Setting Register(Default Value:0x01A9)

Offset: 0x102C			Register Name: AC_DRC_HLT
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x01A9	The limiter threshold setting, which set by the equation that LTin = -LT/6.0206, The format is 8.24. (-10dB)

7.5.4.70. DRC Limiter Threshold Low Setting Register(Default Value:0x34F0)

Offset: 0x102E			Register Name: AC_DRC_LLT
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x34F0	The limiter threshold setting, which set by the equation that LTin = -LT/6.0206, The format is 8.24. (-10dB)

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7.5.4.71. DRC Limiter Slope High Setting Register(Default Value:0x0005)

Offset: 0x1030			Register Name: AC_DRC_HKl
Bit	Read/Write	Default/Hex	Description
15:11	/	/	/
13:0	R/W	0x0005	The slope of the limiter which determine by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is interger. The format is 8.24. (50 :1)

7.5.4.72. DRC Limiter Slope Low Setting Register(Default Value:0x1EB8)

Offset: 0x1032			Register Name: AC_DRC_LKl
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x1EB8	The slope of the limiter which determine by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is interger. The format is 8.24. (50 :1)

7.5.4.73. DRC Limiter High Output at Limiter Threshold(Default Value:0xFBD8)

Offset: 0x1034			Register Name: AC_DRC_HOPL
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0xFBD8	The output of the limiter which determine by equation OPT/6.0206. The format is 8.24 (-25dB)

7.5.4.74. DRC Limiter Low Output at Limiter Threshold(Default Value:0xFBA7)

Offset: 0x1036			Register Name: AC_DRC_LOPL
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0xFBA7	The output of the limiter which determine by equation OPT/6.0206. The format is 8.24 (-25dB)

7.5.4.75. DRC Expander Threshold High Setting Register(Default Value:0x0BA0)

Offset: 0x1038			Register Name: AC_DRC_HET
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x0BA0	The expander threshold setting, which set by the equation that ETin = -ET/6.0206, The format is 8.24. (-70dB)

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7.5.4.76. DRC Expander Threshold Low Setting Register(Default Value:0x7291)

Offset: 0x103A			Register Name: AC_DRC_LET
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x7291	The expander threshold setting, which set by the equation that ETin = -ET/6.0206, The format is 8.24. (-70dB)

7.5.4.77. DRC Expander Slope High Setting Register(Default Value:0x0050)

Offset: 0x103C			Register Name: AC_DRC_HKE
Bit	**Read/Write**	**Default/Hex**	**Description**
15:14			
13:0	R/W	0x0050	The slope of the expander which determine by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is interger and the ke must larger than 50. The format is 8.24. (1:5)

7.5.4.78. DRC Expander Slope Low Setting Register(Default Value:0x0000)

Offset: 0x103E			Register Name: AC_DRC_LKE
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x0000	The slope of the expander which determine by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is interger and the ke must larger than 50. The format is 8.24. (1:5)

7.5.4.79. DRC Expander High Output at Expander Threshold(Default Value:0xF45F)

Offset: 0x1040			Register Name: AC_DRC_HOPE
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0xF45F	The output of the expander which determine by equation OPE/6.0206. The format is 8.24 (-70dB)

7.5.4.80. DRC Expander Low Output at Expander Threshold(Default Value:0x8D6E)

Offset: 0x1042			Register Name: AC_DRC_LOPE
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x8D6E	The output of the expander which determine by equation OPE/6.0206. The format is 8.24 (-70dB)

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7.5.4.81. DRC Linear Slope High Setting Register(Default Value:0x0100)

Offset: 0x1044			Register Name: AC_DRC_HKN
Bit	Read/Write	Default/Hex	Description
15:14	/	/	/
13:0	R/W	0x0100	The slope of the linear which determine by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is interger . The format is 8.24. (1:1)

7.5.4.82. DRC Linear Slope Low Setting Register(Default Value:0x0000)

Offset: 0x1046			Register Name: AC_DRC_LKN
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x0000	The slope of the linear which determine by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is interger . The format is 8.24. (1:1)

7.5.4.83. DRC Smooth Filter Gain High Attack Time Coef Register(Default Value:0x0002)

Offset: 0x1048			Register Name: AC_DRC_SFHAT
Bit	Read/Write	Default/Hex	Description
15:11	/	/	/
10:0	R/W	0x0002	The smooth filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (5ms)

7.5.4.84. DRC Smooth Filter Gain Low Attack Time Coef Register(Default Value:0x5600)

Offset: 0x104A			Register Name: AC_DRC_SFLAT
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x5600	The smooth filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (5ms)

7.5.4.85. DRC Smooth filter Gain High Release Time Coef Register(Default Value:0x0000)

Offset: 0x104C			Register Name: AC_DRC_SFHRT
Bit	Read/Write	Default/Hex	Description
15:11	/	/	/
10:0	R/W	0x0000	The gain smooth filter release time parameter setting, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (200ms)

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7.5.4.86. DRC Smooth filter Gain Low Release Time Coef Register(Default Value:0x0F04)

Offset: 0x104E			Register Name: AC_DRC_SFLRT
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x0F04	The gain smooth filter release time parameter setting, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (200ms)

7.5.4.87. DRC MAX Gain High Setting Register(Default Value:0xFE56)

Offset: 0x1050			Register Name: AC_DRC_MXGHS
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0xFE56	The max gain setting which determine by equation MXG/6.0206. The format is 8.24 and must -20dB <MXG< 30dB (-10dB)

7.5.4.88. DRC MAX Gain Low Setting Register(Default Value:0xCB0F)

Offset: 0x1052			Register Name: AC_DRC_MXGLS
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0xCB0F	The max gain setting which determine by equation MXG/6.0206. The format is 8.24 and must -20dB <MXG < 30dB (-10dB)

7.5.4.89. DRC MIN Gain High Setting Register(Default Value:0xF95B)

Offset: 0x1054			Register Name: AC_DRC_MNGHS
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0xF95B	The min gain setting which determine by equation MXG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -30dB (-30dB)

7.5.4.90. DRC MIN Gain Low Setting Register(Default Value:0x2C3F)

Offset: 0x1056			Register Name: AC_DRC_MNGLS
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x2C3F	The min gain setting which determine by equation MNG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -30dB (-30dB)

7.5.4.91. DRC Expander Smooth Time High Coef Register(Default Value:0x0000)

Offset: 0x1058			Register Name: AC_DRC_EPSHC
Bit	**Read/Write**	**Default/Hex**	**Description**
11:0	R/W	0x0000	The gain smooth filter release and attack time parameter setting in

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			expander region, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (30ms)

7.5.4.92. DRC Expander Smooth Time Low Coef Register(Default Value:0x640C)

Offset: 0x105A			Register Name: AC_DRC_EPSLC
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x640C	The gain smooth filter release and attack time parameter setting in expander region, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (30ms)

7.5.4.93. DRC HPF Gain High Coef Register(Default Value:0x0100)

Offset: 0x105E			Register Name: AC_DRC_HPFHGAIN
Bit	**Read/Write**	**Default/Hex**	**Description**
15:11	/	/	/
10:0	R/W	0x0100	The gain of the hpf coefficient setting which format is 3.24.(gain = 1)

7.5.4.94. DRC HPF Gain Low Coef Register(Default Value:0x0000)

Offset: 0x1060			Register Name: AC_DRC_HPFLGAIN
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x0000	The gain of the hpf coefficient setting which format is 3.24.(gain = 1)

7.5.4.95. DRC Bist control Register(Default Value:0x0000)

Offset: 0x1100			Register Name: AC_DRC_BISTCR
Bit	**Read/Write**	**Default/Hex**	**Description**
15:13	R/W	0x0	DRC SRAM BIST Register Select
12	R/W	0x0	DRC SRAM BIST Address MODE Select
11:9	R/W	0x0	DRC SRAM BIST Write Data Pattern 000: 0x0000_0000 001: 0x5555_5555 010: 0x3333_3333 011: 0x0f0f_0f0f 100: 0x00ff_00ff 101: 0x0000_ffff Others: reserved.
8	R/W	0x0	DRC SRAM BIST Enable A positive edge will trigger the SRAM BIST to start
7:0	/	/	/

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7.5.4.96. DRC Bist Status Register(Default Value:0x0020)

Offset: 0x1102			Register Name: AC_DRC_BISTST
Bit	**Read/Write**	**Default/Hex**	**Description**
15:8	/	/	/
7	R	0x0	DRC SRAM BIST Error Status 0: No Error 1: Error
6:4	R	0x0	DRC SRAM BIST Error Pattern
3:2	R	0x0	DRC SRAM BIST Error Cycles
1	R	0x1	DRC SRAM BIST Stop 0: Running 1: Stop
0	R	0x0	DRC SRAM BIST Busy 0: Idle 1: Busy

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Chapter 8 Interfaces

This chapter describes the H6 V200 interfaces, including:

- TWI
- SPI
- UART
- USB2.0 OTG
- USB3.0 Host Controller
- USB2.0 Host Controller
- SCR
- EMAC
- TSC
- One Wire Interface
- CIR Transmitter
- CIR Receiver
- EPHY
- PCIe

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8.1. TWI

8.1.1. Overview

This TWI Controller is designed as an interface between CPU host and the serial TWI bus. It can support all the standard TWI transfer, including Slave and Master. The communication of the 2-wire bus is carried out by a byte-wise mode based on interrupt or polled handshaking. This TWI Controller can be operated in standard mode (100 kbit/s) or fast-mode, supporting data rate up to 400 kbit/s. Multiple Masters and 10-bit addressing Mode are supported for this specified application. General Call Addressing is also supported in Slave mode

Features:

- Software-programmable for slave or master
- Supports repeated START signal
- Allows 10-bit addressing with TWI bus
- Performs arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Supports speed up to 400 kbit/s (‘fast mode’)
- Allows operation from a wide range of input clock frequencies

8.1.2. Block Diagram

Figure 8-1 shows the block diagram of TWI.

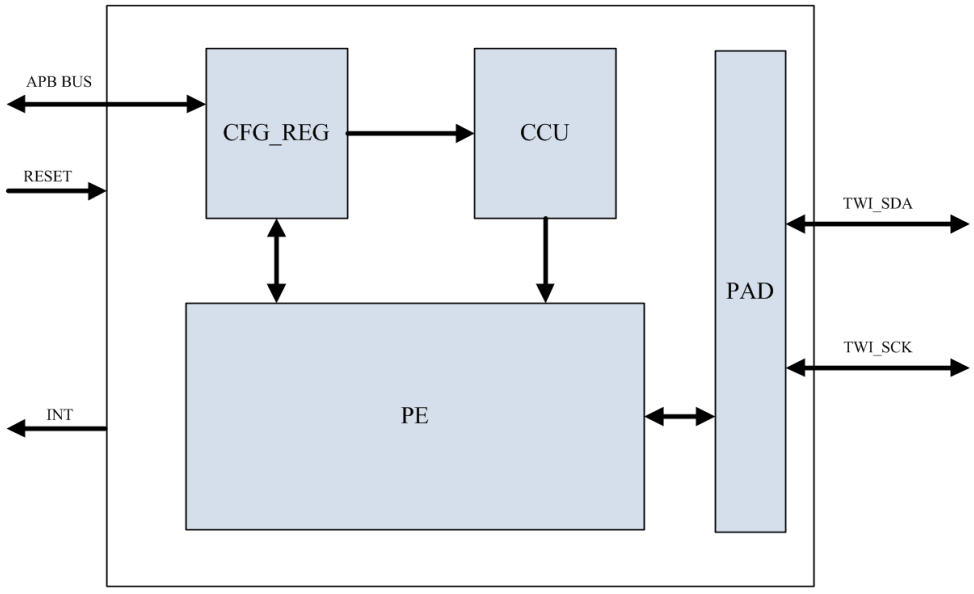


Figure 8-1. TWI Block Diagram

RESET: Module reset signal

INT: Module output interrupt signal

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CFG_REG: Module configuration register in TWI
PE: Packet encoding/decoding
CCU: Module clock controller unit

8.1.3. Operations and Functional Descriptions

8.1.3.1. External Signals

Table 8-1 describes the external signals of TWI. TWI_SCK and TWI_SDA are bidirectional I/O,When TWI is configured as Master device,TWI_SCK is output pin;when TWI is configurable as Slave device,TWI_SCK is input pin.other TWI ports are used as General Purpose I/O ports.For information about General Purpose I/O ports,see **Port Controller** in chapter3.

Table 8-1. TWI External Signals

Signal (x=[2:0])	Description	Type
TWIx_SCK	TWI Clock Signal for CPUX	I/O
TWIx_SDA	TWI Serial Data for CPUX	I/O
S_TWI_SCK	TWI Serial Clock Signal for CPUS	I/O
S_TWI_SDA	TWI Serial Data Signal for CPUS	I/O

8.1.3.2. Clock Sources

Each TWI controller has a fixed clock source.APB2 is the clock source of TWI in CPUX and APBS is the clock source of R-TWI in CPUS.The APB Bus get some clock sources.Users can select one of them to be used as APB clock.Table 8-2 describes the clock sources for TWI.Users can see **Clock Controller Unit(CCU)** in chapter3 for clock setting,configuration and gating information.

Table 8-2. TWI Clock Sources

Clock Sources	Description
APBS Bus	R-TWI in CPUS,for details on APBS refer to CCU
APB2 Bus	TWI in CPUX,for details on APB2 refer to CCU

After select a proper clock, for using the TWI in CPUX,user must open the gating of TWI and release the reset bit. For using the TWI in CPUS,user also need to open the gating of R-TWI and release the reset bit .

For more details on the gating/reset operations ,please refer to the **CCU.**

8.1.3.3. Timing Diagram

Data transferred are always in a unit of 8-bit (1 byte), followed by an acknowledge bit. The number of bytes that can be transmitted is unrestricted. Data is transferred in serial with the MSB first. Between each byte of data transfer, a receiver device will hold the clock line SCK low to force the transmitter into a wait state while waiting the response

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from microprocessor.

The clock line is driven by the master all the time, including the acknowledge-related clock cycle, except for the SCK holding between each byte. After sending each byte, the transmitter releases the SDA line to allow the receiver to pull down the SDA line and send an acknowledge signal (or pull it high to send a "not acknowledge") to the transmitter.

When a slave receiver does not acknowledge the slave address (unable to receive because of no resource available), the data line must be pulled high by the slave so that the master can generate a STOP condition to stop the transfer. When the acknowledge signal is pulled high, slave receiver no longer sends more data. And the master should generate the STOP condition to stop the transfer.

Figure 8-2 provides an illustration the relation of SDA signal line and SCK signal line on the TWI serial bus.

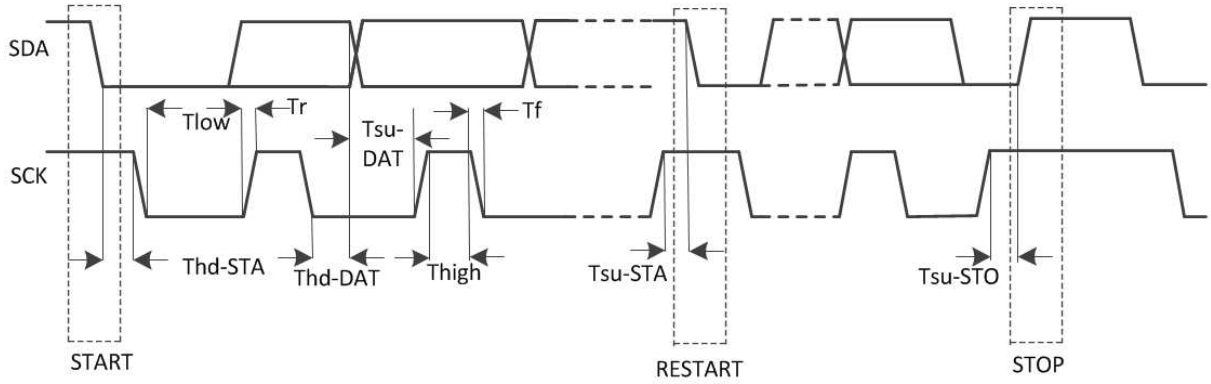


Figure 8-2. TWI Timing Diagram

The timing parameters of TWI timing shows in Table 8-3.

Table 8-3. TWI Timing Constants

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCK clock frequency	Fsck	0	100	0	400	kHz
Setup time in Start	Tsu-STA	4.7	-	0.6	-	us
Hold time in Start	Thd-STA	4.0	-	0.6	-	us
Setup time in Data	Tsu-DAT	250	-	100	-	ns
Hold time in Data	Thd-DAT	5.0	-	-	-	ns
Setup time in Stop	Tsu-STO	4.0	-	0.6	-	us
SCK low level time	Tlow	4.7	-	1.3	-	us
SCK high level time	Thigh	4.0	-	0.6	-	us
SCK/SDA falling time	Tf	-	300	20	300	ns
SCK/SDA rising time	Tr	-	1000	20	300	ns

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8.1.3.4. TWI Controller Operation

There are four operation modes on the TWI bus which dictates the communications method. They are Master Transmit, Master Receive, Slave Transmit and Slave Receive. In general, CPU host controls TWI by writing commands and data to it's registers. TWI transmits an interrupt to CPU when each time a byte transfer is done or a START/STOP conditions is detected. The CPU host can also poll the status register for current status if the interrupt mechanism is not disabled by the CPU host.

When the CPU host wants to start a bus transfer, it initiates a bus START to enter the master mode by setting IM_STA bit of the 2WIRE_CNTR register to high (before it must be low). The TWI will assert INT line and INT_FLAG to indicate a completion for the START condition and each consequent byte transfer. At each interrupt, the micro-processor needs to check the 2WIRE_STAT register for current status. A transfer has to be concluded with STOP condition by setting M_STP bit to high.

In Slave Mode, the TWI also constantly samples the bus and look for its own slave address during addressing cycles. Once a match is found, it is addressed and interrupt the CPU host with the corresponding status. Upon request, the CPU host should read the status, read/write 2WIRE_DATA data register, and set the 2WIRE_CNTR control register. After each byte transfer, a slave device always halt the operation of remote master by holding the next low pulse on SCL line until the microprocessor responds to the status of previous byte transfer or START condition.

8.1.4. Programming Guildlines

The TWI controller operates in 8-bit data format.The data on the TWI_SDA line is always 8 bits long.At first,the TWI controller will sent a start condition.When in the addressing formats of 7-bit,TWI sends out a 8 bits message which include 7 MSB slave address and 1 LSB read/write flag.The least significant of the salve address indicates the direction of transmission.When TWI works in 10 bit slave address mode,the operation will be divided into two steps,for details on the operation please refer to Register 8.1.6.2.

Figure 8-3 shows a software operation flow of TWI Initialization.

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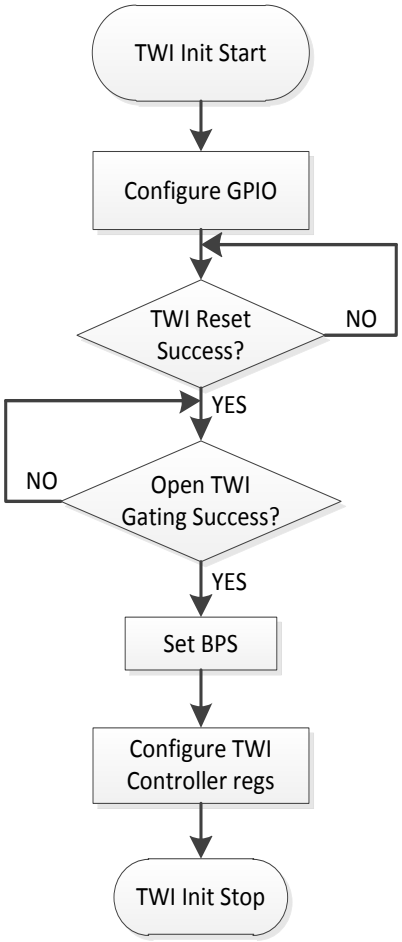


Figure 8-3. TWI Initial Flow

Figure 8-4 shows a software operation flow of TWI write to device.

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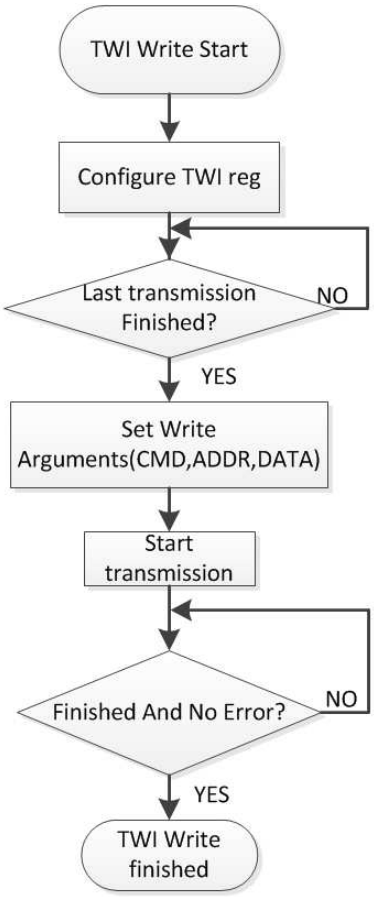


Figure 8-4. TWI Write Flow

Figure 8-5 shows a software operation flow of TWI read from device.

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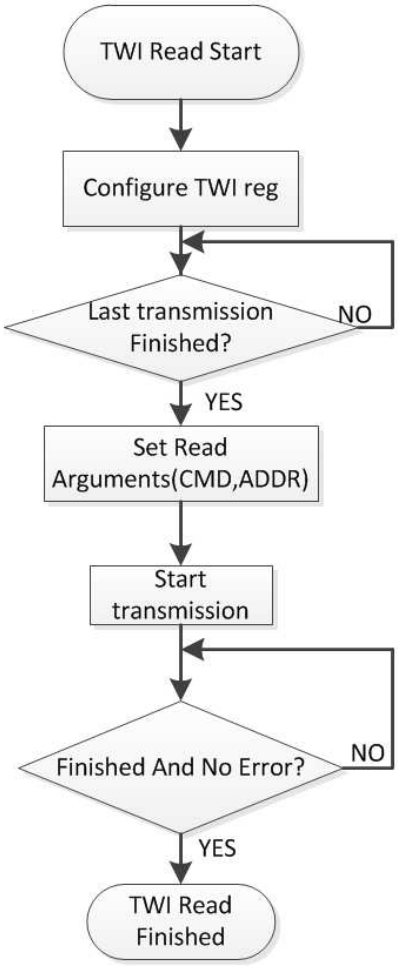


Figure 8-5. TWI Read Flow

8.1.5. Register List

Module Name	Base Address
TWI0	0x0500 2000
TWI1	0x0500 2400
TWI2	0x0500 2800
R-TWI	0x0708 1400

Register Name	Offset	Description
TWI_ADDR	0x0000	TWI Slave address
TWI_XADDR	0x0004	TWI Extended slave address
TWI_DATA	0x0008	TWI Data byte
TWI_CNTR	0x000C	TWI Control register
TWI_STAT	0x0010	TWI Status register
TWI_CCR	0x0014	TWI Clock control register
TWI_SRST	0x0018	TWI Software reset

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TWI_EFR	0x001C	TWI Enhance Feature register
TWI_LCR	0x0020	TWI Line Control register

8.1.6. Register Description

8.1.6.1. TWI Slave Address Register(Default Value:0x0000_0000)

Offset: 0x0000			Register Name: TWI_ADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:1	R/W	0x0	SLA Slave Address 7-bit addressing SLA6, SLA5, SLA4, SLA3, SLA2, SLA1, SLA0 10-bit addressing 1, 1, 1, 1, 0, SLAX[9:8]
0	R/W	0x0	GCE General Call Address Enable 0: Disable 1: Enable

NOTE

For 7-bit addressing:

SLA6 – SLA0 is the 7-bit address of the TWI when in slave mode. When the TWI receives this address after a START condition, it will generate an interrupt and enter slave mode. (SLA6 corresponds to the first bit received from the TWI bus.) If GCE is set to '1', the TWI will also recognize the general call address (00h).

For 10-bit addressing:

When the address received starts with 11110b, the TWI recognizes this as the first part of a 10-bit address and if the next two bits match ADDR[2:1] (i.e. SLAX9 and SLAX8 of the device's extended address), it sends an ACK. (The device does not generate an interrupt at this point.) If the next byte of the address matches the XADDR register (SLAX7 – SLAX0), the TWI generates an interrupt and goes into slave mode.

8.1.6.2. TWI Extend Address Register(Default Value:0x0000_0000)

Offset: 0x0004			Register Name: TWI_XADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	SLAX

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			Extend Slave Address SLAX[7:0]

8.1.6.3. TWI Data Register(Default Value:0x0000_0000)

Offset: 0x0008			Register Name: TWI_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	TWI_DATA Data byte for transmitting or received

8.1.6.4. TWI Control Register(Default Value:0x0000_0000)

Offset: 0x000C			Register Name: TWI_CNTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	INT_EN Interrupt Enable 0: The interrupt line always low 1: The interrupt line will go high when INT_FLAG is set.
6	R/W	0x0	BUS_EN TWI Bus Enable 0: The TWI bus inputs ISDA/ISCL are ignored and the TWI Controller will not respond to any address on the bus 1: The TWI will respond to calls to its slave address – and to the general call address if the GCE bit in the ADDR register is set. **NOTE** **In master operation mode, this bit should be set to '1'.**
5	R/WAC	0x0	M_STA Master Mode Start When M_STA is set to '1', TWI Controller enters master mode and will transmit a START condition on the bus when the bus is free. If the M_STA bit is set to '1' when the TWI Controller is already in master mode and one or more bytes have been transmitted, then a repeated START condition will be sent. If the M_STA bit is set to '1' when the TWI is being accessed in slave mode, the TWI will complete the data transfer in slave mode then enter master mode when the bus has been released. The M_STA bit is cleared automatically after a START condition has been sent: writing a '0' to this bit has no effect.
4	R/W1C	0x0	M_STP Master Mode Stop If M_STP is set to '1' in master mode, a STOP condition is transmitted on the

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			TWI bus. If the M_STP bit is set to '1' in slave mode, the TWI will behave as if a STOP condition has been received, but no STOP condition will be transmitted on the TWI bus. If both M_STA and M_STP bits are set, the TWI will first transmit the STOP condition (if in master mode) then transmit the START condition. The M_STP bit is cleared automatically: writing a '0' to this bit has no effect.
3	R/W1C	0x0	INT_FLAG Interrupt Flag INT_FLAG is automatically set to '1' when any of 28 (out of the possible 29) states is entered (see 'STAT Register' below). The only state that does not set INT_FLAG is state F8h. If the INT_EN bit is set, the interrupt line goes high when IFLG is set to '1'. If the TWI is operating in slave mode, data transfer is suspended when INT_FLAG is set and the low period of the TWI bus clock line (SCL) is stretched until '1' is written to INT_FLAG. The TWI clock line is then released and the interrupt line goes low.
2	R/W	0x0	A_ACK Assert Acknowledge When A_ACK is set to '1', an Acknowledge (low level on SDA) will be sent during the acknowledge clock pulse on the TWI bus if: 1. Either the whole of a matching 7-bit slave address or the first or the second byte of a matching 10-bit slave address has been received. 2. The general call address has been received and the GCE bit in the ADDR register is set to '1'. 3. A data byte has been received in master or slave mode. When A_ACK is '0', a Not Acknowledge (high level on SDA) will be sent when a data byte is received in master or slave mode. If A_ACK is cleared to '0' in slave transmitter mode, the byte in the DATA register is assumed to be the 'last byte'. After this byte has been transmitted, the TWI will enter state C8h then return to the idle state (status code F8h) when INT_FLAG is cleared. The TWI will not respond as a slave unless A_ACK is set.
1:0	/	/	/

8.1.6.5. TWI Status Register(Default Value:0x0000_00F8)

Offset: 0x0010			Register Name: TWI_STAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0xF8	STA Status Information Byte

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			Code Status 0x00: Bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK transmitted 0x58: Data byte received in master mode, not ACK transmitted 0x60: Slave address + Write bit received, ACK transmitted 0x68: Arbitration lost in address as master, slave address + Write bit received, ACK transmitted 0x70: General Call address received, ACK transmitted 0x78: Arbitration lost in address as master, General Call address received, ACK transmitted 0x80: Data byte received after slave address received, ACK transmitted 0x88: Data byte received after slave address received, not ACK transmitted 0x90: Data byte received after General Call received, ACK transmitted 0x98: Data byte received after General Call received, not ACK transmitted 0xA0: STOP or repeated START condition received in slave mode 0xA8: Slave address + Read bit received, ACK transmitted 0xB0: Arbitration lost in address as master, slave address + Read bit received, ACK transmitted 0xB8: Data byte transmitted in slave mode, ACK received 0xC0: Data byte transmitted in slave mode, ACK not received 0xC8: Last byte transmitted in slave mode, ACK received 0xD0: Second Address byte + Write bit transmitted, ACK received 0xD8: Second Address byte + Write bit transmitted, ACK not received 0xF8: No relevant status information, INT_FLAG=0 Others: Reserved

8.1.6.6. TWI Clock Register(Default Value:0x0000_0000)

Offset: 0x0014			**Register Name: TWI_CCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:3	R/W	0x0	CLK_M
2:0	R/W	0x0	CLK_N The TWI bus is sampled by the TWI at the frequency defined by F0: Fsamp = F 0 = Fin / 2^CLK_N

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			The TWI OSCL output frequency, in master mode, is F1 / 10: F1 = F0 / (CLK_M + 1) Foscl = F1 / 10 = Fin / (2^CLK_N * (CLK_M + 1)*10) For Example： Fin = 48MHz (APB clock input) For 400kHz full speed 2Wire, CLK_N = 2, CLK_M=2 F0 = 48MHz/2^2=12MHz, F1= F0/(10*(2+1)) = 0.4MHz For 100kHz standard speed 2Wire, CLK_N=2, CLK_M=11 F0=48MHz/2^2=12MHz, F1=F0/(10*(11+1)) = 0.1MHz

8.1.6.7. TWI Soft Reset Register(Default Value:0x0000_0000)

Offset: 0x0018			Register Name: TWI_SRST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/WAC	0x0	SOFT_RST Soft Reset Write ‘1’ to this bit to reset the TWI and clear to ‘0’ when completing Soft Reset operation.

8.1.6.8. TWI Enhance Feature Register(Default Value:0x0000_0000)

Offset: 0x001C			Register Name: TWI_EFR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
0:1	R/W	0x0	DBN Data Byte number follow Read Command Control 00 : No Data Byte to be wrote after read command 01 : Only 1 byte data to be wrote after read command 10 : Bytes data can be wrote after read command 11 : Bytes data can be wrote after read command

8.1.6.9. TWI Line Control Register(Default Value:0x0000_003A)

Offset: 0x0020			Register Name: TWI_LCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R	0x1	SCL_STATE Current State of TWI_SCL 0 : Low 1 : High

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4	R	0x1	SDA_STATE Current State of TWI_SDA 0 : Low 1 : High
3	R/W	0x1	SCL_CTL TWI_SCL Line State Control Bit When line control mode is enabled (bit[2] set), value of this bit decide the output level of TWI_SCL 0 : Output low level 1 : Output high level
2	R/W	0x0	SCL_CTL_EN TWI_SCL Line State Control Enable When this bit is set, the state of TWI_SCL is control by the value of bit[3]. 0 : Disable TWI_SCL line control mode 1 : Enable TWI_SCL line control mode
1	R/W	0x1	SDA_CTL TWI_SDA Line State Control Bit When line control mode is enabled (bit[0] set), value of this bit decide the output level of TWI_SDA 0 : Output low level 1 : Output high level
0	R/W	0x0	SDA_CTL_EN TWI_SDA Line State Control Enable When this bit is set, the state of TWI_SDA is control by the value of bit[1]. 0 : Disable TWI_SDA line control mode 1 : Enable TWI_SDA line control mode

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8.2. SPI

8.2.1. Overview

The SPI is a full-duplex, synchronous, serial communication interface which allows rapid data communication with software interrupts. The SPI controller contains one 64x8 receiver buffer (RXFIFO) and one 64x8 transmit buffer (TXFIFO). It can work at Master mode and Slave mode.

Features:

- Full-duplex synchronous serial interface
- 5 clock sources
- Master/Slave configurable
- Four chip selects to support multiple peripherals
- 8-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable
- Interrupt or DMA support
- Support 3-Wire/4-Wire SPI
- Support programmable serial data frame length: 0 bit to 32 bits
- Support Standard SPI,Dual-Output/Dual-Input SPI, Quad-Output/Quad-Input SPI

8.2.2. Block Diagram

Figure 8-6 shows a block diagram of the SPI.

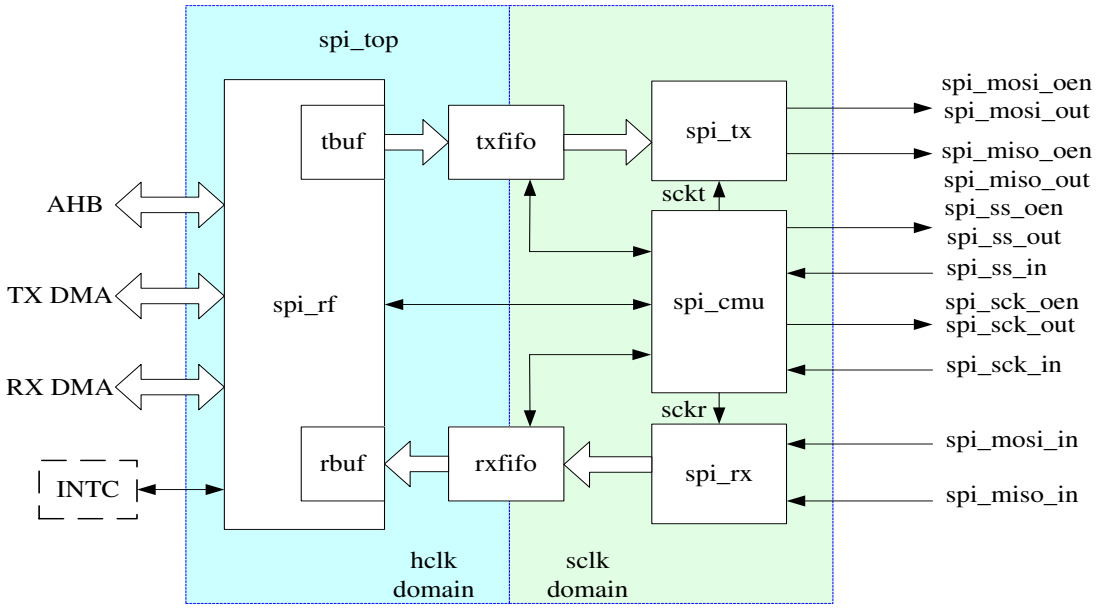


Figure 8-6. SPI Block Diagram

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The SPI comprises with:
spi_rf: Responsible for implementing the internal register, interrupt and DMA Request.
spi_tbuf: The data length transmitted from AHB to txfifo is converted into 8bits,then the data is written into the rxfifo.
spi_rbuf: The block is used as converted the rxfifo data into read data length of AHB.
txfifo, rxfifo: For transmit and receive transfers, data transmitted from the SPI to the external serial device is written into the txfifo; data received from the external serial device into SPI is pushed into the rxfifo.
spi_cmu: Responsible for implementing SPI bus clock, chip select, internal sample and the generation of transfer clock.
spi_tx: Responsible for implementing SPI data transfer ,the interface of the internal txfifo and status register.
spi_rx: Responsible for implementing SPI data receive, the interface of the internal rxfifo and status register.

8.2.3. Operations and Functional Descriptions

8.2.3.1. External Signals

Table 8-4 describes the external signals of SPI. MOSI and MISO are bidirectional I/O, when SPI is configured as Master device, CLK and CS is output pin; when SPI is configurable as Slave device, CLK and CS is input pin. The unused SPI ports are used as General Purpose I/O ports.

Table 8-4. SPI External Signals

Signal	Description	Type
SPI0_CS	SPI Chip Select Signal, Low Active.	I/O
SPI0_CLK	SPI Clock Signal	I/O
SPI0_MOSI	SPI Master Data Out, Slave Data In.	I/O
SPI0_MISO	SPI Master Data In, Slave Data Out.	I/O
SPI0_WP	Write protection and active low or Serial Data Input and Output for Quad Input or Quad Output.	I/O
SPI0_HOLD	The HOLD pin is used to temporarily pause serial communication without deselecting or resetting the device. While the HOLD pin is asserted, transitions on the SCK pin and data on the SI pin will be ignored, or Serial Data Input and Output for Quad Input or Quad Output.	I/O
SPI1_CS	SPI Chip Select Signal, Low Active.	I/O
SPI1_CLK	SPI Clock Signal	I/O
SPI1_MOSI	SPI Master Data Out, Slave Data In.	I/O
SPI1_MISO	SPI Master Data In, Slave Data Out.	I/O

8.2.3.2. Clock Sources

Each SPI controller gets five different clocks, users can select one of them to make SPI Clock Source. Table 8-5 describes the clock sources for SPI.

Table 8-5. SPI Clock Sources

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Clock Sources	Description
OSC24M	24MHz Crystal
PLL_PERIPH0(1X)	Peripheral Clock, default value is 600MHz
PLL_PERIPH1(1X)	Peripheral Clock, default value is 600MHz
PLL_PERIPH0(2X)	Peripheral Clock, default value is 1200MHz
PLL_PERIPH1(2X)	Peripheral Clock, default value is 1200MHz

8.2.3.3. Typical Application

Figure 8-7 shows the application block diagram when the SPI master device is connected to a slave device.

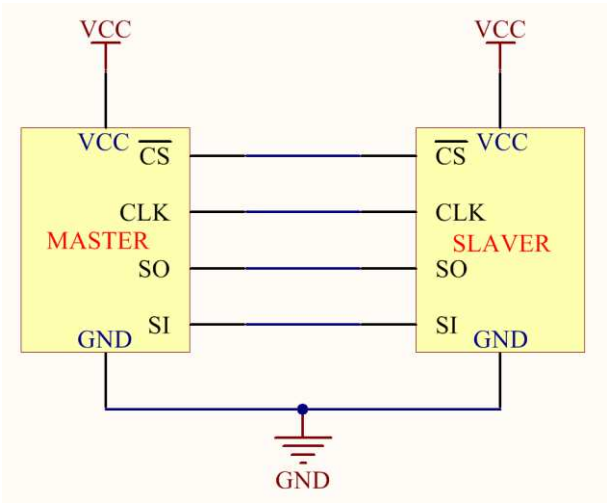


Figure 8-7. SPI Application Block Diagram

8.2.3.4. SPI Transmit Format

The SPI supports 4 different formats for data transfer. Software can select one of the four modes in which the SPI works by setting the bit1(Polarity) and bit0(Phase) of **SPI Transfer Control Register**. The SPI controller master uses the SPI_SCLK signal to transfer data in and out of the shift register. Data is clocked using any one of four programmable clock phase and polarity combinations.

During Phase 0, Polarity 0 and Phase 1, Polarity 1 operations, output data changes on the falling clock edge and input data is shifted in on the rising edge.

During Phase 1, Polarity 0 and Phase 0, Polarity 1 operations, output data changes on the rising edges of the clock and is shifted in on falling edges.

The POL defines the signal polarity when SPI_SCLK is in idle state. The SPI_SCLK is high level when POL is '1' and it is low level when POL is '0'. The PHA decides whether the leading edge of SPI_SCLK is used for setup or sample data. The leading edge is used for setup data when PHA is '1' and for sample data when PHA is '0'. The four modes are listed in Table 8-6.

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Table 8-6. SPI Transmit Format

SPI Mode	POL	PHA	Leading Edge	Trailing Edge
0	0	0	Rising, Sample	Falling, Setup
1	0	1	Rising, Setup	Falling, Sample
2	1	0	Falling, Sample	Rising, Setup
3	1	1	Failing, Setup	Rising, Sample

Figure 8-8 and Figure 8-9 describe four waveforms for SPI_SCLK.

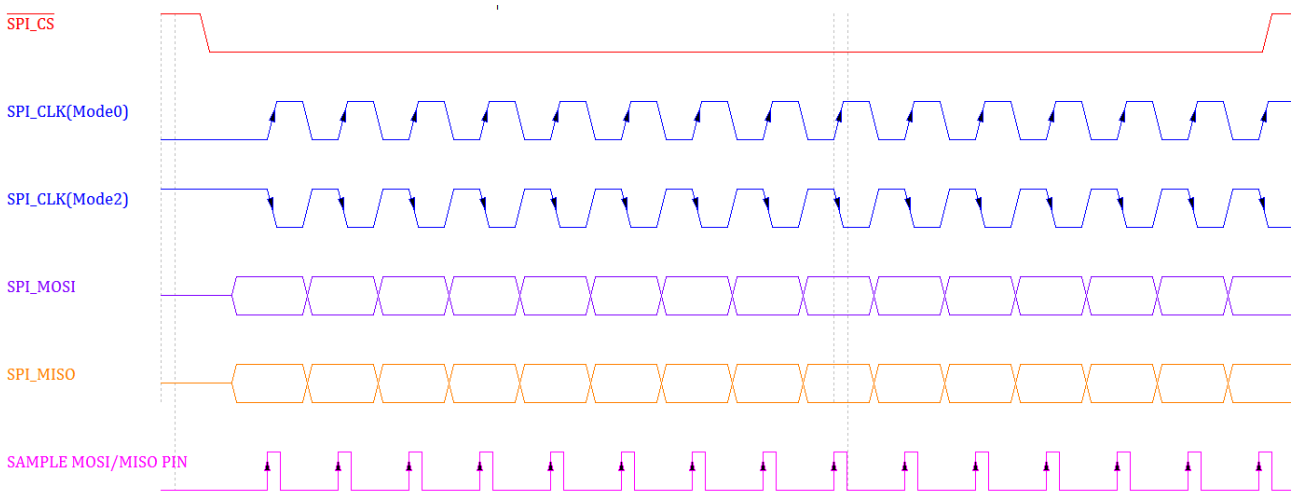


Figure 8-8. SPI Phase 0 Timing Diagram

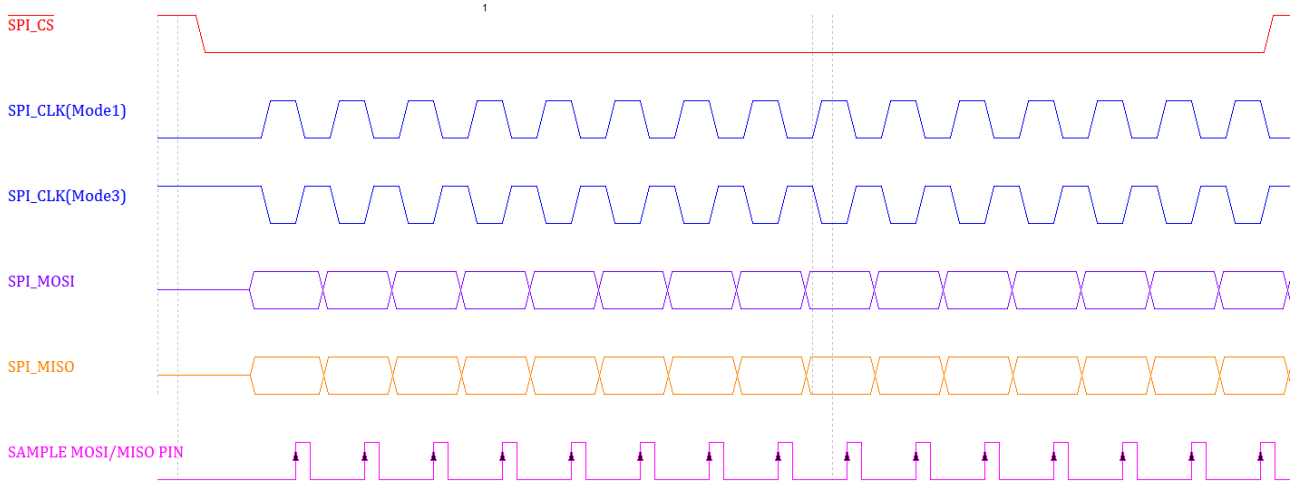


Figure 8-9. SPI Phase 1 Timing Diagram

8.2.3.5. SPI Master and Slave Mode

The SPI controller can be configured to a Master or Slave device. Master mode is selected by setting the **MODE** bit in

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the **SPI Global Control Register;** Slave mode is selected by clearing the the **MODE** bit in the **SPI Global Control Register**.

In Master mode, SPI_CLK is generated and transmitted to external device, and data from the TX FIFO is transmitted on the MOSI pin, the data from slave is received on the MISO pin and sent to RX FIFO. Chip Select(SPI_SS) is active low signal. SPI_SS must be set low before data are transmitted or received. SPI_SS can be selected SPI auto control or software manual control. When using auto control, **SS_OWNER**(the bit 6 in the **SPI Transfer Control Register**) must be cleared(default value is 0);when using manual control, **SS_OWNER** must be set, Chip Select level is controlled by **SS_LEVEL** bit(the bit 7 in the **SPI Transfer Control Register**).

In Slave mode, after software selects the **MODE** bit to '0',it waits for master initiate a transaction. When the Master assert SPI_SS and SPI_CLK is transmitted to the Slave, the Slave data is transmitted from TX FIFO on MISO pin and data from MOSI pin is received in RX FIFO.

8.2.3.6. SPI 3-Wire Mode

The SPI 3-Wire Mode is only valid when the SPI controller work in Master mode, and selected when the **Work Mode Select(bit[1:0])** is equal to 0x2 in the **SPI Bit-Aligned Transfer Configure Register**. and in the 3-Wire mode, the input data and the output data use the same single data line. The following figure describes this mode.

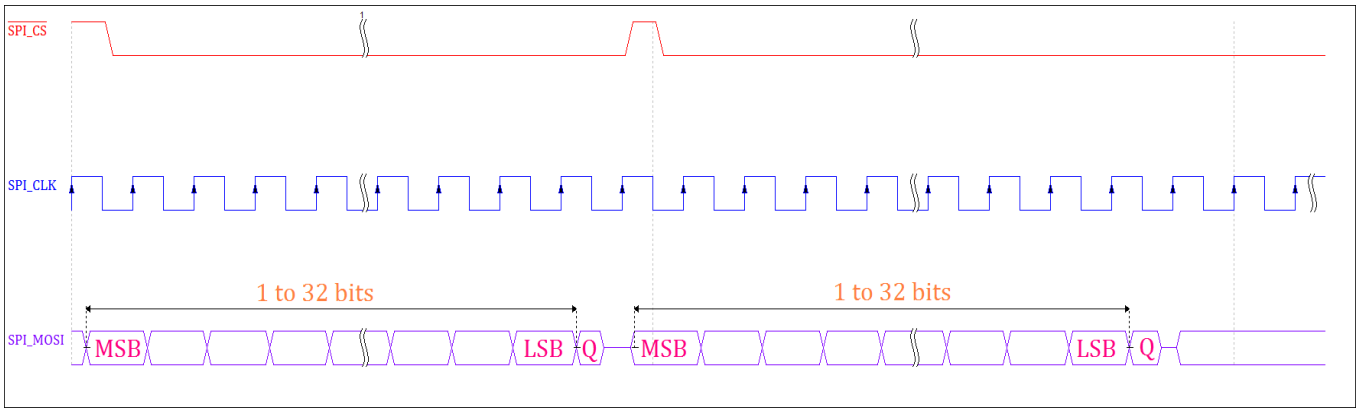


Figure 8-10. SPI 3-Wire Mode

8.2.3.7. SPI Dual Read Mode

The Dual read mode(SPI x2) is selected when the **DRM**(bit28) is set in the **SPI Master Burst Control Counter Register**. Using the dual mode allows data to be transferred to or from the device at two times the rate of standard single mode SPI devices, data can be read at fast speed using two data bits(MOSI and MISO) at a time. The following figure describes the Dual Input/Dual Output SPI(the first) and the Dual IO SPI(the second).

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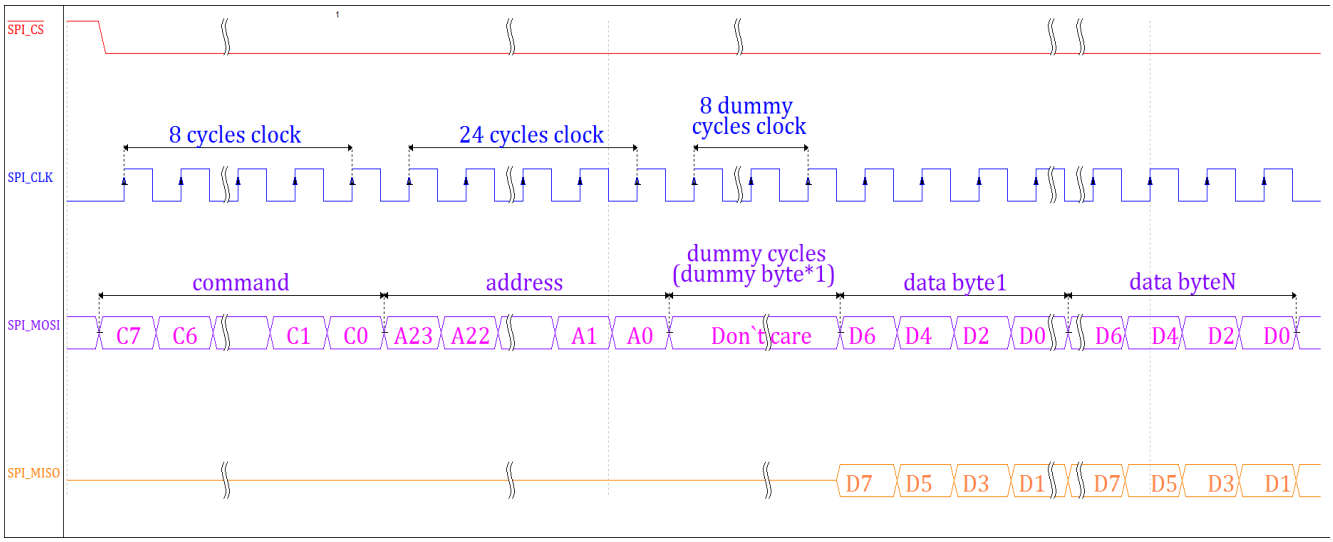


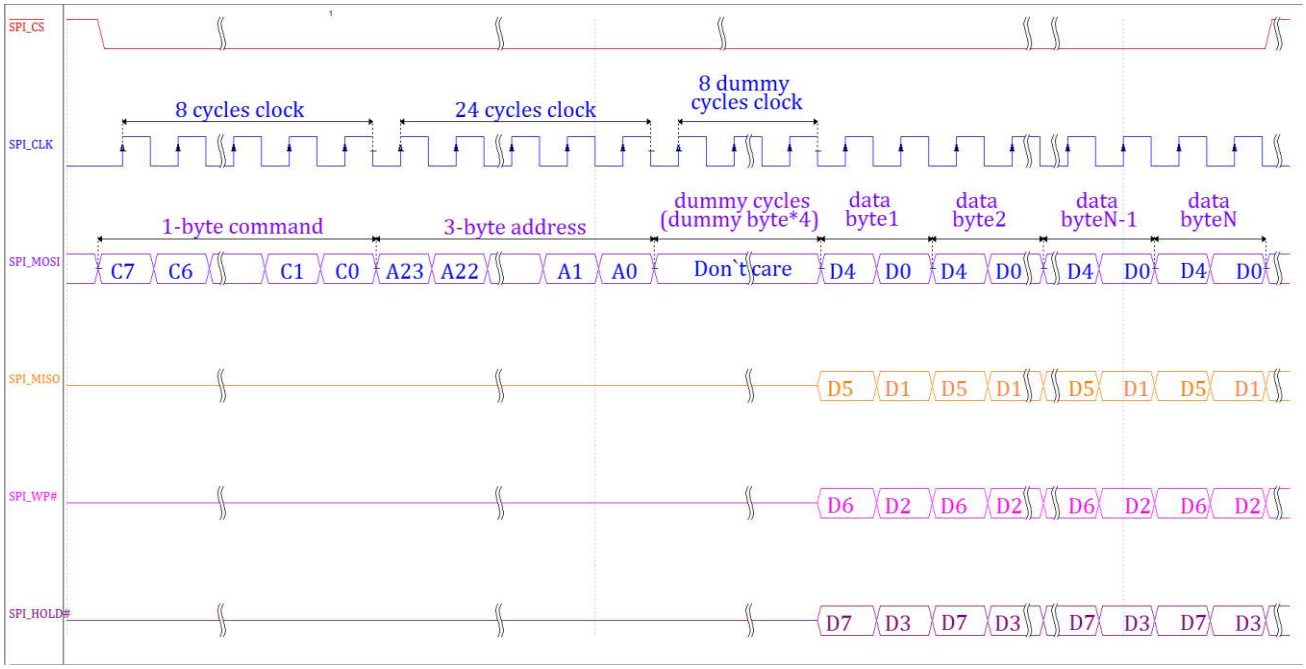
Figure 8-11. SPI Dual Read Mode

NOTE

In the dual Input/dual Output SPI, the command, address, and the dummy bytes outputs in unit of a single bit in serial mode through SPI_MOSI line, only the data bytes are output(write) and input(read) in unit of dual bits through the SPI_MOSI and SPI_MISO.

8.2.3.8. SPI Quad Mode

The Quad read mode(SPI x4) is selected when the **Quad_EN**(bit29) is set in the **SPI Master Burst Control Counter Register**. Using the quad mode allows data to be transferred to or from the device at 4 times the rate of standard single mode SPI devices, data can be read at fast speed using four data bits(MOSI, MISO, IO2(WP#)and IO3(HOLD#)) at the same time. The following figure describes the Quad Input/Quad Output SPI



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Figure 8-12. SPI Quad Read Mode

NOTE

In the Quad Input/Quad Output SPI, the command, address, and the dummy bytes are output in unit of a single bit in serial mode through SPI_MOSI line. Only the data bytes are output(write) and input(read) in unit of quad bits through the SPI_MOSI, SPI_MISO, SPI_WP# and SPI_HOLD#.

8.2.4. Programming Guidelines

8.2.4.1. CPU or DMA Operation

The SPI transfers serial data between the processor and external device. CPU and DMA are the two main operational modes for SPI. For each SPI, data is simultaneously transmitted(shifted out serially) and received (shifted in serially).SPI has 2 channels, TX channel and RX channel. TX channel has the path from TX FIFO to external device. RX channel has the path from external device to RX FIFO.

Write Data: CPU or DMA must write data on the register SPI_TXD, data on the register are automatically moved to TX FIFO.

Read Data: To Read data from RX FIFO,CPU or DMA must access the register SPI_RXD and data are automatically sent to the register SPI_RXD.

In CPU or DMA mode, the SPI sends an completed interrupt(the TC bit in SPI Interrupt Status Register) to the processor at the end of each transfer.

8.2.4.2. Transmit/Receive Burst in Master Mode

In SPI Master mode, the transmit and receive burst(byte in unit) are configured before the SPI transfers serial data between the processor and external device. The transmit burst write in MWTC(bit[23:0]) of **SPI Master Transmit Counter Register.** The transmit burst in single mode before automatically sending dummy burst write in STC(bit[23:0]) of **SPI Master Burst Control Counter Register.** For dummy data, SPI controller can automatically sent before receive by writing DBC(bit[27:24]) in **SPI Master Burst Control Counter Register**. If users don't use SPI controller to sent dummy data automatically, then the dummy bursts are used as the transmit counters to write together in MWTC(bit[23:0]) of **SPI Master Transmit Counter Register.** In Master mode, the total burst numbers write in MBC(bit[23:0]) of **SPI Master Burst Counter Register.** When all transmit burst and receive burst are transferred, SPI contr oller will send an completed interrupt, at the same time, SPI controller will clear DBC,MWTC and MBC.

8.2.4.3. SPI Sample Mode and Run Clock Configuration

The SPI Controller runs at 3kHz~100MHz at its interface to external SPI devices. The internal SPI Clock should run at the same frequency as the outgoing clock in master mode. The SPI clock is selected different clock sources, SPI must

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configure different work mode. There are three work mode: normal sample mode, delay half cycle sample mode, delay one cycle sample mode. Delay half cycle sample mode is the default mode of SPI controller. When SPI runs at 40MHz or below 40MHz, SPI can work at normal sample mode or delay half cycle sample mode. When SPI runs over 75MHz,Set the **SDC** bit in **SPI Transfer Control Register** to '1' to make the internal read sample point with a half cycle delay of SPI_CLK, which is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave. The different configuration of SPI sample mode shows in Table 8-7.

Table 8-7. SPI Sample Mode and Run Clock

SPI Sample Mode	SDM(bit13)	SDC(bit11)	Run Clock
normal sample	1	0	<=24MHz
delay half cycle sample	0	0	<=40MHz
delay one cycle sample	0	1	>=75MHz

8.2.5. Register List

Module Name	Base Address
SPI0	0x0501 0000
SPI1	0x0501 1000

Register Name	Offset	Description
SPI_GCR	0x0004	SPI Global Control Register
SPI_TCR	0x0008	SPI Transfer Control register
/	0x000C	/
SPI_IER	0x0010	SPI Interrupt Control register
SPI_ISR	0x0014	SPI Interrupt Status register
SPI_FCR	0x0018	SPI FIFO Control register
SPI_FSR	0x001C	SPI FIFO Status register
SPI_WCR	0x0020	SPI Wait Clock Counter register
SPI_CCR	0x0024	SPI Clock Rate Control register
/	0x0028	/
/	0x002C	/
SPI_MBC	0x0030	SPI Burst Counter register
SPI_MTC	0x0034	SPI Transmit Counter Register
SPI_BCC	0x0038	SPI Burst Control register
SPI_BATCR	0x003C	SPI Bit-Aligned Transfer Configure Register
SPI_3W_CCR	0x0040	SPI 3Wire CLOCK Configuration Register
SPI_TBR	0x0044	SPI TX Bit Register
SPI_RBR	0x0048	SPI RX Bit Register
SPI_NDMA_MODE_CTL	0x0088	SPI Normal DMA Mode Control Register
SPI_TXD	0x0200	SPI TX Data register
SPI_RXD	0x0300	SPI RX Data register

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8.2.6. Register Description

8.2.6.1. SPI Global Control Register(Default Value: 0x0000_0080)

Offset:0x0004			Register Name: SPI_GCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	SRST Soft reset Writing '1' to this bit will clear the SPI controller, and auto clear to '0' when reset operation completes Writing '0' has no effect.
30:8	/	/	/
7	R/W	0x1	TP_EN Transmit Pause Enable In master mode, it is used to control transmit state machine to stop smart burst sending when RX FIFO is full. 1: stop transmit data when RXFIFO full 0: normal operation, ignore RXFIFO status Can't be written when XCH=1
6:2	/	/	/
1	R/W	0x0	MODE SPI Function Mode Select 0: Slave Mode 1: Master Mode Can't be written when XCH=1
0	R/W	0x0	EN SPI Module Enable Control 0: Disable 1: Enable After transforming from bit_mode to byte_mode, it must Enable the SPI Module again.

8.2.6.2. SPI Transfer Control Register(Default Value: 0x0000_0087)

Offset: 0x0008			Register Name: SPI_TCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	XCH Exchange Burst In master mode it is used to start SPI burst 0: Idle 1: Initiates exchange. Writing "1" to this bit will start the SPI burst, and will auto clear after finishing the bursts transfer specified by BC. Writing "1" to SRST will also clear this bit. Writing '0' to this bit has no effect.

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			Can’t be written when XCH=1.
30:15	/	/	/
14	R/W	0x0	SDDM Sending Data Delay Mode 0:normal sending 1:delay sending Set the bit to"1" to make the data that should be sent with a delay of half cycle of SPI_CLK in dual IO mode for SPI mode 0.
13	R/W	0x0	SDM Master Sample Data Mode 1: Normal Sample Mode 0: Delay Sample Mode In Normal Sample Mode, SPI master samples the data at the correct edge for each SPI mode; In Delay Sample Mode, SPI master samples data at the edge that is half cycle delayed by the correct edge defined in respective SPI mode.
12	R/W	0x0	FBS First Transmit Bit Select 0: MSB first 1: LSB first Can’t be written when XCH=1.
11	R/W	0x0	SDC Master Sample Data Control Set this bit to ‘1’ to make the internal read sample point with a delay of half cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave. 0: normal operation, do not delay internal read sample point 1: delay internal read sample point Can’t be written when XCH=1.
10	R/W	0x0	RPSM Rapids Mode Select Select rapid mode for high speed write. 0: normal write mode 1: rapid write mode Can’t be written when XCH=1.
9	R/W	0x0	DDB Dummy Burst Type 0: The bit value of dummy SPI burst is zero 1: The bit value of dummy SPI burst is one Can’t be written when XCH=1.
8	R/W	0x0	DHB Discard Hash Burst In master mode it controls whether discarding unused SPI bursts 0: Receiving all SPI bursts in BC period 1: Discard unused SPI bursts, only fetching the SPI bursts during dummy burst period. The bursts number is specified by TC.

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			Can’t be written when XCH=1.
7	R/W	0x1	SS_LEVEL When control SS signal manually (SPI_CTRL_REG.SS_CTRL==1), set this bit to ‘1’ or ‘0’ to control the level of SS signal. 0: set SS to low 1: set SS to high Can’t be written when XCH=1.
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software Can’t be written when XCH=1.
5:4	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted Can’t be written when XCH=1.
3	R/W	0x0	SSCTL In master mode, this bit selects the output wave form for the SPI_SSx signal. Only valid when SS_OWNER = 0. 0: SPI_SSx remains asserted between SPI bursts 1: Negate SPI_SSx between SPI bursts Can’t be written when XCH=1.
2	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) Can’t be written when XCH=1.
1	R/W	0x1	CPOL SPI Clock Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) Can’t be written when XCH=1.
0	R/W	0x1	CPHA SPI Clock/Data Phase Control 0: Phase 0 (Leading edge for sample data) 1: Phase 1 (Leading edge for setup data) Can’t be written when XCH=1.

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8.2.6.3. SPI Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SPI_IER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W	0x0	SS_INT_EN SSI Interrupt Enable Chip Select Signal (SSx) from valid state to invalid state 0: Disable 1: Enable
12	R/W	0x0	TC_INT_EN Transfer Completed Interrupt Enable 0: Disable 1: Enable
11	R/W	0x0	TF_UDR_INT_EN TXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
10	R/W	0x0	TF_OVF_INT_EN TX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
9	R/W	0x0	RF_UDR_INT_EN RXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	RF_OVF_INT_EN RX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
7	/	/	/
6	R/W	0x0	TF_FUL_INT_EN TX FIFO Full Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TX_EMP_INT_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	TX_ERQ_INT_EN TX FIFO Empty Request Interrupt Enable 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	RF_FUL_INT_EN RX FIFO Full Interrupt Enable

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			0: Disable 1: Enable
1	R/W	0x0	RX_EMP_INT_EN RX FIFO Empty Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RF_RDY_INT_EN RX FIFO Ready Request Interrupt Enable 0: Disable 1: Enable

8.2.6.4. SPI Interrupt Status Register(Default Value: 0x0000_0032)

Offset: 0x0014			Register Name: SPI_ISR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W1C	0x0	SSI SS Invalid Interrupt When SSI is 1, it indicates that SS has changed from valid state to invalid state. Writing 1 to this bit clears it.
12	R/W1C	0x0	TC Transfer Completed In master mode, it indicates that all bursts specified by BC has been exchanged. In other condition, When set, this bit indicates that all the data in TXFIFO has been loaded in the Shift register, and the Shift register has shifted out all the bits. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed
11	R/W1C	0x0	TF_UDF TXFIFO Underrun This bit is set when if the TXFIFO is underrun. Writing 1 to this bit clears it. 0: TXFIFO is not underrun 1: TXFIFO is underrun
10	R/W1C	0x0	TF_OVF TXFIFO Overflow This bit is set when if the TXFIFO is overflow. Writing 1 to this bit clears it. 0: TXFIFO is not overflow 1: TXFIFO is overflowed
9	R/W1C	0x0	RX_UDF RXFIFO Underrun When set, this bit indicates that RXFIFO has underrun. Writing 1 to this bit clears it.
8	R/W1C	0x0	RX_OVF RXFIFO Overflow When set, this bit indicates that RXFIFO has overflowed. Writing 1 to this bit

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			clears it. 0: RXFIFO is available. 1: RXFIFO has overflowed.
7	/	/	/
6	R/W1C	0x0	TX_FULL TXFIFO Full This bit is set when if the TXFIFO is full . Writing 1 to this bit clears it. 0: TXFIFO is not Full 1: TXFIFO is Full
5	R/W1C	0x1	TX_EMP TXFIFO Empty This bit is set if the TXFIFO is empty. Writing 1 to this bit clears it. 0: TXFIFO contains one or more words. 1: TXFIFO is empty
4	R/W1C	0x1	TX_READY TXFIFO Ready 0: TX_WL > TX_TRIG_LEVEL 1: TX_WL <= TX_TRIG_LEVEL This bit is set any time if TX_WL <= TX_TRIG_LEVEL. Writing “1” to this bit clears it. Where TX_WL is the water level of RXFIFO
3	/	/	/
2	R/W1C	0x0	RX_FULL RXFIFO Full This bit is set when the RXFIFO is full . Writing 1 to this bit clears it. 0: Not Full 1: Full
1	R/W1C	0x1	RX_EMP RXFIFO Empty This bit is set when the RXFIFO is empty . Writing 1 to this bit clears it. 0: Not empty 1: empty
0	R/W1C	0x0	RX_RDY RXFIFO Ready 0: RX_WL < RX_TRIG_LEVEL 1: RX_WL >= RX_TRIG_LEVEL This bit is set any time if RX_WL >= RX_TRIG_LEVEL. Writing “1” to this bit clears it. Where RX_WL is the water level of RXFIFO.

8.2.6.5. SPI FIFO Control Register(Default Value: 0x0040_0001)

Offset: 0x0018			**Register Name: SPI_FCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	TX_FIFO_RST TX FIFO Reset Writing ‘1’ to this bit will reset the control portion of the TX FIFO and auto

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			clear to '0' when completing reset operation, writing to '0' has no effect.
30	R/W	0x0	TF_TEST_ENB TX Test Mode Enable 0: disable 1: enable In normal mode, TX FIFO can only be read by SPI controller, writing '1' to this bit will switch TX FIFO read and write function to AHB bus. This bit is used to test the TX FIFO, don't set in normal operation and don't set RF_TEST and TF_TEST at the same time.
29:25	/	/	/
24	R/W	0x0	TF_ DRQ_EN TX FIFO DMA Request Enable 0: Disable 1: Enable
23:16	R/W	0x40	TX_TRIG_LEVEL TX FIFO Empty Request Trigger Level
15	R/WAC	0x0	RF_RST RXFIFO Reset Writing '1' to this bit will reset the control portion of the receiver FIFO, and auto clear to '0' when completing reset operation, writing '0' to this bit has no effect.
14	R/W	0x0	RF_TEST RX Test Mode Enable 0: Disable 1: Enable In normal mode, RX FIFO can only be written by SPI controller, writing '1' to this bit will switch RX FIFO read and write function to AHB bus. This bit is used to test the RX FIFO, don't set in normal operation and don't set RF_TEST and TF_TEST at the same time.
13:9	/	/	/
8	R/W	0x0	RF_ DRQ_EN RX FIFO DMA Request Enable 0: Disable 1: Enable
7:0	R/W	0x1	RX_TRIG_LEVEL RX FIFO Ready Request Trigger Level

8.2.6.6. SPI FIFO Status Register(Default Value: 0x0000_0000)

Offset: 0x001C			**Register Name: SPI_FSR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	TB_WR TX FIFO Write Buffer Write Enable
30:28	R	0x0	TB_CNT TX FIFO Write Buffer Counter

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			These bits indicate the number of words in TX FIFO Write Buffer
27:24	/	/	/
23:16	R	0x0	TF_CNT TX FIFO Counter These bits indicate the number of words in TX FIFO 0: 0 byte in TX FIFO 1: 1 byte in TX FIFO … 64 64 bytes in TX FIFO other: Reserved
15	R	0x0	RB_WR RX FIFO Read Buffer Write Enable
14:12	R	0x0	RB_CNT RX FIFO Read Buffer Counter These bits indicate the number of words in RX FIFO Read Buffer
11:8	/	/	/
7:0	R	0x0	RF_CNT RX FIFO Counter These bits indicate the number of words in RX FIFO 0: 0 byte in RX FIFO 1: 1 byte in RX FIFO … 64: 64 bytes in RX FIFO other: Reserved

8.2.6.7. SPI Wait Clock Register(Default Value: 0x0000_0000)

Offset: 0x0020			**Register Name: SPI_WCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:16	R/W	0x0	SWC Dual mode direction switch wait clock counter (for master mode only). 0: No wait states inserted n: n SPI_SCLK wait states inserted These bits control the number of wait states to be inserted before start dual data transfer in dual SPI mode. The SPI module counts SPI_SCLK by SWC for delaying next word data transfer. Can't be written when XCH=1.
15:0	R/W	0x0	WCC Wait Clock Counter (In Master mode) These bits control the number of wait states to be inserted in data transfers. The SPI module counts SPI_SCLK by WCC for delaying next word data transfer. 0: No wait states inserted N: N SPI_SCLK wait states inserted

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8.2.6.8. SPI Clock Control Register(Default Value: 0x0000_0002)

Offset: 0x0024			Register Name: SPI_CCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12	R/W	0x0	DRS Divide Rate Select (Master Mode Only) 0: Select Clock Divide Rate 1 1: Select Clock Divide Rate 2
11:8	R/W	0x0	CDR1_M Clock Divide Rate 1 (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = Source_CLK / (2^CDR1_M).
7:0	R/W	0x2	CDR2_N Clock Divide Rate 2 (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = Source_CLK / (2*(CDR2_N + 1)).

8.2.6.9. SPI Master Burst Counter Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: SPI_MBC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	MBC Master Burst Counter In master mode, this field specifies the total burst number. 0: 0 burst 1: 1 burst … N: N bursts **NOTE** **Total transfer data, include the TXD, RXD and dummy burst.**

8.2.6.10. SPI Master Transmit Counter Register(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: SPI_MTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	MWTC Master Write Transmit Counter

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			In master mode, this field specifies the burst number that should be sent to TXFIFO before automatically sending dummy burst. For saving bus bandwidth, the dummy burst (all zero bits or all one bits) is sent by SPI Controller automatically. 0: 0 burst 1: 1 burst … N: N bursts

8.2.6.11. SPI Master Burst Control Counter Register(Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: SPI_BCC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	Quad_EN Quad_Mode_EN 0: Quad mode disable 1: Quad mode enable Quad mode includes Quad-Input and Quad-Output.
28	R/W	0x0	DRM Master Dual Mode RX Enable 0: RX use single-bit mode 1: RX use dual mode 1. Can't be written when XCH=1; 2. It is only valid when Quad_Mode_EN=0.
27:24	R/W	0x0	DBC Master Dummy Burst Counter In master mode, this field specifies the burst number that should be sent before receive in dual SPI mode. The data does not care by the device. 0: 0 burst 1: 1 burst … N: N bursts Can't be written when XCH=1
23:0	R/W	0x0	STC Master Single Mode Transmit Counter In master mode, this field specifies the burst number that should be sent in single mode before automatically sending dummy burst. This is the first transmit counter in all bursts. 0: 0 burst 1: 1 burst … N: N bursts Can't be written when XCH=1

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8.2.6.12. SPI Bit-Aligned Transfer Configure Register(Default Value: 0x0000_00A0)

Offset: 0x0040			Register Name: SPI_BATC
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	***TCE*** Transfer Control Enable In master mode, it is used to start to transfer the serial bits frame, it is only valid when ***Work Mode Select==0x10/0x11.*** 0: Idle 1: Initiates transfer. Writing "1" to this bit will start to transfer serial bits frame(the value comes from the ***SPI TX Bit Register*** or ***SPI RX Bit Register***), and will auto clear after the bursts transfer completely. Writing '0' to this bit has no effect.
30	R/W	0x0	***MSMS*** Master Sample Standard 1: Standard Sample Mode 0: Delay Sample Mode In Standard Sample Mode, SPI master samples the data at the standard rising edge of SCLK for each SPI mode; In Delay Sample Mode, SPI master samples data at the edge that is half cycle delayed by the standard rising edge of SCLK defined in respective SPI mode.
29:26	/	/	
25	R/W1C	0x0	***TBC*** Transfer Bits Completed When set, this bit indicates that the last bit of the serial data frame in ***SPI TX Bit Register****(or* ***SPI RX Bit Register****)* has been transferred completely. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed It is only valid when ***Work Mode Select==0x10/0x11.***
24	R/W	0x0	***TBC_INT_EN*** Transfer Bits Completed Interrupt Enable 0: Disable 1: Enable It is only valid when ***Work Mode Select==0x10/0x11.***
23:22	/	/	/
21:16	R/W	0x00	Configure the length of serial data frame(burst) of RX 000000: 0bit 000001: 1bit … 100000: 32bits Other values: reserved It is only valid when ***Work Mode Select==0x10/0x11,*** and can't be written when TCE=1.
15:14	/	/	/

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13:8	R/W	0x00	Configure the length of serial data frame(burst) of TX 000000: 0bit 000001: 1bit … 100000: 32bits Other values: reserved It is only valid when ***Work Mode Select==0x10/0x11,*** and can't be written when TCE=1.
7	R/W	0x1	SS_LEVEL When control SS signal manually , set this bit to '1' or '0' to control the level of SS signal. 0: set SS to low 1: set SS to high It is only valid when ***Work Mode Select==0x10/0x11,*** and only ***work in Mode0***, can't be written when TCE=1.
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software It is only valid when ***Work Mode Select==0x10/0x11,*** and only ***work in Mode0***, can't be written when TCE=1.
5	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) It is only valid when ***Work Mode Select==0x10/0x11,*** and only ***work in Mode0***, can't be written when TCE=1.
4	/	/	/
3:2	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted It is only valid when ***Work Mode Select= =0x10/0x11,*** and only ***work in Mode0***, can't be written when TCE=1.
1:0	R/W	0x0	Work Mode Select 00: Data frame is byte aligned in Standard SPI, Dual-Output/Dual Input SPI, Dual IO SPI and Quad-Output/Quad-Input SPI. 01: Reserve 10: Data frame is bit aligned in 3-Wire SPI 11: Data frame is bit aligned in Standard SPI

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8.2.6.13. SPI Bit-Aligned CLOCK Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: SPI_BA_CCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	CDR_N Clock Divide Rate (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = Source_CLK / (2*(CDR_N + 1)).

NOTE

This register is only valid when *Work Mode Select==0x10/0x11*.

8.2.6.14. SPI TX Bit Register(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: SPI_TBR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VTB The Value of the Transmit Bits This register is used to store the value of the transmitted serial data frame. Note: In the process of transmission, the LSB is transmitted first.

NOTE

This register is only valid when *Work Mode Select==0x10/0x11*.

8.2.6.15. SPI RX Bit Register(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: SPI_RBR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VRB The Value of the Receive Bits This register is used to store the value of the received serial data frame. In the process of transmission, the LSB is transmitted first.

NOTE

This register is only valid when *Work Mode Select==0x10/0x11*.

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8.2.6.16. SPI Normal DMA Mode Control Register(Default Value: 0x0000_00E5)

Offset: 0x0088			Register Name: NDFC_NDMA_MODE_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R/W	0x11	00:dma_active is low 01:dma_active is high 10:dma_active is controlled by dma_request(DRQ) 11:dma_active is controlled by controller
5	R/W	0x1	0: active fall do not care ack 1: active fall must after detect ack is high
4:0	R/W	0x05	The delay cycles The counts of hold cycles from DMA last signal high to dma_active high

8.2.6.17. SPI TX Data Register(Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: SPI_TXD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TDATA Transmit Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are rooms in TXFIFO, one burst data is written to TXFIFO and the depth is increased by 1. In half-word accessing method, two SPI burst data are written and the TXFIFO depth is increase by 2. In word accessing method, four SPI burst data are written and the TXFIFO depth is increased by 4. **NOTE** **This address is writable-only if TF_TEST is '0', and if TF_TEST is set to '1', this address is readable and writable to test the TX FIFO through the AHB bus.**

8.2.6.18. SPI RX Data Register(Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: SPI_RXD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	RDATA Receive Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are data in RXFIFO, the top word is returned and the RXFIFO depth is decreased by 1. In half-word accessing method, two SPI bursts are returned and the RXFIFO depth is decrease by 2. In word accessing method, the four SPI bursts are returned and the RXFIFO depth is decreased by 4.

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			NOTE **This address is readable-only if RF_TEST is '0', and if RF_TEST is set to '1', this address is readable and writable to test the RX FIFO through the AHB bus.**

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8.3. UART

8.3.1. Overview

The UART is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.

The UART contains registers to control the character length, baud rate, parity generation/checking, and interrupt generation. Although there is only one interrupt output signal from the UART, there are several prioritized interrupt types that can be responsible for its assertion. Each of the interrupt types can be separately enabled/ disabled with the control registers.

The UART has 16450 and 16550 modes of operation, which are compatible with a range of standard software drivers. In 16550 mode, transmit and receive operations are both buffered by FIFOs. In 16450 mode, these FIFOs are disabled.

The UART supports word lengths from five to eight bits, an optional parity bit and 1, 1 ½ or 2 stop bits, and is fully programmable by an AMBA APB CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, together with separate transmit and receive FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided.

Interrupts can be generated for a range of TX Buffer/FIFO, RX Buffer/FIFO, Modem Status and Line Status conditions.

For integration in systems where Infrared SIR serial data format is required, the UART can be configured to have a software-programmable IrDA SIR Mode. If this mode is not selected, only the UART (RS232 standard) serial data format is available.

Features:

- Compatible with industry-standard 16550 UARTs
- 256 Bytes Transmit and Receive data FIFOs
- Capable of speed up to 5 Mbit/s
- Supports 5 to 8 data bits and 1/1.5/2 stop bits
- Supports Even, Odd or No Parity
- Supports DMA controller interface
- Supports Software/ Hardware Flow Control
- Supports IrDA 1.0 SIR
- Supports RS-485/9-bit mode

8.3.2. Block Diagram

Figure 8-13 shows a block diagram of the UART.

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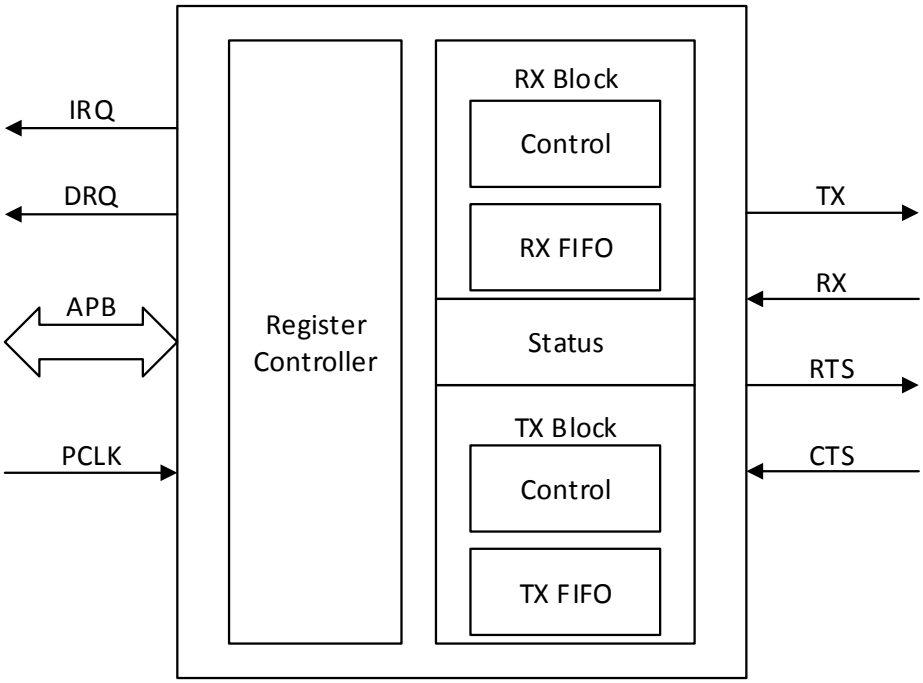


Figure 8-13. UART Block Diagram

8.3.3. Operations and Functional Descriptions

8.3.3.1. External Signals

Table 8-8 describes the external signals of UART.

Table 8-8. UART External Signals

Signal	Type	Description
UART0_TX	O	Serial Data Output
UART0_RX	I	Serial Data Input
UART1_TX	O	Serial Data Output
UART1_RX	I	Serial Data Input
UART1_CTS	I	Clear to Send
UART1_RTS	O	Request to Send
UART2_TX	O	Serial Data Output
UART2_RX	I	Serial Data Input
UART2_CTS	I	Clear to Send
UART2_RTS	O	Request to Send
UART3_TX	O	Serial Data Output
UART3_RX	I	Serial Data Input
UART3_CTS	I	Clear to Send
UART3_RTS	O	Request to Send
R_UART0_TX	O	Serial Data Output

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R_UART0_RX	I	Serial Data Input

8.3.3.2. Clock Sources

Table 8-9 describes the clock sources of UART.

Table 8-9. UART Clock Sources

Clock Sources	Description
APB2_CLK	Clock of APB2

8.3.3.3. Typical Application

Figure 8-14 shows the application block diagram of UART.

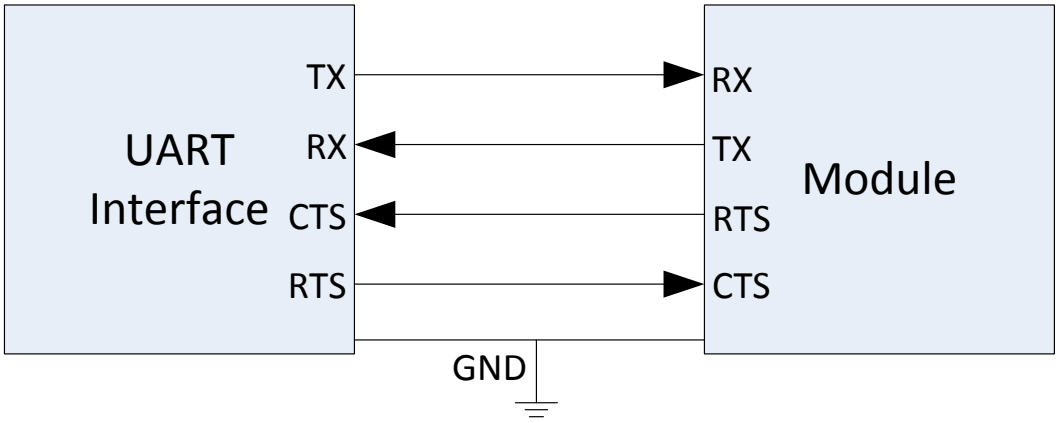


Figure 8-14. UART Application Diagram

8.3.3.4. UART Timing Diagram

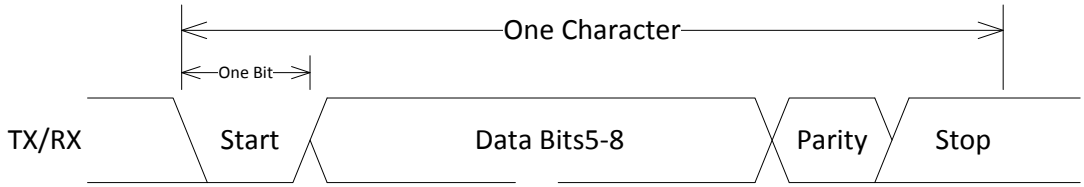


Figure 8-15. UART Serial Data Format

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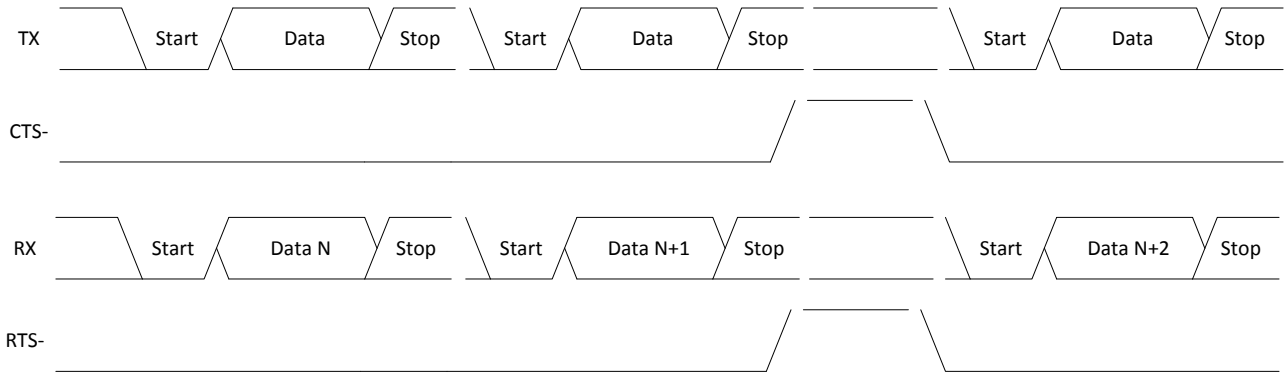


Figure 8-16. RTS/CTS Autoflow Control Timing

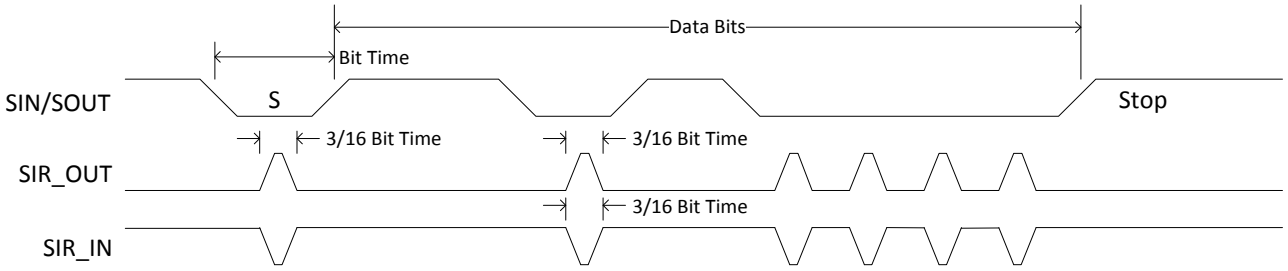


Figure 8-17. Serial IrDA Data Format

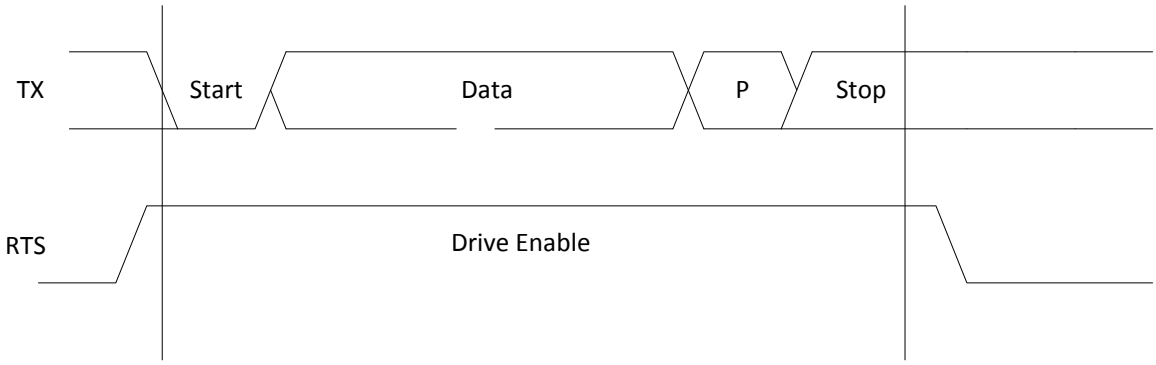


Figure 8-18. RS-485 Timing

8.3.3.5. UART Operating Mode

8.3.3.5.1. Basic Mode Setting

The UART_LCR register can set basic parameter of a data frame: data width, stop bit number, parity type.

A frame transfer of the UART includes the start signal, data signal, parity bit and stop signal. The LSB is transmitted first.

Start signal(start bit): It is the start flag of a data frame. According to UART protocol, the low level of TXD signal indicates the start of a data frame. When the UART does transmit data, the level need hold high.

Data signal(data bit): The data bit width can be configured as 5-bit,6-bit,7-bit,8-bit through different applications.

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Parity bit: It is 1-bit error correction signal. Parity bit includes odd parity, even parity. The UART can enable and disable the parity bit by setting the UART_LCR register.

Stop Signal(stop bit): It is the stop bit of a data frame. The stop bit can be set to 1-bit,1.5-bit and 2-bit by the UART_LCR register. The high level of TXD signal indicates the end of a data frame.

8.3.3.5.2. Baud Rate Setting

The baud rate is calculated as follows: Baud rate = SCLK /（16 * divisor）.SCLK is usually APB2 and can be set in CCU.

Divisor is frequency divider of UART. The frequency divider has 16-bit,the low 8-bit is in the UART_DLL register, the high 8-bit is in the UART_DLH register.

The relationship between different UART mode and error rate is as follows.

Table 8-10. UART Mode Baud and Error Rates

Clock source	Divisor	Baud rate	Over sampling	Error(%)
24000000	5000	300	16	0
24000000	2500	600	16	0
24000000	1250	1200	16	0
24000000	625	2400	16	0
24000000	313	4800	16	-0.16
24000000	156	9600	16	0.16
24000000	78	19200	16	0.16
24000000	39	38400	16	0.16
24000000	26	57600	16	0.16
24000000	13	115200	16	0.16
48000000	13	230400	16	0.16
64000000	7	576000	16	-0.794
75000000	5	921600	16	1.725
48000000	3	1000000	16	0
24000000	1	1500000	16	0
48000000	1	3000000	16	0
64000000	1	4000000	16	0

Table 8-11. IrDA Mode Baud and Error Rates

Clock source	Divisor	Baud rate	Encoding	Error(%)
24000000	5000	300	3/16	0
24000000	2500	600	3/16	0
24000000	1250	1200	3/16	0
24000000	625	2400	3/16	0
24000000	313	4800	3/16	-0.16

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24000000	156	9600	3/16	0.16
24000000	78	19200	3/16	0.16
24000000	39	38400	3/16	0.16
24000000	26	57600	3/16	0.16
24000000	13	115200	3/16	0.16

Table 8-12. RS485 Mode Baud and Error Rates

Clock source	Divisor	Baud rate	Encoding	Error(%)
24000000	5000	300	16	0
24000000	2500	600	16	0
24000000	1250	1200	16	0
24000000	625	2400	16	0
24000000	313	4800	16	-0.16
24000000	156	9600	16	0.16
24000000	78	19200	16	0.16
24000000	39	38400	16	0.16
24000000	26	57600	16	0.16
24000000	13	115200	16	0.16

8.3.3.5.3. DLAB Setting

DLAB control bit (UART_LCR[7]) is the access control bit of divisor Latch register.

If DLAB is 0, then 0x00 offset address is TX/RX FIFO register, 0x04 offset address is IER register.

If DLAB is 1, then 0x00 offset address is DLL register, 0x04 offset address is DLH register.

When UART initial, divisor need be set. That is, writing 1 to DLAB can access the DLL and DLH register, after finished setting, writing 0 to DLAB can access the TX/RX FIFO register.

8.3.3.5.4. CHCFG_AT_BUSY Setting

The function of CHCFG_AT_BUSY（UART_HALT[1]） and CHANGE_UPDATE（UART_HALT[2]） is as follows.

CHCFG_AT_BUSY(configure at busy): Enable the bit, software can also set UART controller when UART is busy, such as the LCR,DLH,DLL register.

CHANGE_UPDATE(change update): If CHCFG_AT_BUSY is enabled, and CHANGE_UPDATE is written to 1, the configuration of UART controller can be updated. After completed update, the bit is cleared to 0 automatically.

Setting divisor, performs the following steps:

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Step1 Write CHCFG_AT_BUSY to 1

Step2 Write DLAB to 1, and set DLH and DLL

Step3 Write CHANGE_UPDATE to update configuration. The bit is cleared to 0 automatically after completed update.

8.3.3.5.5. UART Busy

UART_USR[0] is a busy flag of UART controller or not.

When TX transmits data, or RX receives data,or TX FIFO is not empty, or RX FIFO is not empty, then the BUSY flag bit can be set to 1 by hardware, which indicates the UART controller is busy.

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8.3.4. Programming Guidlines

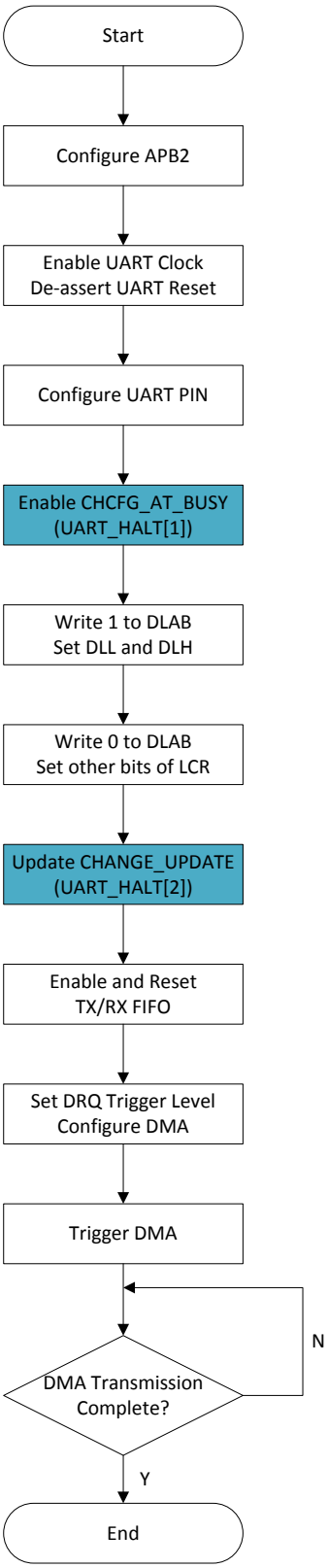


Figure 8-19. UART DRQ Flow Chart

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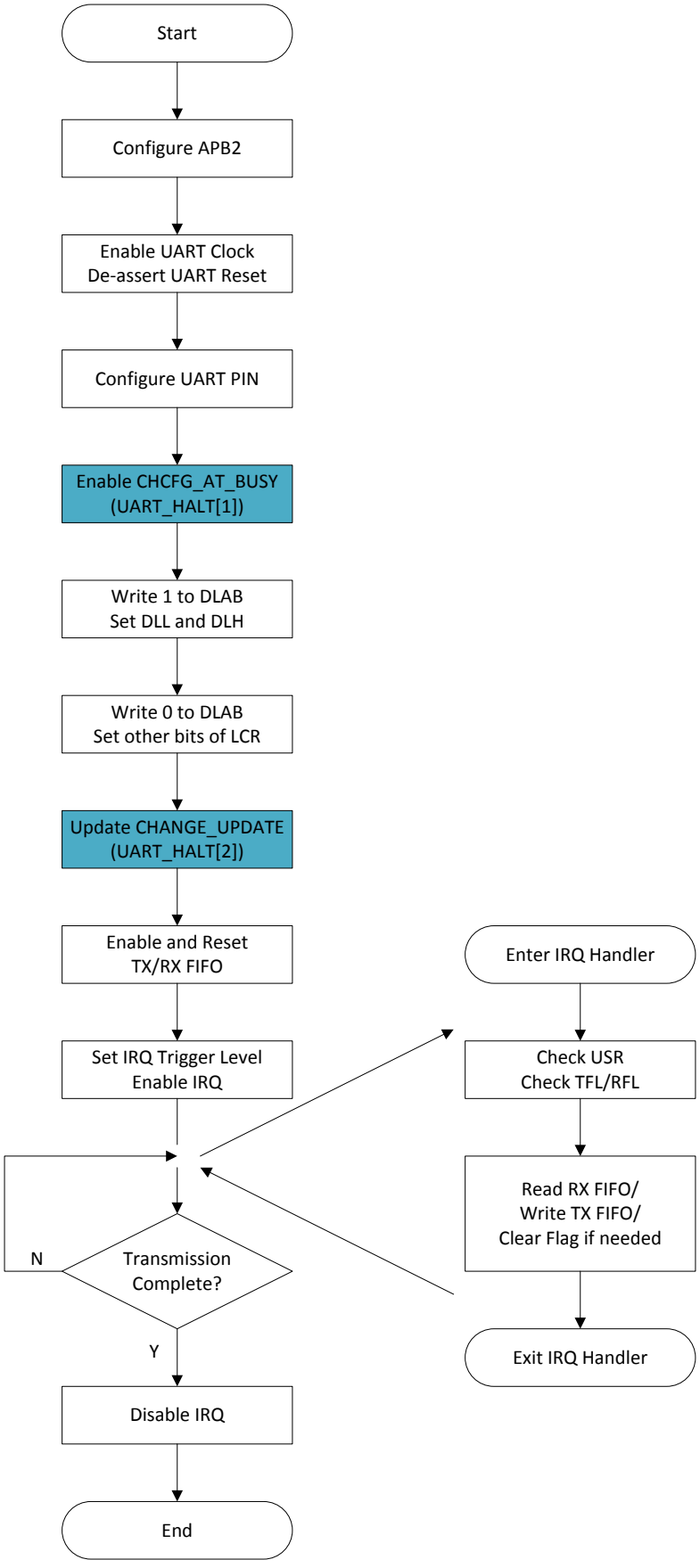


Figure 8-20. UART IRQ Flow Chart

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8.3.5. Register List

Module Name	Base Address
UART0	0x05000000
UART1	0x05000400
UART2	0x05000800
UART3	0x05000C00
R_UART0	0x07080000

Register Name	Offset	Description
UART_RBR	0x0000	UART Receive Buffer Register
UART_THR	0x0000	UART Transmit Holding Register
UART_DLL	0x0000	UART Divisor Latch Low Register
UART_DLH	0x0004	UART Divisor Latch High Register
UART_IER	0x0004	UART Interrupt Enable Register
UART_IIR	0x0008	UART Interrupt Identity Register
UART_FCR	0x0008	UART FIFO Control Register
UART_LCR	0x000C	UART Line Control Register
UART_MCR	0x0010	UART Modem Control Register
UART_LSR	0x0014	UART Line Status Register
UART_MSR	0x0018	UART Modem Status Register
UART_SCH	0x001C	UART Scratch Register
UART_USR	0x007C	UART Status Register
UART_TFL	0x0080	UART Transmit FIFO Level Register
UART_RFL	0x0084	UART Receive FIFO Level Register
UART_HSK	0x0088	UART DMA Handshake Configuration Register
UART_HALT	0x00A4	UART Halt TX Register
UART_DBG_DLL	0x00B0	UART Debug DLL Register
UART_DBG_DLH	0x00B4	UART Debug DLH Register
UART_485_CTL	0x00C0	UART RS485 Control and Status Register
RS485_ADDR_MATCH	0x00C4	UART RS485 Address Match Register
BUS_IDLE_CHK	0x00C8	UART RS485 Bus Idle Check Register
TX_DLY	0x00CC	UART TX Delay Register

8.3.6. Register Description

8.3.6.1. UART Receiver Buffer Register(Default Value: 0x0000_0000)

Offset: 0x00			Register Name: UART_RBR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	RBR

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			Receiver Buffer Register Data byte received on the serial input port (sin) in UART mode, or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set. If in FIFO mode and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an overrun error occurs.

8.3.6.2. UART Transmit Holding Register(Default Value: 0x0000_0000)

Offset: 0x00			Register Name: UART_THR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	W	0x0	THR Transmit Holding Register Data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in FIFO mode and FIFOs are enabled (FCR[0] = 1) and THRE is set, 16 number of characters of data may be written to the THR before the FIFO is full. Any attempt to write data when the FIFO is full results in the write data being lost.

8.3.6.3. UART Divisor Latch Low Register(Default Value: 0x0000_0000)

Offset: 0x00			Register Name: UART_DLL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DLL Divisor Latch Low Lower 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

8.3.6.4. UART Divisor Latch High Register(Default Value: 0x0000_0000)

Offset: 0x04			Register Name: UART_DLH
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:8	/	/	/
7:0	R/W	0x0	DLH Divisor Latch High Upper 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

8.3.6.5. UART Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: 0x04			Register Name: UART_IER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	PTIME Programmable THRE Interrupt Mode Enable This is used to enable/disable the generation of THRE Interrupt. 0: Disable 1: Enable
6:5	/	/	/
4	R/W	0x0	RS485_INT_EN RS485 Interrupt Enable 0:Disable 1:Enable
3	R/W	0x0	EDSSI Enable Modem Status Interrupt This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 0: Disable 1: Enable
2	R/W	0x0	ELSI Enable Receiver Line Status Interrupt This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0: Disable 1: Enable
1	R/W	0x0	ETBEI Enable Transmit Holding Register Empty Interrupt This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0: Disable 1: Enable
0	R/W	0x0	ERBFI Enable Received Data Available Interrupt This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts.

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			0: Disable 1: Enable

8.3.6.6. UART Interrupt Identity Register(Default Value: 0x0000_0001)

Offset: 0x08			Register Name: UART_IIR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R	0x0	FEFLAG FIFOs Enable Flag This is used to indicate whether the FIFOs are enabled or disabled. 00: Disable 11: Enable
5:4	/	/	/
3:0	R	0x1	IID Interrupt ID This indicates the highest priority pending interrupt which can be one of the following types: 0000: modem status 0001: no interrupt pending 0010: THR empty 0011:RS485 Interrupt 0100: received data available 0110: receiver line status 0111: busy detect 1100: character timeout Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

Interrupt ID	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset
0001	-	None	None	-
0110	Highest	Receiver line status	Overrun/parity/ framing errors or break interrupt	Reading the line status register
0011	Second	RS485 Interrupt	In RS485 mode, receives address data and match setting address	Writes 1 to addr flag to reset
0100	Third	Received data available	Receiver data available (non-FIFO mode or FIFOs disabled) or RCVR FIFO trigger level reached (FIFO mode and FIFOs enabled)	Reading the receiver buffer register (non-FIFO mode or FIFOs disabled) or the FIFO drops below the trigger level (FIFO mode and FIFOs enabled)
1100	Fourth	Character timeout indication	No characters in or out of the RCVR FIFO during the last 4 character times and there is at least 1character in it during This time	Reading the receiver buffer register
0010	Fifth	Transmit holding register	Transmitter holding register empty (Program THRE Mode disabled) or XMIT FIFO at or	Reading the IIR register (if source of interrupt); or, writing into THR (FIFOs or THRE Mode not selected or disabled) or

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		empty	below threshold (Program THRE Mode enabled)	XMIT FIFO above threshold (FIFOs and THRE Mode selected and enabled).
0000	Sixth	Modem status	Clear to send or data set ready or ring indicator or data carrier detect. Note that if auto flow control mode is enabled, a change in CTS (that is, DCTS set) does not cause an interrupt.	Reading the Modem status Register
0111	Seventh	Busy detect indication	UART_16550_COMPATIBLE = NO and master has tried to write to the Line Control Register while the UART is busy (USR[0] is set to one).	Reading the UART status register

8.3.6.7. UART FIFO Control Register(Default Value: 0x0000_0000)

Offset: 0x08			Register Name: UART_FCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	W	0x0	RT RCVR Trigger This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. 00: 1 character in the FIFO 01: FIFO ¼ full 10: FIFO ½ full 11: FIFO-2 less than full
5:4	W	0x0	TFT TX Empty Trigger This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. It also determines when the dma_tx_req_n signal is asserted when in certain modes of operation. 00: FIFO empty 01: 2 characters in the FIFO 10: FIFO ¼ full 11: FIFO ½ full
3	W	0x0	DMAM DMA Mode 0: Mode 0 In this mode, if PTE is high and TX FIFO is enable, the TX DMA request will send when TFL is less than or equal to FIFO Trigger Level. If PTE is high and TX FIFO is disabled, the TX DMA request will send when THRE is empty. If PTE is low, the TX DMA request will send when the TX FIFO is empty. If dma_pte_rx is high and RX FIFO is enabled, the rx drq will send when RFL is equal to or more than FIFO Trigger Level. 1: Mode 1

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			In this mode, if TX FIFO is enable and the PTE is high, the TX DMA request will send when TFL is less than or equal to FIFO Trigger Level. If PTE is low, the TX DMA request will send when TX FIFO is empty and the request stops only when TX FIFO is full. If RFL is equal to or more than FIFO Trigger Level, the rx drq will be set 1, in otherwise, it will be set 0.
2	W	0x0	XFIFOR XMIT FIFO Reset This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request. It is 'self-clearing'. It is not necessary to clear this bit.
1	W	0x0	RFIFOR RCVR FIFO Reset This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request. It is 'self-clearing'. It is not necessary to clear this bit.
0	W	0x0	FIFOE Enable FIFOs This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset.

8.3.6.8. UART Line Control Register(Default Value: 0x0000_0000)

Offset: 0x0C			Register Name: UART_LCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	DLAB Divisor Latch Access Bit It is writeable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers. 0: Select RX Buffer Register (RBR) / TX Holding Register(THR) and Interrupt Enable Register (IER) 1: Select Divisor Latch LS Register (DLL) and Divisor Latch MS Register (DLM)
6	R/W	0x0	BC Break Control Bit This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE = Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5:4	R/W	0x0	EPS Even Parity Select

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			It is writeable only when UART is not busy (USR[0] is zero) and always writable readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). Setting the LCR[5] is unset to reverse the LCR[4]. 00: Odd Parity 01: Even Parity 1X: Reverse LCR[4] In RS485 mode, it is the 9th bit--address bit. 11:9th bit = 0, indicates that this is a data byte. 10:9th bit = 1, indicates that this is an address byte. **NOTE** **When use this function, PEN(LCR[3]) must set to 1.**
3	R/W	0x0	PEN Parity Enable It is writeable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0: parity disabled 1: parity enabled
2	R/W	0x0	STOP Number of stop bits It is writeable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 0: 1 stop bit 1: 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit
1:0	R/W	0x0	DLS Data Length Select It is writeable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits

8.3.6.9. UART Modem Control Register(Default Value: 0x0000_0000)

Offset: 0x10			**Register Name: UART_MCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R/W	0x0	UART_FUNCTION Select IrDA or RS485 0:UART Mode 1:IrDA SIR Mode 2:RS485 Mode

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			3:Reverse
5	R/W	0x0	AFCE Auto Flow Control Enable When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled. 0: Auto Flow Control Mode disabled 1: Auto Flow Control Mode enabled
4	R/W	0x0	LOOP Loop Back Mode 0: Normal Mode 1: Loop Back Mode This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3	/	/	/
2	/	/	/
1	R/W	0x0	RTS Request to Send This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. 0: rts_n de-asserted (logic 1) 1: rts_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	R/W	0x0	DTR Data Terminal Ready This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n。 0: dtr_n de-asserted (logic 1) 1: dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.

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8.3.6.10. UART Line Status Register(Default Value: 0x0000_0060)

Offset:0x14			Register Name: UART_LSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R	0x0	FIFOERR RX Data Error in FIFO When FIFOs are disabled, this bit is always 0. When FIFOs are enabled, this bit is set to 1 when there is at least one PE, FE, or BI in the RX FIFO. It is cleared by a read from the LSR register provided there are no subsequent errors in the FIFO.
6	R	0x1	TEMT Transmitter Empty If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register and the TX Shift Register are empty. If the FIFOs are enabled, this bit is set whenever the TX FIFO and the TX Shift Register are empty. In both cases, this bit is cleared when a byte is written to the TX data channel.
5	R	0x1	THRE TX Holding Register Empty If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register is empty and ready to accept new data and it is cleared when the CPU writes to the TX Holding Register. If the FIFOs are enabled, this bit is set to "1" whenever the TX FIFO is empty and it is cleared when at least one byte is written to the TX FIFO.
4	R	0x0	BI Break Interrupt This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sir_in, is held in a logic '0' state for longer than the sum of *start time* + *data bits* + *parity* + *stop bits*. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of *start time* + *data bits* + *parity* + *stop bits*. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.
3	RC	0x0	FE Framing Error This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit

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			(LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0: no framing error 1:framing error Reading the LSR clears the FE bit.
2	RC	0x0	PE Parity Error This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0: no parity error 1: parity error Reading the LSR clears the PE bit.
1	RC	0x0	OE Overrun Error This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0: no overrun error 1: overrun error Reading the LSR clears the OE bit.
0	R	0x0	DR Data Ready This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 0: no data ready 1: data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

8.3.6.11. UART Modem Status Register(Default Value: 0x0000_0000)

Offset: 0x18			**Register Name: UART_MSR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R	0x0	DCD Line State of Data Carrier Detect This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. 0: dcd_n input is de-asserted (logic 1) 1: dcd_n input is asserted (logic 0)
6	R	0x0	RI

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			Line State of Ring Indicator This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. 0: ri_n input is de-asserted (logic 1) 1: ri_n input is asserted (logic 0)
5	R	0x0	DSR Line State of Data Set Ready This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with UART. 0: dsr_n input is de-asserted (logic 1) 1: dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR).
4	R	0x0	CTS Line State of Clear To Send This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with UART. 0: cts_n input is de-asserted (logic 1) 1: cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS).
3	RC	0x0	DDCD Delta Data Carrier Detect This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. 0: no change on dcd_n since last read of MSR 1: change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. **NOTE** **Ff the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted.**
2	RC	0x0	TERI Trailing Edge Ring Indicator This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. 0: no change on ri_n since last read of MSR 1: change on ri_n since last read of MSR Reading the MSR clears the TERI bit.
1	RC	0x0	DDSR Delta Data Set Ready This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. 0: no change on dsr_n since last read of MSR 1: change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). If the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset

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			occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted.
0	RC	0x0	DCTS Delta Clear to Send This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 0: no change on ctsdsr_n since last read of MSR 1: change on ctsdsr_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). If the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted.

8.3.6.12. UART Scratch Register(Default Value: 0x0000_0000)

Offset: 0x1C			Register Name: UART_SCH
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	SCRATCH_REG Scratch Register This register is for programmers to use as a temporary storage space. It has no defined purpose in the UART.

8.3.6.13. UART Status Register(Default Value: 0x0000_0006)

Offset: 0x7C			Register Name: UART_USR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R	0x0	RFF Receive FIFO Full This is used to indicate that the receive FIFO is completely full. 0: Receive FIFO not full 1: Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.
3	R	0x0	RFNE Receive FIFO Not Empty This is used to indicate that the receive FIFO contains one or more entries. 0: Receive FIFO is empty 1: Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.
2	R	0x1	TFE Transmit FIFO Empty This is used to indicate that the transmit FIFO is completely empty. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty.
1	R	0x1	TFNF

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			Transmit FIFO Not Full This is used to indicate that the transmit FIFO in not full. 0: Transmit FIFO is full 1: Transmit FIFO is not full This bit is cleared when the TX FIFO is full.
0	R	0x0	BUSY UART Busy Bit 0: Idle or inactive 1: Busy

8.3.6.14. UART Transmit FIFO Level Register(Default Value: 0x0000_0000)

Offset: 0x80			Register Name: UART_TFL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:0	R	0x0	TFL Transmit FIFO Level This is indicates the number of data entries in the transmit FIFO.

8.3.6.15. UART Receive FIFO Level Register(Default Value: 0x0000_0000)

Offset: 0x84			Register Name: UART_RFL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:0	R	0x0	RFL Receive FIFO Level This is indicates the number of data entries in the receive FIFO.

8.3.6.16. UART DMA Handshake Configuration Register(Default Value: 0x0000_00E5)

Offset: 0x88			Register Name: UART_HSK
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0xE5	Handshake configuration 0xA5: DMA wait cycle mode 0xE5: DMA handshake mode

8.3.6.17. UART Halt TX Register(Default Value: 0x0000_0000)

Offset: 0xA4			Register Name: UART_HALT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	PTE

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			The sending of TX_REQ. In DMA1 mode (FIFO on), if PTE is set 1, when TFL is less than trig, send the DMA request. If PTE is set 0, when FIFO is empty, send the DMA request. The DMA request will stop when FIFO is full. In DMA0 mode, if PTE is set 1 and FIFO on, when TFL is less than trig, send DMA request. If PTE is set 1 and FIFO off, when THRE is empty, send DMA request. If PTE is set 0, when FIFO is empty, send DMA request.
6	R/W	0x0	DMA_PTE_RX The sending of RX_DRQ. In DMA1 mode, when RFL is more than or equal to trig or receive timeout, send DRQ. In DMA0 mode, if DMA_PTE_RX = 1 and FIFO on, when RFL is more than trig, send DRQ. In other cases, once the receive data is valid, send DRQ.
5	R/W	0x0	SIR_RX_INVERT SIR Receiver Pulse Polarity Invert 0: Not invert receiver signal 1: Invert receiver signal
4	R/W	0x0	SIR_TX_INVERT SIR Transmit Pulse Polarity Invert 0: Not invert transmit pulse 1: Invert transmit pulse
3	/	/	/
2	R/WAC	0x0	CHANGE_UPDATE After the user using HALT[1] to change the baudrate or LCR configuration, write 1 to update the configuration and waiting this bit self clear to 0 to finish update process. Write 0 to this bit has no effect. 1: Update trigger, Self clear to 0 when finish update.
1	R/W	0x0	CHCFG_AT_BUSY This is an enable bit for the user to change LCR register configuration and baudrate register (DLH and DLL) when the UART is busy (USB[0] is 1). 1: Enable change when busy
0	R/W	0x0	HALT_TX Halt TX This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 0 : Halt TX disabled 1 : Halt TX enabled  **NOTE** **If FIFOs are not enabled, the setting has no effect on operation.**

8.3.6.18. UART DBG DLL Register(Default Value: 0x0000_0000)

Offset: 0xB0			Register Name: UART_DBG_DLL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DEBUG DLL

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8.3.6.19. UART DBG DLH Register(Default Value: 0x0000_0000)

Offset: 0xB4			Register Name: UART_DBG_DLH
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DEBUG DLH

8.3.6.20. UART RS485 Control and Status Register(Default Value: 0x0000_0000)

Offset: 0xC0			Register Name: UART_485_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	Reserved
6	R/W1C	0x0	AAD_ADDR_F In AAD mode, when UART receives an address byte and the byte is the same as RS485_ADDR_MATCH, this bit will be set 1.If RS485 interrupt is enabled, the RS485 interrupt will arrive. Write 1 to clear this bit and reset the RS485 interrupt.
5	R/W1C	0x0	RS485_ADDR_DET_F This is a flag of the detecting of address bytes. When UART receives an address byte, this bit will be set 1.If the RS485 Interrupt is enabled, the RS485 interrupt will arrive. 1:An address byte is detected 0:No address byte is detected Write 1 to clear this bit and reset the RS485 interrupt.
4	/	/	reverse
3	R/W	0x0	RX_BF_ADDR In NMM mode, If set this bit as 1, UART will receive all the bytes into FIFO before receiving an address byte. If set as 0, it will not. 1:Receive 0:Not Receive
2	R/W	0x0	RX_AF_ADDR In NMM mode, if set this bit as 1, UART will receive all the bytes into FIFO after receiving an address byte. If set as 0, it will not. 1:Receive 0:Not Receive
1:0	R/W	0x0	RS485_SLAVE_MODE_SEL RS485 Slave Mode 00: Normal Multidrop Operation（NMM） 01: Auto Address Detection Operation（AAD） 10: reserved 11: reserved

8.3.6.21. UART RS485 Address Match Register(Default Value: 0x0000_0000)

Offset: 0xC4			Register Name: RS485_ADDR_MATCH
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:8	/	/	/
7:0	R/W	0x0	ADDR_MATCH The matching address uses in AAD mode. It is only available is AAD.

8.3.6.22. UART RS485 Bus Idle Check Register(Default Value: 0x0000_0000)

Offset: 0xC8			Register Name: BUS_IDLE_CHK
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	BUS_IDLE_CHK_EN 1: Enable bus idle check function 0: Disable bus idle check function
6	R	0x0	BUS_STATUS The Flag of Bus Status 1:busy 0:idle
5:0	R	0x0	ADJ_TIME Bus Idle Time. The unit is 8*16*Tclk.

8.3.6.23. UART TX Delay Register(Default Value: 0x0000_0000)

Offset: 0xCC			Register Name: TX_DLY
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DLY The delay time between the last stop bit and the next start bit. The uint is 16*Tclk. It is used to control the space between two bytes in TX.

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8.4. USB2.0 OTG

8.4.1. Overview

The USB2.0 OTG is a Dual-Role Device controller, which supports both device and host functions which can also be configured as a Host-only or Device-only controller, fully compliant with the USB 2.0 Specification. It can support high-speed (HS, 480-Mbps), full-speed (FS, 12-Mbps), and low-speed (LS, 1.5-Mbps) transfers in Host mode. It can support high-speed (HS, 480-Mbps), and full-speed (FS, 12-Mbps) in Device mode. Standard USB transceiver can be used through its UTMI+PHY Level3 interface. The UTMI+PHY interface is bidirectional with 8-bit data bus. For saving CPU bandwidth, USB-OTG DMA interface can support external DMA controller to take care of the data transfer between the memory and USB-OTG FIFO. The USB-OTG core also supports USB power saving functions.

Features:

- Complies with USB 2.0 Specification
- Supports High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps), and Low-Speed (LS, 1.5-Mbps) in Host mode
- Supports High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps) in Device mode
- Supports the UTMI+ Level 3 interface. The 8-bit bidirectional data buses are used
- Supports bi-directional endpoint0 for Control transfer
- Supports up to 8 User-Configurable Endpoints for Bulk, Isochronousl and Interrupt bi-directional transfers (Endpoint1, Endpoint2, Endpoint3, Endpoint4)
- Supports up to (4KB+64Bytes) FIFO for EPs (including EP0)
- Supports High-Bandwidth Isochronous & Interrupt transfers
- Automated splitting/combining of packets for Bulk transfers
- Supports point-to-point and point-to-multipoint transfer in both Host and Peripheral mode
- Includes automatic ping capabilities
- Soft connect/disconnect function
- Performs all transaction scheduling in hardware
- Power Optimization and Power Management capabilities
- Includes interface to an external Normal DMA controller for every EPs

8.4.2. Block Diagram

Figure 8-21 shows the block diagram of USB OTG Controller.

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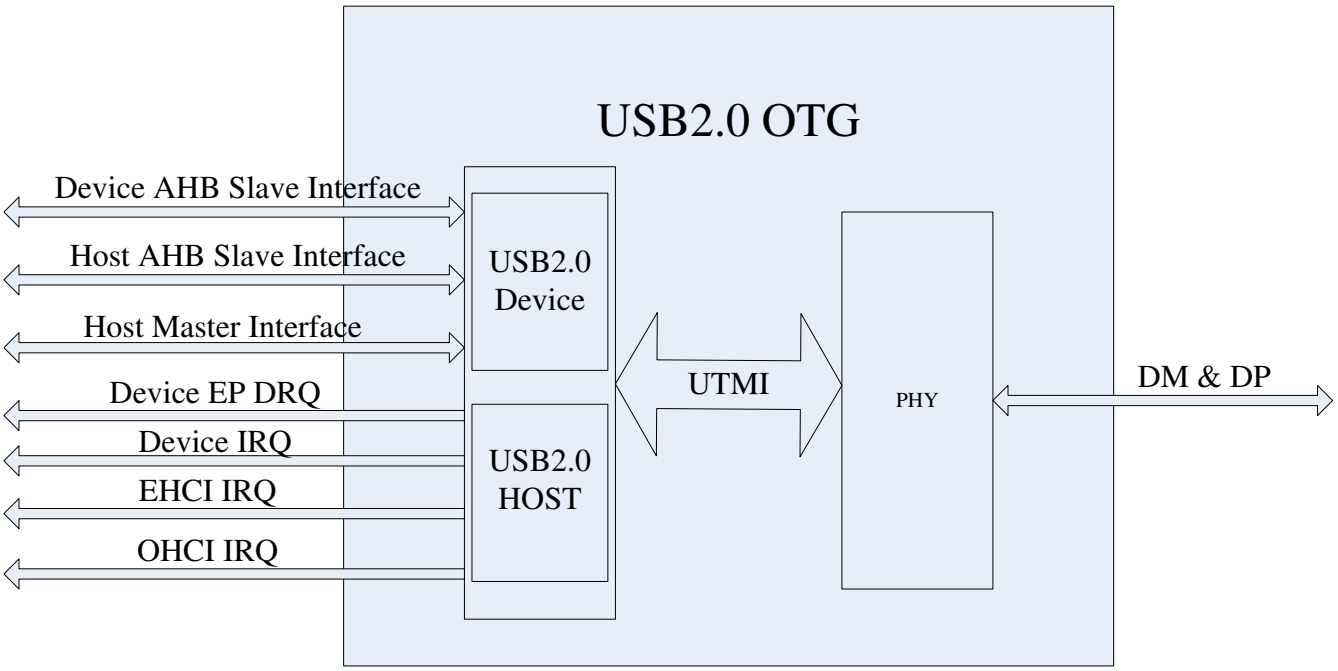


Figure 8-21. USB OTG Controller Block Diagram

8.4.3. External Signals

Table 8-13. USB2.0 OTG External Signals

Signal	Description	Type
USB0-DP	USB2.0 OTG differential signal postive	AI/O
USB0-DM	USB2.0 OTG differential signal negative	AI/O

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8.5. USB3.0 Host Controller

8.5.1. Overview

USB3.0 Host Controller is fully compliant with the USB 3.0 specification, eXtensible Host Controller Interface (XHCI) Specification. The controller supports Super-Speed (SS, 5-Gbps), High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps) and Low-Speed (LS, 1.5-Mbps).

Features:

- Supports Super-Speed (SS, 5-Gbps), High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps) and Low-Speed (LS,1.5-Mbps) in Host mode
- AHB, AXI, or Native Master interface for DMA operation
- AHB, AXI, or Native Slave interface for read and write access to the core's Control and Status Registers (CSRs) and debug access to the RAMs.
- USB 3.0 PIPE3 PHY interface
- USB 2.0 UTMI+ (L3) PHY interface
- Simultaneous IN and OUT transfer support in superspeed mode

8.5.2. Block Diagram

Figure 8-22 shows the system-level block diagram of USB3.0 Host Controller.

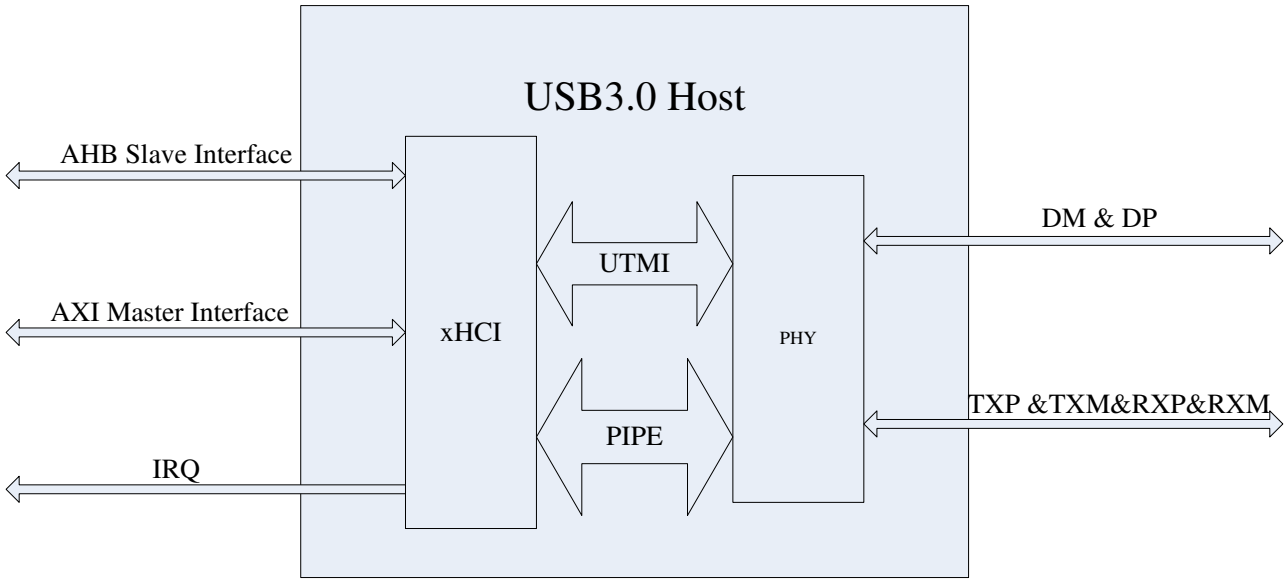


Figure 8-22. USB3.0 Host Controller Block Diagram

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8.5.3. Operations and Functional Descriptions

8.5.3.1. External Signals

Table 8-14. USB3.0 Host External Signals

Signal	Description	Type
USB1-DP	USB3.0 Host differential signal postive	AI/O
USB1-DM	USB3.0 Host differential signal negative	AI/O
USB1-SSRXP	USB3.0 Host SuperSpeed differential signal RX postive	AI/O
USB1-SSRXM	USB3.0 Host SuperSpeed differential signal RX negative	AI/O
USB1-SSTXP	USB3.0 Host SuperSpeed differential signal TX postive	AI/O
USB1-SSTXM	USB3.0 Host SuperSpeed differential signal TX negative	AI/O

8.5.3.2. Clock and Reset

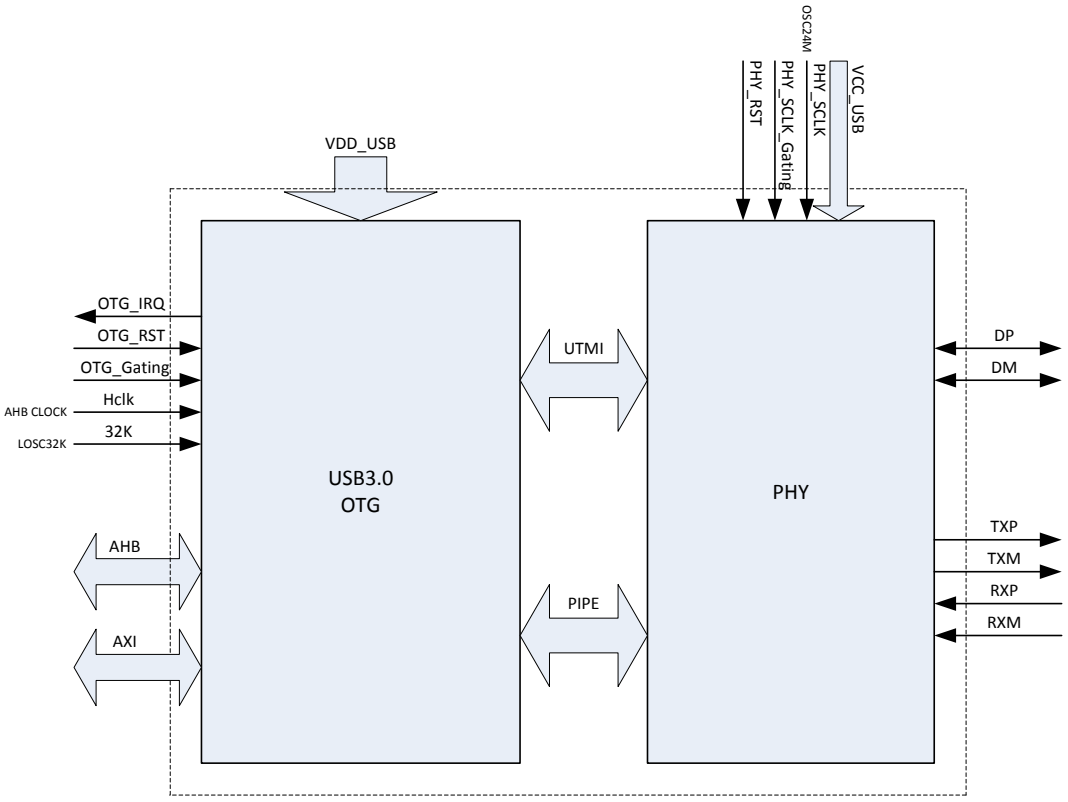


Figure 8-23. USB3.0 Host Clock and Reset

8.5.3.3. Function Implementation

Please refer to USB3.0 Specification, USB2.0 Specification, eXtensible Host Controller Interface(XHCI) Specification, Version 1.1.

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8.6. USB2.0 Host Controller

8.6.1. Overview

USB2.0 Host Controller is fully compliant with the USB 2.0 specification, Enhanced Host Controller Interface (EHCI) Specification, Revision 1.0, and the Open Host Controller Interface (OHCI) Specification Release 1.0a. The controller supports high-speed, 480-Mbps transfers (40 times faster than USB 1.1 full-speed mode) using an EHCI Host Controller, as well as full and low speeds through one or more integrated OHCI Host Controllers.

The USB2.0 Host controller includes the following features:

- Supports industry-standard AMBA High-Performance Bus (AHB) and it is fully compliant with the AMBA Specification, Revision 2.0. Supports bus.
- Supports 32-bit Little Endian AMBA AHB Slave Bus for Register Access.
- Supports 32-bit Little Endian AMBA AHB Master Bus for Memory Access.
- Including an internal DMA Controller for data transfer with memory.
- Complies with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.
- Supports High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps), and Low-Speed (LS, 1.5-Mbps) Device.
- Supports the UTMI+ Level 3 interface. The 8-bit bidirectional data buses are used.
- Supports only 1 USB Root Port shared between EHCI and OHCI.

8.6.2. Block Diagram

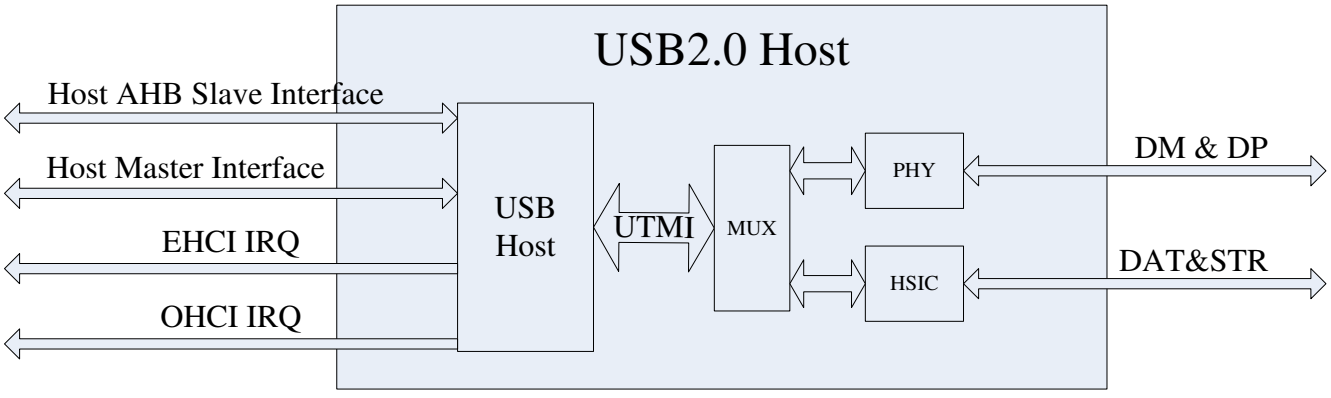


Figure 8-24. USB2.0 Host Controller Block Diagram

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8.6.3. Operations and Functional Descriptions

8.6.3.1. External Signals

Table 8-15. USB2.0 Host External Signals

Signal	Description	Type
USB2-DP	USB2.0 Host differential signal postive	AI/O
USB2-DM	USB2.0 Host differential signal negative	AI/O

8.6.3.2. Clock and Reset

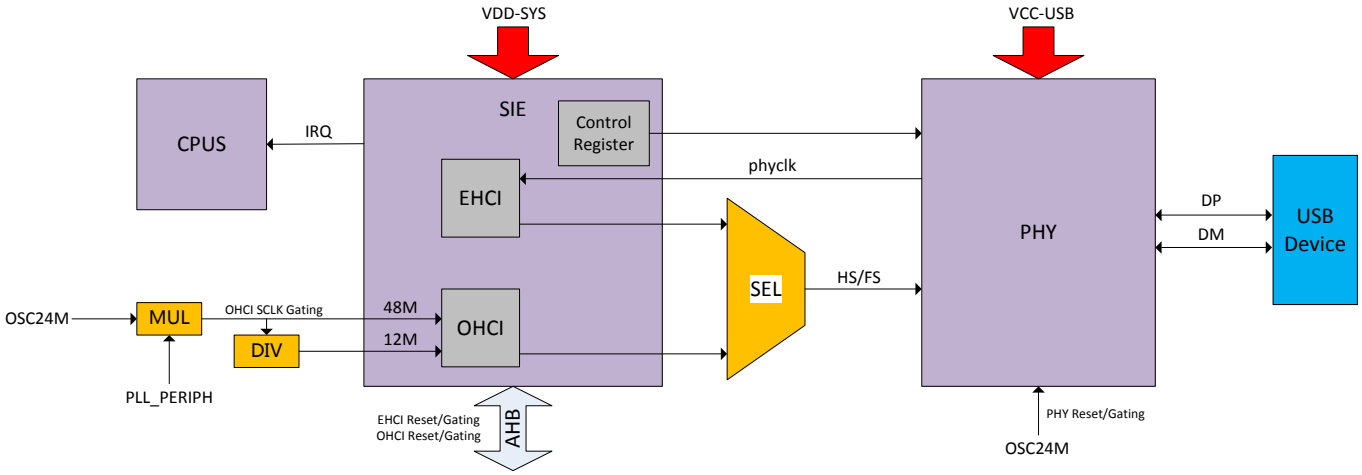


Figure 8-25. USB2.0 Host Clock Description

8.6.3.3. Function Implementation

Please refer to USB2.0 Specification, Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.

8.6.4. Register List

Module Name	Base Address
USB2.0_HOST	0x05311000

Register Name	Offset	Description
EHCI Capability Register		
E_CAPLENGTH	0x000	EHCI Capability register Length Register
E_HCIVERSION	0x002	EHCI Host Interface Version Number Register

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E_HCSPARAMS	0x004	EHCI Host Control Structural Parameter Register
E_HCCPARAMS	0x008	EHCI Host Control Capability Parameter Register
E_HCSPPORTROUTE	0x00C	EHCI Companion Port Route Description
EHCI Operational Register		
E_USBCMD	0x010	EHCI USB Command Register
E_USBSTS	0x014	EHCI USB Status Register
E_USBINTR	0x018	EHCI USB Interrupt Enable Register
E_FRINDEX	0x01C	EHCI USB Frame Index Register
E_CTRLDSSEGMENT	0x020	EHCI 4G Segment Selector Register
E_PERIODICLISTBASE	0x024	EHCI Frame List Base Address Register
E_ASYNCLISTADDR	0x028	EHCI Next Asynchronous List Address Register
E_CONFIGFLAG	0x050	EHCI Configured Flag Register
E_PORTSC	0x054	EHCI Port Status/Control Register
OHCI Control and Status Partition Register		
O_HcRevision	0x400	OHCI Revision Register
O_HcControl	0x404	OHCI Control Register
O_HcCommandStatus	0x408	OHCI Command Status Register
O_HcInterruptStatus	0x40C	OHCI Interrupt Status Register
O_HcInterruptEnable	0x410	OHCI Interrupt Enable Register
O_HcInterruptDisable	0x414	OHCI Interrupt Disable Register
OHCI Memory Pointer Partition Register		
O_HcHCCA	0x418	OHCI HCCA Base
O_HcPeriodCurrentED	0x41C	OHCI Period Current ED Base
O_HcControlHeadED	0x420	OHCI Control Head ED Base
O_HcControlCurrentED	0x424	OHCI Control Current ED Base
O_HcBulkHeadED	0x428	OHCI Bulk Head ED Base
O_HcBulkCurrentED	0x42c	OHCI Bulk Current ED Base
O_HcDoneHead	0x430	OHCI Done Head Base
OHCI Frame Counter Partition Register		
O_HcFmInterval	0x434	OHCI Frame Interval Register
O_HcFmRemaining	0x438	OHCI Frame Remaining Register
O_HcFmNumber	0x43C	OHCI Frame Number Register
O_HcPerioddicStart	0x440	OHCI Periodic Start Register
O_HcLSThreshold	0x444	OHCI LS Threshold Register
OHCI Root Hub Partition Register		
O_HcRhDescriptorA	0x448	OHCI Root Hub Descriptor Register A
O_HcRhDesriptorB	0x44C	OHCI Root Hub Descriptor Register B
O_HcRhStatus	0x450	OHCI Root Hub Status Register
O_HcRhPortStatus	0x454	OHCI Root Hub Port Status Register
HCI Controller and PHY Interface Register		
HCI Interface	0x800	HCI Interface Register
PHY Control	0x810	PHY Control Register
HSIC PHY tune1	0x81C	HSIC PHY Tune1 Register
HSIC PHY tune2	0x820	HSIC PHY Tune2 Register
HSIC PHY tune3	0x824	HSIC PHY Tune3 Register

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HCI SIE Port Disable Control	0x828	HCI SIE Port Disable Control Register

8.6.5. EHCI Register Description

8.6.5.1. EHCI Identification Register(Default Value:0x10)

Offset:0x0000			Register Name: CAPLENGTH
Bit	**Read/Write**	**Default/Hex**	**Description**
7:0	R	0x10	CAPLENGTH The value in these bits indicates an offset to add to register base to find the beginning of the Operational Register Space.

8.6.5.2. EHCI Host Interface Version Number Register(Default Value:0x0100)

Offset: 0x0002			Register Name: HCIVERSION
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R	0x0100	HCIVERSION This is a 16-bit register containing a BCD encoding of the EHCI revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision.

8.6.5.3. EHCI Host Control Structural Parameter Register(Default Value:0x0000_0004)

Offset: 0x0004			Register Name: HCSPARAMS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	R	0x0	Debug Port Number This register identifies which of the host controller ports is the debug port. The value is the port number (one based) of the debug port. This field will always be '0'.
19:16	/	/	/
15:12	R	0x0	Number of Companion Controller (N_CC) This field indicates the number of companion controllers associated with this USB2.0 host controller. A zero in this field indicates there are no companion host controllers. And a value larger than zero in this field indicates there are companion USB1.1 host controller(s). This field will always be '0'.
11:8	R	0x0	Number of Port per Companion Controller(N_PCC) This field indicates the number of ports supported per companion host

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<table>
<tr><td></td><td></td><td></td><td>controller host controller. It is used to indicate the port routing configuration to system software.
This field will always fix with ‘0’.</td></tr>
<tr><td>7</td><td>R</td><td>0x0</td><td>Port Routing Rules
This field indicates the method used by this implementation for how all ports are mapped to companion controllers. The value of this field has the following interpretation:
<table>
<tr><td>Value</td><td>Meaning</td></tr>
<tr><td>0</td><td>The first N_PCC ports are routed to the lowest numbered function companion host controller, the next N_PCC port are routed to the next lowest function companion controller, and so on.</td></tr>
<tr><td>1</td><td>The port routing is explicitly enumerated by the first N_PORTS elements of the HCSP-PORTTOUTE array.</td></tr>
</table>
This field will always be ‘0’.</td></tr>
<tr><td>6:4</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>3:0</td><td>R</td><td>0x1</td><td>N_PORTS
This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Valid values are in the range of 0x1 to 0x0f.
This field is always 1.</td></tr>
</table>

8.6.5.4. EHCI Host Control Capability Parameter Register(Default Value:0x0000_0008)

Offset: 0x0008			**Register Name: HCCPARAMS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R	0x0	EHCI Extended Capabilities Pointer (EECP) This optional field indicates the existence of a capabilities list. A value of 00b indicates no extended capabilities are implemented. A non-zero value in this register indicates the offset in PCI configuration space of the first EHCI extended capabiliby. The pointer value must be 40h or greater if implemented to maintain to consistency of the PCI header defined for this calss of device. The value of this field is always ‘00b’.
7:4	R	0x0	Isochronous Scheduling Threshold This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. When bit[7] is zero, the value of the least significant 3 bits indicates the number of micro-frames a host controller can hold a set of isochronous data structures(one or more) before flushing the state. When bit[7] is a one, then host software assumes the host controller may cache an isochronous data structure for an entire frame.

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3	/	/	/
2	R	0x0	Asynchronous Schedule Park Capability If this bit is set to a one, then the host controller supports the park feature for high-speed queue heads in the Asynchronous Schedule. The feature can be disabled or enabled and set to a specific level by using the Asynchronous Schedule Park Mode Enable and Asynchronous Schedule Park Mode Count fields in the USBCMD register.
1	R	0x0	Programmable Frame List Flag If this bit is set to a zero, then system software must use a frame list length of 1024 elements with this host controller. The USBCMD register Frame List Size field is a read-only register and should be set to zero. If set to 1, then system software can specify and use the frame list in the USBCMD register Frame List Size field to cofigure the host controller. The frame list must always aligned on a 4K page boundary. This requirement ensures that the frame list is always physically contiguous.
0	/	/	/

8.6.5.5. EHCI Companion Port Route Description(Default Value:0x0000_0000)

Offset: 0x000C			**Register Name: HCSP-PORTROUTE**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	HCSP-PORTROUTE This optional field is valid only if Port Routing Rules field in HCSPARAMS register is set to a one. This field is used to allow a host controller implementation to explicitly describe to which companion host controller each implemented port is mapped. This field is a 15-element nibble array (each 4 bit is one array element). Each array location corresponds one-to-one with a physical port provided by the host controller (e.g. PORTROUTE [0] corresponds to the first PORTSC port, PORTROUTE [1] to the second PORTSC port, etc.). The value of each element indicates to which of the companion host controllers this port is routed. Only the first N_PORTS elements have valid information. A value of zero indicates that the port is routed to the lowest numbered function companion host controller. A value of one indicates that the port is routed to the next lowest numbered function companion host controller, and so on.

8.6.5.6. EHCI USB Command Register(Default Value:0x0008_0000)

Offset: 0x0010			**Register Name: USBCMD**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x08	Interrupt Threshold Control The value in this field is used by system software to select the maximum rate at which the host controller will issue interrupts. The only valid values

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<table>
<tr><td></td><td></td><td></td><td>are defined below:
<table><tr><td>Value</td><td>Minimum Interrupt Interval</td></tr><tr><td>0x00</td><td>Reserved</td></tr><tr><td>0x01</td><td>1 micro-frame</td></tr><tr><td>0x02</td><td>2 micro-frame</td></tr><tr><td>0x04</td><td>4 micro-frame</td></tr><tr><td>0x08</td><td>8 micro-frame(default, equates to 1 ms)</td></tr><tr><td>0x10</td><td>16 micro-frame(2ms)</td></tr><tr><td>0x20</td><td>32 micro-frame(4ms)</td></tr><tr><td>0x40</td><td>64 micro-frame(8ms)</td></tr></table>Any other value in this register yields undefined results.
The default value in this field is 0x08 .
Software modifications to this bit while HC Halted bit is equal to zero results in undefined behavior.</td></tr>
<tr><td>15:12</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>11</td><td>R</td><td>0x0</td><td>Asynchronous Schedule Park Mode Enable(OPTIONAL)
If the Asynchronous Park Capability bit in the HCCPARAMS register is a one, then this bit defaults to a 1 and is R/W. Otherwise the bit must be a zero and is Read Only. Software uses this bit to enable or disable Park mode. When this bit is one, Park mode is enabled. When this bit is zero, Park mode is disabled.</td></tr>
<tr><td>10</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>9:8</td><td>R</td><td>0x0</td><td>Asynchronous Schedule Park Mode Count(OPTIONAL)
Asynchronous Park Capability bit in the HCCPARAMS register is a one,
Then this field defaults to 0x3 and is W/R. Otherwise it defaults to zero and is R. It contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the Asynchronous schedule before continuing traversal of the Asynchronous schedule.
Valid value are 0x1 to 0x3.Software must not write a zero to this bit when Park Mode Enable is a one as it will result in undefined behavior.</td></tr>
<tr><td>7</td><td>R/W</td><td>0x0</td><td>Light Host Controller Reset(OPTIONAL)
This control bit is not required.
If implemented, it allows the driver to reset the EHCI controller without affecting the state of the ports or relationship to the companion host controllers. For example, the PORSTC registers should not be reset to their default values and the CF bit setting should not go to zero (retaining port ownership relationships).
A host software read of this bit as zero indicates the Light Host Controller Reset has completed and it si safe for software to re-initialize the host controller. A host software read of this bit as a one indicates the Light Host</td></tr>
<tr><td>6</td><td>R/W</td><td>0x0</td><td>Interrupt on Async Advance Doorbell
This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Soft-
Ware must write a 1 to this bit to ring the doorbell.</td></tr>
</table>

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<table>
<tr><td></td><td></td><td></td><td>When the host controller has evicted all appropriate cached schedule state, it sets the Interrupt on Async Advance status bit in the USBSTS. if the Interrupt on Async Advance Enable bit in the USBINTR register is a one then the host controller will assert an interrupt at the next interrupt threshold.
The host controller sets this bit to a zero after it has set the Interrupt on Async Advance status bit in the USBSTS register to a one.
Software should not write a one to this bit when the asynchronous schedule is disabled. Doing so will yield undefined results.</td></tr>
<tr><td>5</td><td>R/W</td><td>0x0</td><td>Asynchronous Schedule Enable
This bit controls whether the host controller skips processing the Asynchronous Schedule. Values mean:<table><tr><td>Bit Value</td><td>Meaning</td></tr><tr><td>0</td><td>Do not process the Asynchronous Schedule.</td></tr><tr><td>1</td><td>Use the ASYNLISTADDR register to access the Asynchronous Schedule.</td></tr></table>The default value of this field is ‘0b’.</td></tr>
<tr><td>4</td><td>R/W</td><td>0x0</td><td>Periodic Schedule Enable
This bit controls whether the host controller skips processing the Periodic Schedule. Values mean:<table><tr><td>Bit Value</td><td>Meaning</td></tr><tr><td>0</td><td>Do not process the Periodic Schedule.</td></tr><tr><td>1</td><td>Use the PERIODICLISTBASE register to access the Periodic Schedule.</td></tr></table>The default value of this field is ‘0b’.</td></tr>
<tr><td>3:2</td><td>R/W</td><td>0x0</td><td>Frame List Size
This field is R/W only if Programmable Frame List Flag in the HCCPARAMS registers is set to a one. This field specifies the size of the
Frame list. The size the frame list controls which bits in the Frame Index Register should be used for the Frame List Current index. Values mean:<table><tr><td>Bits</td><td>Meaning</td></tr><tr><td>00b</td><td>1024 elements(4096bytes)Default value</td></tr><tr><td>01b</td><td>512 elements(2048byts)</td></tr><tr><td>10b</td><td>256 elements(1024bytes)For resource-constrained condition</td></tr><tr><td>11b</td><td>reserved</td></tr></table>The default value is ‘00b’.</td></tr>
<tr><td>1</td><td>R/W</td><td>0x0</td><td>Host Controller Reset
This control bit is used by software to reset the host controller. The effects of this on Root Hub registers are similar to a Chip Hardware Reset.
When software writes a one to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports.
All operational registers, including port registers and port state machines are set to their initial values. Port ownership reverts to the companion host controller(s). Software must reinitialize the host controller as described in</td></tr>
</table>

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			Section 4.1 of the CHEI Specification in order to return the host controller to an operational state. This bit is set to zero by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a zero to this register. Software should not set this bit to a one when the HC Halted bit in the USBSTS register is a zero. Attempting to reset an actively running host controller will result in undefined behavior.
0	R/W	0x0	Run/Stop When set to a 1, the Host Controller proceeds with execution of the schedule. When set to 0, the Host Controller completes the current and any actively pipelined transactions on the USB and then halts. The Host Controller must halt within 16 micro-frames after software clears this bit. The HC Halted bit indicates when the Host Controller has finished its pending pipelined transactions and has entered the stopped state. Software must not write a one to this field unless the Host Controller is in the Halt State. The default value is 0x0.

8.6.5.7. EHCI USB Status Register(Default Value:0x0000_1000)

Offset: 0x0014			**Register Name: USBSTS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R	0x0	Asynchronous Schedule Status The bit reports the current real status of Asynchronous Schedule. If this bit is a zero then the status of the Asynchronous Schedule is disabled. If this bit is a one then the status of the Asynchronous Schedule is enabled. The Host Controller is not required to immediately disable or enable the Asynchronous Schedule when software transitions the Asynchronous Schedule Enable bit in the USBCMD register. When this bit and the Asynchronous Schedule Enable bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0).
14	R	0x0	Periodic Schedule Status The bit reports the current real status of the Periodic Schedule. If this bit is a zero then the status of the Periodic Schedule is disabled. If this bit is a one then the status of the Periodic Schedule is enabled. The Host Controller is not required to *immediately* disable or enable the Periodic Schedule when software transitions the *Periodic Schedule Enable* bit in the USBCMD register. When this bit and the *Periodic Schedule Enable* bit are the same value, the Periodic Schedule is either enabled (1) or disabled (0).
13	R	0x0	Reclamation This is a read-only status bit, which is used to detect an empty asynchronous schedule.
12	R	0x1	HC Halted

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			This bit is a zero whenever the Run/Stop bit is a one. The Host Controller Sets this bit to one after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the Host Controller Hardware (e.g. internal error). The default value is '1'.
11:6	/	/	/
5	R/W1C	0x0	Interrupt on Async Advance System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a one to the Interrupt on Async Advance Doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source.
4	R/W1C	0x0	Host System Error The Host Controller set this bit to 1 when a serious error occurs during a host system access involving the Host Controller module. When this error occurs, the Host Controller clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs.
3	R/W1C	0x0	Frame List Rollover The Host Controller sets this bit to a one when the Frame List Index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size is 1024, the Frame Index Register rolls over every time FRINDEX [13] toggles. Similarly, if the size is 512, the Host Controller sets this bit to a one every time FRINDEX [12] toggles.
2	R/W1C	0x0	Port Change Detect The Host Controller sets this bit to a one when any port for which the Port Owner bit is set to zero has a change bit transition from a zero to a one or a Force Port Resume bit transition from a zero to a one as a result of a J-K transition detected on a suspended port. This bit will also be set as a result of the Connect Status Chang being set to a one after system software has relinquished ownership of a connected port by writing a one to a port's Port Owner bit.
1	R/W1C	0x0	USB Error Interrupt(USBERRINT) The Host Controller sets this bit to 1 when completion of USB transaction results in an error condition(e.g. error counter underflow).If the TD on which the error interrupt occurred also had its IOC bit set, both. This bit and USBINT bit are set.
0	R/W1C	0x0	USB Interrupt(USBINT) The Host Controller sets this bit to a one on the completion of a USB transaction, which results in the retirement of a Transfer Descriptor that had its IOC bit set. The Host Controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes)

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8.6.5.8. EHCI USB Interrupt Enable Register(Default Value:0x0000_0000)

Offset: 0x0018			Register Name: USBINTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W	0x0	Interrupt on Async Advance Enable When this bit is 1, and the Interrupt on Async Advance bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.
4	R/W	0x0	Host System Error Enable When this bit is 1, and the Host System Error Status bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit.
3	R/W	0x0	Frame List Rollover Enable When this bit is 1, and the Frame List Rollover bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.
2	R/W	0x0	Port Change Interrupt Enable When this bit is 1, and the Port Chang Detect bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Chang Detect bit.
1	R/W	0x0	USB Error Interrupt Enable When this bit is 1, and the USBERRINT bit in the USBSTS register is 1,the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit.
0	R/W	0x0	USB Interrupt Enable When this bit is 1, and the USBINT bit in the USBSTS register is 1,the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit.

8.6.5.9. EHCI Frame Index Register(Default Value:0x0000_0000)

Offset: 0x001C			Register Name: FRINDEX
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0	Frame Index The value in this register increment at the end of each time frame (e.g. micro-frame).Bits[N:3] are used for the Frame List current index. It means that each location of the frame list is accessed 8 times(frames or Micro-frames) before moving to the next index. The following illustrates Values of N based on the value of the Frame List Size field in the USBCMD register.

USBCMD[Frame List Size]	Number Elements	N

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			00b	1024	12
			01b	512	11
			10b	256	10
			11b	Reserved	

NOTE

This register must be written as a DWord. Byte writes produce undefined results.

8.6.5.10. EHCI Periodic Frame List Base Address Register(Default Value:0x0000_0000)

Offset: 0x0024			Register Name: PERIODICLISTBASE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	0x0	Base Address These bits correspond to memory address signals [31:12], respectively. This register contains the beginning address of the Periodic Frame List in the system memory. System software loads this register prior to starting the schedule execution by the Host Controller. The memory structure referenced by this physical memory pointer is assumed to be 4-K byte aligned. The contents of this register are combined with the Frame Index Register (FRINDEX) to enable the Host Controller to step through the Periodic Frame List in sequence.
11:0	/	/	/

NOTE

Writes must be Dword Writes.

8.6.5.11. EHCI Current Asynchronous List Address Register(Default Value:0x0000_0000)

Offset: 0x0028			Register Name: ASYNCLISTADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	R/W	0x0	Link Pointer (LP) This field contains the address of the next asynchronous queue head to be executed. These bits correspond to memory address signals [31:5], respectively.
4:0	/	/	/

NOTE

Write must be DWord Writes.

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8.6.5.12. EHCI Configure Flag Register(Default Value:0x0000_0000)

Offset: 0x0050			Register Name: CONFIGFLAG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	Configure Flag(CF) Host software sets this bit as the last action in its process of configuring the Host Controller. This bit controls the default port-routing control logic as follow: Value: 0 — Port routing control logic default-routs each port to an implementation dependent classic host controller. Value: 1 — Port routing control logic default-routs all ports to this host controller. The default value of this field is '0'.

NOTE

This register is not used in the normal implementation.

8.6.5.13. EHCI Port Status and Control Register(Default Value:0x0000_2000)

Offset: 0x0054			Register Name: PORTSC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21	R/W	0x0	Wake on Disconnect Enable(WKDSCNNT_E) Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. This field is zero if Port Power is zero. The default value in this field is '0'.
20	R/W	0x0	Wake on Connect Enable(WKCNNT_E) Writing this bit to a one enable the port to be sensitive to device connects as wake-up events. This field is zero if Port Power is zero. The default value in this field is '0'.
19:16	R/W	0x0	Port Test Control The value in this field specifies the test mode of the port. The encoding of the test mode bits are as follow: Bits: 0000b — The port is NOT operating in a test mode. Bits: 0001b — Test J_STATE

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<table>
<tr><td></td><td></td><td></td><td>
<table>
<tr><td>0010b</td><td>Test K_STATE</td></tr>
<tr><td>0011b</td><td>Test SE0_NAK</td></tr>
<tr><td>0100b</td><td>Test Packet</td></tr>
<tr><td>0101b</td><td>Test FORCE_ENABLE</td></tr>
<tr><td>0110b-
1111b</td><td>
Reserved</td></tr>
</table>
The default value in this field is ‘0000b’.
</td></tr>
<tr><td>15:14</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>13</td><td>R/W</td><td>0x1</td><td>Port Owner
This bit unconditionally goes to a 0b when the Configured bit in the CONFIGFLAG register makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configured bit is zero.
System software uses this field to release ownership of the port to selected host controller (in the event that the attached device is not a high-speed device).Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port.
Default Value = 1b.</td></tr>
<tr><td>12</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>11:10</td><td>R</td><td>0x0</td><td>Line Status
These bits reflect the current logical levels of the D+ (bit11) and D-(bit10) signal lines. These bits are used for detection of low-speed USB devices prior to port reset and enable sequence. This read only field is valid only when the port enable bit is zero and the current connect status bit is set to a one.
The encoding of the bits are:
<table>
<tr><td>Bit[11:10]</td><td>USB State</td><td>Interpretation</td></tr>
<tr><td>00b</td><td>SE0</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
<tr><td>10b</td><td>J-state</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
<tr><td>01b</td><td>K-state</td><td>Low-speed device, release ownership of port.</td></tr>
<tr><td>11b</td><td>Undefined</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
</table>
This value of this field is undefined if Port Power is zero.</td></tr>
<tr><td>9</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>8</td><td>R/W</td><td>0x0</td><td>Port Reset
1=Port is in Reset. 0=Port is not in Reset. Default value = 0.
When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to ensure the reset sequence, as specified in the USB Specification Revision 2.0, completes.
when software writes this bit to a one , it must also write a zero to the Port Enable bit.</td></tr>
</table>

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<table>
<tr><td></td><td></td><td></td><td>Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detects that the attached device is high-speed during reset, then the host controller must have the port in the enabled state with 2ms of software writing this bit to a zero.
The HC Halted bit in the USBSTS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HC Halted bit is a one.
This field is zero if Port Power is zero.</td></tr>
<tr><td>7</td><td>R/W</td><td>0x0</td><td>Suspend
Port Enabled Bit and Suspend bit of this register define the port states as follows:
<table><tr><td>Bits[Port Enables, Suspend]</td><td>Port State</td></tr><tr><td>0x</td><td>Disable</td></tr><tr><td>10</td><td>Enable</td></tr><tr><td>11</td><td>Suspend</td></tr></table>When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Not that the bit status does not change until the port is suspend and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB.
A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when:
① Software sets the Force Port Resume bit to a zero(from a one).
② Software sets the Port Reset bit to a one(from a zero).
If host software sets this bit to a one when the port is not enabled(i.e. Port enabled bit is a zero), the results are undefined.
This field is zero if Port Power is zero.
The default value in this field is ‘0’.</td></tr>
<tr><td>6</td><td>R/W</td><td>0x0</td><td>Force Port Resume
1 = Resume detected/driven on port. 0 = No resume (K-state) detected/ driven on port. Default value = 0.
This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspend and software transitions this bit to a one, then the effects on the bus are undefined.
Software sets this bit to a 1 drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a</td></tr>
</table>

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			one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero. This field is zero if Port Power is zero.
5	R/W1C	0x0	Over-current Change Default = 0. This bit gets set to a one when there is a change to Over-current Active. Software clears this bit by writing a one to this bit position.
4	R	0x0	Over-current Active 0 = This port does not have an over-current condition. 1 = This port currently has an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed. The default value of this bit is '0'.
3	R/W1C	0x0	Port Enable/Disable Change Default = 0. 1 = Port enabled/disabled status has changed. 0 = No change. For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a Port Error). Software clears this bit by writing a 1 to it. This field is zero if Port Power is zero.
2	R/W	0x0	Port Enabled/Disabled 1=Enable, 0=Disable. Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field. The host controller will only set this bit to a one when the reset sequence determines that the attached device is a high-speed device. Ports can be disabled by either a fault condition(disconnect event or other fault condition) or by host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. When the port is disabled, downstream propagation of data is blocked on this port except for reset. The default value of this field is '0'. This field is zero if Port Power is zero.
1	R/W1C	0x0	Connect Status Change 1=Change in Current Connect Status, 0=No change, Default=0. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has

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			cleared the changed condition, hub hardware will be “setting” an already-set bit. Software sets this bit to 0 by writing a 1 to it. This field is zero if Port Power is zero.
0	R	0x0	Current Connect Status Device is present on port when the value of this field is a one, and no device is present on port when the value of this field is a zero. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change(Bit 1) to be set. This field is zero if Port Power zero.



NOTE

This register is only reset by hardware or in response to a host controller reset.

8.6.6. OHCI Register Description

8.6.6.1. HcRevision Register(Default Value:0x10)

Offset: 0x0400				**Register Name: HcRevision**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:8	/	/	/	/
7:0	R	R	0x10	Revision This read-only field contains the BCD representation of the version of the HCI specification that is implemented by this HC. For example, a value of 0x11 corresponds to version 1.1. All of the HC implementations that are compliant with this specification will have a value of 0x10.

8.6.6.2. HcControl Register(Default Value:0x0000_0000)

Offset: 0x0404				**Register Name: HcRevision**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:11	/	/	/	/
10	R/W	R	0x0	RemoteWakeupEnable This bit is used by HCD to enable or disable the remote wakeup feature upon the detection of upstream resume signaling. When this bit is set and the ResumeDetected bit in *HcInterruptStatus* is set, a remote wakeup is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt.
9	R/W	R/W	0x0	RemoteWakeupConnected

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<table>
<tr><td></td><td></td><td></td><td></td><td>This bit indicates whether HC supports remote wakeup signaling. If remote wakeup is supported and used by the system, it is the responsibility of system firmware to set this bit during POST. HC clear the bit upon a hardware reset but does not alter it upon a software reset. Remote wakeup signaling of the host system is host-bus-specific and is not described in this specification.</td></tr>
<tr><td>8</td><td>R/W</td><td>R</td><td>0x0</td><td>InterruptRouting
This bit determines the routing of interrupts generated by events registered in HcInterruptStatus. If clear, all interrupt are routed to the normal host bus interrupt mechanism. If set interrupts are routed to the System Management Interrupt. HCD clears this bit upon a hardware reset, but it does not alter this bit upon a software reset. HCD uses this bit as a tag to indicate the ownership of HC.</td></tr>
<tr><td>7:6</td><td>R/W</td><td>R/W</td><td>0x0</td><td>HostControllerFunctionalState for USB
<table><tr><td>00b</td><td>USBReset</td></tr><tr><td>01b</td><td>USBResume</td></tr><tr><td>10b</td><td>USBOperational</td></tr><tr><td>11b</td><td>USBSuspend</td></tr></table>A transition to USBOperational from another state causes SOF generation to begin 1 ms later. HCD may determine whether HC has begun sending SOFs by reading the StartoFrame field of HcInterruptStatus.
This field may be changed by HC only when in the USBSUSPEND state. HC may move from the USBSUSPEND state to the USBRESUME state after detecting the resume signaling from a downstream port.
HC enters USBSUSPEND after a software reset, whereas it enters USBRESET after a hardware reset. The latter also resets the Root Hub and asserts subsequent reset signaling to downstream ports.</td></tr>
<tr><td>5</td><td>R/W</td><td>R</td><td>0x0</td><td>BulkListEnable
This bit is set to enable the processing of the Bulk list in the next Frame. If cleared by HCD, processing of the Bulk list does not occur after the next SOF. HC checks this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcBulkCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcBulkCurrentED before re-enabling processing of the list.</td></tr>
<tr><td>4</td><td>R/W</td><td>R</td><td>0x0</td><td>ControlListEnable
This bit is set to enable the processing of the Control list in the next Frame. If cleared by HCD, processing of the Control list does not occur after the next SOF. HC must check this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcControlCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcControlCurrentED before re-enabling processing of the list.</td></tr>
<tr><td>3</td><td>R/W</td><td>R</td><td>0x0</td><td>IsochronousEnable
This bit is used by HCD to enable/disable processing of isochronous EDs. While processing the periodic list in a Frame, HC checks the status of this bit when it finds an Isochronous ED (F=1). If set (enabled), HC continues</td></tr>
</table>

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				processing the EDs. If cleared (disabled), HC halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists. Setting this bit is guaranteed to take effect in the next Frame (not the current Frame).
2	R/W	R	0x0	PeriodicListEnable This bit is set to enable the processing of periodic list in the next Frame. If cleared by HCD, processing of the periodic list does not occur after the next SOF. HC must check this bit before it starts processing the list.
1:0	R/W	R	0x0	ControlBulkServiceRatio This specifies the service ratio between Control and Bulk EDs. Before processing any of the nonperiodic lists, HC must compare the ratio specified with its internal count on how many nonempty Control EDs have been processed, in determining whether to continue serving another Control ED or switching to Bulk EDs. The internal count will be retained when crossing the frame boundary. In case of reset, HCD is responsible for restoring this value. CBSR: 0 → 1:1; 1 → 2:1; 2 → 3:1; 3 → 4:1 The default value is 0x0.

8.6.6.3. HcCommandStatus Register(Default Value:0x0000_0000)

Offset: 0x0408				Register Name: HcCommandStatus
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:18	/	/	0x0	Reserved
17:16	R	R/W	0x0	SchedulingOverrunCount These bits are incremented on each scheduling overrun error. It is initialized to 00b and wraps around at 11b. This will be incremented when a scheduling overrun is detected even if SchedulingOverrun in *HcInterruptStatus* has already been set. This is used by HCD to monitor any persistent scheduling problem.
15:4	/	/	/	/
3	R/W	R/W	0x0	OwershipChangeRequest This bit is set by an OS HCD to request a change of control of the HC. When set HC will set the OwnershipChange field in *HcInterruptStatus*. After the changeover, this bit is cleared and remains so until the next request from OS HCD.
2	R/W	R/W	0x0	BulkIListFilled This bit is used to indicate whether there are any TDs on the Bulk list. It is

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				set by HCD whenever it adds a TD to an ED in the Bulk list. When HC begins to process the head of the Bulk list, it checks BLF. As long as BulkListFilled is 0, HC will not start processing the Bulk list. If BulkListFilled is 1, HC will start processing the Bulk list and will set BF to 0. If HC finds a TD on the list, then HC will set BulkListFilled to 1 causing the Bulk list processing to continue. If no TD is found on the Bulk list, and if HCD does not set BulkListFilled, then BulkListFilled will still be 0 when HC completes processing the Bulk list and Bulk list processing will stop.
1	R/W	R/W	0x0	ControlListFilled This bit is used to indicate whether there are any TDs on the Control list. It is set by HCD whenever it adds a TD to an ED in the Control list. When HC begins to process the head of the Control list, it checks CLF. As long as ControlListFilled is 0, HC will not start processing the Control list. If CF is 1, HC will start processing the Control list and will set ControlListFilled to 0. If HC finds a TD on the list, then HC will set ControlListFilled to 1 causing the Control list processing to continue. If no TD is found on the Control list, and if the HCD does not set ControlListFilled, then ControlListFilled will still be 0 when HC completes processing the Control list and Control list processing will stop.
0	R/W	R/E	0x0	HostControllerReset This bit is by HCD to initiate a software reset of HC. Regardless of the functional state of HC, it moves to the USBSuspend state in which most of the operational registers are reset except those stated otherwise; e.g, the InteruptRouting field of HcControl, and no Host bus accesses are allowed. This bit is cleared by HC upon the completion of the reset operation. The reset operation must be completed within 10 ms. This bit, when set, should not cause a reset to the Root Hub and no subsequent reset signaling should be asserted to its downstream ports.

8.6.6.4. HcInterruptStatus Register(Default Value:0x0000_0000)

Offset: 0x040c				**Register Name: HcInterruptStatus**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:7	/	/	/	/
6	R/W	R/W	0x0	RootHubStatusChange This bit is set when the content of *HcRhStatus* or the content of any of *HcRhPortStatus*[NumberofDownstreamPort] has changed.
5	R/W	R/W	0x0	FrameNumberOverflow This bit is set when the MSb of *HcFmNumber* (bit 15) changes value, from 0 to 1 or from 1 to 0, and after *HccaFrameNumber* has been updated.
4	R/W	R/W	0x0	UnrecoverableError This bit is set when HC detects a system error not related to USB. HC should not proceed with any processing nor signaling before the system error has been corrected. HCD clears this bit after HC has been reset.

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3	R/W	R/W	0x0	ResumeDetected This bit is set when HC detects that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling causing this bit to be set. This bit is not set when HCD sets the USBRseume state.
2	R/W	R/W	0x0	StartofFrame This bit is set by HC at each start of frame and after the update of HccaFrameNumber. HC also generates a SOF token at the same time.
1	R/W	R/W	0x0	WritebackDoneHead This bit is set immediately after HC has written *HcDoneHead* to *HccaDoneHead*. Further updates of the *HccaDoneHead* will not occur until this bit has been cleared. HCD should only clear this bit after it has saved the content of *HccaDoneHead*.
0	R/W	R/W	0x0	SchedulingOverrun This bit is set when the USB schedule for the current Frame overruns and after the update of *HccaFrameNumber*. A scheduling overrun will also cause the SchedulingOverrunCount of *HcCommandStatus* to be Incremented.

8.6.6.5. HcInterruptEnable Register(Default Value:0x0000_0000)

Offset: 0x0410				**Register Name: HcInterruptEnable**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31	R/W	R	0x0	MasterInterruptEnable A '0' writtern to this field is ignored by HC. A '1' written to this field enables interrupt generation due to events specified in the other bits of this register. This is used by HCD as Master Interrupt Enable.
30:7	/	/	/	/
6	R/W	R	0x0	RootHubStatusChange Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Root Hub Status Change;
5	R/W	R	0x0	FrameNumberOverflow Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Frame Number Over Flow;
4	R/W	R	0x0	UnrecoverableError Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Unrecoverable Error;
3	R/W	R	0x0	ResumeDetected Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Resume Detected;
2	R/W	R	0x0	StartofFrame Interrupt Enable 0 Ignore;

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				1 Enable interrupt generation due to Start of Flame;
1	R/W	R	0x0	WritebackDoneHead Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Write back Done Head;
0	R/W	R	0x0	SchedulingOverrun Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Scheduling Overrun;

8.6.6.6. HcInterruptDisable Register(Default Value:0x0000_0000)

Offset: 0x0414				Register Name: HcInterruptDisable
Bit	Read/Write		Default	Description
	HCD	HC		
31	R/W	R	0x0	MasterInterruptEnable A written '0' to this field is ignored by HC. A '1' written to this field disables interrupt generation due events specified in the other bits of this register. This field is set after a hardware or software reset.
30:7	/	/	/	/
6	R/W	R	0x0	RootHubStatusChange Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Root Hub Status Change;
5	R/W	R	0x0	FrameNumberOverflow Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Frame Number Over Flow;
4	R/W	R	0x0	UnrecoverableError Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Unrecoverable Error;
3	R/W	R	0x0	ResumeDetected Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Resume Detected;
2	R/W	R	0x0	StartofFrame Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Start of Flame;
1	R/W	R	0x0	WritebackDoneHead Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Write back Done Head;
0	R/w	R	0x0	SchedulingOverrun Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Scheduling Overrun;

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8.6.6.7. HcHCCA Register(Default Value:0x0000_0000)

Offset: 0x0418				Register Name: HcHCCA
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:8	R/W	R	0x0	HCCA[31:8] This is the base address of the Host Controller Communication Area. This area is used to hold the control structures and the Interrupt table that are accessed by both the Host Controller and the Host Controller Driver.
7:0	R	R	0x0	HCCA[7:0] The alignment restriction in HcHCCA register is evaluated by examining the number of zeros in the lower order bits. The minimum alignment is 256 bytes, therefore, bits 0 through 7 must always return 0 when read.

8.6.6.8. HcPeriodCurrentED Register(Default Value:0x0000_0000)

Offset: 0x041C				Register Name: HcPeriodCurrentED(PCED)
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R	R/W	0x0	PCED[31:4] This is used by HC to point to the head of one of the Periodec list which will be processed in the current Frame. The content of this register is updated by HC after a periodic ED has been processed. HCD may read the content in determining which ED is currently being processed at the time of reading.
3:0	R	R	0x0	PCED[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.6.6.9. HcControlHeadED Register(Default Value:0x0000_0000)

Offset: 0x0420				Register Name: HcControlHeadED[CHED]
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R	0x0	EHCD[31:4] The HcControlHeadED register contains the physical address of the first Endpoint Descriptor of the Control list. HC traverse the Control list starting with the HcControlHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0	R	R	0x0	EHCD[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED,

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				through bit 0 to bit 3 must be zero in this field.

8.6.6.10. HcControlCurrentED Register

Offset: 0x424				Register Name: HcControlCurrentED[CCED]
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R/W	0x0	CCED[31:4] The pointer is advanced to the next ED after serving the present one. HC will continue processing the list from where it left off in the last Frame. When it reaches the end of the Control list, HC checks the ControlListFilled of in HcCommandStatus. If set, it copies the content of HcControlHeadED to HcControlCurrentED and clears the bit. If not set, it does nothing. HCD is allowed to modify this register only when the ControlListEnable of HcControl is cleared. When set, HCD only reads the instantaneous value of this register. Initially, this is set to zero to indicate the end of the Control list.
3:0	R	R	0x0	CCED[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.6.6.11. HcBulkHeadED Register(Default Value:0x0000_0000)

Offset: 0x428				Register Name: HcBulkHeadED[BHED]
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R	0x0	BHED[31:4] The HcBulkHeadED register contains the physical address of the first Endpoint Descriptor of the Bulk list. HC traverses the Bulk list starting with the HcBulkHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0	R	R	0x0	BHED[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.6.6.12. HcBulkCurrentED Register(Default Value:0x0000_0000)

Offset: 0x42C			Register Name: HcBulkCurrentED [BCED]
Bit	Read/Write	Default/Hex	Description

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	HCD	HC		
31:4	R/W	R/W	0x0	BulkCurrentED[31:4] This is advanced to the next ED after the HC has served the present one. HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, HC checks the ControlListFilled of HcControl. If set, it copies the content of *HcBulkHeadED* to *HcBulkCurrentED* and clears the bit. If it is not set, it does nothing. HCD is only allowed to modify this register when the BulkListEnable of *HcControl* is cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to zero to indicate the end of the Bulk list.
3:0	R	R	0x0	BulkCurrentED [3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.6.6.13. HcDoneHead Register(Default Value:0x0000_0000)

Offset: 0x430				Register Name: HcDoneHead
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R	R/W	0x0	HcDoneHead[31:4] When a TD is completed, HC writes the content of *HcDoneHead* to the NextTD field of the TD. HC then overwrites the content of *HcDoneHead* with the address of this TD. This is set to zero whenever HC writes the content of this register to HCCA. It also sets the WritebackDoneHead of *HcInterruptStatus*.
3:0	R	R	0x0	HcDoneHead[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.6.6.14. HcFmInterval Register(Default Value:0x0000_2EDF)

Offset: 0x0434				Register Name: HcFmInterval Register
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	R/W	R	0x0	FrameIntervalToggler HCD toggles this bit whenever it loads a new value to FrameInterval.
30:16	R/W	R	0x0	FSLargestDataPacket This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun.

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				The field value is calculated by the HCD.
15:14	/	/	/	/
13:0	R/W	R	0x2edf	FrameInterval This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to be 11,999. HCD should store the current value of this field before resetting HC. By setting the HostControllerReset field of *HcCommandStatus* as this will cause the HC to reset this field to its nominal value. HCD may choose to restore the stored value upon the completion of the Reset sequence.

8.6.6.15. HcFmRemaining Register(Default Value:0x0000_0000)

Offset: 0x0438				**Register Name: HcFmRemaining**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31	R	R/W	0x0	FrameRemaining Toggle This bit is loaded from the FrameIntervalToggle field of *HcFmInterval* whenever FrameRemaining reaches 0. This bit is used by HCD for the synchronization between FrameInterval and FrameRemaining.
30:14	/	/	/	/
13:0	R	RW	0x0	FramRemaining This counter is decremented at each bit time. When it reaches zero, it is reset by loading the FrameInterval value specified in *HcFmInterval* at the next bit time boundary. When entering the USBOPERATIONAL state, HC re-loads the content with the FrameInterval of *HcFmInterval* and uses the updated value from the next SOF.

8.6.6.16. HcFmNumber Register(Default Value:0x0000_0000)

Offset: 0x043c				**Register Name: HcFmNumber**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:16	/	/	/	/
15:0	R	R/W	0x0	FrameNumber This is incremented when *HcFmRemaining* is re-loaded. It will be rolled over to 0x0 after 0x0ffff. When entering the USBOPERATIONAL state, this will be incremented automatically. The content will be written to HCCA after HC has incremented the FrameNumber at each frame boundary and sent a SOF but before HC reads the first ED in that Frame. After writing to HCCA, HC will set the StartofFrame in *HcInterruptStatus.*

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8.6.6.17. HcPeriodicStart Register(Default Value:0x0000_0000)

Offset: 0x0440				Register Name: HcPeriodicStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:14	/	/	/	/
13:0	R/W	R	0x0	PeriodicStart After a hardware reset, this field is cleared. This is then set by HCD during the HC initialization. The value is calculated roughly as 10% off from *HcFmInterval*. A typical value will be 0x2A3F (0x3e67??). When *HcFmRemaining* reaches the value specified, processing of the periodic lists will have priority over Control/Bulk processing. HC will therefore start processing the Interrupt list after completing the current Control or Bulk transaction that is in progress.

8.6.6.18. HcLSThreshold Register(Default Value:0x0000_0628)

Offset: 0x444				Register Name: HcLSThreshold
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:12	/	/	/	Reserved
11:0	R/W	R	0x0628	LSThreshold This field contains a value which is compared to the FrameRemaining field prior to initiating a Low Speed transaction. The transaction is started only if FrameRemaining ³ this field. The value is calculated by HCD with the consideration of transmission and setup overhead.

8.6.6.19. HcRhDescriptorA Register(Default Value:0x0200_1201)

Offset: 0x448				Register Name: HcRhDescriptorA
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:24	R/W	R	0x2	PowerOnToPowerGoodTime[POTPGT] This byte specifies the duration HCD has to wait before accessing a powered-on port of the Root Hub. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as POTPGT * 2ms.
23:13	/	/	/	/
12	R/W	R	0x1	NoOverCurrentProtection This bit describes how the overcurrent status for the Root Hub ports are reported. When this bit is cleared, the OverCurrentProtectionMode field specifies global or per-port reporting. 0 Over-current status is reported collectively for all downstream ports.

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				1 No overcurrent protection supported.
11	R/W	R	0x0	OverCurrentProtectionMode This bit describes how the overcurrent status for the Root Hub ports are reported. At reset, these fields should reflect the same mode as PowerSwitchingMode. This field is valid only if the NoOverCurrentProtection field is cleared. 0 Over-current status is reported collectively for all downstream ports. 1 Over-current status is reported on per-port basis.
10	R	R	0x0	Device Type This bit specifies that the Root Hub is not a compound device. The Root Hub is not permitted to be a compound device. This field should always read/write 0.
9	R/W	R	0x1	PowerSwitchingMode This bit is used to specify how the power switching of the Root Hub ports is controlled. It is implementation-specific. This field is only valid if the NoPowerSwitching field is cleared. 0 All ports are powered at the same time. 1 Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switching. If the PortPowerControlMask bit is set, the port responds only to port power commands (Set/ClearPortPower). If the port mask is cleared, then the port is controlled only by the global power switch (Set/ClearGlobalPower).
8	R/W	R	0x0	NoPowerSwithcing These bits are used to specify whether power switching is supported or ports are always powered. It is implementation-specific. When this bit is cleared, the PowerSwitchingMode specifies global or per-port switching. 0 Ports are power switched. 1 Ports are always powered on when the HC is powered on.
7:0	R	R	0x01	NumberDownstreamPorts These bits specify the number of downstream ports supported by the Root Hub. It is implementation-specific. The minimum number of ports is 1. The maximum number of ports supported.

8.6.6.20. HcRhDescriptorB Register (Default Value:0x0000_0000)

Offset: 0x44c				Register Name: HcRhDescriptorB
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:16	R/W	R	0x0	PortPowerControlMask Each bit indicates if a port is affected by a global power control command

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<table>
<tr><td></td><td></td><td></td><td></td><td>when PowerSwitchingMode is set. When set, the port's power state is only affected by per-port power control (Set/ClearPortPower). When cleared, the port is controlled by the global power switch (Set/ClearGlobalPower). If the device is configured to global switching mode (PowerSwitchingMode = 0), this field is not valid.
<table><tr><td>Bit0</td><td>Reserved</td></tr><tr><td>Bit1</td><td>Ganged-power mask on Port #1.</td></tr><tr><td>Bit2</td><td>Ganged-power mask on Port #2.</td></tr><tr><td>…</td><td></td></tr><tr><td>Bit15</td><td>Ganged-power mask on Port #15.</td></tr></table></td></tr>
<tr><td>15:0</td><td>R/W</td><td>R</td><td>0x0</td><td>DeviceRemovable
Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable.
<table><tr><td>Bit0</td><td>Reserved</td></tr><tr><td>Bit1</td><td>Device attached to Port #1.</td></tr><tr><td>Bit2</td><td>Device attached to Port #2.</td></tr><tr><td>…</td><td></td></tr><tr><td>Bit15</td><td>Device attached to Port #15.</td></tr></table></td></tr>
</table>

8.6.6.21. HcRhStatus Register(Default Value:0x0000_0000)

Offset: 0x450				Register Name: HcRhStatus Register
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	W	R	0x0	(write)ClearRemoteWakeupEnable Write a ‘1’ clears DeviceRemoteWakeupEnable. Write a ‘0’ has no effect.
30:18	/	/	/	/
17	R/W	R	0x0	OverCurrentIndicatorChang This bit is set by hardware when a change has occurred to the OverCurrentIndicator field of this register. The HCD clears this bit by writing a ‘1’.Writing a ‘0’ has no effect.
16	R/W	R	0x0	(read)LocalPowerStartusChange The Root Hub does not support the local power status features, thus, this bit is always read as ‘0’. (write)SetGlobalPower In global power mode (PowerSwitchingMode=0), This bit is written to ‘1’ to turn on power to all ports (clear PortPowerStatus). In per-port power mode, it sets PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a ‘0’ has no effect.
15	R/W	R	0x0	(read)DeviceRemoteWakeupEnable This bit enables a ConnectStatusChange bit as a resume event, causing a USBSUSPEND to USBRESUME state transition and setting the ResumeDetected interrupt.

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				0 ConnectStatusChange is not a remote wakeup event. 1 ConnectStatusChange is a remote wakeup event. (write)SetRemoteWakeupEnable Writing a '1' sets DeviceRemoveWakeupEnable. Writing a '0' has no effect.
14:2	/	/	/	/
1	R	R/W	0x0	OverCurrentIndicator This bit reports overcurrent conditions when the global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal. If per-port overcurrent protection is implemented this bit is always '0'
0	R/W	R	0x0	(Read)LocalPowerStatus When read, this bit returns the LocalPowerStatus of the Root Hub. The Root Hub does not support the local power status feature; thus, this bit is always read as '0'. (Write)ClearGlobalPower When write, this bit is operated as the ClearGlobalPower. In global power mode (PowerSwitchingMode=0), This bit is written to '1' to turn off power to all ports (clear PortPowerStatus). In per-port power mode, it clears PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a '0' has no effect.

8.6.6.22. HcRhPortStatus Register(Default Value:0x0000_0100)

Offset: 0x454				Register Name: HcRhPortStatus
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:21	/	/	0x0	Reserved
20	R/W	R/W	0x0	PortResetStatusChange This bit is set at the end of the 10-ms port reset signal. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 port reset is not complete 1 port reset is complete
19	R/W	R/W	0x0	PortOverCurrentIndicatorChange This bit is valid only if overcurrent conditions are reported on a per-port basis. This bit is set when Root Hub changes the PortOverCurrentIndicator bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 no change in PortOverCurrentIndicator 1 PortOverCurrentIndicator has changed
18	R/W	R/W	0x0	PortSuspendStatusChange This bit is set when the full resume sequence has been completed. This sequence includes the 20-s resume pulse, LS EOP, and 3-ms resychronization delay. The HCD writes a '1' to clear this bit. Writing a '0'

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<table>
<tr><td></td><td></td><td></td><td></td><td>has no effect. This bit is also cleared when ResetStatusChange is set.<table><tr><td>0</td><td>resume is not completed</td></tr><tr><td>1</td><td>resume completed</td></tr></table></td></tr>
<tr><td>17</td><td>R/W</td><td>R/W</td><td>0x0</td><td>PortEnableStatusChange
This bit is set when hardware events cause the PortEnableStatus bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a ‘1’ to clear this bit. Writing a ‘0’ has no effect.<table><tr><td>0</td><td>no change in PortEnableStatus</td></tr><tr><td>1</td><td>change in PortEnableStatus</td></tr></table></td></tr>
<tr><td>16</td><td>R/W</td><td>R/W</td><td>0x0</td><td>ConnectStatusChange
This bit is set whenever a connect or disconnect event occurs. The HCD writes a ‘1’ to clear this bit. Writing a ‘0’ has no effect. If CurrentConnectStatus is cleared when a SetPortReset,SetPortEnable, or SetPortSuspend write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected.<table><tr><td>0</td><td>no change in PortEnableStatus</td></tr><tr><td>1</td><td>change in PortEnableStatus</td></tr></table>
  NOTE
If the DeviceRemovable[NDP] bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.</td></tr>
<tr><td>15:10</td><td>/</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>9</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)LowSpeedDeviceAttached
This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid only when the CurrentConnectStatus is set.<table><tr><td>0</td><td>full speed device attached</td></tr><tr><td>1</td><td>low speed device attached</td></tr></table>
(write)ClearPortPower
The HCD clears the PortPowerStatus bit by writing a ‘1’ to this bit. Writing a ‘0’ has no effect.</td></tr>
<tr><td>8</td><td>R/W</td><td>R/W</td><td>0x1</td><td>(read)PortPowerStatus
This bit reflects the port’s power status, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. HCD sets this bit by writing SetPortPower or SetGlobalPower. HCD clears this bit by writing ClearPortPower or ClearGlobalPower. Which power control switches are enabled is determined by PowerSwitchingMode and PortPortControlMask[NumberDownstreamPort]. In global switching mode(PowerSwitchingMode=0), only Set/ClearGlobalPower controls this bit. In per-port power switching (PowerSwitchingMode=1), if the</td></tr>
</table>

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<table>
<tr><td></td><td></td><td></td><td></td><td>PortPowerControlMask[NDP] bit for the port is set, only Set/ClearPortPower commands are enabled. If the mask is not set, only Set/ClearGlobalPower commands are enabled. When port power is disabled, CurrentConnectStatus, PortEnableStatus, PortSuspendStatus, and PortResetStatus should be reset.
<table><tr><td>0</td><td>port power is off</td></tr><tr><td>1</td><td>port power is on</td></tr></table>
(write)SetPortPower
The HCD writes a ‘1’ to set the PortPowerStatus bit. Writing a ‘0’ has no effect.
  NOTE
This bit is always reads ‘1b’ if power switching is not supported.</td></tr>
<tr><td>7:5</td><td>/</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>4</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortResetStatus
When this bit is set by a write to SetPortReset, port reset signaling is asserted. When reset is completed, this bit is cleared when PortResetStatusChange is set. This bit cannot be set if CurrentConnectStatus is cleared.
<table><tr><td>0</td><td>port reset signal is not active</td></tr><tr><td>1</td><td>port reset signal is active</td></tr></table>
(write)SetPortReset
The HCD sets the port reset signaling by writing a ‘1’ to this bit. Writing a ‘0’ has no effect. If CurrentConnectStatus is cleared, this write does not set PortResetStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to reset a disconnected port.</td></tr>
<tr><td>3</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortOverCurrentIndicator
This bit is only valid when the Root Hub is configured in such a way that overcurrent conditions are reported on a per-port basis. If per-port overcurrent reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. This bit always reflects the overcurrent input signal.
<table><tr><td>0</td><td>no overcurrent condition.</td></tr><tr><td>1</td><td>overcurrent condition detected.</td></tr></table>
(write)ClearSuspendStatus
The HCD writes a ‘1’ to initiate a resume. Writing a ‘0’ has no effect. A resume is initiated only if PortSuspendStatus is set.</td></tr>
<tr><td>2</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortSuspendStatus
This bit indicates the port is suspended or in the resume sequence. It is set by a SetSuspendState write and cleared when PortSuspendStatusChange is set at the end of the resume interval. This bit cannot be set if CurrentConnectStatus is cleared. This bit is also cleared when PortResetStatusChange is set at the end of the port reset or when</td></tr>
</table>

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<table>
<tr><td></td><td></td><td></td><td></td><td>the HC is placed in the USBRESUME state. If an upstream resume is in progress, it should propagate to the HC.
<table><tr><td>0</td><td>port is not suspended</td></tr><tr><td>1</td><td>port is suspended</td></tr></table>
(write)SetPortSuspend
The HCD sets the PortSuspendStatus bit by writing a ‘1’ to this bit. Writing a ‘0’ has no effect. If CurrentConnectStatus is cleared, this write does not set PortSuspendStatus; instead it sets ConnectStatusChange. This informs the driver that it attempted to suspend a disconnected port.</td></tr>
<tr><td>1</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortEnableStatus
This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes PortEnabledStatusChange to be set. HCD sets this bit by writing SetPortEnable and clears it by writing ClearPortEnable. This bit cannot be set when CurrentConnectStatus is cleared. This bit is also set, if not already, at the completion of a port reset when ResetStatusChange is set or port suspend when SuspendStatusChange is set.
<table><tr><td>0</td><td>port is disabled</td></tr><tr><td>1</td><td>port is enabled</td></tr></table>
(write)SetPortEnable
The HCD sets PortEnableStatus by writing a ‘1’. Writing a ‘0’ has no effect. If CurrentConnectStatus is cleared, this write does not set PortEnableStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to enable a disconnected Port.</td></tr>
<tr><td>0</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)CurrentConnectStatus
This bit reflects the current state of the downstream port.
<table><tr><td>0</td><td>No device connected</td></tr><tr><td>1</td><td>Device connected</td></tr></table>(write)ClearPortEnable
The HCD writes a ‘1’ to clear the PortEnableStatus bit. Writing ‘0’ has no effect. The CurrentConnectStatus is not affected by any write.

  NOTE
This bit is always readed as ‘1’ when the attached device is nonremovalble(DviceRemoveable[NumberDownstreamPort]).</td></tr>
</table>

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8.6.7. HCI Controller and PHY Interface Description

8.6.7.1. HCI Interface Register(Default Value:0x1000_0000)

Offset: 0x800			Register Name: USB_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	Reserved.
28	R	0x1	DMA Transfer Status Enable 0: Disable 1: Enable
27:26	/	/	/
25	R/W	0x0	OHCI Count Select 1: Simulation mode, the counters will be much shorter then real time 0: Normal mode, the counters will count full time
24	R/W	0x0	Simulation Mode 1: Set PHY in a non-driving mode so the EHCI can detect device connection, this is used only for simulation 0: No effect
23:21	/	/	/
20	R/W	0x0	EHCI HS Force Set 1 to this field force the ehci enter the high speed mode during bus reset. This field only valid when the bit 1 is set.
19:13	/	/	/
12	R/W	0x0	PP2VBUS 1: ULPI wrapper interface will automatically set or clear DrvVbus register in ULPI PHY according to the port power status form the root hub 0: ULPI wrapper will ignore the difference between power status of root hub and ULPI PHY
11	R/W	0x0	AHB Master Interface INCR16 Enable 1: Use INCR16 when appropriate 0: do not use INCR16,use other enabled INCRX or unspecified length burst INCR
10	R/W	0x0	AHB Master Interface INCR8 Enable 1: Use INCR8 when appropriate 0: Do not use INCR8,use other enabled INCRX or unspecified length burst INCR
9	R/W	0x0	AHB Master Interface Burst Type INCR4 Enable 1: Use INCR4 when appropriate 0: Do not use INCR4,use other enabled INCRX or unspecified length burst INCR
8	R/W	0x0	AHB Master Interface INCRX Align Enable 1: start INCRx burst only on burst x-align address 0: Start burst on any double word boundary

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			NOTE **This bit must enable if any bit of 11:9 is enabled.**
7:1	/	/	/
0	R/W	0x0	ULPI Bypass Enable 1: Enable UTMI interface, disable ULPI interface 0: Enable ULPI interface, disable UTMI interface

8.6.7.2. PHY Control Register(Default Value: 0x0000_0002)

Offset: 0x810			Register Name: PHY Control
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	BIST_EN_A
15:9	/	/	/
8	R/W	0x0	500K PULLUP ENABLE
7:2	/	/	/
1	R/W	0x1	SIDDQ write 1 to enable phy
0	R/W	0x0	VC_CLK

8.6.7.3. HSIC PHY Tune1 Register(Default Value: 0x0000_0010)

Offset: 0x81C			Register Name: HSIC_PHY_Tune1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:5	/	/	TXRPUTUNE
5:4	R/W	0x1	TXRPDTUNE
3:0	R/W	0x0	TXSRTUNE

8.6.7.4. HSIC PHY Tune2 Register(Default Value: 0x0000_0010)

Offset: 0x820			Register Name: HSIC_PHY_Tune2
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	BIST_EN
30	R/W	0x0	TESTBURNIN
29	R/W	0x0	TESTDATAOUTSEL
28	R/W	0x0	TESTCLK
27:24	R/W	0x0	TESTADDR
23:16	R/W	0x0	TESTDATAIN
15:4	R/W	0x1	SIDDQ
3:0	R/W	0x0	REFCLK DIV

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8.6.7.5. HSIC PHY Tune3 Register(Default Value: 0x0000_0010)

Offset: 0x824			Register Name: HSIC PHY tune3 Register
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
5			HSIC BIST_ERROR
4			HSIC BIST_DONE
3:2	/	/	HSIC TESTDATA OUT[3:2]
1	R/W	0x1	Non_HSIC_MODE_BIST_ERROR testdata out[1]
0	R/W	0x0	Non_HSIC_MODE_BIST_DONE testdata out[0]

8.6.7.6. HCI SIE Port Disable Control Register(Default Value:0x1000_0000)

Offset: 0x828			Register Name: USB_SPDCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	SE0 Status This bit is set when no-se0 is detected before SOF when bit[1:0] is 10b or 11b
15:2	/	/	/
1:0	R/W	0x0	Port Disable Control 00: Port Disable when no-se0 detect before SOF 01: Port Disable when no-se0 detect before SOF 10: No Port Disable when no-se0 detect before SOF 11: Port Disable when no-se0 3 time detect before SOF during 8 frames

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8.7. SCR

8.7.1. Overview

The Smart Card Reader (SCR) is a communication controller that transmits data between the system and Smart Card. The controller can perform a complete smart card session, including card activation, card deactivation. Cold/warm reset, Answer to Reset (ATR) response reception, data transfers, etc.

Features:

- Supports APB slave interface for easy integration with AMBA-based host systems
- Supports the ISO/IEC 7816-3:1997(E) and EMV2000 (4.0) Specifications
- Performs functions needed for complete smart card sessions, including:
  - Card activation and deactivation
  - Cold/warm reset
  - Answer to Reset (ATR) response reception
  - Data transfers to and from the card
- Supports adjustable clock rate and bit rate
- Configurable automatic byte repetition
- Supports commonly used communication protocols:
  - T=0 for asynchronous half-duplex character transmission
  - T=1 for asynchronous half-duplex block transmission
- Supports FIFOs for receive and transmit buffers (up to 128 characters) with threshold
- Supports configurable timing functions:
  - Smart card activation time
  - Smart card reset time
  - Guard time
  - Timeout timers
- Supports synchronous and any other non-ISO 7816 and non-EMV cards
- Supports the ISO/IEC 7816-3:1997(E) and EMV2000 (4.0) Specifications

8.7.2. Block Diagram

The top diagram of Smart Card Reader is below.

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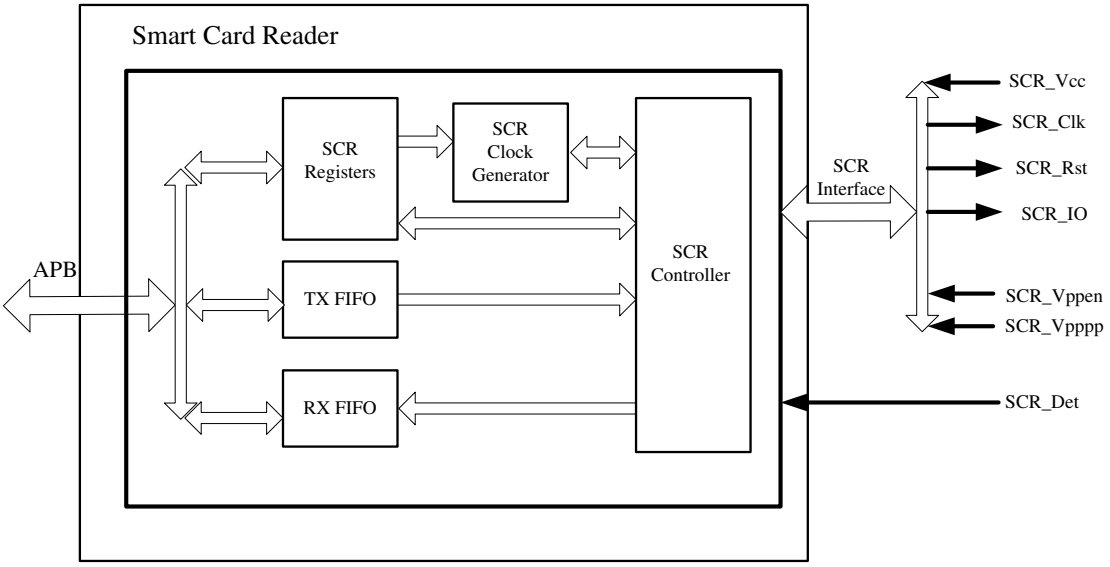


Figure 8-26. SCR Block Diagram

8.7.3. Operations and Functional Descriptions

8.7.3.1. External Signals

The following table describes the external signals of SCR.

Table 8-16. SCR External Signals

Signal(x=[1:0])	Description	Type
SIMx_PWREN	Smart Card Power Enable	O
SIMx_CLK	Smart Card Clock	O
SIMx_DATA	Smart Card Data	I/O
SIMx_RST	Smart Card Reset	O
SIMx_DET	Smart Card Detect	I
SIMx_VPPEN	Smart Card Program Voltage Enable	O
SIMx_VPPPP	Smart Card Vpp Pause and Program Control	O

8.7.3.2. Timing Diagram

Please refer ISO/IEC 7816 and EMV2000 Specification.

8.7.3.3. Clock Generator

The Clock Generator generates the Smart Card Clock signal and the Baud Clock Impulse signal, used in timing the Smart Card Reader.

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The Smart Card Clock signal is used as the main clock for the smart card. Its frequency can be adjusted using the Smart Card Clock Divisor (SCCDIV). This value is used to divide the system clock. The SCCLK frequency is given by the following equation:

$$f_{scclk} = \frac{f_{sysclk}}{2*(SCCDIV+1)}$$

f_{scclk} -- Smart Card Clock Frequency

f_{sysclk} -- System Clock (PCLK) Frequency

The Baud Clock Impulse signal is used to transmit and receive serial between the SCR and the Smart Card. The baud rate can be modified using the Baud Clock Divisor (BAUDDIV). The value is used to divide the system clock. The BUAD rate is given by the following equation:

$$BAUD = \frac{f_{sysclk}}{2*(BAUDDIV+1)}$$

$BAUD$ -- Baud rate of the data stream between Smart Card and Reader.

The duration of one bit, Elementary Time Unit (ETU), is defined in the ISO/IEC 7816-3 specification. During the first answer to reset response after the cold reset, the initial ETU must be equal to 372 Smart Card Clock Cycles.

$$\frac{1}{BAUD} = ETU = \frac{372}{f_{scclk}}$$

In this case, the BAUDDIV should be

$$BAUDDIV = \frac{372*f_{sysclk}}{2*f_{scclk}} - 1 = 372*(SCCDIV+1) - 1 .$$

After the ATR is completed, the ETU can be changed according to Smart Card abilities.

$$\frac{1}{BAUD} = ETU = \frac{F}{D} * \frac{1}{f_{scclk}}$$

Parameters F and D are defined in the ISO/IEC 7816-3 Specification.

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8.7.3.4. SCIO Pad Configuration

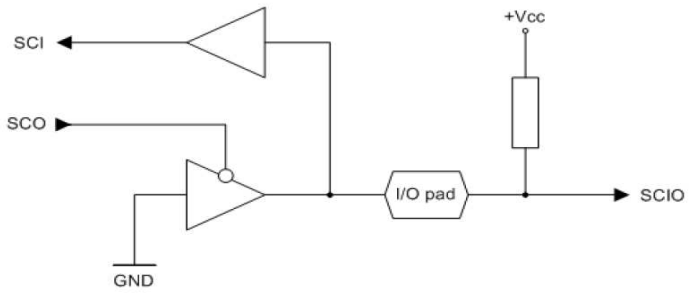


Figure 8-27. SCIO Pad Configuration Diagram

8.7.4. Register List

Module Name	Base Address
SCR0	0x05005000
SCR1	0x05005400

Register Name	Offset	Description
SCR_CSR	0x0000	Smart Card Reader Control and Status Register
SCR_INTEN	0x0004	Smart Card Reader Interrupt Enable Register 1
SCR_INTST	0x0008	Smart Card Reader Interrupt Status Register 1
SCR_FCSR	0x000C	Smart Card Reader FIFO Control and Status Register
SCR_FCNT	0x0010	Smart Card Reader RX and TX FIFO Counter Register
SCR_RPT	0x0014	Smart Card Reader RX and TX Repeat Register
SCR_DIV	0x0018	Smart Card Reader Clock and Baud Divisor Register
SCR_LTIM	0x001C	Smart Card Reader Line Time Register
SCR_CTIM	0x0020	Smart Card Reader Character Time Register
SCR_LCTLR	0x0030	Smart Card Reader Line Control Register
SCR_FSM	0x003C	Smart Card Reader FSM Register
SCR_DT	0x0040	Smart Card Reader Debounce Time Register
SCR_FIFO	0x0100	Smart Card Reader RX and TX FIFO Access Point

8.7.5. Register Description

8.7.5.1. Smart Card Reader Control and Status Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: SCR_CSR
Bit	Read/Write	Default/Hex	Description
31	R	0x0	SCDET Smart Card Detected This bit is set to ‘1’ when the scdetect input is active at least for a debounce

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			time.
30:25	/	/	/
24	R/W	0x0	SCDETPOL Smart Card Detect Polarity This bit set polarity of scdetect signal. 0: Low Active 1: High Active
23:22	R/W	0x0	Protocol Selection (PTLSEL) 00: T=0. 01: T=1, no character repeating and no guard time is used when T=1 protocol is selected. 10: Reserved 11: Reserved
21	R/W	0x0	ATRSTFLUSH ATR Start Flush FIFO When enabled, both FIFOs are flushed before the ATR is started.
20	R/W	0x0	TSRXE TS Receive Enable When set to '1', the TS character (the first ATR character) will be store in RXFIFO during card session.
19	R/W	0x0	CLKSTPPOL Clock Stop Polarity The value of the scclk output during the clock stop state.
18	R/W	0x0	PECRXE Parity Error Character Receive Enable Enables storage of the characters received with wrong parity in RX FIFO.
17	R/W	0x0	MSBF MSB First When high, inverse bit ordering convention (msb to lsb) is used.
16	R/W	0x0	DATAPOL Data Plorarity When high, inverse level convention is used (A='1', Z='0').
15:12	/	/	/
11	R/W	0x0	DEACT_Deactivation Setting of this bit initializes the deactivation sequence. When the deactivation is finished, the DEACT bit is automatically cleared.
10	R/W	0x0	ACT Activation. Setting of this bit initializes the activation sequence. When the activation is finished, the ACT bit is automatically cleared.
9	R/W	0x0	WARMRST Warm Reset Command. Writing '1' to this bit initializes Warm Reset of the Smart Card. This bit is always read as '0'.
8	R/W	0x0	CLKSTOP Clock Stop. When this bit is asserted and the smart card I/O line is in 'Z' state, the SCR core stops driving of the smart card clock signal after the

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			CLKSTOPDELAY time expires. The smart card clock is restarted immediately after the CLKSTOP signal is deasserted. New character transmission can be started after CLKSTARTDELAY time. The expiration of both times is signaled by the CLKSTOPRUN bit in the interrupt registers.
7:3	/	/	/
2	R/W	0x0	GINTEN Global Interrupt Enable. When high, IRQ output assertion is enabled.
1	R/W	0x0	RXEN Receiving Enable. When enabled the characters sent by the Smart Card are received by the UART and stored in RX FIFO. Receiving is internally disabled while a transmission is in progress.
0	R/W	0x0	TXEN Transmission Enable. When enabled the characters are read from TX FIFO and transmitted through UART to the Smart Card.

8.7.5.2. Smart Card Reader Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: SCR_INTEN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23	R/W	0x0	SCDEA Smart Card Deactivation Interrupt Enable.
22	R/W	0x0	SCACT Smart Card Activation Interrupt Enable.
21	R/W	0x0	SCINS Smart Card Inserted Interrupt Enable.
20	R/W	0x0	SCREM Smart Card Removed Interrupt Enable.
19	R/W	0x0	ATRDONE ATR Done Interrupt Enable.
18	R/W	0x0	ATRFAIL ATR Fail Interrupt Enable.
17	R/W	0x0	C2CFULL Two Consecutive Characters Limit Interrupt Enable.
16	R/W	0x0	CLKSTOPRUN Smart Card Clock Stop/Run Interrupt Enable.
15:13	/	/	/
12	R/W	0x0	RXPERR RX Parity Error Interrupt Enable.
11	R/W	0x0	RXDONE RX Done Interrupt Enable.
10	R/W	0x0	RXFIFOTHD RX FIFO Threshold Interrupt Enable.
9	R/W	0x0	RXFIFOFULL

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			RX FIFO Full Interrupt Enable.
8:5	/	/	/
4	R/W	0x0	TXPERR TX Parity Error Interrupt Enable.
3	R/W	0x0	TXDONE TX Done Interrupt Enable.
2	R/W	0x0	TXFIFOTHD TX FIFO Threshold Interrupt Enable.
1	R/W	0x0	TXFIFOEMPTY TX FIFO Empty Interrupt Enable.
0	R/W	0x0	TXFIFODONE TX FIFO Done Interrupt Enable.

8.7.5.3. Smart Card Reader Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: SCR_INTST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23	R/W1C	0x0	SCDEA Smart Card Deactivation Interrupt. When enabled, this interrupt is asserted after the Smart Card deactivation sequence is complete. Write '1' to clear.
22	R/W1C	0x0	SCACT Smart Card Activation Interrupt. When enabled, this interrupt is asserted after the Smart Card activation sequence is complete. Write '1' to clear.
21	R/W1C	0x0	SCINS Smart Card Inserted Interrupt. When enabled, this interrupt is asserted after the smart card insertion. Write '1' to clear.
20	R/W1C	0x0	SCREM Smart Card Removed Interrupt. When enabled, this interrupt is asserted after the smart card removal. Write '1' to clear.
19	R/W1C	0x0	ATRDONE ATR Done Interrupt. When enabled, this interrupt is asserted after the ATR sequence is successfully completed. Write '1' to clear.
18	R/W1C	0x0	ATRFAIL ATR Fail Interrupt. When enabled, this interrupt is asserted if the ATR sequence fails. Write '1' to clear.
17	R/W1C	0x0	C2CFULL Two Consecutive Characters Limit Interrupt. When enabled, this interrupt

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			is asserted if the time between two consecutive characters, transmitted between the Smart Card and the Reader in both directions, is equal the Two Characters Delay Limit described below. The C2CFULL interrupt is internally enabled from the ATR start to the deactivation or ATR restart initialization. It is recommended to use this counter to detect unresponsive Smart Cards. Write '1' to clear.
16	R/W1C	0x0	CLKSTOPRUN Smart Card Clock Stop/Run Interrupt. When enabled, this interrupt is asserted in two cases: 1. When the smart card clock is stopped. 2. When the new character can be started after the clock restart. To distinguish between the two interrupt cases, we recommend reading the CLKSTOP bit in SCR_CTRL1 register. Write '1' to clear.
15:13	/	/	/
12	R/W1C	0x0	RXPERR RX Parity Error Interrupt. When enabled, this interrupt is asserted after the character with wrong parity was received when the number of repeated receptions exceeds RXREPEAT value or T=1 protocol is used. Write '1' to clear.
11	R/W1C	0x0	RXDONE RX Done Interrupt. When enabled, this interrupt is asserted after a character was received from the Smart Card. Write '1' to clear.
10	R/W1C	0x0	RXFIFOTHD RX FIFO Threshold Interrupt. When enabled, this interrupt is asserted if the number of bytes in RX FIFO is equal or exceeds the RX FIFO threshold. Write '1' to clear.
9	R/W1C	0x0	RXFIFOFULL RX FIFO Full Interrupt. When enabled, this interrupt is asserted if the RX FIFO is filled up. Write '1' to clear.
8:5	/	/	/
4	R/W1C	0x0	TXPERR TX Parity Error Interrupt. When enabled, this interrupt is asserted if the Smart Card signals wrong character parity during the guard time after the character transmission was repeated TXREPEAT times or T=1 protocol is used. Write '1' to clear.
3	R/W1C	0x0	TXDONE TX Done Interrupt. When enabled, this interrupt is asserted after one character was transmitted to the smart card. Write '1' to clear.
2	R/W1C	0x0	TXFIFOTHD TX FIFO Threshold Interrupt. When enabled, this interrupt is asserted if

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			the number of bytes in TX FIFO is equal or less than the TX FIFO threshold. Write '1' to clear.
1	R/W1C	0x0	TXFIFOEMPTY TX FIFO Empty Interrupt. When enabled, this interrupt is asserted if the TX FIFO is emptied out. Write '1' to clear.
0	R/W1C	0x0	TXFIFODONE TX FIFO Done Interrupt. When enabled, this interrupt is asserted after all bytes from TX FIFO ware transferred to the Smart Card. Write '1' to clear.

8.7.5.4. Smart Card Reader FIFO Control and Status Register(Default Value: 0x0000_0101)

Offset: 0x000C			Register Name: SCR_FCSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10	R/W	0x0	RXFIFOFLUSH Flush RX FIFO. RX FIFO is flushed, when '1' is written to this bit.
9	R	0x0	RXFIFOFULL RX FIFO Full.
8	R	0x1	RXFIFOEMPTY RX FIFO Empty.
7:3	/	/	/
2	R/W	0x0	TXFIFOFLUSH Flush TX FIFO. TX FIFO is flushed, when '1' is written to this bit.
1	R	0x0	TXFIFOFULL TX FIFO Full.
0	R	0x1	TXFIFOEMPTY TX FIFO Empty.

8.7.5.5. Smart Card Reader FIFO Count Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SCR_FIFOCNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	RXFTH RX FIFO Threshold These bits set the interrupt threshold of RX FIFO. The interrupt is asserted when the number of bytes it receives is equal to, or exceeds the threshold.
23:16	R/W	0x0	TXFTH TX FIFO Threshold These bits set the interrupt threshold of TX FIFO. The interrupt is asserted when the number of bytes in TX FIFO is equal to or less than the threshold.

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15:8	R	0x0	RXFCNT RX FIFO Counter These bits provide the number of bytes stored in the RXFIFO.
7:0	R	0x0	TXFCNT TX FIFO Counter These bits provide the number of bytes stored in the TXFIFO.

8.7.5.6. Smart Card Reader Repeat Control Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: SCR_REPEAT
Bit	**Read/Write**	**Default/Hex**	**Description**
15:8	/	/	/
7:4	R/W	0x0	RXRPT RX Repeat This is a 4-bit register that specifies the number of attempts to request character re-transmission after wrong parity was detected. The re-transmission of the character is requested using the error signal during the guard time.
3:0	R/W	0x0	TXRPT TX Repeat This is a 4-bit register that specifies the number of attempts to re-transmit the character after the Smart Card signals the wrong parity during the guard time.

8.7.5.7. Smart Card Reader Clock Divisor Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: SCR_CLKDIV
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	BAUDDIV Baud Clock Divisor. This 16-bit register defines the divisor value used to generate the Baud Clock impulses from the system clock. $BAUD = \frac{f_{sysclk}}{2*(BAUDDIV+1)}$
15:0	R/W	0x0	SCCDIV Smart Card Clock Divisor. This 16-bit register defines the divisor value used to generate the Smart Card Clock from the system clock. $f_{scclk} = \frac{f_{sysclk}}{2*(SCCDIV+1)}$ f_{scclk} is the frequency of Smart Card Clock Signal. f_{sysclk} is the frequency of APB Clock.

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8.7.5.8. Smart Card Reader Line Time Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: SCR_LTIM
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	ATR ATR Start Limit. This 16-bit register defines the maximum time between the rising edge of the *scrstn* signal and the start of ATR response. ATR Start Limit = 128* ATR* T_{scclk} .
15:8	R/W	0x0	RST Reset Duration. This 16-bit register sets the duration of the Smart Card reset sequence. This value is same for the cold and warm reset. Cold/Warm Reset Duration = 128* RST* T_{scclk} .
7:0	R/W	0x0	ACT Activation/Deactivation Time. This 16-bit register sets the duration of each part of the activation and deactivation sequence. Activation/Deactivation Duration = 128* ACT * T_{scclk} . $T_{scclk} = \frac{1}{f_{scclk}}$ is the Smart Card Clock Cycle.

8.7.5.9. Smart Card Reader Character Time Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SCR_CTIM
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	CHARLIMIT Character Limit. This 16-bit register sets the maximum time between the leading edges of two consecutive characters. The value is ETUs.
15:8	/	/	/
7:0	R/W	0x0	GUARDTIME Character Guard time. This 8-bit register sets a delay at the end of each character transmitted from the Smart Card Reader to the Smart Card. The value is in ETUs. The parity error is besides signaled during the guard time.

8.7.5.10. Smart Card Reader Line Control Register(Default Value: 0x0000_0000)

Offset: 0x0030	Register Name: SCR_PAD

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Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	DSCVPPPP Direct Smart Card Vpp Pause/Prog. It provides direct access to SCVPPPP output.
6	R/W	0x0	DSCVPPEN Direct Smart Card Vpp Enable. It provides direct access to SCVPPEN output.
5	R/W	0x0	AUTOADEAVPP Automatic Vpp Handling. When high, it enables automatic handling of DSVPPEN and DSVPPPP signals during activation and deactivation sequence.
4	R/W	0x0	DSCVCC Direct Smart Card VCC. When DIRACCPADS='1', the DSCVCC bit provides direct access to SCVCC pad.
3	R/W	0x0	DSCRST Direct Smart Card Clock. When DIRACCPADS='1', the DSCRST bit provides direct access to SCRST pad.
2	R/W	0x0	DSCCLK Direct Smart Card Clock. When DIRACCPADS='1', the DSCCLK bit provides direct access to SCCLK pad.
1	R/W	0x0	DSCIO Direct Smart Card Input/Output. When DIRACCPADS='1', the DSCIO bit provides direct access to SCIO pad.
0	R/W	0x0	DIRACCPADS Direct Access to Smart Card Pads. When high, it disables a serial interface functionality and enables direct control of the smart card pads using following 4 bits.

8.7.5.11. Smart Card Reader FSM Register(Default Value: 0x0000_0000)

Offset: 0x003c			Register Name: SCR_FSM
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R	0x0	ATR_STRUCTURE_FSM
23:16	R	0x0	ATR_FSM
15:8	R	0x0	ACT_FSM
7:0	R	0x0	SCR_FSM

8.7.5.12. Smart Card Reader Debounce Time Register(Default Value: 0x0000_03ff)

Offset: 0x0040			Register Name: SCR_DT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x3ff	SCR_DEBOUNCE_TIME

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			Set the debounce time value for card insert detecting.The time uint is the cycle of SCCLK.

8.7.5.13. Smart Card Reader FIFO Data Register(Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: SCR_FIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	FIFO_DATA This 8-bit register provides access to the RX and TX FIFO buffers. The TX FIFO is accessed during the APB write transfer. The RX FIFO is accessed during the APB read transfer.

8.7.5.14. Smart Card Reader Version Register(Default Value: 0x0001_0000)

Offset: 0x03FC			Register Name: SCR_VER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
24:16	R	0x1	GEN_VER Generation version.
15:8	R	0x0	SUB_VER Sub version.
7:0	R	0x0	PRJ_VER Project version.

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8.8. EMAC

8.8.1. Overview

The Ethernet Medium Access Controller (EMAC) enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2002 standard. It supports 10/100/1000-Mbps external PHY with RMII/RGMII interface in both full and half duplex mode. The Internal DMA is designed for packet-oriented data transfers based on a linked list of descriptors. 4K Byte TXFIFO and 16K Byte RXFIFO are provided to keeping continuous transmission and reception. Flow Control, CRC Pad & Stripping, and address filtering are also supported in this module.

Features:

- Supports 10/100/1000-Mbps data transfer rates
- Supports RMII/RGMII PHY interface
- Supports MDIO
- Supports both full-duplex and half-duplex operation
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Supports a variety of flexible address filtering modes
- Separate 32-bit status returned for transmission and reception packets
- Optimization for packet-oriented DMA transfers with frame delimiters
- Supports linked-list descriptor list structure
- Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 4 KB of data
- Comprehensive status reporting for normal operation and transfers with errors
- 4KB TXFIFO for transmission packets and 16KB RXFIFO for reception packets
- Programmable interrupt options for different operational conditions

8.8.2. Block Diagram

The EMAC Controller block diagram is shown below.

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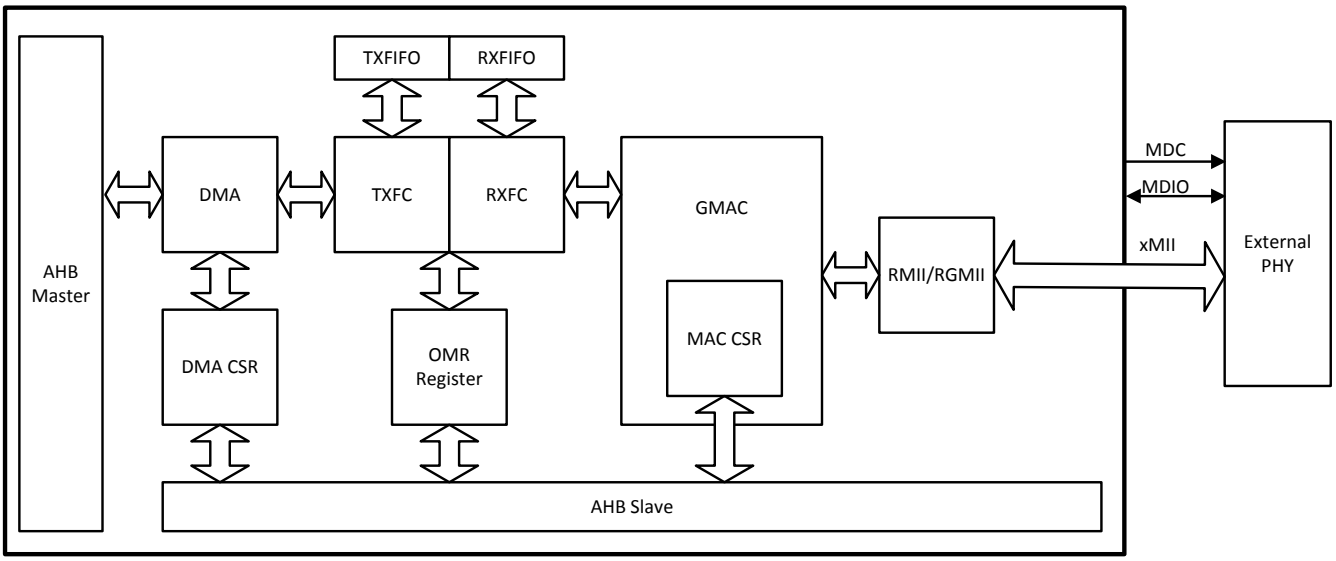


Figure 8-28. EMAC Block Diagram

8.8.3. Operations and Functional Descriptions

8.8.3.1. External Signals

Table 8-17 describes the pin mapping of EMAC.

Table 8-17. EMAC Pin Mapping

Pin Name	RGMII	RMII
RGMII_RXD3/RMII_NULL	RXD3	
RGMII_RXD2/RMII_NULL	RXD2	
RGMII_RXD1/RMII_RXD1	RXD1	RXD1
RGMII_RXD0/RMII_RXD0	RXD0	RXD0
RGMII_RXCK/RMII_NULL	RXCK	
RGMII_RXCTL/RMII_CRS_DV	RXCTL	CRS_DV
RGMII_NULL/RMII_RXER		RXER
RGMII_TXD3/RMII_NULL	TXD3	
RGMII_TXD2/RMII_NULL	TXD2	
RGMII_TXD1/RMII_TXD1	TXD1	TXD1
RGMII_TXD0/RMII_TXD0	TXD0	TXD0
RGMII_NULL/RMII_NULL		
RGMII_TXCK/RMII_TXCK	TXCK	TXCK
RGMII_TXCTL/RMII_TXEN	TXCTL	TXEN
RGMII_NULL/RMII_NULL		
RGMII_CLKIN/RMII_NULL	CLKIN	
MDC	MDC	MDC

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MDIO	MDIO	MDIO

Table 8-18 describes the pin list of RGMII.

Table 8-18. EMAC RGMII Pin List

Pin Name	Description	Type
RGMII_TXD[3:0]	EMAC RGMII Transmit Data	O
RGMII_TXCTL	EMAC RGMII Transmit Control	O
RGMII_TXCK	EMAC RGMII Transmit Clock	O
RGMII_RXD[3:0]	EMAC RGMII Receive Data	I
RGMII_RXCTL	EMAC RGMII Receive Control	I
RGMII_RXCK	EMAC RGMII Receive Clock	I
RGMII_CKIN	EMAC RGMII 125M Reference Clock Input	I
MDC	EMAC Management Data Clock	O
MDIO	EMAC Management Data Input Output	I/O

Table 8-19 describes the pin list of RMII.

Table 8-19. EMAC RMII Pin List

Pin Name	Description	Type
RMII_TXD[1:0]	EMAC RMII Transmit Data	O
RMII_TXEN	EMAC RMII Transmit Enable	O
RMII_TXCK	EMAC RMII Transmit Clock	I
RMII_RXD[1:0]	EMAC RMII Receive Data	I
RMII_CRS_DV	EMAC RMII Receive Data Valid	I
RMII_RXERR	EMAC RMII Receive Error	I
MDC	EMAC Management Data Clock	O
MDIO	EMAC Management Data Input Output	I/O

8.8.3.2. Clock Sources

Table 8-20 describes the clock of EMAC.

Table 8-20. EMAC Clock

Clock Name	Description	Type
RGMII_TXCK/ RMII_TXCK	In RGMII mode, output 2.5MHz/25MHz/125MHz. In RMII mode, input 5MHz/50MHz.	O/I
RGMII_RXCK/ RMII_NULL	In RGMII mode, input 2.5MHz/25MHz/125MHz. In RMII mode, no input	I
RGMII_CLKIN/ RMII_NULL	In RGMII mode, input 125M Reference Clock In RMII mode, no clock	I

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8.8.3.3. Typical Application

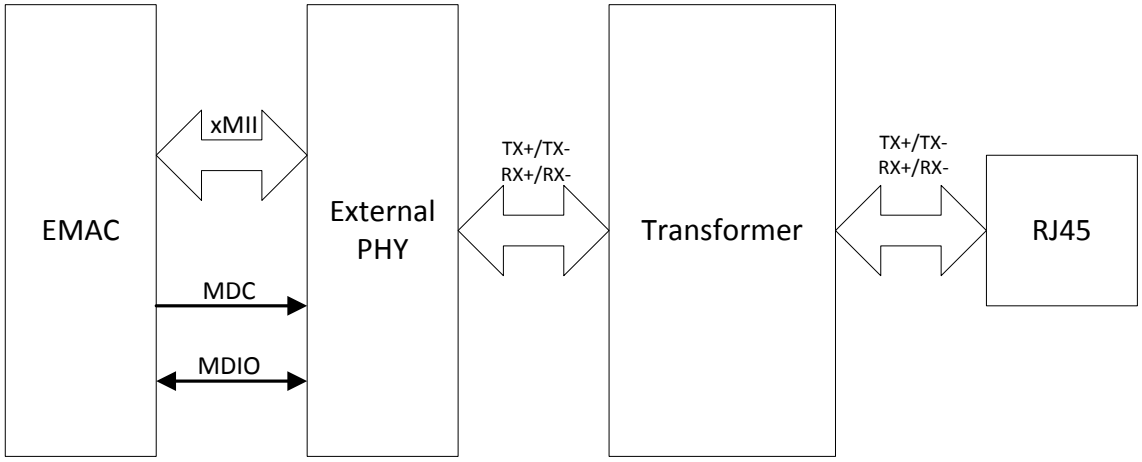


Figure 8-29. EMAC Typical Application

8.8.3.4. EMAC RX/TX Descriptor

The internal DMA of EMAC transfers data between host memory and internal RX/TX FIFO with a linked list of descriptors. Each descriptor is consisted of four words, and contains some necessary information to transfer TX and RX frames. The descriptor list structure is shown in Figure 8-30. The address of each descriptor must be 32-bit aligned.

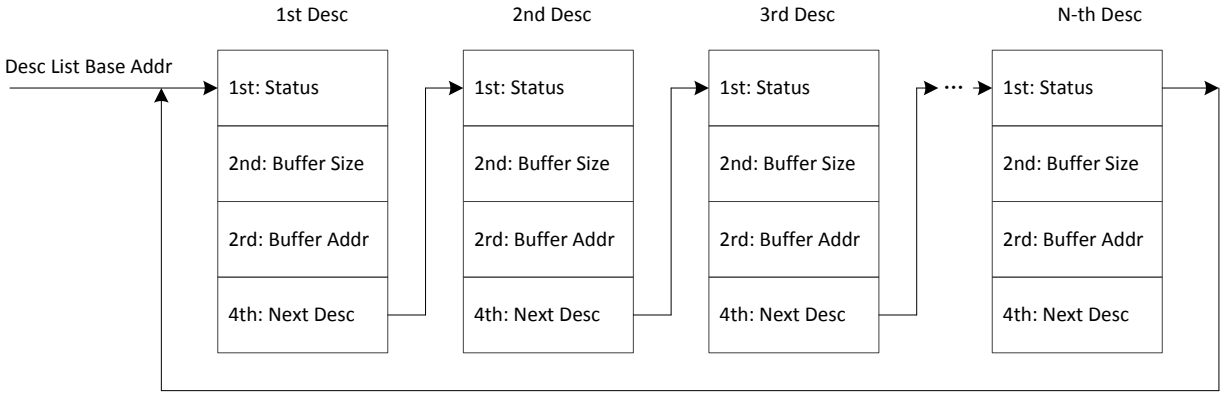


Figure 8-30. EMAC RX/TX Descriptor List

8.8.3.5. Transmit Descriptor

(1).1st Word of Transmit Descriptor

Bits	Description
31	TX_DESC_CTL

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	When set, current descriptor can be used by DMA. This bit is cleared by DMA when the whole frame is transmitted or all data in current descriptor's buffer are transmitted.
30:17	Reserved
16	TX_HEADER_ERR When set, the checksum of transmitted frame's header is wrong.
15	Reserved
14	TX_LENGHT_ERR When set, the length of transmitted frame is wrong.
13	Reserved
12	TX_PAYLOAD_ERR When set, the checksum of transmitted frame's payload is wrong.
11	Reserved
10	TX_CRS_ERR When set, carrier is lost during transmission.
9	TX_COL_ERR_0 When set, the frame is aborted because of collision after contention period.
8	TX_COL_ERR_1 When set, the frame is aborted because of too many collisions.
7	Reserved.
6:3	TX_COL_CNT The number of collisions before transmission.
2	TX_DEFER_ERR When set, the frame is aborted because of too much deferral.
1	TX_UNDERFLOW_ERR When set, the frame is aborted because of TX FIFO underflow error.
0	TX_DEFER When set in Half-Duplex mode, the EMAC defers the frame transmission.

(2).2nd Word of Transmit Descriptor

Bits	Description
31	TX_INT_CTL When set and the current frame have been transmitted, the TX_INT in Interrupt Status Register will be set.
30	LAST_DESC When set, current descriptor is the last one for current frame.
29	FIR_DESC When set, current descriptor is the first one for current frame.
28:27	CHECKSUM_CTL These bits control to insert checksums in transmit frame.
26	CRC_CTL When set, CRC field is not transmitted.
25:11	Reserved
10:0	BUF_SIZE The size of buffer specified by current descriptor.

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(3).3rd Word of Transmit Descriptor

Bits	Description
31:0	BUF_ADDR The address of buffer specified by current descriptor.

(4).4th Word of Transmit Descriptor

Bits	Description
31:0	NEXT_DESC_ADDR The address of next descriptor. It must be 32-bit aligned.

8.8.3.6. Receive Descriptor

(1).1st Word of Receive Descriptor

Bits	Description
31	RX_DESC_CTL When set, current descriptor can be used by DMA. This bit is cleared by DMA when complete frame is received or current descriptor's buffer is full.
30	RX_DAF_FAIL When set, current frame don't pass DA filter.
29:16	RX_FRM_LEN When LAST_DESC is not set and no error bit is set, this field is the length of received data for current frame. When LAST_DESC is set, RX_OVERFLOW_ERR and RX_NO_ENOUGH_BUF_ERR are not set, this field is the length of receive frame.
15	Reserved
14	RX_NO_ENOUGH_BUF_ERR When set, current frame is clipped because of no enough buffer.
13	RX_SAF_FAIL When set, current fame don't pass SA filter.
12	Reserved.
11	RX_OVERFLOW_ERR When set, a buffer overflow error occurred and current frame is wrong.
10	Reserved
9	FIR_DESC When set, current descriptor is the first descriptor for current frame.
8	LAST_DESC When set, current descriptor is the last descriptor for current frame.
7	RX_HEADER_ERR When set, the checksum of frame's header is wrong.
6	RX_COL_ERR

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	When set, there is a late collision during reception in half-duplex mode.
5	Reserved.
4	RX_LENGTH_ERR When set, the length of current frame is wrong.
3	RX_PHY_ERR When set, the receive error signal from PHY is asserted during reception.
2	Reserved.
1	RX_CRC_ERR When set, the CRC filed of received frame is wrong.
0	RX_PAYLOAD_ERR When set, the checksum or length of received frame's payload is wrong.

(2).2nd Word of Receive Descriptor

Bits	Description
31	RX_INT_CTL When set and a frame have been received, the RX_INT will not be set.
30:11	Reserved
10:0	BUF_SIZE The size of buffer specified by current descriptor.

(3).3rd Word of Receive Descriptor

Bits	Description
31:0	BUF_ADDR The address of buffer specified by current descriptor.

(4).4th Word of Receive Descriptor

Bits	Description
31:0	NEXT_DESC_ADDR The address of next descriptor. This field must be 32-bit aligned.

8.8.4. Register List

Module Name	Base Address
EMAC	0x05020000

Register Name	Offset	Description
EMAC_BASIC_CTL0	0x0000	EMAC Basic Control Register0
EMAC_BASIC_CTL1	0x0004	EMAC Basic Control Register1

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EMAC_INT_STA	0x0008	EMAC Interrupt Status Register
EMAC_INT_EN	0x000C	EMAC Interrupt Enable Register
EMAC_TX_CTL0	0x0010	EMAC Transmit Control Register0
EMAC_TX_CTL1	0x0014	EMAC Transmit Control Register1
EMAC_TX_FLOW_CTL	0x001C	EMAC Transmit Flow Control Register
EMAC_TX_DMA_DESC_LIST	0x0020	EMAC Transmit Descriptor List Address Register
EMAC_RX_CTL0	0x0024	EMAC Receive Control Register0
EMAC_RX_CTL1	0x0028	EMAC Receive Control Register1
EMAC_RX_DMA_DESC_LIST	0x0034	EMAC Receive Descriptor List Address Register
EMAC_RX_FRM_FLT	0x0038	EMAC Receive Frame Filter Register
EMAC_RX_HASH0	0x0040	EMAC Hash Table Register0
EMAC_RX_HASH1	0x0044	EMAC Hash Table Register1
EMAC_MII_CMD	0x0048	EMAC Management Interface Command Register
EMAC_MII_DATA	0x004C	EMAC Management Interface Data Register
EMAC_ADDR_HIGH0	0x0050	EMAC MAC Address High Register0
EMAC_ADDR_LOW0	0x0054	EMAC MAC Address High Register0
EMAC_ADDR_HIGHx	0x0050+0x8*N(N=1~7)	EMAC MAC Address High RegisterN(N:1~7)
EMAC_ADDR_LOWx	0x0054+0x8*N(N=1~7)	EMAC MAC Address Low RegisterN(N:1~7)
EMAC_TX_DMA_STA	0x00B0	EMAC Transmit DMA Status Register
EMAC_TX_CUR_DESC	0x00B4	EMAC Current Transmit Descriptor Register
EMAC_TX_CUR_BUF	0x00B8	EMAC Current Transmit Buffer Address Register
EMAC_RX_DMA_STA	0x00C0	EMAC Receive DMA Status Register
EMAC_RX_CUR_DESC	0x00C4	EMAC Current Receive Descriptor Register
EMAC_RX_CUR_BUF	0x00C8	EMAC Current Receive Buffer Address Register
EMAC_RGMII_STA	0x00D0	EMAC RGMII Status Register

8.8.5. Register Description

8.8.5.1. EMAC Basic Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0000			**Register Name: EMAC_BASIC_CTL0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:2	R/W	0x0	SPEED 00: 1000 Mbit/s 01: Reserved 10: 10 Mbit/s 11: 100 Mbit/s
1	R/W	0x0	LOOPBACK 0: Disable 1: Enable
0	R/W	0x0	DUPLEX 0: Half-duplex

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			1: Full-duplex

8.8.5.2. EMAC Basic Control Register1 (Default Value: 0x0800_0000)

Offset: 0x0004			Register Name: EMAC_BASIC_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:24	R/W	0x8	BURST_LEN The burst length of RX and TX DMA transfer.
23:2	/	/	/
1	R/W	0x0	RX_TX_PRI RX TX DMA priority 0: Same priority 1: RX priority over TX
0	R/W	0x0	SOFT_RST Soft Reset all Registers and Logic 0: No valid 1: Reset **NOTE** **All clock inputs must be valid before soft rest. This bit is cleared internally when the reset operation is completed fully. Before write any register, this bit should read a 0.**

8.8.5.3. EMAC Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: EMAC_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W1C	0x0	RGMII_LINK_STA_P RMII Link Status Changed Interrupt Pending 0: No Pending 1: Pending Write ‘1’ to clear
15:14	/	/	/
13	R/W1C	0x0	RX_EARLY_P RX DMA Filled First data Buffer of the Receive Frame Interrupt Pending 0: No Pending 1: Pending Write ‘1’ to clear
12	R/W1C	0x0	RX_OVERFLOW_P RX FIFO Overflow Error Interrupt Pending 0: No Pending

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			1: Pending Write '1' to clear
11	R/W1C	0x0	RX_TIMEOUT_P RX Timeout Interrupt Pending 0: No Pending 1: Pending Write '1' to clear .When this bit asserted, the length of receive frame is greater than 2048 bytes(10240 when JUMBO_FRM_EN is set)
10	R/W1C	0x0	RX_DMA_STOPPED_P When this bit asserted, the RX DMA FSM is stopped.
9	R/W1C	0x0	RX_BUF_UA _P RX Buffer UA Interrupt Pending 0: No Pending 1: Pending Write '1' to clear .When this asserted, the RX DMA can't acquire next RX descriptor and RX DMA FSM is suspended. The ownership of next RX descriptor should be changed to RX DMA. The RX DMA FSM will resume when write to DMA_RX_START bit or next receive frame is coming.
8	R/W1C	0x0	RX_P Frame RX Completed Interrupt Pending 0: No Pending 1: Pending Write '1' to clear. When this bit is asserted, a frame reception is completed. The RX DMA FSM remains in the running state.
7:6	/	/	/
5	R/W1C	0x0	TX_EARLY_P Frame is transmitted to FIFO totally Interrupt Pending 0: No Pending 1: Pending Write '1' to clear. When this bit asserted
4	R/W1C	0x0	TX_UNDERFLOW_P TX FIFO Underflow Interrupt Pending 0: No Pending 1: Pending Write '1' to clear
3	R/W1C	0x0	TX_TIMEOUT_P Transmitter Timeout Interrupt Pending 0: No Pending 1: Pending Write '1' to clear
2	R/W1C	0x0	TX_BUF_UA_P TX Buffer UA Interrupt Pending 0: No Pending 1: Pending When this asserted, the TX DMA can not acquire next TX descriptor and TX

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			DMA FSM is suspended. The ownership of next TX descriptor should be changed to TX DMA. The TX DMA FSM will resume when write to DMA_TX_START bit.
1	R/W1C	0x0	TX_DMA_STOPPED_P Transmission DMA Stopped Interrupt Pending 0: No Pending 1: Pending Write '1' to clear
0	R/W1C	0x0	TX_P Frame Transmission Interrupt Pending 0: No Pending 1: Pending Write '1' to clear

8.8.5.4. EMAC Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: EMAC_INT_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W	0x0	RX_EARLY_INT_EN Early Receive Interrupt 0: Disable 1: Enable
12	R/W	0x0	RX_OVERFLOW_INT_EN Receive Overflow Interrupt 0: Disable 1: Enable
11	R/W	0x0	RX_TIMEOUT_INT_EN Receive Timeout Interrupt 0: Disable 1: Enable
10	R/W	0x0	RX_DMA_STOPPED_INT_EN Receive DMA FSM Stopped Interrupt 0: Disable 1: Enable
9	R/W	0x0	RX_BUF_UA_INT_EN Receive Buffer Unavailable Interrupt 0: Disable 1: Enable
8	R/W	0x0	RX_INT_EN Receive interrupt 0: Disable 1: Enable
7:6	/	/	/

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5	R/W	0x0	TX_EARLY_INT_EN Early Transmit Interrupt 0: Disable 1: Enable
4	R/W	0x0	TX_UNDERFLOW_INT_EN Transmit Underflow Interrupt 0: Disable 1: Enable
3	R/W	0x0	TX_TIMEOUT_INT_EN Transmit Timeout Interrupt 0: Disable 1: Enable
2	R/W	0x0	TX_BUF_UA_INT_EN Transmit Buffer Available Interrupt 0: Disable 1: Enable
1	R/W	0x0	TX_DMA_STOPPED_INT_EN Transmit DMA FSM Stopped Interrupt 0: Disable 1: Enable
0	R/W	0x0	TX_INT_EN Transmit interrupt 0: Disable 1: Enable

8.8.5.5. EMAC Transmit Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0010			**Register Name: EMAC_TX_CTL0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TX_EN Enable Transmitter. 0: Disable 1: Enable When disable, transmit will continue until current transmit finish.
30	R/W	0x0	TX_FRM_LEN_CTL Frame Transmit Length Control 0: Up to 2,048 bytes (JUMBO_FRM_EN==0) Up to 10,240 bytes (JUMBO_FRM_EN==1) 1: Up to 16,384 bytes Any bytes after that is cut off
29:0	/	/	/

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8.8.5.6. EMAC Transmit Control Register1 (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: EMAC_TX_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TX_DMA_START Transmit DMA FSM Start 0: No valid 1: Start This cleared internally and always read a 0
30	R/W	0x0	TX_DMA_EN 0x0: Stop TX DMA after the completion of current frame transmission. 0x1: Start and run TX DMA.
29:11	/	/	/
10:8	R/W	0x0	TX_TH The threshold value of TX DMA FIFO. When TX_MD is 0, transmission starts when the size of frame in TX DMA FIFO is greater than the threshold. In addition, full frames with a length less than the threshold are transferred automatically. 000: 64 001: 128 010: 192 011: 256 Others: Reserved
7:2	/	/	/
1	R/W	0x0	TX_MD Transmission Mode 0: TX start after TX DMA FIFO bytes is greater than TX_TH 1: TX start after TX DMA FIFO located a full frame
0	R/W	0x0	FLUSH_TX_FIFO Flush the data in the TX FIFO. 0: Enable 1: Disable

8.8.5.7. EMAC Transmit Flow Control Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: EMAC_TX_FLOW_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TX_FLOW_CTL_STA This bit indicates a pause frame transmission is in progress. When the configuration of flow control is ready, set this bit to transmit a pause frame in full-duplex mode or activate the backpressure function. After completion of transmission, this bit will be cleared automatically. Before write register TX_FLOW_CTRL, this bit must be read as 0.
30:22	/	/	/

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21:20	R/W	0x0	TX_PAUSE_FRM_SLOT The threshold of the pause timer at which the input flow control signal is checked for automatic retransmission of pause frame. The threshold values should be always less than the PAUSE_TIME
19:4	R/W	0x0	PAUSE_TIME The pause time field in the transmitted control frame.
3:2	/	/	/
1	R/W	0x0	ZQP_FRM_EN 0: Disable 1: Enable When set, enable the functionality to generate Zero-Quanta Pause control frame.
0	R/W	0x0	TX_FLOW_CTL_EN TX Flow Control Enable 0: Disable 1: Enable When set, enable flow control operation to transmit pause frames in full-duplex mode, or enable the back-pressure operation in half-duplex mode.

8.8.5.8. EMAC Transmit DMA Descriptor List Address Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: EMAC_TX_DMA_LIST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX_DESC_LIST The base address of transmit descriptor list. It must be 32-bit aligned.

8.8.5.9. EMAC Receive Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: EMAC_RX_CTL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	RX_EN Enable Receiver 0: Disable receiver after current reception 1: Enable
30	R/W	0x0	RX_FRM_LEN_CTL Frame Receive Length Control 0: Up to 2,048 bytes (JUMBO_FRM_EN==0) Up to 10,240 bytes (JUMBO_FRM_EN==1) 1: Up to 16,384 bytes any bytes after that is cut off
29	R/W	0x0	JUMBO_FRM_EN Jumbo Frame Enable

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			0: Disable 1: Enable Jumbo frames of 9,018 bytes without reporting a giant
28	R/W	0x0	STRIP_FCS When set, strip the Pad/FCS field on received frames only when the length's field value is less than or equal to 1,500 bytes.
27	R/W	0x0	CHECK_CRC Check CRC Enable 0: disable 1: calculate CRC and check the IPv4 Header Checksum.
26:18	/	/	/
17	R/W	0x0	RX_PAUSE_FRM_MD 0: Only detect multicast pause frame specified in the 802.3x standard. 1: In addition to detect multicast pause frame specified in the 802.3x standard, also detect unicast pause frame with address specified in MAC Address 0 High Register and MAC address 0 Low Register.
16	R/W	0x0	RX_FLOW_CTL_EN When set, enable the functionality that decode the received pause frame and disable its transmitter for a specified time by pause frame.
15:0	/	/	/

8.8.5.10. EMAC Receive Control Register1 (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: EMAC_RX_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	RX_DMA_START When set, the RX DMA will go no to work. It is cleared internally and always read a 0.
30	R/W	0x0	RX_DMA_EN Receive DMA Enable 0: Stop RX DMA after finish receiving current frame 1: Start and run RX DMA
29:25	/	/	/
24	R/W	0x0	RX_FIFO_FLOW_CTL Receive FIFO Flow Control Enable 0: Disable 1: Enable,base on RX_FLOW_CTL_TH_DEACT and RX_FLOW_CTL_TH_ACT
23:22	R/W	0x0	RX_FLOW_CTL_TH_DEACT Threshold for Deactivating Flow Control 00: Full minus 1 KB 01: Full minus 2 KB 10: Full minus 3 KB 11: Full minus 4 KB valid in both half-duplex mode and full-duplex mode.

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21:20	R/W	0x0	RX_FLOW_CTL_TH_ACT Threshold for Activating Flow Control 00: Full minus 1 KB 01: Full minus 2 KB 10: Full minus 3 KB 11: Full minus 4 KB valid in both half-duplex mode and full-duplex mode.
19:6	/	/	/
5:4	R/W	0x0	RX_TH Threshold for RX DMA FIFO Start 00: 64 01: 32 10: 96 11: 128 only valid when RX_MD == 0, full frames with a length less than the threshold are transferred automatically.
3	R/W	0x0	RX_ERR_FRM 0: RX DMA drops frames with error 1: RX DMA forwards frames with error
2	R/W	0x0	RX_RUNT_FRM When set, forward undersized frames with no error and length less than 64bytes
1	R/W	0x0	RX_MD Receive Mode 0: RX start read after RX DMA FIFO bytes is greater than RX_TH 1: RX start read after RX DMA FIFO located a full frame
0	R/W	0x0	FLUSH_RX_FRM Flush Receive Frames 00: Enable when receive descriptors/buffers is unavailable 1: Disable

8.8.5.11. EMAC Receive DMA Descriptor List Address Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: EMAC_RX_DMA_LIST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RX_DESC_LIST The base address of receive descriptor list. It must be 32-bit aligned.

8.8.5.12. EMAC Receive Frame Filter Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: EMAC_RX_FRM_FLT
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DIS_ADDR_FILTER

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			Disable Address Filter 0: Enable 1: Disable
30:18	/	/	/
17	R/W	0x0	DIS_BROADCAST Disable Receive Broadcast Frames 0: Receive 1: Drop
16	R/W	0x0	RX_ALL_MULTICAST Receive All Multicast Frames Filter 0: Filter according to HASH_MULTICAST 1: Receive All
15:14	/	/	
13:12	R/W	0x0	CTL_FRM_FILTER Receive Control Frames Filter 00: Drop all control frames 01: Drop all control frames 10: Receive all control frames 11: Receive all control frames when pass the address filter
11:10	/	/	/
9	R/W	0x0	HASH_MULTICAST Filter Multicast Frames Set 0: by comparing the DA field in DA MAC address registers 1: according to the hash table
8	R/W	0x0	HASH_UNICAST Filter Unicast Frames Set 0: by comparing the DA field in DA MAC address registers 1: according to the hash table
7	/	/	/
6	R/W	0x0	SA_FILTER_EN Receive SA Filter Enable 0: Receive frames and update the result of SA filter 1: Update the result of SA filter. In addition, if the SA field of received frame does not match the values in SA MAC address registers, drop this frame.
5	R/W	0x0	SA_INV_FILTER Receive SA Invert Filter Set 0: Pass Frames whose SA field matches SA MAC address registers 1: Pass Frames whose SA field not matches SA MAC address registers
4	R/W	0x0	DA_INV_FILTER 0: Normal filtering of frames is performed 1: Filter both unicast and multicast frames by comparing DA field in inverse filtering mode
3:2	/	/	/
1	R/W	0x0	FLT_MD 0: If the HASH_MULTICAST or HASH_UNICAST is set, the frame is passed only when it matches the Hash filter

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			1: Receive the frame when it pass the address register filter or the hash filter(set by HASH_MULTICAST or HASH_UNICAST)
0	R/W	0x0	RX_ALL Receive All Frame Enable 0: Receive the frames that pass the SA/DA address filter 1: Receive all frames and update the result of address filter(pass or fail) in the receive status word

8.8.5.13. EMAC Receive Hash Table Register0 (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: EMAC_RX_HASH0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HASH_TAB0 The upper 32 bits of Hash table for receive frame filter.

8.8.5.14. EMAC Receive Hash Table Register1 (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: EMAC_RX_HASH1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HASH_TAB1 The lower 32 bits of Hash table for receive frame filter.

8.8.5.15. EMAC MII Command Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: EMAC_MII_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22:20	R/W	0x0	MDC_DIV_RATIO_M MDC Clock Divide Ratio 000: 16 001: 32 010: 64 011: 128 Others: Reserved **NOTE** **MDC Clock is divided from AHB clock**
19:17	/	/	/
16:12	R/W	0x0	PHY_ADDR PHY Address
11:9	/	/	/
8:4	R/W	0x0	PHY_REG_ADDR

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			PHY Register Address
3:2	/	/	/
1	R/W	0x0	MII_WR MII Write and Read 0: Read 1: Write
0	R/W	0x0	MII_BUSY 0: write no valid, read 0 indicate finish in read or write operation 1: write start read or write operation, read 1 indicate busy.

8.8.5.16. EMAC MII Data Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: EMAC_MII_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	MII_DATA Written to or read from the register in the selected PHY.

8.8.5.17. EMAC MAC Address High Register0 (Default Value: 0x0000_FFFF)

Offset: 0x0050			Register Name: EMAC_ADDR_HIGH0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFFFF	MAC_ADDR_HIGH0 The upper 16bits of the 1st MAC address.

8.8.5.18. EMAC MAC Address Low Register0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0054			Register Name: EMAC_ADDR_LOW0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0xFFFFFFFF	MAC_ADDR_LOW0 The lower 32bits of 1st MAC address.

8.8.5.19. EMAC MAC Address High RegisterN (Default Value: 0x0000_0000)

Offset: 0x0050+0x8*N (N=1~7)			Register Name: EMAC_ADDR_HIGHN
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MAC_ADDR_CTL MAC Address Valid 0: Not valid 1: Valid

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30	R/W	0x0	MAC_ADDR_TYPE MAC Address Type 0: used to compare with the destination address of the received frame 1: used to compare with the source address of the received frame
29:24	R/W	0x0	MAC_ADDR_BYTE_CTL MAC address byte control mask. The lower bit of mask controls the lower byte of in MAC address. When the bit of mask is 1, do not compare the corresponding byte.
23:16	/	/	/
15:0	R/W	0x0	MAC_ADDR_HIGH The upper 16bits of the MAC address.

8.8.5.20. EMAC MAC Address Low Register N (Default Value: 0x0000_0000)

Offset: 0x0054+0x8*N (N=1~7)			Register Name: EMAC_ADDR_LOWN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	MAC_ADDR_ LOWN The lower 32bits of MAC address N (N: 1~7).

8.8.5.21. EMAC Transmit DMA Status Register (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: EMAC_TX_DMA_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R	0x0	TX_DMA_STA The state of Transmit DMA FSM. 000: STOP, When reset or disable TX DMA 001: RUN_FETCH_DESC, Fetching TX DMA descriptor 010: RUN_WAIT_STA, Waiting for the status of TX frame 011: RUN_TRANS_DATA, Passing frame from host memory to TX DMA FIFO 100: Reserved 101: Reserved 111: RUN_CLOSE_DESC, Closing TX descriptor 110: SUSPEND, TX descriptor unavailable or TX DMA FIFO underflow

8.8.5.22. EMAC Transmit DMA Current Descriptor Register (Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: EMAC_TX_DMA_CUR_DESC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	The address of current transmit descriptor.

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8.8.5.23. EMAC Transmit DMA Current Buffer Address Register (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: EMAC_TX_DMA_CUR_BUF
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	The address of current transmit DMA buffer.

8.8.5.24. EMAC Receive DMA Status Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: EMAC_RX_DMA_STA
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2:0	R	0x0	RX_DMA_STA The State of RX DMA FSM. 000: STOP, When reset or disable RX DMA 001: RUN_FETCH_DESC, Fetching RX DMA descriptor 010: Reserved. 011: RUN_WAIT_FRM, Waiting for frame. 100: SUSPEND, RX descriptor unavailable; 101: RUN_CLOSE_DESC, Closing RX descriptor. 110: Reserved. 111: RUN_TRANS_DATA, Passing frame from host memory to RX DMA FIFO;

8.8.5.25. EMAC Receive DMA Current Descriptor Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: EMAC_RX_DMA_CUR_DESC
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	The address of current receive descriptor

8.8.5.26. EMAC Receive DMA Current Buffer Address Register (Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: EMAC_RX_DMA_CUR_BUF
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	The address of current receive DMA buffer

8.8.5.27. EMAC RGMII Status Register (Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: EMAC_RGMII_STA
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R	0x0	RGMII_LINK The link status of RGMII interface

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			0: down 1: up
2:1	R	0x0	RGMII_LINK_SPD The link speed of RGMII interface 00: 2.5 MHz 01: 25 MHz 10: 125 MHz 11: Reserved
0	R	0x0	RGMII_LINK_MD The link mode of RGMII interface 0: Half-Duplex 1: Full-Duplex

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8.9. TSC

8.9.1. Overview

The transport stream controller(TSC) is responsible for de-multiplexing and pre-processing the inputting multimedia data defined in ISO/IEC 13818-1.

The transport stream controller receives multimedia data stream from SSI (Synchronous Serial Port)/SPI (Synchronous Parallel Port) inputs and de-multiplexing the data into Packets by PID (Packet Identify). Before the Packet to be store to memory by DMA, it can be pre-processing by the Transport Stream Descrambler.

The transport stream controller can be used for almost all multi-media application cases, for example: DVB Set top Box, IPTV, Streaming-media Box, multi-media players and so on.

Features:

- Supports SPI/SSI interface,interface timing parameters are configurable
- 32 channels PID filter for each TSF
- Multiple transport stream packet (188, 192, 204) format support
- Hardware packet synchronous byte error detecting
- Hardware PCR packet detecting
- 64x16-bits FIFO for TSG, 64x32-bits FIFO for TSF
- Configurable SPI transport stream generator for streams in DRAM memory
- Supports DVB-CSA V1.1, DVB-CSA V2.1 Descrambler

8.9.2. Block Diagram

Figure 8-31 shows a block diagram of the TSC.

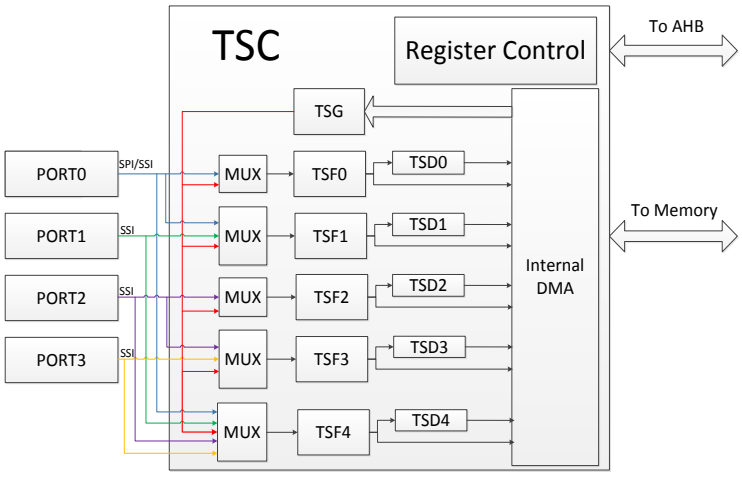


Figure 8-31. TSC Block Diagram

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NOTE

TSC – TS Controller
TSF – TS Filter
TSD – TS Descrambler
TSG – TS Generator

8.9.3. Operations and Functional Descriptions

8.9.3.1. External Signals

Table 8-21 describes the external signals of TSC.

Table 8-21. TSC External Signals

Signal	Description	Type
TS0_CLK	Clock of SPI/SSI data input	I
TS0_ERR	Error indicate	I
TS0_SYNC	Packet sync (or Start flag) for TS packet	I
TS0_DVLD	Data valid flag for TS data input	I
TS0_D[7:0]	TS data input. Data[7:0] are used in SPI mode; Only Data[0] is used in SSI mode.	I
TS1_CLK	Clock of SPI/SSI data input	I
TS1_ERR	Error indicate	I
TS1_SYNC	Packet sync (or Start flag) for TS packet	I
TS1_DVLD	Data valid flag for TS data input	I
TS1_D0	TS data input	I
TS2_CLK	Clock of SPI/SSI data input	I
TS2_ERR	Error indicate	I
TS2_SYNC	Packet sync (or Start flag) for TS packet	I
TS2_DVLD	Data valid flag for TS data input	I
TS2_D0	TS data input	I
TS3_CLK	Clock of SPI/SSI data input	I
TS3_ERR	Error indicate	I
TS3_SYNC	Packet sync (or Start flag) for TS packet	I
TS3_DVLD	Data valid flag for TS data input	I
TS3_D0	TS data input	I

8.9.3.2. Clock Sources

The following table describes the clock sources of TSC.

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Table 8-22. TSC Clock Sources

Clock Sources	Description
OSC24M	24MHz Crystal
PLL_PERIPH0(1X)	Peripheral Clock,default value is 600MHz

8.9.3.3. Timing Diagram

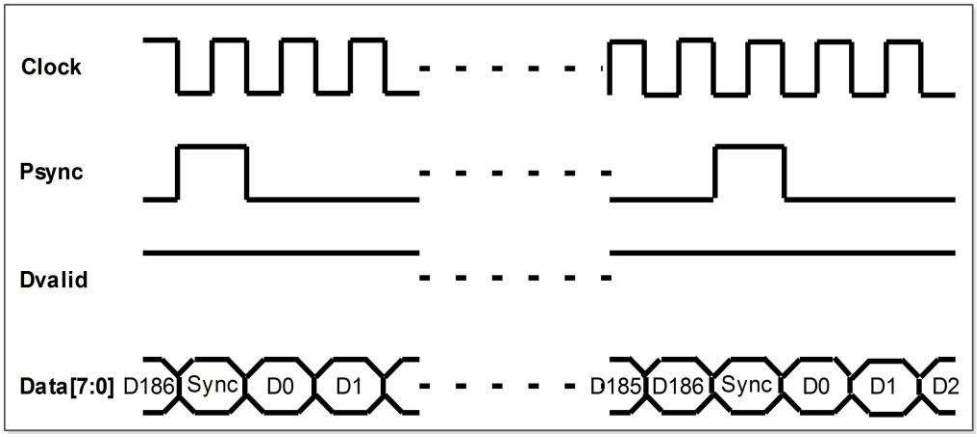


Figure 8-32. Input Timing for SPI Mode

(CLOCK = Rising Edge, PSYNC = High Active, DVALID = High Active, Packet Size = 188 Bytes)

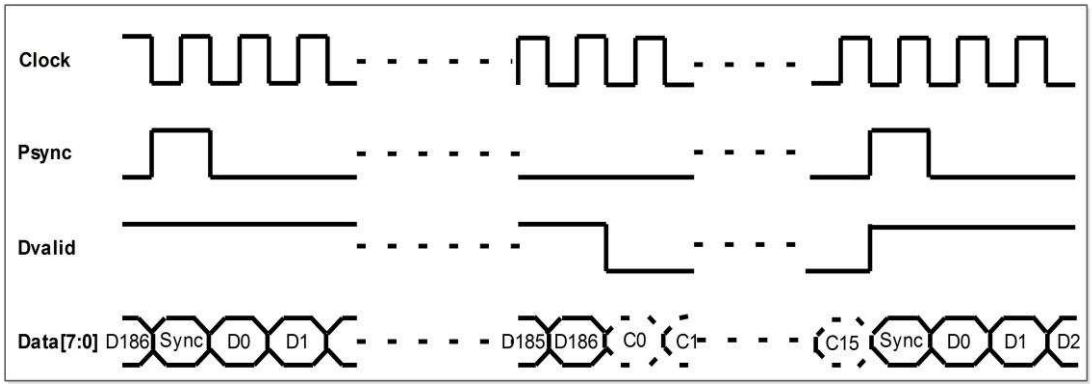
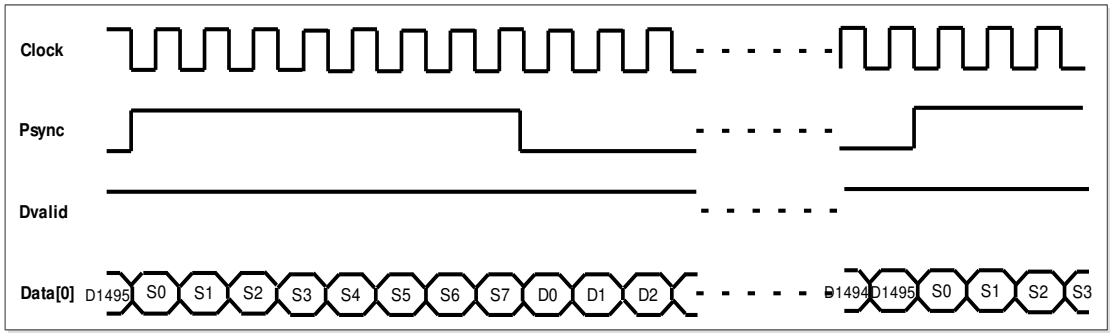


Figure 8-33. Alternative Input Timing for SPI Mode

(CLOCK = Rising Edge, PSYNC = High Active, DVALID = High Active, Packet Size = 188 Bytes)



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Figure 8-34. Alternative Input Timing for SSI Mode

(CLOCK = Rising Edge, PSYNC = High Active, DVALID = High Active, Packet Size = 188 Bytes)

8.9.3.4. Typical Application

Application 1: 2-port DVB TS, recording while playbacking at the same time.

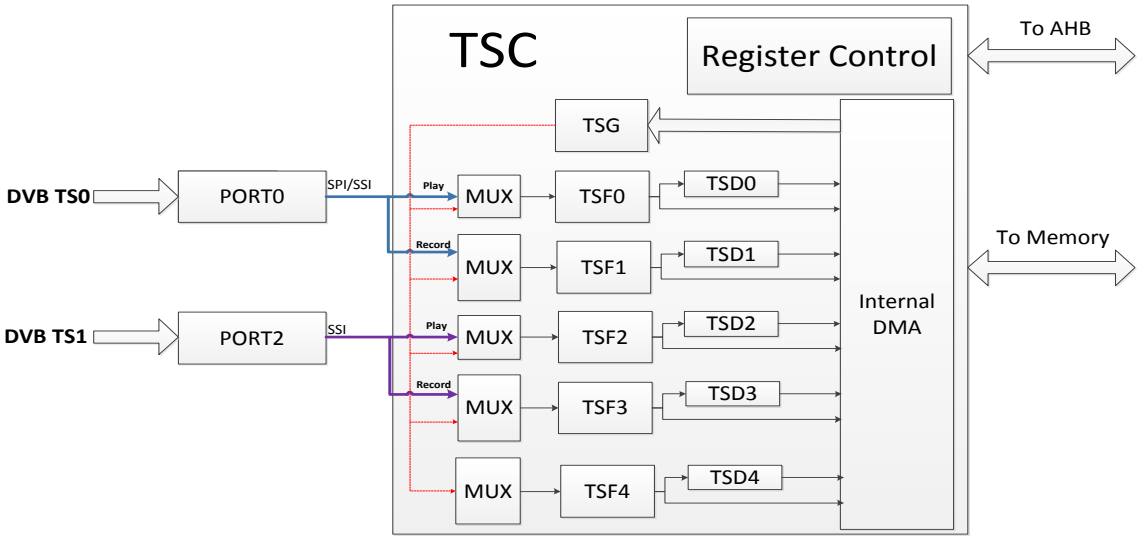


Figure 8-35. Typical Application1 Block Diagram

Application2: 2-port IPTV TS, recording while playbacking at the same time.

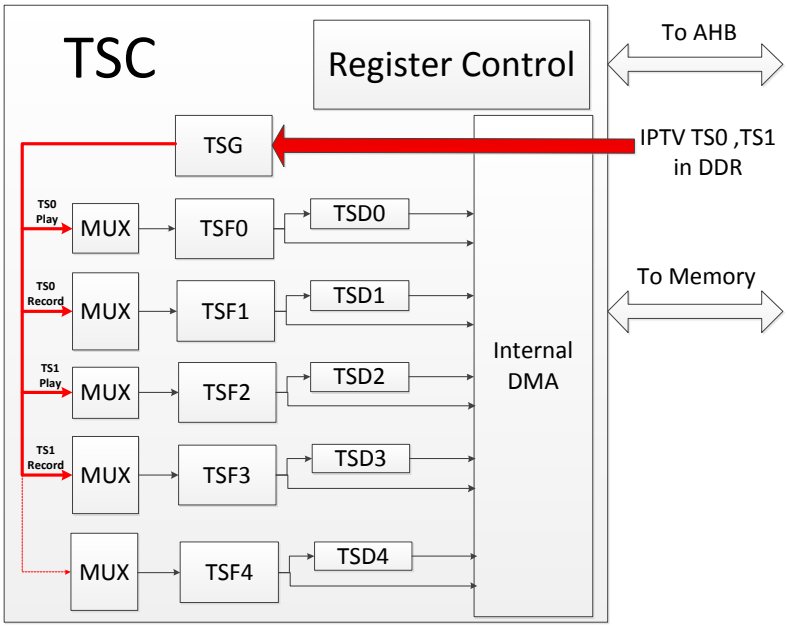


Figure 8-36. Typical Application2 Block Diagram

Application3: 1-port DVB TS, 1-port IPTV TS, recording while playbacking at the same time.

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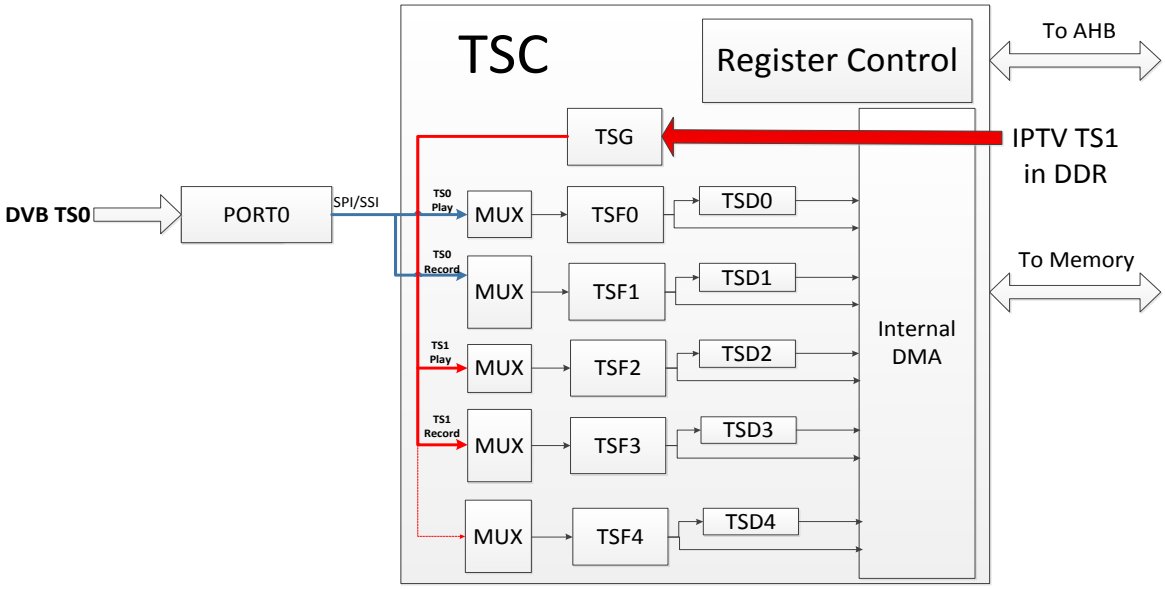


Figure 8-37. Typical Application3 Block Diagram

8.9.4. Programming Guidelines

8.9.4.1. Initialization

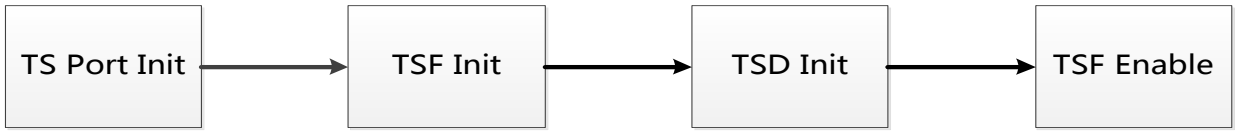


Figure 8-38. TSC Initialization

The PID,DMA ADDR,DMA SIZE,Write Pointer,Read Pointer Register for TSF must clear to 0 first after power-up.

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8.9.4.2. PID Changing

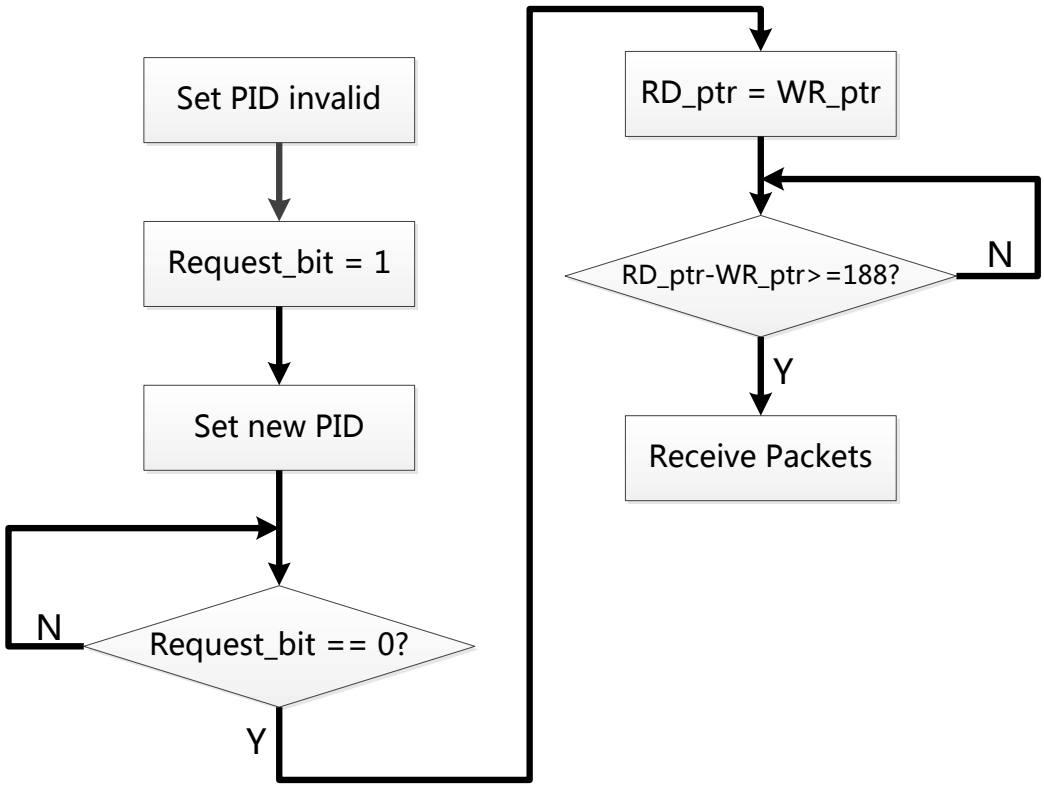


Figure 8-39. PID Changing

Request_bit is the bit8 in TSF Control and Status Register.

8.9.5. Register List

Module Name	Base Address
TSC	0x05060000
TSG	0x05060040
TSF0	0x05060100
TSD0	0x05060180
TSF1	0x05060200
TSD1	0x05060280
TSF2	0x05060300
TSD2	0x05060380
TSF3	0x05060400
TSD3	0x05060480
TSF4	0x05060500
TSD4	0x05060580

Register Name	Offset	Description

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TSC_PCTLR	TSC + 0x10	TSC Port Control Register
TSC_PPARR	TSC + 0x14	TSC Port Parameter Register
TSC_TSFMUXR	TSC + 0x20	TSC TSF Input Multiplex Control Register
TSC_KLAD_INDEX	TSC + 0x28	TSC KLAD Index Register
TSC_IRQ_STATUS	TSC + 0x30	TSC Interrupt Status Register
TSG_CTLR	TSG + 0x00	TSG Control Register
TSG_PPR	TSG + 0x04	TSG Packet Parameter Register
TSG_STAR	TSG + 0x08	TSG Status Register
TSG_CCR	TSG + 0x0C	TSG Clock Control Register
TSG_BBAR	TSG + 0x10	TSG Buffer Base Address Register
TSG_BSZR	TSG + 0x14	TSG Buffer Size Register
TSG_BPR	TSG + 0x18	TSG Buffer Pointer Register
TSF_CTLR	TSF + 0x00	TSF Control Register
TSF_PPR	TSF + 0x04	TSF Packet Parameter Register
TSF_STAR	TSF + 0x08	TSF Status Register
TSF_DIER	TSF + 0x10	TSF DMA Interrupt Enable Register
TSF_OIER	TSF + 0x14	TSF Overlap Interrupt Enable Register
TSF_DISR	TSF + 0x18	TSF DMA Interrupt Status Register
TSF_OISR	TSF + 0x1C	TSF Overlap Interrupt Status Register
TSF_PCRCR	TSF + 0x20	TSF PCR Control Register
TSF_PCRDR	TSF + 0x24	TSF PCR Data Register
TSF_CENR	TSF + 0x30	TSF Channel Enable Register
TSF_CPER	TSF + 0x34	TSF Channel PES Enable Register
TSF_CDER	TSF + 0x38	TSF Channel Descramble Enable Register
TSF_CINDR	TSF + 0x3C	TSF Channel Index Register
TSF_CCTLR	TSF + 0x40	TSF Channel Control Register
TSF_CSTAR	TSF + 0x44	TSF Channel Status Register
TSF_CCWIR	TSF + 0x48	TSF Channel CW Index Register
TSF_CPIDR	TSF + 0x4C	TSF Channel PID Register
TSF_CBBAR	TSF + 0x50	TSF Channel Buffer Base Address Register
TSF_CBSZR	TSF + 0x54	TSF Channel Buffer Size Register
TSF_CBWPR	TSF + 0x58	TSF Channel Buffer Write Pointer Register
TSF_CBRPR	TSF + 0x5C	TSF Channel Buffer Read Pointer Register
TSD_CTLR	TSD + 0x00	TSD Control Register
TSD_CWIR	TSD + 0x1C	TSD Control Word Index Register
TSD_CWR	TSD + 0x20	TSD Control Word Register

8.9.6. Register Description

8.9.6.1. TSC Port Control Register(Default Value: 0x0000_000E)

Offset: 0x10			Register Name: TSC_PCTLR
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:4	/	/	/
3	R/W	0x1	TSInPort3Ctrl TS Input Port3 Control 0 : Reserved 1 : SSI It is not allowed to write 0 to this bit.
2	R/W	0x1	TSInPort2Ctrl TS Input Port2 Control 0 : Reserved 1 : SSI
1	R/W	0x1	TSInPort1Ctrl TS Input Port1 Control 0 : Reserved 1 : SSI It is not allowed to write 0 to this bit.
0	R/W	0x0	TSInPort0Ctrl TS Input Port0 Control 0 : SPI 1 : SSI

8.9.6.2. TSC Port Parameter Register(Default Value: 0x0000_0000)

Offset: 0x14			**Register Name:TSC_PPARR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	TS Input Port3 SSI Data Order 0: MSB first for one byte data 1: LSB first for one byte data
27	R/W	0x0	TS Input Port3 CLOCK Signal Polarity 0 : Rise edge capturing 1: Fall edge capturing
26	R/W	0x0	TS Input Port3 ERROR Signal Polarity 0: High level active 1: Low level active
25	R/W	0x0	TS Input Port3 DVALID Signal Polarity 0: High level active 1: Low level active
24	R/W	0x0	TS Input Port3 PSYNC Signal Polarity 0: High level active 1: Low level active
23:21	/	/	/
20	R/W	0x0	TS Input Port2 SSI Data Order 0: MSB first for one byte data 1: LSB first for one byte data

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19	R/W	0x0	TS Input Port2 CLOCK Signal Polarity 0 : Rise edge capturing 1: Fall edge capturing
18	R/W	0x0	TS Input Port2 ERROR Signal Polarity 0: High level active 1: Low level active
17	R/W	0x0	TS Input Port2 DVALID Signal Polarity 0: High level active 1: Low level active
16	R/W	0x0	TS Input Port2 PSYNC Signal Polarity 0: High level active 1: Low level active
15:13	/	/	/
12	R/W	0x0	TS Input Port1 SSI Data Order 0: MSB first for one byte data 1: LSB first for one byte data
11	R/W	0x0	TS Input Port1 CLOCK Signal Polarity 0 : Rise edge capturing 1: Fall edge capturing
10	R/W	0x0	TS Input Port1 ERROR Signal Polarity 0: High level active 1: Low level active
9	R/W	0x0	TS Input Port1 DVALID Signal Polarity 0: High level active 1: Low level active
8	R/W	0x0	TS Input Port1 PSYNC Signal Polarity 0: High level active 1: Low level active
7:5	/	/	/
4	R/W	0x0	TS Input Port0 SSI Data Order 0: MSB first for one byte data 1: LSB first for one byte data
3	R/W	0x0	TS Input Port0 CLOCK Signal Polarity 0 : Rise edge capturing 1: Fall edge capturing
2	R/W	0x0	TS Input Port0 ERROR Signal Polarity 0: High level active 1: Low level active
1	R/W	0x0	TS Input Port0 DVALID Signal Polarity 0: High level active 1: Low level active
0	R/W	0x0	TS Input Port0 PSYNC Signal Polarity 0: High level active 1: Low level active

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8.9.6.3. TSC TSF Input Multiplex Control Register(Default Value: 0x0000_0000)

Offset: 0x20			Register Name: TSC_TSFMUXR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:16	R/W	0x0	TSF4InputMuxCtrl TSF4 Input Multiplex Control 0000 : Data from TSG 0001 : Data from TS IN Port0 0010 : Data from TS IN Port1 0011 : Data from TS IN Port2 0100 : Data from TS IN Port3 Others : Reserved
15:12	R/W	0x0	TSF3InputMuxCtrl TSF3 Input Multiplex Control 0000 : Data from TSG 0001 : Data from TS IN Port2 0010 : Data from TS IN Port3 Others : Reserved
11:8	R/W	0x0	TSF2InputMuxCtrl TSF2 Input Multiplex Control 0000 : Data from TSG 0001 : Data from TS IN Port2 Others : Reserved
7:4	R/W	0x0	TSF1InputMuxCtrl TSF1 Input Multiplex Control 0000 : Data from TSG 0001 : Data from TS IN Port0 0010 : Data from TS IN Port1 Others : Reserved
3:0	R/W	0x0	TSF0InputMuxCtrl TSF0 Input Multiplex Control 0000 : Data from TSG 0001 : Data from TS IN Port0 Others : Reserved

8.9.6.4. TSC KLAD Index Register(Default Value: 0x0000_000a)

Offset: 0x28			Register Name: TSC_KLAD_INDEX
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:8	R/W	0x0	TSD Index The index of the TSD to setup key. 000 : TSD0 001 : TSD1

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			010 : TSD2 011 : TSD3 100 : TSD4 Others: Reserved
7	/	/	/
6:4	R/W	0x0	Key Index Setup key to write. 000 : Key0 001 : Key1 010 : Key2 011 : Key3 100 : Key4 101 : Key5 110 : Key6 111 : Key7
3:1	/	/	/
0	R/W	0x0	Odd/Even Key Select Select Odd Key or Even Key. 0 : Odd Key 1 : Even Key

8.9.6.5. TSC Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x30			Register Name:TSC_INT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R	0x0	TSG Interrupt Global Status When all TSG interrupt status bits are cleared ,this bit will be cleared by hardware.
15:5	/	/	/
4	R	0x0	TSF4 Interrupt Global Status When all TSF4 interrupt status bits are cleared ,this bit will be cleared by hardware.
3	R	0x0	TSF3 Interrupt Global Status When all TSF3 interrupt status bits are cleared ,this bit will be cleared by hardware.
2	R	0x0	TSF2 Interrupt Global Status When all TSF2 interrupt status bits are cleared ,this bit will be cleared by hardware.
1	R	0x0	TSF1 Interrupt Global Status When all TSF1 interrupt status bits are cleared ,this bit will be cleared by hardware.
0	R	0x0	TSF0 Interrupt Global Status When all TSF0 interrupt status bits are cleared ,this bit will be cleared by

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			hardware.

8.9.6.6. TSG Control and Status Register(Default Value: 0x0000_0000)

Offset: TSG+0x00			Register Name: TSG_CSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R	0x0	TSGSts Status for TS Generator 00: IDLE state 01: Running state 10: PAUSE state Others: Reserved
23:10	/	/	/
9	R/W	0x0	TSGLBufMode Loop Buffer Mode When set to '1', the TSG external buffer is in loop mode.
8	R/W	0x0	TSGSyncByteChkEn Sync Byte Check Enable Enable/ Disable check SYNC byte for receiving new packet 0: Disable 1: Enable If enable check SYNC byte and an error SYNC byte is receiver, TS Generator would come into PAUSE state. If the correspond interrupt is enabled, the interrupt would happen.
7:3	/	/	/
2	R/W	0x0	TSGPauseBit Pause Bit for TS Generator Write '1' to pause TS Generator. TS Generator would stop fetch new data from DRAM. After finishing this operation, this bit will clear to zero by hardware. In PAUSE state, write '1' to resume this state.
1	R/W	0x0	TSGStopBit Stop Bit for TS Generator Write '1' to stop TS Generator. TS Generator would stop fetch new data from DRAM. The data already in its FIFO should be sent to TS filter. After finishing this operation, this bit will clear to zero by hardware.
0	R/W	0x0	TSGStartBit Start Bit for TS Generator Write '1' to start TS Generator. TS Generator would fetch data from DRAM and generate SPI stream to TS filter. This bit will clear to zero by hardware after TS Generator is running.

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8.9.6.7. TSG Packet Parameter Register(Default Value: 0x0047_0000)

Offset: TSG+0x04			Register Name: TSG_PPR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x47	SyncByteVal Sync Byte Value This is the value of sync byte used in the TS Packet.
15:8	/	/	/
7	R/W	0x0	SyncBytePos Sync Byte Position 0: the 1st byte position 1: the 5th byte position This bit is only used for 192 bytes packet size.
6:2	/	/	/
1:0	R/W	0x0	PktSize Packet Size Byte Size for one TS packet 0: 188 bytes Others: Reserved

8.9.6.8. TSG Interrupt Enable and Status Register(Default Value: 0x0000_0000)

Offset: TSG+0x08			Register Name: TSG_IESR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	TSGEndIE TS Generator (TSG) End Interrupt Enable 0: Disable 1: Enable If set this bit, the interrupt would assert to CPU when all data in external DRAM are sent to TS PID filter.
18	R/W	0x0	TSGFFIE TS Generator (TSG) Full Finish Interrupt Enable 0: Disable 1: Enable
17	R/W	0x0	TSGHFIE TS Generator (TSG) Half Finish Interrupt Enable 0: Disable 1: Enable
16	R/W	0x0	TSGErrSyncByteIE TS Generator (TSG) Error Sync Byte Interrupt Enable 0: Disable 1: Enable

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15:4	/	/	/
3	R/W1C	0x0	TSGEndSts TS Generator (TSG) End Status Write '1' to clear.
2	R/W1C	0x0	TSGFFSts TS Generator (TSG) Full Finish Status Write '1' to clear.
1	R/W1C	0x0	TSGHFSts TS Generator (TSG) Half Finish Status Write '1' to clear.
0	R/W1C	0x0	TSGErrSyncByteSts TS Generator (TSG) Error Sync Byte Status Write '1' to clear.

8.9.6.9. TSG Clock Control Register(Default Value: 0x0000_0000)

Offset: TSG+0x0C			Register Name: TSG_CCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	TSGCDF_N TSG Clock Divide Factor (N) The Numerator part of TSG Clock Divisor Factor.
15:0	R/W	0x0	TSGCDF_D TSG Clock Divide Factor (D) The Denominator part of TSG Clock Divisor Factor. Frequency of output clock: Fo = (Fi*(N+1))/(8*(D+1)). Fi is the input special clock of TSC, and D must not less than N.

8.9.6.10. TSG Buffer Base Address Register(Default Value: 0x0000_0000)

Offset: TSG+0x10			Register Name: TSG_BBAR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	RW	0x0	TSGBufBase Buffer Base Address This value is a start address of TSG buffer. This value should be 4-word (16Bytes) align, and the lowest 4-bit of this value should be zero.

8.9.6.11. TSG Buffer Size Register(Default Value: 0x0000_0000)

Offset: TSG+0x14			Register Name:TSG_BSZR
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:24	/	/	/
23:0	R/W	0x0	TSGBufSize Data Buffer Size for TS Generator It is in byte unit. The size should be 4-word (16Bytes) align, and the lowest 4 bits should be zero.

8.9.6.12. TSG Buffer Pointer Register(Default Value: 0x0000_0000)

Offset: TSG+0x18			Register Name: TSG_BPR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R	0x0	TSGBufPtr Data Buffer Pointer for TS Generator Current TS generator data buffer read pointer (in byte unit)

8.9.6.13. TSF Control and Status Register(Default Value: 0x0000_0000)

Offset: TSF+0x00			Register Name: TSF_CSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/WAC	0x0	Channel Change PID Request This bit is used to send a request to hardware for changing the PID of the channel.It will be cleared by hardware when the channel changing finish. Writing '0' has no effect.
7:3	/	/	/
2	R/W	0x0	TSF Enable 00: Disable TSF Input 01: Enable TSF Input
1	/	/	/
0	R/W	0x0	TSFGSRF TSF Global Soft Reset Writing '1' by software will reset all status and state machine of TSF. And it is cleared by hardware after finish reset. Writing '0' by software has no effect.

8.9.6.14. TSF Packet Parameter Register(Default Value: 0x0047_0000)

Offset: TSF+0x04			Register Name: TSF_PPR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	LostSyncThd Lost Sync Packet Threshold

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			It is used for packet sync lost by checking the value of sync byte.
27:24	R/W	0x0	SyncThd Sync Packet Threshold It is used for packet sync by checking the value of sync byte.
23:16	R/W	0x47	SyncByteVal Sync Byte Value This is the value of sync byte used in the TS Packet.
15:10	/	/	/
9:8	R/W	0x0	SyncMthd Packet Sync Method 00: By PSYNC signal 01: By sync byte 10: By both PSYNC and Sync Byte 11: Reserved
7	R/W	0x0	SyncBytePos Sync Byte Position 0: the 1st byte position 1: the 5th byte position This bit is only used for 192 bytes packet size.
6:2	/	/	/
1:0	R/W	0x0	PktSize Packet Size Byte Size for one TS packet 00: 188 bytes 01: 192 bytes 10: 204 bytes 11: Reserved

8.9.6.15. TSF Interrupt Enable and Status Register(Default Value: 0x0000_0000)

Offset: TSF+0x08			Register Name: TSF_IESR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	TSFFOIE TS PID Filter (TSF) Internal FIFO Overrun Interrupt Enable 0: Disable 1: Enable
18	R/W	0x0	TSFPPDIE TS PCR Packet Detect Interrupt Enable 0: Disable 1: Enable
17	R/W	0x0	TSFCOIE TS PID Filter (TSF) Channel Overlap Interrupt Global Enable 0: Disable

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			1: Enable
16	R/W	0x0	TSFCDIE TS PID Filter (TSF) Channel DMA Interrupt Global Enable 0: Disable 1: Enable
15:4	/	/	/
3	R/W1C	0x0	TSFFOIS TS PID Filter (TSF) Internal FIFO Overrun Status Write '1' to clear.
2	R/W1C	0x0	TSFPPDIS TS PCR Packet Found Status When it is '1', one TS PCR Packet is found. Write '1' to clear.
1	R	0x0	TSFCOIS TS PID Filter (TSF) Channel Overlap Status It is global status for 32 channel. It would clear to zero after all channels status bits are cleared.
0	R	0x0	TSFCDIS TS PID Filter (TSF) Channel DMA Status It is global status for 32 channel. It would clear to zero after all channels status bits are cleared.

8.9.6.16. TSF DMA Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: TSF+0x10			Register Name: TSF_DIER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DMAIE DMA Interrupt Enable DMA interrupt enable bits for channel 0~31.

8.9.6.17. TSF Overlap Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: TSF+0x14			Register Name: TSF_OIER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	OLPIE Overlap Interrupt Enable Overlap interrupt enable bits for channel 0~31.

8.9.6.18. TSF DMA Interrupt Status Register(Default Value: 0x0000_0000)

Offset: TSF+0x18			Register Name: TSF_DISR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W1C	0x0	DMAIS

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			DMA Interrupt Status DMA interrupt Status bits for channel 0~31. Set by hardware, and can be cleared by software writing '1'. When both these bits and the corresponding DMA Interrupt Enable bits set, the TSF interrupt will generate.

8.9.6.19. TSF Overlap Interrupt Status Register(Default Value: 0x0000_0000)

Offset: TSF+0x1C			Register Name: TSF_OISR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W1C	0x0	OLPIS Overlap Interrupt Status Overlap interrupt Status bits for channel 0~31. Set by hardware, and can be cleared by software writing '1'. When both these bits and the corresponding Overlap Interrupt Enable bits set, the TSF interrupt will generate.

8.9.6.20. TSF PCR Control Register(Default Value: 0x0000_0000)

Offset: TSF+0x20			Register Name: TSF_PCRCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	PCRDE PCR Detecting Enable 0: Disable 1: Enable
15:13	/	/	/
12:8	R/W	0x0	PCRCIND Channel Index m for Detecting PCR packet (m from 0 to 31)
7:1	/	/	/
0	R	0x0	PCRLSB PCR Contest LSB 1 bit--PCR[0].

8.9.6.21. TSF PCR Data Register(Default Value: 0x0000_0000)

Offset: TSF+0x24			Register Name: TSF_PCRDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PCRMSB PCR Data High 32 bits--PCR[33:1].

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8.9.6.22. TSF Channel Enable Register(Default Value: 0x0000_0000)

Offset: TSF+0x30			Register Name: TSF_CENR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	FilterEn Filter Enable for Channel 0~31 0: Disable 1: Enable From Disable to Enable, internal status of the corresponding filter channel will be reset.

8.9.6.23. TSF Channel PES Enable Register(Default Value: 0x0000_0000)

Offset: TSF+0x34			Register Name: TSF_CPER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	PESEn PES Packet Enable for Channel 0~31 0: Disable 1: Enable These bits should not be changed during the corresponding channel enable.

8.9.6.24. TSF Channel Descramble Enable Register(Default Value: 0x0000_0000)

Offset: TSF+0x38			Register Name: TSF_CDER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DescEn Descramble Enable for Channel 0~31 0: Disable 1: Enable These bits should not be changed during the corresponding channel enable.

8.9.6.25. TSF Channel Index Register(Default Value: 0x0000_0000)

Offset: TSF+0x3C			Register Name: TSF_CINDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4:0	R/W	0x0	CHIND Channel Index This value is the channel index for channel private registers access. Range is from 0x00 to 0x1f. Address range of channel private registers is 0x40~0x7f.

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8.9.6.26. TSF Channel CW Index Register(Default Value: 0x0000_0000)

Offset: TSF+0x48			Register Name: TSF_CCWIR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	CWIND Related Control Word Index Index to the control word used by this channel when Descramble Enable of this channel enable. This value is useless when the corresponding Descramble Enable is '0'.

8.9.6.27. TSF Channel PID Register(Default Value: 0x1FFF_0000)

Offset: TSF+0x4C			Register Name: TSF_CPIDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x1fff	PIDMSK Filter PID Mask for Channel
15:0	R/W	0x0	PIDVAL Filter PID value for Channel

8.9.6.28. TSF Channel Buffer Base Address Register(Default Value: 0x0000_0000)

Offset: TSF+0x50			Register Name: TSF_CBBAR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TSFBufBAddr Data Buffer Base Address for Channel It is 4-word (16Bytes) align address. The LSB four bits should be zero.

8.9.6.29. TSF Channel Buffer Size Register(Default Value: 0x0000_0000)

Offset: TSF+0x54			Register Name: TSF_CBSZR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	CHDMAIntThd DMA Interrupt Threshold for Channel The unit is TS packet size. When received packet (has also stored in DRAM) size is beyond (>=) threshold value, the corresponding channel interrupt is generated to CPU. TSC should count the new received packet again, when exceed the specified threshold value, one new interrupt is generated again. 00: 1/2 data buffer packet size 01: 1/4 data buffer packet size 10: 1/8 data buffer packet size

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			11: 1/16 data buffer packet size
23:21	/	/	/
20:0	R/W	0x0	CHBufPktSz Data Buffer Packet Size for Channel The exact buffer size of buffer is N+1 bytes. The maximum buffer size is 2MB. This size should be 4-word (16Bytes) aligned. The LSB four bits should be zero.

8.9.6.30. TSF Channel Buffer Write Pointer Register(Default Value: 0x0000_0000)

Offset: TSF+0x58			Register Name: TSF_CBWPR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:0	R/W	0x0	BufWrPtr Data Buffer Write Pointer (in Bytes) This value is changed by hardware, when data is filled into buffer, this pointer is increased. And this pointer can be set by software, but it should not be changed by software during the corresponding channel is enable.

8.9.6.31. TSF Channel Buffer Read Pointer Register(Default Value: 0x0000_0000)

Offset: TSF+0x5C			Register Name: TSF_CBRPR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:0	R/W	0x0	BufRdPtr Data Buffer Read Pointer (in Bytes) This pointer should be changed by software after the data of buffer is readed.

8.9.6.32. TSD Control Register(Default Value: 0x0000_0000)

Offset: TSD+0x00			Register Name: TSD_CTLR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	TS Descramble Flag Clear 0: Clear 1: Not clear
15:2	/	/	/
1:0	R/W	0x0	DescArith Descramble Arithmetic 00: DVB CSA V1.1 01: DVB CSA V2.1

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			Others: Reserved

8.9.6.33. TSD Control Word Index Register(Default Value: 0x0000_0000)

Offset: TSD+0x1C			Register Name: TSD_CWIR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	CWI Control Word Index This value is the Control index for Control word access. Range is from 0x00 to 0x7.
3:0	R/W	0x0	CWII Control Word Internal Index 0000 : Odd Control Word 1ST 32-bit, OCW[31:0]; 0001 : Odd Control Word 2ND 32-bit, OCW[63:32]; 0010 : Odd Control Word 3TH 32-bit, OCW[95:64]; 0011 : Odd Control Word 4TH 32-bit, OCW[127:96]; 0100 : Even Control Word 1ST 32-bit, ECW[31:0]; 0101 : Even Control Word 2ND 32-bit, ECW[63:32]; 0110 : Even Control Word 3TH 32-bit, ECW[95:64]; 0111 : Even Control Word 4TH 32-bit, ECW[127:96];

8.9.6.34. TSD Control Word Register(Default Value: 0x0000_0000)

Offset: TSD+0x20			Register Name: TSD_CWR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CWD Content of Control Word corresponding to the TSD_CWIR value

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8.10. One Wire Interface

8.10.1. Overview

The One Wire Interface implements the hardware protocol of the Master function of the 1-Wire protocol, which uses a single wire for communication between the Master (1-Wire controller) and the Slaves (1-Wire external compliant devices).

The One Wire Interface is implemented as an open-drain output at the device level. Therefore, an external pull-up resistance is required and protocol use the return-to-1 mechanism (that is, after any command by any of the connected devices, the line is pulled to a logical high level).

The One Wire Interface can work at Simple mode or Standard mode at one time.

Features:

- Hardware implement of 1-Wire protocol
- Supports master function
- Supports Simple mode and Standard mode

8.10.2. Block Diagram

The block diagram of the One Wire Interface is shown below.

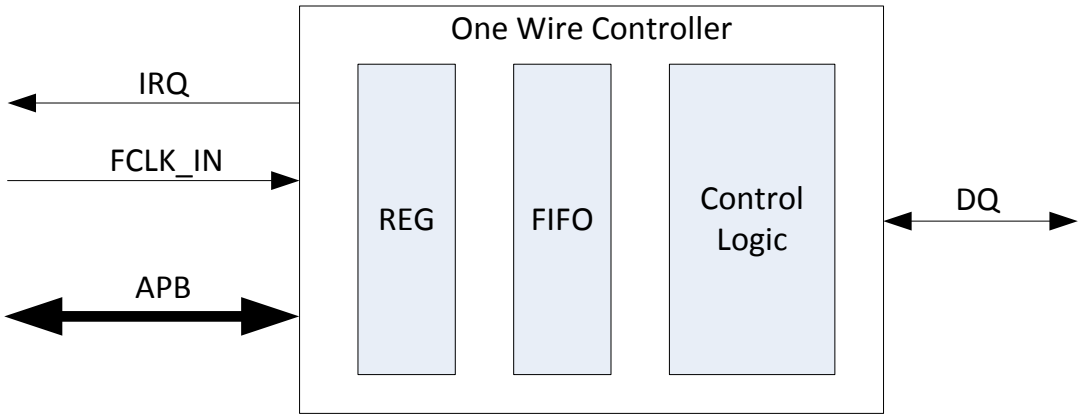


Figure 8-40. One Wire Interface Block Diagram

8.10.3. Operations and Functional Descriptions

8.10.3.1. External Signals

Table 8-23 describes the external signals of One Wire Interface.

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Table 8-23. One Wire Interface External Signals

Signal Name	Description	Type
S_OWC	Data In/Out of One Wire Interface	I/O

8.10.3.2. Clock and Reset

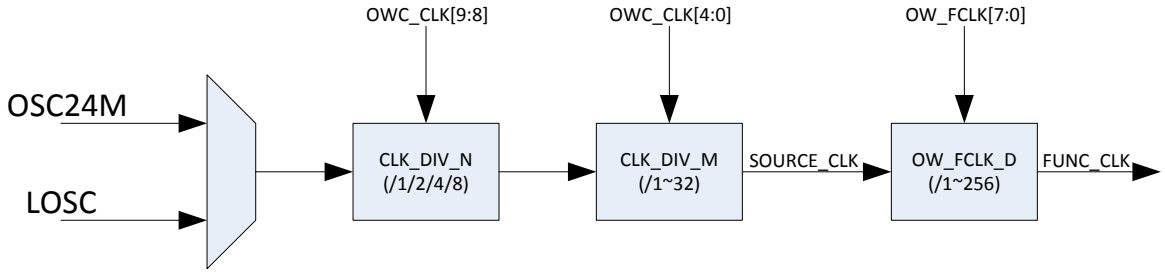


Figure 8-41. One Wire Interface Clock Description

8.10.3.3. Typical Application

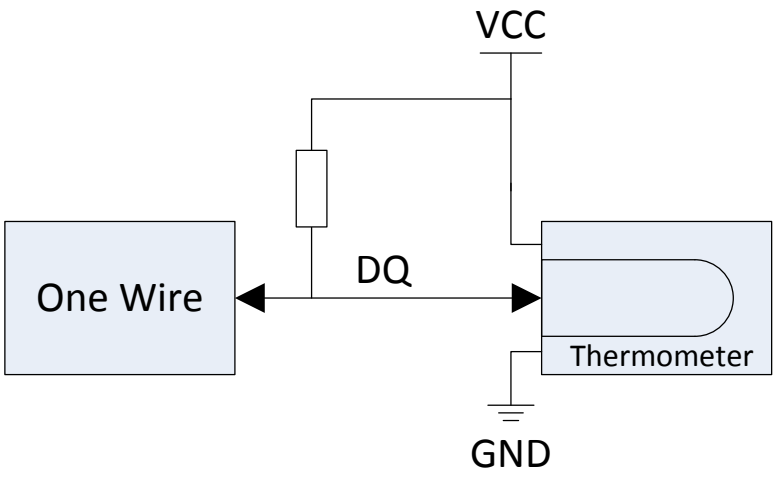


Figure 8-42. Typical Application

8.10.3.4. Function Implementation

8.10.3.4.1. Simple Mode

The bus of Simple Mode is a master-slave bus system using a simple one-wire, asynchronous, bi-directional, serial interface with a maximum bit-rate of about 5 Kbit/s.

It is a command-based protocol in which the host sends a command byte to the slave. The command directs the slave

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either to store the next eight bits of data received to a register specified by the command byte (Write command), or to output the eight bits of data from a register specified by the command byte (Read command). Command and data bytes consist of a stream of bits where the least-significant bit of a command or data byte is transmitted first. The first 7 bits of the command word are the register address and the last command bit transmitted is the read/write (R/W) bit. The following figure illustrates a typical read cycle.

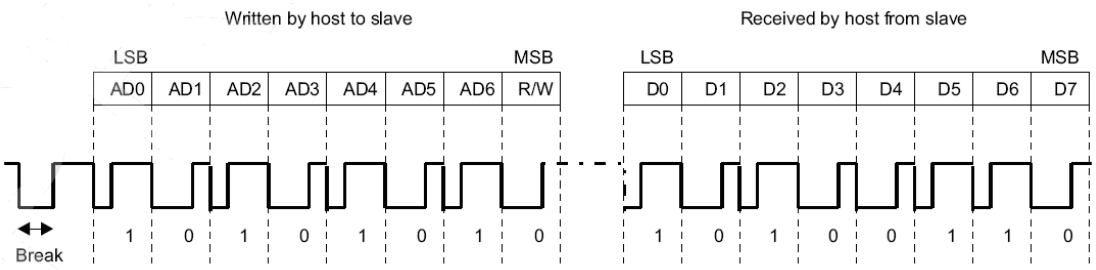


Figure 8-43. Typical Read Cycle

In the figure, the 1 of the R/W bit indicates a write command where the 0 indicates the read command.

In Simple mode, the slave can be reset by using the break pulse. If the host does not get an expected response from the slave or if the host needs to restart a communication before it is complete, the host can hold the line low and generate a break to reset the communication engine. The Break timing is illustrated as follow.

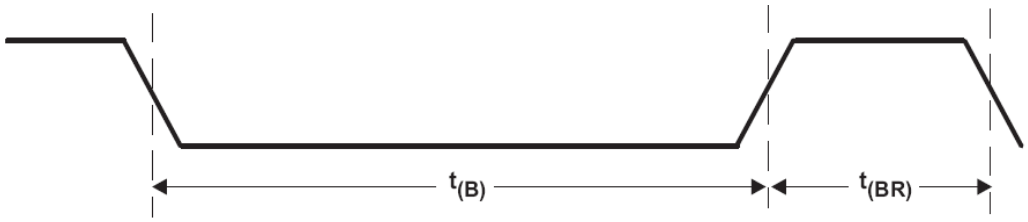


Figure 8-44. Break Timing

Table 8-24. Break Timing Parameters

Timing Parameter	For Device	Minimum	Maximum
t(B)	All	190us	
t(BR)	All	40us	

It is not required, but it is recommended to precede each communication with a break for the reliable communication.

After a successful break pulse (if have), the host and slave are ready for bit transmission. Each bit to transmit (either from the host to the slave or from the slave to the host) is preceded by a low-going edge on the line.

The host transmitted bit timing is shown as follow.

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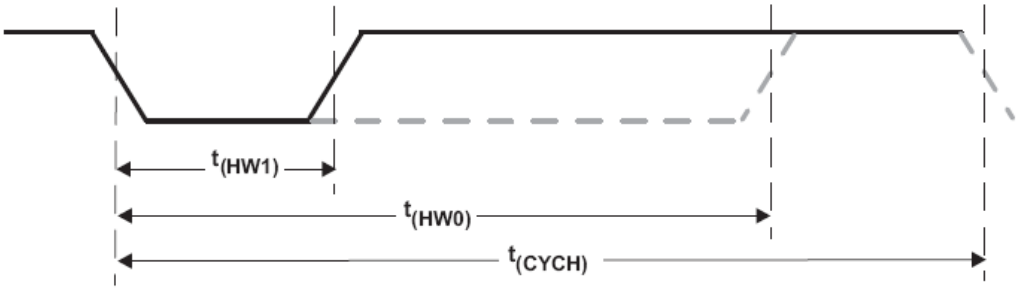


Figure 8-45. Host Bit Timing

And the slave transmitted bit timing is shown as follow.

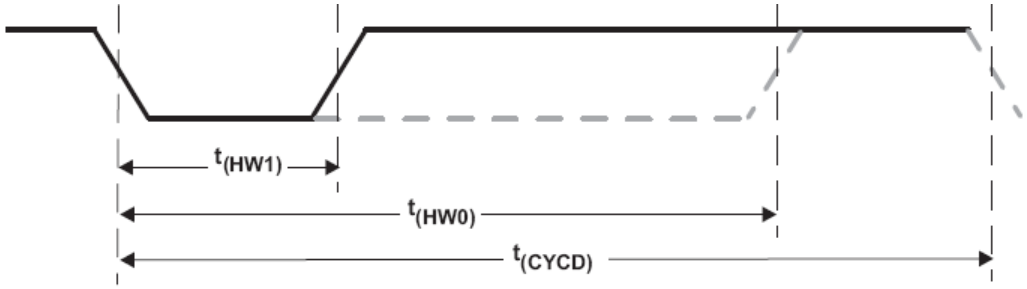


Figure 8-46. Slave Bit Timing

After the last bit of address is sent on a read cycle, the slave starts outputting the data after the specified response time, t(RSPS). The response time is measured from the fall time of the command R/W bit to the fall time of the first data bit returned by the slave and therefore includes the entire bit time for the R/W bit. Because the minimum response time equal to the minimum bit cycle time, this means that the first data bit may begin as soon as the command R/W bit time ends. The timing is shown as follow.

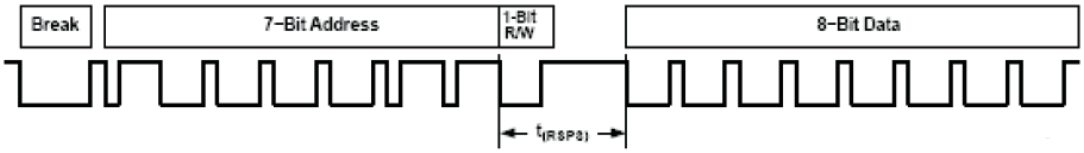


Figure 8-47. t(RSPS) Requirement

Table 8-25.Response Time Parameters

Timing Parameter	For Device	Minimum	Maximum
t(RSPS)	All	190us	320us

Also, to avoid short noise spike coupled onto the HDQ line, some filtering may be prudent.

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8.10.3.4.2. Standard Mode

The Standard Mode consists of 4 types of signaling on the data line, which are Initialization Sequence, Write Zero, Write One and Read Data.

The host first sends an initialization pulse and then waits for the slave to respond with a presence pulse before enabling any communication sequence. The initialization pulse and presence pulse are shown as follow.

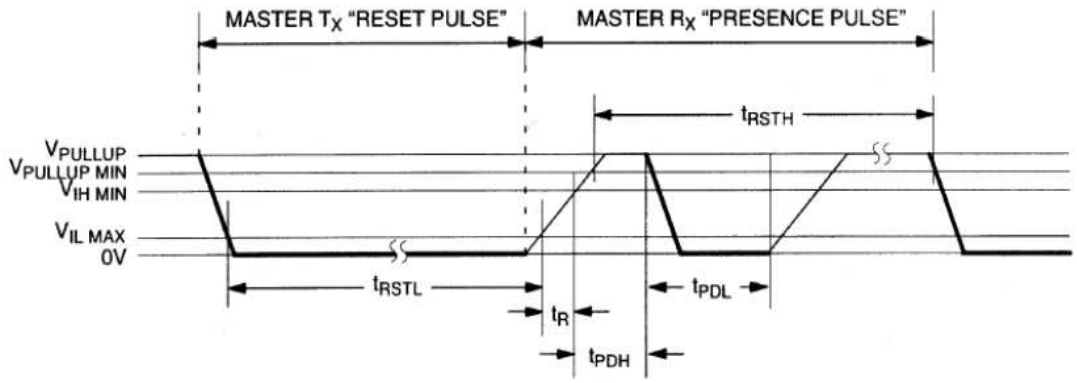


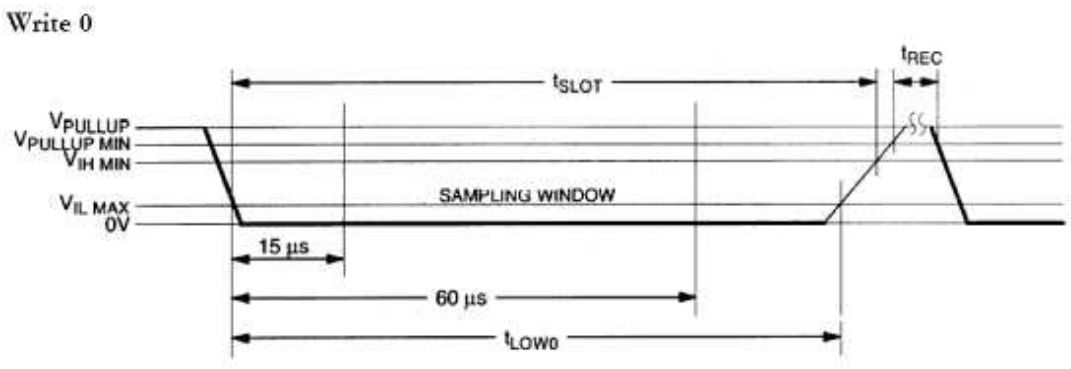
Figure 8-48. Initialization Pulse and Presence Pulse

Table 8-26. Initialization Pulse and Presence Pulse Timing Parameters

Timing Parameter	Minimum	Maximum
t(RSTL)	480us	
t(RSTH)	480us	
t(PDH)	15us	60us
t(PDL)	60us	240us

The other two types of signaling are Writing Zero and Writing One. The both write time slots must be a minimum of 60us in duration with a minimum of a 1us recovery time between individual write cycles. The slave device sample the data line in a window of 15us to 60us after the data line falls. If the line is high, a Write One occurs. If the line is low, a Write Zero occurs.

The Write Zero time slot is shown as follow.



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Figure 8-49. Write 0 Time Slot

Table 8-27. Write 0 Time Slot Timing Parameters

Timing Parameter	Minimum	Maximum
T(LOW0)	60us	t(SLOT)
t(SLOT)	T(LOW0)	120 us
t(REC)	1us	

When Write One occurs, the data line must be pulled to a logic low level and then released, allowing the data line to pull up to a high level within 15us after the start of the write time slot. The Write One time slot is shown as follow.

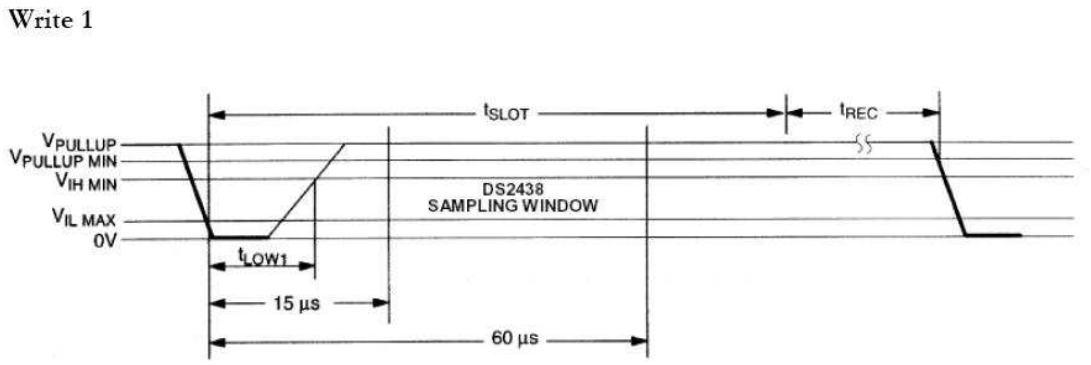


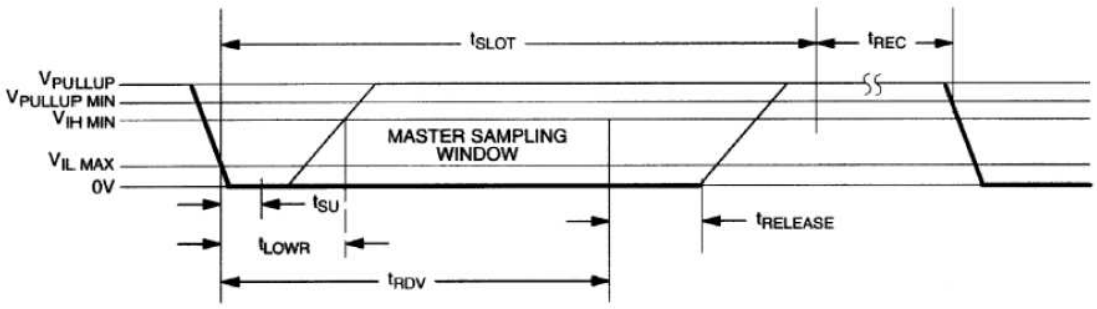
Figure 8-50. Write 1 Time Slot

Table 8-28. Write 1 Time Slot Timing Parameters

Timing Parameter	Minimum	Maximum
t(SLOT)	60us	120 us
t(LOW1)	1us	15us
t(REC)	1us	

The last signaling type is Read Data. A read time slot is initiated when the bus master pulls the data line from a logic high level to logic low level. The data line must remain at a low logic level for a minimum of 1 us; output data from the slave is then valid within the next 14 us maximum.

The bus master therefore must stop driving the data line low in order to read its state 15 us from the start of the read slot. All read time slots must be a minimum of 60us in duration with a minimum of a 1 us recovery time between individual read slots. The Read Data slot is shown as follow.



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Figure 8-51. Read Data Slot

Table 8-29. Read Data Slot Timing Parameters

Timing Parameter	Minimum	Maximum
t(SU)		1us
t(LOWR)	1us	15us
t(RDV)	(= 15us)	
t(RELEASE)	0us	45us
t(SLOT)	60 us	120 us
t(REC)	1us	

Cyclic Redundancy Check (CRC) is used by One Wire devices to ensure data integrity. Two different CRC are commonly found in Standard Mode. There are one 8 bit CRC and one 16 bit CRC. CRC8 is used in the ROM section of all devices. CRC8 is also in some devices used to verify other data, like commands issued on the bus. CRC16 is used by some devices to check for errors on larger data sets.

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8.10.4. Programming Guidlines

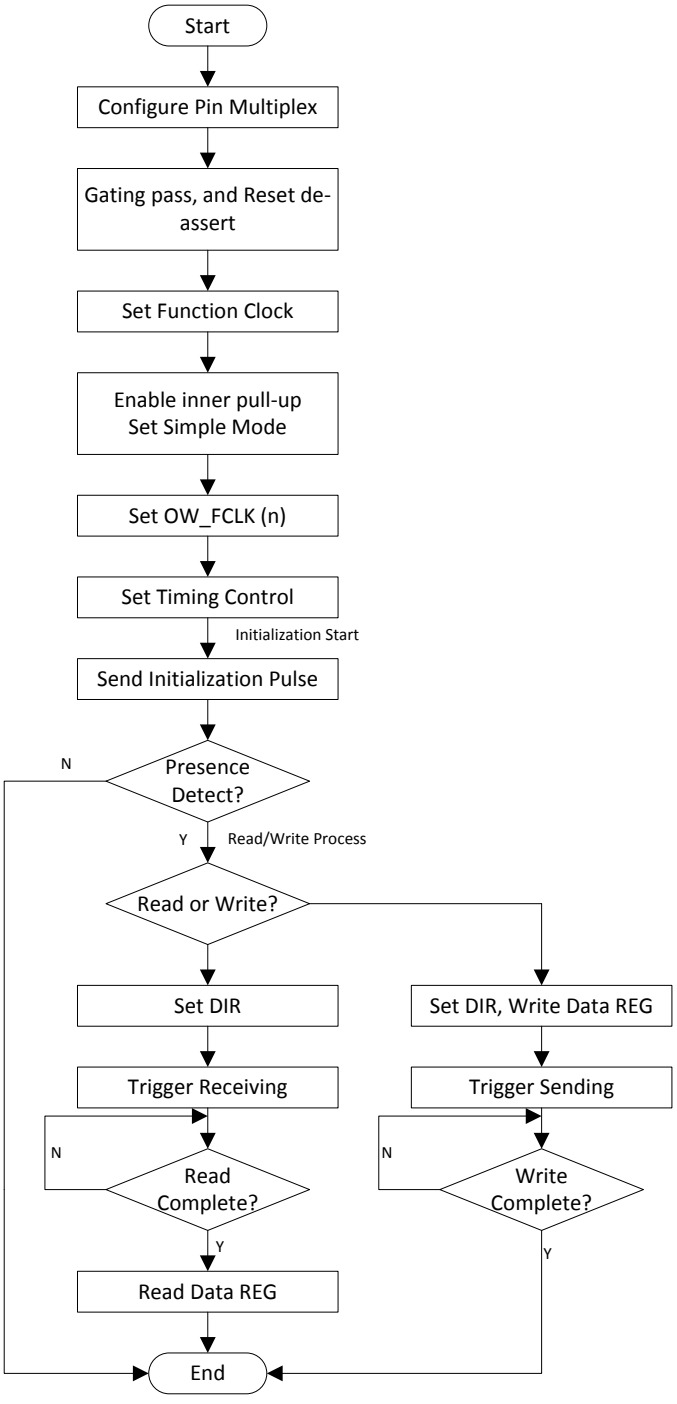


Figure 8-52. One Wire Interface Write/Read Process

8.10.5. Register List

Module Name	Base Address
R_OWC	0x07040400

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Register Name	Offset	Description
OW_DATA	0x0000	One Wire Data Register
OW_CTL	0x0004	One Wire Control Register
OW_SMSC	0x0008	One Wire Standard Mode Special Control Register
OW_SMCRC	0x000C	One Wire Standard Mode CRC Register
OW_INT_STATUS	0x0010	One Wire Interrupt Status Register
OW_INT_MASK	0x0014	One Wire Interrupt Mask Register
OW_FCLK	0x0018	One Wire Function Clock Register
OW_LC	0x001C	One Wire Line Control Register
SM_WR_RD_TCTL	0x0020	Standard Mode Write Read Timing Control Register
SM_RST_PRESENCE_TCTL	0x0024	Standard Mode Reset Presence Timing Control Register
SP_WR_RD_TCTL	0x0028	Simple Mode Timing Control Register
SP_BR_TCTL	0x002C	Simple Mode Break Timing Control Register

8.10.6. Register Description

8.10.6.1. One Wire Data Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: OW_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	SM_DATA These fields are for Simple Mode data send or receive in a one wire transmission. After this byte data transfer finishing, a transmission complete interrupt will generate.
15:8	/	/	/
7:0	R/W	0x0	OW_DATA Data byte for transmitting or received In Simple Mode mode, these fields are for the command byte transmission. When GO bit is set (the INITIALIZATION/BREAK bit is not set at the same time), these fields will be sent as the address and command for a Simple Mode transfer. After the command byte transmission finished, the controller in Simple Mode will send next 8 bit data from SM_DATA when the DIR bit is 1 or receive one byte data to SM_DATA when the DIR bit is 0. In Standard Mode, if the INITIALIZATION/BREAK bit is not set, the controller samples/sends data to/from these fields determining by the DIR bit when the Go bit is set. When the ONE_WIRE_SINGLE_BIT is enabled, only the first bit of these fields is available.

8.10.6.2. One Wire Control Register (Default Value: 0x0003_0000)

Offset: 0x0004			Register Name: OW_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:24	/	/	/
23:20	/	/	/
19:16	R/W	0x3	SAMPLE_TIME These fields determine the sample times in digital circuit.
15:10	/	/	/
9	R/W	0x0	INNER_PULL_UP_ENABLE When this bit is set, the inner pull up for one wire bus is determined by inner output (pull up is off when bus is drive 0) 0: inner pull up is on 1: inner pull up is off when bus is drive 0
8	R/W	0x0	AUTOIDLE Auto Idle 0: Module clock is free-running 1: Module clock is in power saving mode: the function clock is running only when module is accessed or inside logic is in function to process events.
7	/	/	/
6	R	0x0	PRESENCEDETECT Slave Presence Indicator This read-only flag is only used in Standard Mode The value of this field indicates whether there is Presence Pulse responding to the host initialization pulse. The flag is updated when the OW_INT_STATUS[0] Presence Detect Interrupt Flag is set.
5	R/W	0x0	STANDARD_MODE_SINGLE_BIT The single-bit mode is only supported for Standard Mode. After the bit is transferred, Tx-complete or Rx-complete interrupt will generate for corresponding transfer operation. 0: Disabled 1: Enabled
4	R/W	0x0	Go Go Bit Write 1 to start the appropriate operation. If the INITIALIZATION/BREAK bit is set, the controller generates the initialization or break pulse. If the INITIALIZATION/BREAK bit is not set, the controller in Standard Mode samples/sends data to/from the OW_DATA fields determining by the DIR bit, or controller in Simple Mode begins a transfer sequence with the command byte in OW_DATA. Bit returns to 0 after the operation is complete.
3	R/W	0x0	INITIALIZATION/BREAK Initialization/Break Bit Write 1 to send initialization pulse for the Standard Mode or break pulse for the Simple Mode. The OW_DATA register will be flushed when initialization or the break situation is generating. Bit returns to 0 after pulse is sent. The pulse generates after the Go bit is set.
2	R/W	0x0	DIR

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			Direction Bit In Standard Mode, this field determines if next operation (byte operation or bit operation) is read or write. In Simple Mode, this field determines if the current transfer sequence is read or write. 0 = read 1 = write The operation starts after the Go bit is set.
1	R/W	0x0	MS Mode Selection Bit 0: Standard Mode 1: Simple Mode
0	R/W	0x0	GEN Global Enable This field is used to enable or disable the One Wire Controller. A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable

8.10.6.3. One Wire Standard Mode Special Control Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: OW_SMSC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:6	/	/	/
5	R/W	0x0	CRC_ERROR_STATUS These fields indicate the result of the CRC comparing. 0: CRC comparing right 1: CRC comparing wrong
4	/	/	/
3	R/W	0x0	MEM_CRC_COMPARE This field is only used in Standard Mode. When this field is set, the controller will compare the value in the CRC_RECEV field with the data read from the CRC_CALC_INDICATE field, and then returns corresponding result in the CRC_ERROR_STATUS field and generates CRC finish interrupt. The CRC shift register and CRC_CALC_INDICATE field will be cleaned to 0 then. This field will be automatically cleaned when the CRC compare is finish.
2	R/W	0x0	CRC_16BIT_EN This field is only used in Standard Mode. and is set to 1 to select 16bit CRC, else the 8bit CRC is select. 0: CRC_8BIT_EN 1: CRC_16BIT_EN
1	R/W	0x0	WR_MEM_CRC_REQ This field is only used in One Wire mode. When this bit is set, the bit send to

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			the device will be took into calculate the CRC value (CRC8 or CRC16). The calculation will stop when this bit is cleaned. The value will be preserved in the corresponding CRC (CRC8 or CRC16) shift register then.
0	R/W	0x0	RD_MEM_CRC_REQ This field is only used in Standard Mode. When this bit is set, the bit received from the device will be took into calculate the CRC value (CRC8 or CRC16). The calculation will stop when this bit is cleaned. The value will be preserved in the corresponding CRC (CRC8 or CRC16) shift register then.

8.10.6.4. One Wire Standard Mode CRC Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: OW_SMCRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R	0x0	CRC_CALC_INDICATE This field indicates the CRC value calculated by the CRC shift register.
15:0	R/W	0x0	CRC_RECEV The data CRC value (CRC8 or CRC16) will be written to these fields by software for CRC comparing.

8.10.6.5. One Wire Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: OW_INT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W1C	0x0	Deglitch Detected Interrupt Flag This flag indicates a deglitch in the bus. The controller looks for any glitch in the sample window for at least 1us. If the Deglitch Interrupt is enabled, an interrupt will issue when any deglitch occurs in the bus. The interrupt condition is cleared by writing “1” to this field.
4	R/W1C	0x0	CRC Comparing Complete Interrupt Flag This flag is used in Standard Mode., and is used to indicate the CRC comparing has finished. The interrupt condition is cleared by writing “1” to this field.
3	R/W1C	0x0	Transmission Complete Interrupt Flag In Standard Mode., the flag is set when a write operation of one byte or one bit in single-bit mode was completed. The interrupt is generated then. In Simple Mode., the flag is set when a write operation of one byte was completed. The interrupt is also generated. The interrupt condition is cleared by writing “1” to this field.
2	R/W1C	0x0	Read Complete Interrupt Flag In Standard Mode., the flag is set when a byte or a bit in single-bit mode has been successfully read. The interrupt is generated then. In Simple Mode. the flag is set when a byte has been successfully read. The

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			interrupt is also generated then. The interrupt condition is cleared by writing “1” to this field.
1	R/W1C	0x0	Time-out Interrupt Flag This flag is only used in Simple Mode. The flag is set when two event happened. The one event is that after a read command initiated by the host, the slave did not pull the line low within the specified time (512 us). The other event is that another bit transfer does not begin after a specified time (512 us) from the pre-bit beginning. When the above situation occurs, the interrupt generates and the value of this field is set. The interrupt condition is cleared by writing “1” to this field.
0	R/W1C	0x0	Presence Detect Interrupt Flag In Standard Mode., this interrupt status is set when the Initialization Pulse is completed. The interrupt is generated then and the PRESENCEDETECT bit is update. In Simple Mode., the flag is set when the successful completion of a break pulse. The interrupt is also generated then. The interrupt condition is cleared by writing “1” to this field.

8.10.6.6. One Wire Interrupt Mask Register(Default Value: 0x0000_0000)

Offset: 0x0014			**Register Name: OW_INT_MASK**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W	0x0	Deglitch Detected Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	CRC Comparing Complete Interrupt Enable 0: Disable 1: Enable
3	R/W	0x0	Transmission Complete Interrupt Enable 0: Disable 1: Enable
2	R/W	0x0	Read Complete Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	Time-out Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	Presence Detect Interrupt Enable 0: Disable 1: Enable

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8.10.6.7. HDQ/One Wire Function Clock Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: OW_FCLK
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x0	OW_FCLK (n) n-MHz clock is needed to use as a time reference by the machine. Transitions between the states of the state machine as well as actions triggered at precise time deadlines are expressed using the n – MHz clock.
15:8	/	/	/
7:0	R/W	0x0	OW_FCLK_D OW_FCLK = SOURCE_CLK/OW_FCLK_D

8.10.6.8. One Wire Line Control Register(Default Value: 0x0000_0004)

Offset: 0x001C			Register Name: OW_LC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R	0x1	Current state of One Wire Line 0: low 1: high
1	R/W	0x0	One Wire line state control bit When the line control mode is enabled (bit [0] set), value of this bit decides the output level of the One Wire line. 0: output low level 1: output high level
0	R/W	0x0	One Wire line state control enable When this bit is set, the state of One Wire line is control by the value of bit [1]. 0: disable line control mode 1: enable line control mode

8.10.6.9. Standard Mode Write Read Timing Control Register(Default Value: 0x213D_E0BC)

Offset: 0x0020			Register Name: OW_SMSC
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:29	R/W	0x1	TSU Read Data Setup. In standard speed, range: t(SU) < 1 00: 0.5us 01: 1us 10: 2us 11: 4us

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28	/	/	/
27:24	R/W	0x1	REC Recovery Time, t(recovery) = N us. In standard speed, range: 1us <= t(recovery)
23	/	/	/
22:18	R/W	0xf	TRDV Read data valid time, t(rdv) = N us. In standard speed, range: Exactly 15
17:11	R/W	0x3c	TLOW0 Write Zero time Low, Tlow0 = N us. The range setting for TLOW0 is from 0x3c to 0x77. In standard mode, range:60<= t(low0) < t(tslot) <120
10:7	R/W	0x1	TLOW1 Write One time Low, or TLOWR both are same. t(low1) = N us. The range setting for TLOW1 and TLOWR here is from 0x1 to 0xf. In standard speed, range:1 <= t(low1) < 15. t(lowR) = N owr clks. In standard speed, rang = 1 <= t(lowR) <15
6:0	R/W	0x3c	TSLOT Active time slot for write and read data, t(slot) = N us. The range setting for TSLOT is from 0x3c to 0x78. In standard mode, range:60 <= t(slot) <120

8.10.6.10. Standard Mode Reset Presence Timing Control Register(Default Value: 0x3C3F_C1E0)

Offset: 0x0024			Register Name: SM_RST_PRESENCE_TCTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x3c	TPDL PRESENCE_DETECT_LOW t(pdl) = N us. The range setting for TPDL in these fields is from 0 to 0xf0. In standard speed, Range: 60 <= t(pdl) <240.
23:18	R/W	0xf	TPDH PRESENCE_DETECT_HIGH t(pdh) = N us. The range setting for TPDH in these fields is from 0xf to 0x3c. In standard speed, range: 15 <= t(pdh) < 60 .
17:9	R/W	0x1e0	TRSTL RESET_TIME_LOW t(rstl) = N us. The range setting for TRSTL in these fields is from 0 to 0xff. In standard speed, Range: 480 <= t(rstl) < infinity
8:0	R/W	0x1e0	TRSTH RESET_TIME_HIGH, t(rsth) = N us. The range setting for TRSTH in these fields is from 0 to 0xff. In standard speed, Range : 480 <= t(rsth) < infinity

8.10.6.11. Simple Mode Write Read Timing Control Register(Default Value: 0x0A01_58BE)

Offset: 0x0028			Register Name: SP_WR_RD_TCTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	RD_SAMPLE_POINT When controller of the Simple Mode read, the default sample point is at the middle of the THW1 point and the THW0 point, named S(middle). When

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			these fields are set, the corresponding new sample point will be determined. 0000 S(middle) 1000 S(middle)-30us 0001 S(middle)+5us 1001 S(middle)+40us 0010 S(middle)-5us 1010 S(middle)-40us 0011 S(middle)+10us 1011 S(middle)+50us 0100 S(middle)-10us 1100 S(middle)-50us 0101 S(middle)+20us 1101 S(middle)+60us 0110 S(middle)-20us 1110 S(middle)-60us 0111 S(middle)+30us 1111 reserve
27:22	R/W	0x28	THW1_INT t(HW1_INT) = N us. The range setting for THW1_INT in these fields is from 0 to 0x3f, which is the integer part of the THW1. In HDQ mode, Range: t(HW0) <= 50 us.
21:18	R/W	0x0	THW1_DEC THW1_DEC is the decimal part of the THW1. t(HW1_DEC) = N ow_clks. The value for the THW1 = THW1_INT + THW1_DEC.
17:10	R/W	0x56	THW0 t(HW0) = N us. The range setting for THW0 in these fields is from 0 to 0xff. In HDQ mode, Range: t(HW0) <= 145 us.
9:0	R/W	0xbe	TCYCH t(CYCH) = N us. The range setting for TCYCH in these fields is from 0 to 0x3ff. In HDQ mode, Rang: 190 us <= t(CYCH) <= infinity.

8.10.6.12. Simple Mode Break Timing Control Register(Default Value: 0x00BE_0028)

Offset: 0x002C			**Register Name: HDQ_ BR_TCTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0xbe	TB t(B) = N us. The range setting for TB in these fields is from 0 to 0x 3ff. In HDQ mode, Rang: 190 us <= t(B) <= infinity.
15:10	/	/	/
9:0	R/W	0x28	TBR t(BR) = N us. The range setting for TBR in these fields is from 0 to 0xff. In HDQ mode, Rang: 40 us <= t(BR) <= infinity.

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8.11. CIR Transmitter

8.11.1. Overview

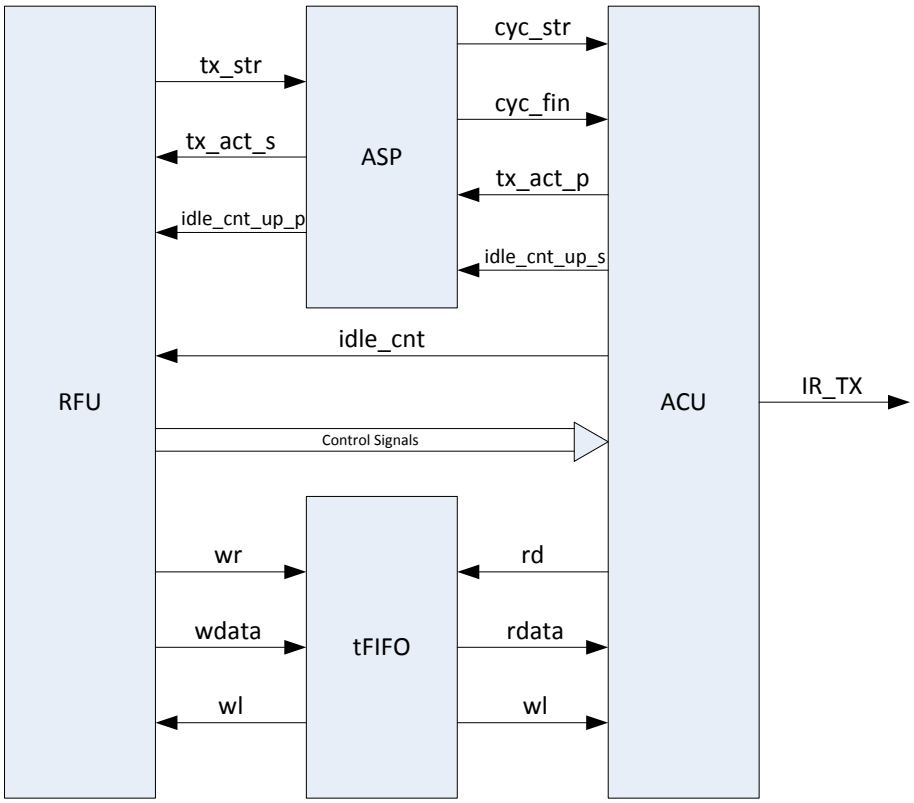
CIR (Consumer Infrared) Transmitter can transfer arbitrary wave, which is modulated with configurable carrier wave such as 38kHz. It only uses low 8-bit of a 32-bit register, it stores with 2 register for a 16-bit number, one is high 8-bit, the other is low 8-bit.

Features:

- Full physical layer implementation
- 128 bytes FIFO for data buffer
- Configurable carrier frequency
- Supports Interrupt and DMA
- Supports DMA shake and wait mode
- Supports arbitrary wave generator

8.11.2. Block Diagram

Figure 8-53 shows the block diagram of CIR Transmitter.



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Figure 8-53. CIR Transmitter Block Diagram

8.11.3. Operations and Functional Descriptions

8.11.3.1. External Signals

Table 8-30 describes the external signals of CIR Transmitter.

Table 8-30. CIR Transmitter External Signals

Signal	Description	Type
CIR_TX	CIR output signal	O

8.11.3.2. Clock Sources

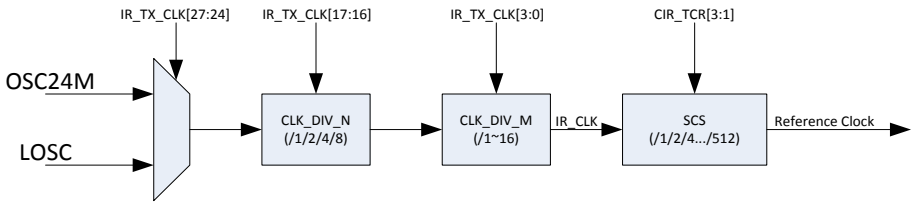


Figure 8-54. CIR Transmitter Clock

8.11.3.3. Typical Application

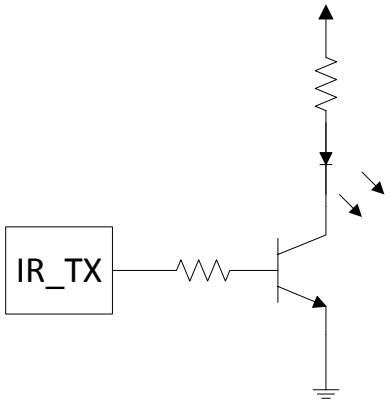


Figure 8-55. CIR Transmitter Application Block Diagram

8.11.3.4. Function Implementation

CIR_TX is used to generate a wave of arbitrary length and shape. It has a low demand for speed, and it can transform data into level sequence of a specific length. Every data is a byte. Bit7 of a byte means whether the level of a

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transmitting wave is high or low. Bit[6:0] is the length of this wave. If current transmitting frequency division is 4, 0x88 is a high level of 32 cycles, 0x08 is a low level of 22 cycles.

CIR_TX has two transmission modes, one is non-cycle transmission, and another one is cycle transmission. Non-cycle transmission is to transmit all the data in TX_FIFO to FIFO space. Cycle transmission is to transmit all the data in FIFO, until there are no signals. The data recovery in FIFO is implemented by clearing read pointer.

8.11.3.5. Timing Diagram

CIR remote control contains many protocols which designed by different manufacturers. Here to NEC protocol as an example, the CIR-TX module uses a variable pulse-width modulation technique to encompass the various formats of infrared encoding for remote-control applications. A message is started by a 9ms AGC burst, which was used to set the gain of the earlier CIR receivers. This AGC burst is then followed by a 4.5ms space, which is then followed by the address and command.

Bit definition: the logical “1” takes 2.25ms to transmit, while a logical “0” is only 1.12ms.

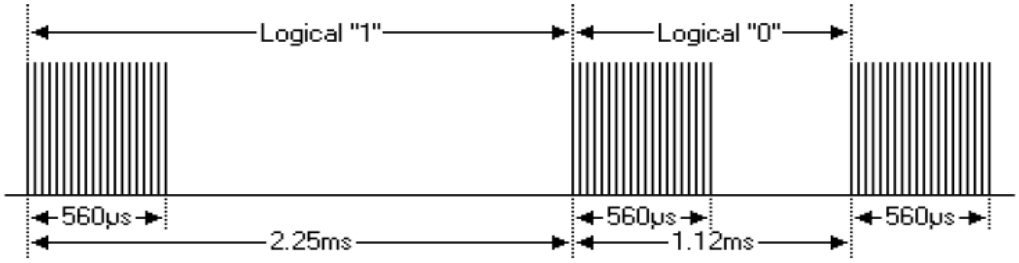


Figure 8-56. CIR One Bit Definition

Timing for a message:

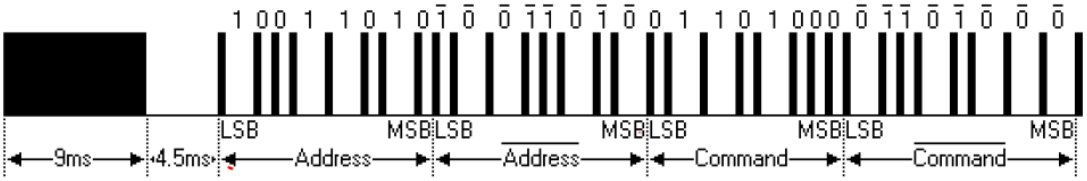
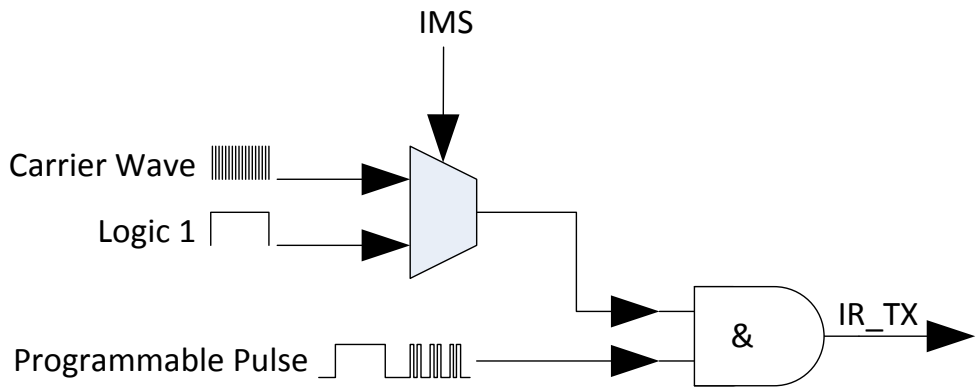


Figure 8-57. CIR Message Timing Diagram

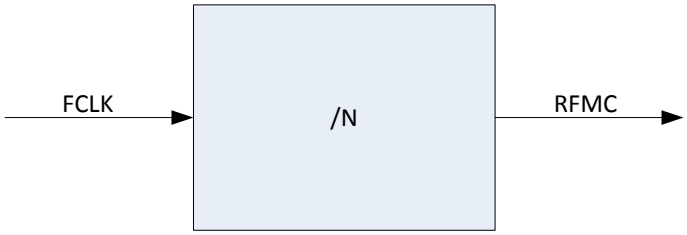
8.11.3.6. Operating Mode

- IMS: Internal modulation select

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- RFMC: Reference frequency of modulated carrier



Default: FCLK = 6MHz, DIV = 0x9E
RFMC = FCLK/DIV = 38KHz

- RCS: Reference clock select
  The data in TX_FIFO is used to describe the pulse in Run-Length Code. The basic unit of pulse width is Reference Clock. For more details of configuration methods, please refer to 1.3.2.
- CIR Transmitter Idle Duration Counter
  It is used in cycle transmission mode. When all the data in FIFO is transmitted, signals can be transmitted after a specific time.
- CIR Transmitter Idle Counter
  It is used to count idle duration of CIR transmitter, and it is used for software.

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8.11.4. Programming Guidlines

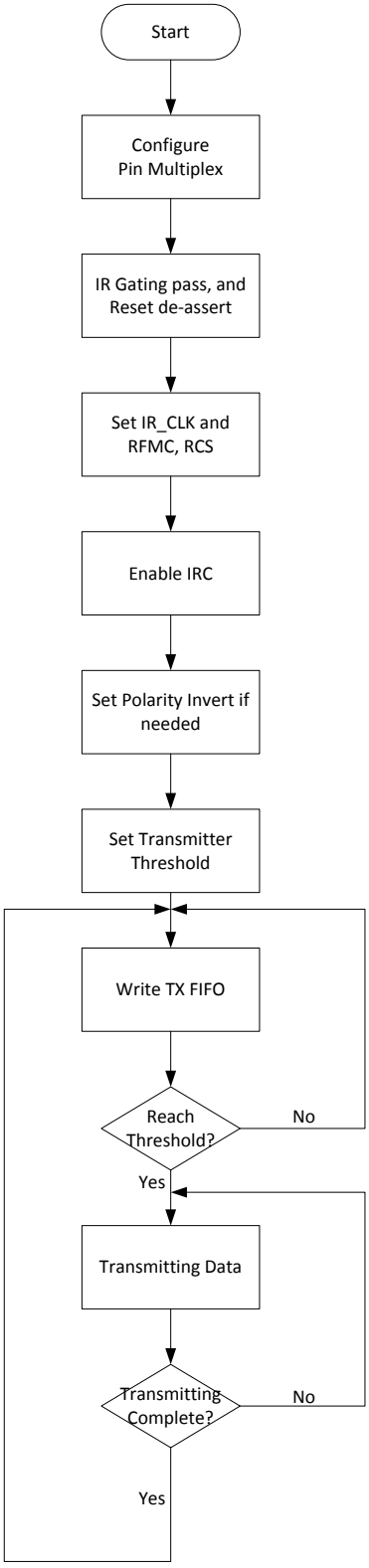


Figure 8-58. CIR Transmitter Process

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8.11.5. Register List

Module Name	Base Address
CIR_TX	0x05070400

Register Name	Offset	Description
CIR_TGLR	0x0000	CIR Transmit Global Register
CIR_TMCR	0x0004	CIR Transmit Modulation Control Register
CIR_TCR	0x0008	CIR Transmit Control Register
CIR_IDC_H	0x000C	CIR Transmit Idle Duration Threshold Register
CIR_IDC_L	0x0010	CIR Transmit Idle Duration Threshold Register
CIR_TICR_H	0x0014	CIR Transmit Idle Counter Register
CIR_TICR_L	0x0018	CIR Transmit Idle Counter Register
CIR_TEL	0x0020	CIR TX FIFO empty Level Register
CIR_TXINT	0x0024	CIR Transmit Interrupt Control Register
CIR_TAC	0x0028	CIR Transmit FIFO Available Counter Register
CIR_TXSTA	0x002C	CIR Transmit Status Register
CIR_TXT	0x0030	CIR Transmit Threshold Register
CIR_DMA	0x0034	CIR DMA Control Register
CIR_TXFIFO	0x0080	CIR Transmit FIFO Data Register

8.11.6. Register Description

8.11.6.1. CIR Transmitter Global Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CIR_TGLR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	IMS Internal Modulation Select 0: the transmitting signal is not modulated 1: the transmitting signal is modulated internally
6:5	R/W	0x0	DRMC Duty ratio of modulated carrier is high level /low level. 00: low level is the one time of high level 01: low level is the two times of high level 10: low level is the three times of high level 11: reserved
4:3	/	/	/
2	R/W	0x0	TPPI Transmit Pulse Polarity Invert 0: Not invert transmit pulse

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			1: Invert transmit pulse
1	R/W	0x0	TR Transmit Reset When this bit is set, the transmitting is reset. The FIFO will be flush, the TIC filed and CSS field will be clean during Transmit Reset. This field will automatically clear when the Transmit Reset is finished, and the CIR transmitter will state Idle .
0	R/W	0x0	TXEN Transmit Block Enable 0: Disable the CIR Transmitter 1: Enable the CIR Transmitter

8.11.6.2. CIR Transmitter Modulation Control Register(Default Value: 0x0000_009E)

Offset: 0x0004			Register Name: CIR_TMCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x9E	RFMC Reference Frequency of modulated carrier. Reference Frequency of modulated carrier based on a division of a fixed functional clock(FCLK).The range of the modulated carrier is usually 30kHz to 60kHz. The most consumer electronics is 38kHz. The default modulated carrier is 38kHz when FCLK is 6MHz. RFMC= FCLK/N.

8.11.6.3. CIR Transmitter Control Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CIR_TCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	CSS Cyclical Pulse Start/Stop Control Start to transmit when set to '1', 0: Stop when cleared to '0'. From start to stop, all data in FIFO must be transmitted. 1: Start.
6:4	/	/	/
3:1	R/W	0x0	RCS Reference Clock Select for CIR Transmit 000: CIR Transmit reference clock is ir_clk 001: CIR Transmit reference clock is ir_clk/2 010: CIR Transmit reference clock is ir_clk/4 011: CIR Transmit reference clock is ir_clk/8

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			100: CIR Transmit reference clock is ir_clk/64 101: CIR Transmit reference clock is ir_clk/128 110: CIR Transmit reference clock is ir_clk/256 111: CIR Transmit reference clock is ir_clk/512
0	R/W	0x0	TTS Type of the transmission signal 0: The transmitting wave is single non-cyclical pulse. 1: The transmitting wave is cyclical short-pulse.

8.11.6.4. CIR Transmitter Idle Duration Counter High Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: CIR_IDC_H
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x0	IDC_H Idle Duration Counter threshold(High 4 bit) Idle Duration = 128*IDC*Ts (IDC = 0~4095)

8.11.6.5. CIR Transmitter Idle Duration Counter Low Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: CIR_IDC_L
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	IDC_L Idle Duration Counter threshold(Low 8 bit) Idle Duration = 128*IDC*Ts (IDC = 0~4095)

8.11.6.6. CIR Transmitter Idle Counter High Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: CIR_TICR_H
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	TIC_H Transmit Idle Counter_H(High 8 bit) Count in 128*Ts (Sample Duration, 1/Fs) when transmitter is idle, and it should be reset when the transmitter active. When this counter reaches the maximum value (0xFFFF), it will stop automatically, and should not be cleared to zero.

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8.11.6.7. CIR Transmitter Idle Counter Low Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: CIR_TICR_L
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	TIC_L Transmit Idle Counter_L(Low 8 bit) Count in 128*Ts (Sample Duration, 1/Fs) when transmitter is idle, and it should be reset when the transmitter active. When this counter reaches the maximum value (0xFFFF), it will stop automatically, and should not be cleared to zero.

8.11.6.8. CIR Transmitter FIFO Empty Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: CIR_TEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	TEL TX FIFO empty Level for DRQ and IRQ. TRIGGER_LEVEL = TEL + 1

8.11.6.9. CIR Transmitter Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: CIR_TXINT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	DRQ_EN TX FIFO DMA Enable 0: Disable 1: Enable When set to '1', the Tx FIFO DRQ is asserted if the number of the transmitting data in the FIFO is less than the RAL. The DRQ is de-asserted when condition fails.
1	R/W	0x0	TAI_EN TX FIFO Available Interrupt Enable 0:Disable 1:Enable
0	R/W	0x0	TPEI_EN Transmit Packet End Interrupt Enable for Cyclical Pulse 0:Disable 1:Enable TUI_EN

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			Transmitter FIFO under run Interrupt Enable for Non-cyclical Pulse 0: Disable 1: Enable

8.11.6.10. CIR Transmitter FIFO Available Counter Register(Default Value: 0x0000_0080)

Offset: 0x0028			Register Name: CIR_TAC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x80	TAC TX FIFO Available Space Counter 0x00: No available space in TX FIFO 0x01: 1 byte available space in TX FIFO 0x02: 2 byte available space in TX FIFO … 0x80: 128 byte available space in TX FIFO

8.11.6.11. CIR Transmitter Status Register(Default Value: 0x0000_0002)

Offset: 0x002C			Register Name: CIR_TXSTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R	0x0	STCT Status of CIR Transmitter 0x0:Idle 0x1:Active This bit will automatically set when the controller begins transmit the data in the FIFO. The “1” will last when the data in the FIFO. It will automatically be cleaned to “0” when all data in the FIFO is transmitted. The bit is for debug. **Output Level of Idle state is determined by level of the last data output.**
2	R	0x0	DRQ DMA Request Flag When set to ‘1’, the Tx FIFO DRQ is asserted if the number of the transmitting data in the FIFO is less than the RAL. The DRQ is de-asserted when condition fails. This bit is for debug.
1	R/W	0x1	TAI TX FIFO Available Interrupt Flag 0: TX FIFO not available by its level 1: TX FIFO available by its level This bit can be cleared by software writing ‘1’.

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0	R/W	0x0	TPE Transmitter Packet End Flag for Cyclical Pulse 0: Transmissions of address, control and data fields not completed 1: Transmissions of address, control and data fields completed TUR Transmitter FIFO Under Run Flag for Non-cyclical Pulse 0: No transmitter FIFO under run 1: Transmitter FIFO under run This bit is cleared by writing a '1'.

8.11.6.12. CIR Transmitter Threshold Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: CIR_TXT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	NCTT Non-cyclical Pulse Transmit Threshold The controller will trigger transmitting the data in the FIFO when the data byte number has reaches the Transmit Threshold set in this field.

8.11.6.13. CIR Transmitter DMA Control Register(Default Value: 0x0000_00A5)

Offset: 0x0034			Register Name: CIR_DMA_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0xA5	DMA Handshake Configuration 0xA5: DMA wait cycle mode 0xEA: DMA handshake mode

8.11.6.14. CIR Transmitter FIFO Data Register(Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: CIR_TXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	W	0x0	Transmit Byte FIFO When the transmitting is trigger, the data in the FIFO will be transmitted until the data number is finished to be transmitted.

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8.12. CIR Receiver

8.12.1. Overview

CIR (Consumer Infrared) receiver is a capturer of the pulse from IR Receiver Module and uses Run-Length Code (RLC) to encode the pulse. The CIR receiver samples the input signal on the programmable frequency and records these samples into RX FIFO when one CIR signal is found on the air. The CIR receiver uses Run-Length Code (RLC) to encode pulse width. The encoded data is buffered in a 64 levels and 8-bit width RX FIFO; the MSB bit is used to record the polarity of the receiving CIR signal. The high level is represented as '1' and the low level is represented as '0'. The rest 7 bits are used for the length of RLC. The maximum length is 128. If the duration of one level (high or low level) is more than 128, another byte is used.

In the air, there is always some noise. One threshold can be set to filter the noise to reduce system loading and improve the system stability.

Features:

- Full physical layer implementation
- Supports CIR for remote control or wireless keyboard
- 64x8 bits FIFO for data buffer
- Programmable FIFO thresholds
- Interrupt Support
- Sample clock up to 1 MHz

8.12.2. Block Diagram

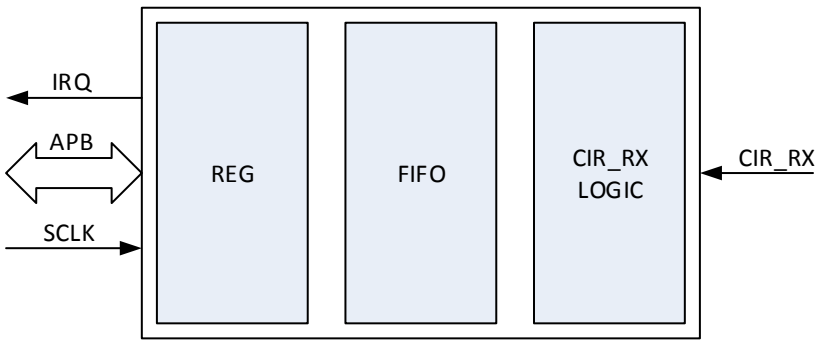


Figure 8-59. CIR Receiver Block Diagram

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8.12.3. Operations and Functional Descriptions

8.12.3.1. External Signals

Table 8-31 describes the external signals of CIR Receiver.

Table 8-31. CIR Receiver External Signals

Signal	Description	Type
CIR_RX	CIR input signal	I

8.12.3.2. Clock Sources

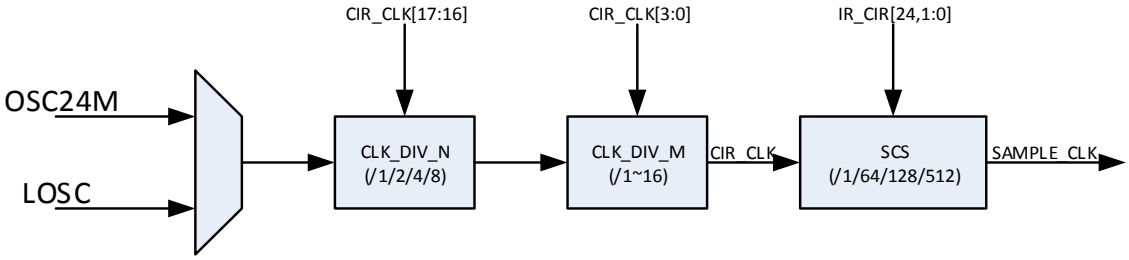


Figure 8-60. CIR Receiver Clock

8.12.3.3. Typical Application

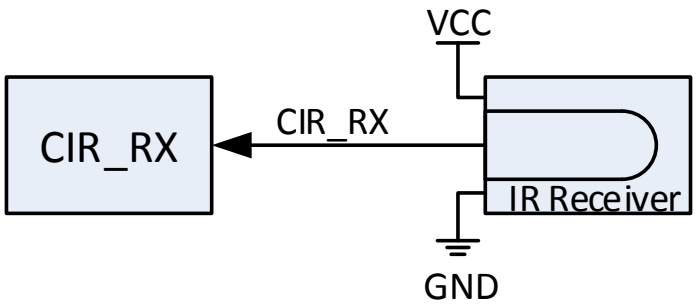


Figure 8-61. CIR Receiver Application Diagram

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8.12.3.4. Function Implementation



Figure 8-62. NEC Protocol

In fact, CIR module is a timer with capture function.

When CIR_RX signals satisfy ATHR (Active Threshold), CIR can start to capture. In the process, the signal is ignored if the pulse width of the signal is less than NTHR. when CIR_RX signals satisfy ITHR (Idle Threshold), the capture process is stopped and the Receiver Packet End interrupt is generated, then Receiver Packet End Flag is asserted.

In a capture process, every effective pulse is buffered to FIFO in bytes according to the form of Run-Length Code. The MSB bit of a byte is polarity of pulse, and the rest 7 bits is pulse width by taking Sample Clock as basic unit. This is the code form of RLC-Byte. When the level changes or the pulse width counting overflows, RLC-Byte is buffered to FIFO. The CIR_RX module receives infrared signals transmitted by the infrared remote control, the software decodes the signals.

8.12.3.5. Operating Mode

- Sample Clock

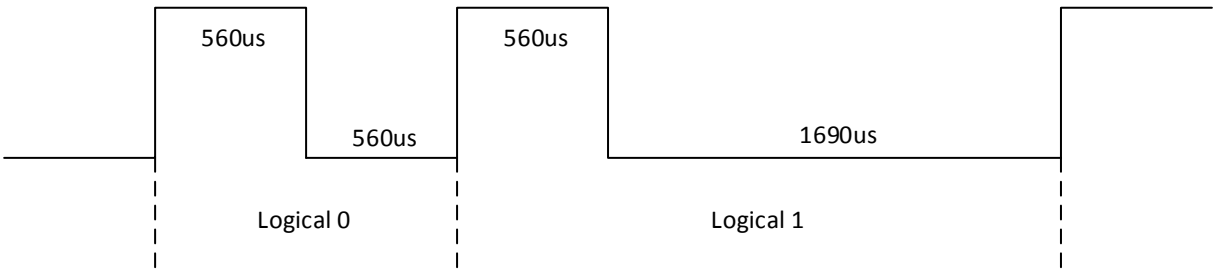


Figure 8-63. Logical ‘0’ and Logical ‘1’ of NEC Protocol

For NEC protocol, a logical "1" takes 2.25ms(560us+1680us) to transmit, while a logical "0" is only half of that, being 1.12ms(560us+560us). For example, if sample clock is 31.25 kHz, sample cycle is 32us,then 18 sample cycles is 560us.So the RLC of 560us low level is 0x12, the RLC of 560us high level is 0x92. Then a logical “1” takes code 0x12 and code 0xb5 to transmit, a logical “0” takes code 0x12 and code 0x92 to transmit.

- ATHR(Active Threshold)

When CIR is in Idle state,if electrical level of CIR_RX signal changes (positive jump or negative jump), and the duration reaches this threshold, then CIR takes the starting of the signal as a lead code, turns into active state and starts to capture CIR_RX signals.

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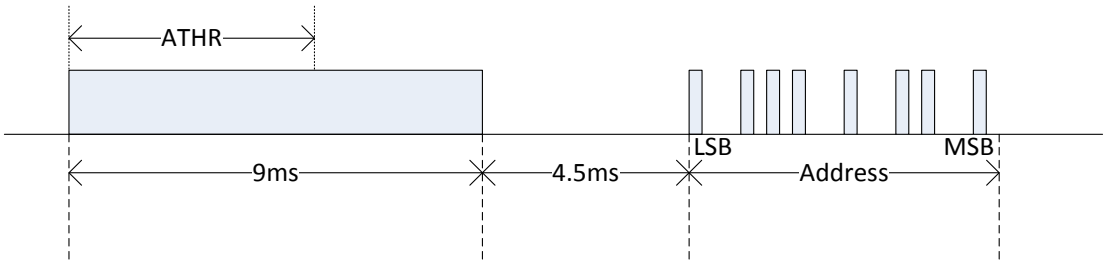


Figure 8-64.ATHR Definition

- ITHR(Idle Threshold)

If electrical level of CIR_RX signals has no change, and the duration reaches this threshold, then CIR enters into Idle state and ends this capture.

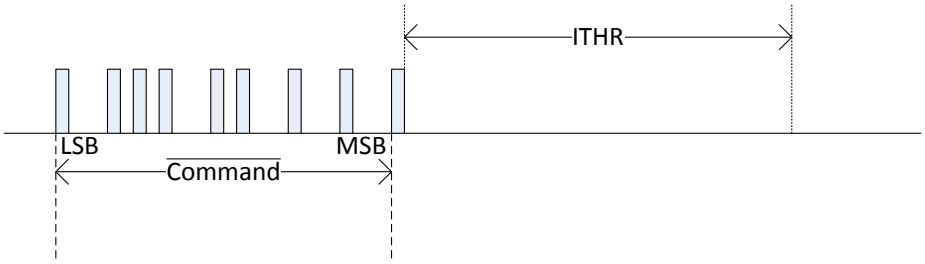


Figure 8-65. ITHR Definition

- NTHR(Noise Threshold)

In capture process,the pulse is ignored if the pulse width is less than Noise Threshold.

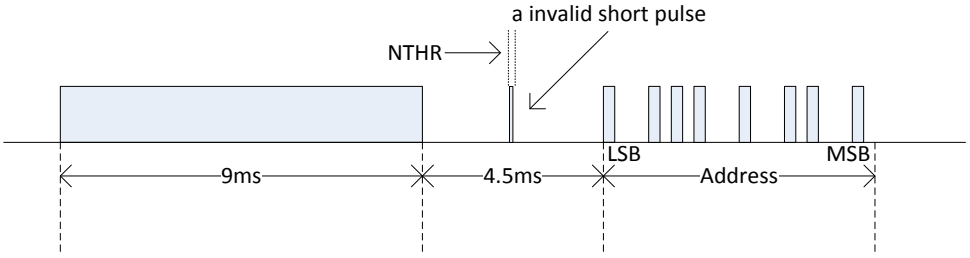


Figure 8-66. NTHR Definition

- APAM(Active Pulse Accept Mode)

APAM is used to fit the type of lead code. If a pulse does not fit the type of lead code, it is not regarded as a lead code even if the pulse width reaches ATHR.

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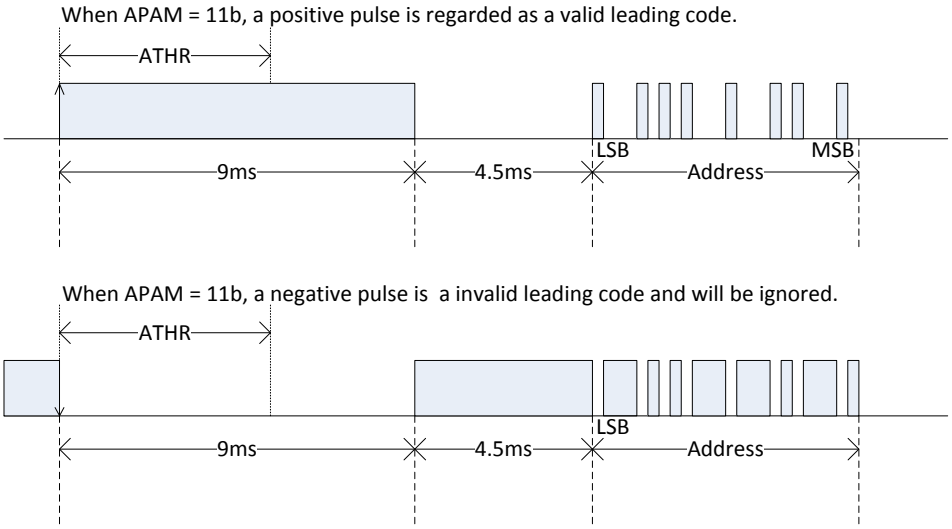


Figure 8-67. APAM Definition

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8.12.4. Programming Guidelines

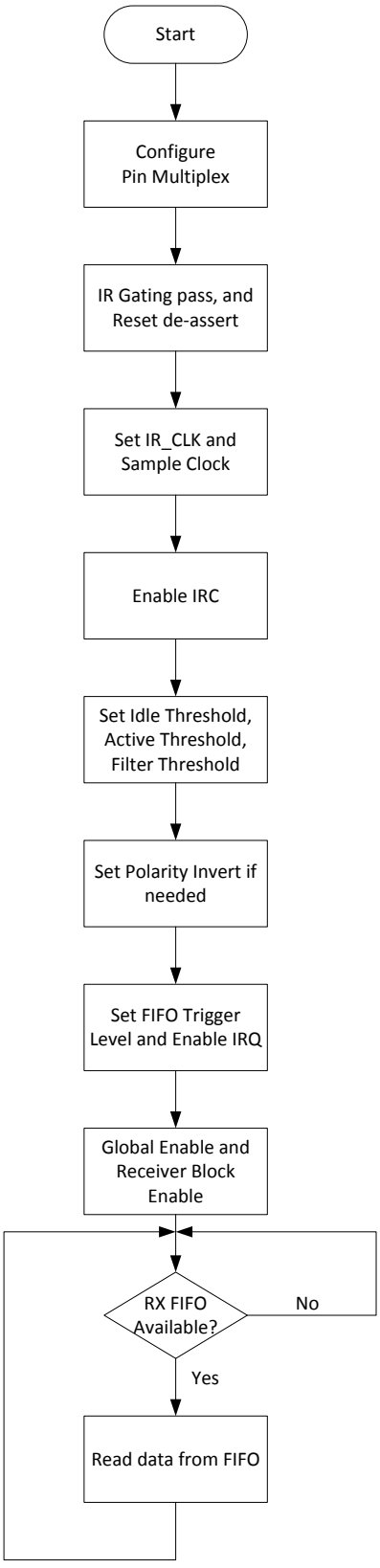


Figure 8-68. CIR Receiver Process

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8.12.5. Register List

Module Name	Base Address
CIR_RX	0x07040000

Register Name	Offset	Description
CIR_CTL	0x0000	CIR Control Register
CIR_RXPCFG	0x0010	CIR Receiver Pulse Configure Register
CIR_RXFIFO	0x0020	CIR Receiver FIFO Register
CIR_RXINT	0x002C	CIR Receiver Interrupt Control Register
CIR_RXSTA	0x0030	CIR Receiver Status Register
CIR_RXCFG	0x0034	CIR Receiver Configure Register

8.12.6. Register Description

8.12.6.1. CIR Receiver Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CIR_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R/W	0x0	Active Pulse Accept Mode 00, 01: Both positive and negative pulses are valid as a leading code. 10: Only negative pulse is valid as a leading code. 11: Only positive pulse is valid as a leading code.
5:4	R/W	0x0	CIR ENABLE 00~10: Reserved 11: CIR mode enable
3:2	/	/	/
1	R/W	0x0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0x0	GEN Global Enable A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable

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8.12.6.2. CIR Receiver Pulse Configure Register(Default Value: 0x0000_0004)

Offset: 0x0010			Register Name: CIR_RXPCFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x1	RPPI Receiver Pulse Polarity Invert. 0: Do not invert receiver signal 1: Invert receiver signal
1:0	/	/	/

8.12.6.3. CIR Receiver FIFO Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: CIR_RXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	Receiver Byte FIFO

8.12.6.4. CIR Receiver Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: CIR_RXINT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:8	R/W	0x0	RAL RX FIFO Available Received Byte Level for interrupt and DMA request TRIGGER_LEVEL = RAL + 1
5	R/W	0x0	DRQ_EN RX FIFO DMA Enable 0: Disable 1: Enable When set to '1', the Receiver FIFO DRQ is asserted if reaching RAL. The DRQ is de-asserted when condition fails.
4	R/W	0x0	RAI_EN RX FIFO Available Interrupt Enable 0: Disable 1: Enable When set to '1', the Receiver FIFO IRQ is asserted if reaching RAL. The IRQ is de-asserted when condition fails.
3:2	/	/	/
1	R/W	0x0	RPEI_EN Receiver Packet End Interrupt Enable 0: Disable 1: Enable

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0	R/W	0x0	ROI_EN Receiver FIFO Overrun Interrupt Enable 0: Disable 1: Enable

8.12.6.5. CIR Receiver Status Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: CIR_RXSTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:8	R	0x0	RAC RX FIFO Available Counter 0: No available data in RX FIFO 1: 1 byte available data in RX FIFO 2: 2 byte available data in RX FIFO … 64: 64 byte available data in RX FIFO
7	R	0x0	STAT Status of CIR 0: Idle 1: busy
6:5	/	/	/
4	R/W	0x0	RA RX FIFO Available 0: RX FIFO not available according its level 1: RX FIFO available according its level This bit is cleared by writing a ‘1’.
3:2	/	/	/
1	R/W	0x0	RPE Receiver Packet End Flag 0: STO was not detected. In CIR mode, one CIR symbol is receiving or not detected. 1: STO field or packet abort symbol (7’b0000,000 and 8’b0000,0000 for MIR and FIR) is detected. In CIR mode, one CIR symbol is received. This bit is cleared by writing a ‘1’.
0	R/W	0x0	ROI Receiver FIFO Overrun 0: Receiver FIFO not overrun 1: Receiver FIFO overrun This bit is cleared by writing a ‘1’.

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8.12.6.6. CIR Receiver Configure Register(Default Value: 0x0000_1828)

Offset: 0x0034			Register Name: CIR_RXCFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:25	/	/	/
24	R/W	0x0	SCS2 Bit2 of Sample Clock Select for CIR This bit is defined by SCS bits below.
23	R/W	0x0	ATHC Active Threshold Control for CIR 0: ATHR in Unit of (Sample Clock) 1: ATHR in Unit of (128*Sample Clocks)
22:16	R/W	0x0	ATHR Active Threshold for CIR These bits control the duration of CIR from Idle to Active State. The duration can be calculated by ((ATHR + 1)*(ATHC? Sample Clock: 128*Sample Clock)).
15:8	R/W	0x18	ITHR Idle Threshold for CIR The Receiver uses it to decide whether the CIR command has been received. If there is no CIR signal on the air, the receiver is staying in IDLE status. One active pulse will bring the receiver from IDLE status to Receiving status. After the CIR is end, the inputting signal will keep the specified level (high or low level) for a long time. The receiver can use this idle signal duration to decide that it has received the CIR command. The corresponding flag is asserted. If the corresponding interrupt is enabled, the interrupt line is asserted to CPU. When the duration of signal keeps one status (high or low level) for the specified duration ((ITHR + 1)*128 sample_clk), this means that the previous CIR command has been finished.
7:2	R/W	0xa	NTHR Noise Threshold for CIR When the duration of signal pulse (high or low level) is less than NTHR, the pulse is taken as noise and should be discarded by hardware. 0: all samples are recorded into RX FIFO 1: If the signal is only one sample duration, it is taken as noise and discarded. 2: If the signal is less than (<=) two sample duration, it is taken as noise and discarded. … 61: if the signal is less than (<=) sixty-one sample duration, it is taken as noise and discarded.
1:0	R/W	0x0	SCS Sample Clock Select for CIR SCS2 | SCS[1] | SCS[0] | Sample Clock 0 | 0 | 0 | CIR_CLK/64 0 | 0 | 1 | CIR_CLK /128

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			0	1	0	CIR_CLK /256	
			0	1	1	CIR_CLK /512	
			1	0	0	CIR_CLK	
			1	0	1	Reserved	
			1	1	0	Reserved	
			1	1	1	Reserved	

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8.13. EPHY

8.13.1. Overview

- System resources are controlled by ATE
- Fully IEEE 802.3 10/100 Base-TX compliant and supports EEE
- Auto negotiation and parallel detection capability for automatic speed and duplex selection
- Programmable loopback mode for diagnostic
- Supports WOL (Wake-On-Lan) functionality
- Design for Testability with extensive testability feature and 95% fault coverage
- Power consumption (100Base-TX) less than 140mW

8.13.2. Register List

Module Name	Base Address
ATE_EPHY	0x6000

Register Name	Offset	Description
EPHY_CTL	0x0000	Ethernet PHY Control Register
EPHY_BIST	0x0002	Ethernet PHY BIST Register

8.13.3. Register Description

8.13.3.1. Ethernet PHY Control Register(Default Value: 0x0005)

Offset: 0x0000			Register Name: EPHY_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
15:12	R/W	0x0	BPS_EFFUSE
11	R/W	0x0	XMII_SEL 0: MII 1: RMII
10:9	R/W	0x0	EPHY_MODE Operation Mode Selection 00 : Normal Mode 01 : Sim Mode 10 : AFE Test Mode 11 : /

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8:4	R/W	0x0	PHY_ADDR PHY Address
3	R/W	0x0	BIST_CLK_EN 0 : BIST clk disable 1 : BIST clk enable
2	R/W	0x1	CLK_SEL 0 : 27MHz 1 : 24MHz
1	R/W	0x0	LED_POL 0 : High active 1 : Low active
0	R/W	0x1	SHUTDOWN 0 : Power up 1 : Shutdown

8.13.3.2. Ethernet PHY Control Register(Default Value: 0x0000)

Offset: 0x0002			Register Name: EPHY_BIST
Bit	**Read/Write**	**Default/Hex**	**Description**
15	/	/	/
14:12	R/W	0x0	BIST_STATUS bist_status[5]:BIST_FAIL_RMII2MII bist_status[4]:BIST_FAIL_MII2RMII bist_status[3]:BIST_FAIL_PLPIC
11	/	/	/
10:8	R/W	0x0	BIST_FINISH bist_status[2]:BIST_FINISH_RMII2MII bist_status[1]:BIST_FINISH_MII2RMII bist_status[0]:BIST_FINISH_PLPIC
7:1	/	/	/
0	R/W	0x0	BIST_START 0 : disable 1 : Start

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8.14. PCIe

8.14.1. Overview

The PCI Express (PCIe) Controller is a general purpose I/O interconnect, which provides low pin count, high reliability, and high-speed data transfer at rates of up to 5.0 Gbps per lane per direction.

Features:

- Only supports Root Complex (RC) mode
- Embedded PCI Express PHY, supports x1 Gen2 (5.0Gbps) lane
- Single virtual channel (VC)
- 256 bytes maximum payload size
- Supports 2 Inbound windows and 2 Outbound windows
- Supports Message Signaled Interrupts (MSI)
- Embedded DMA, support 2 write channels and 2 read channels
- Complies with PCI Express Base 2.0 Specification

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8.14.2. Block Diagram

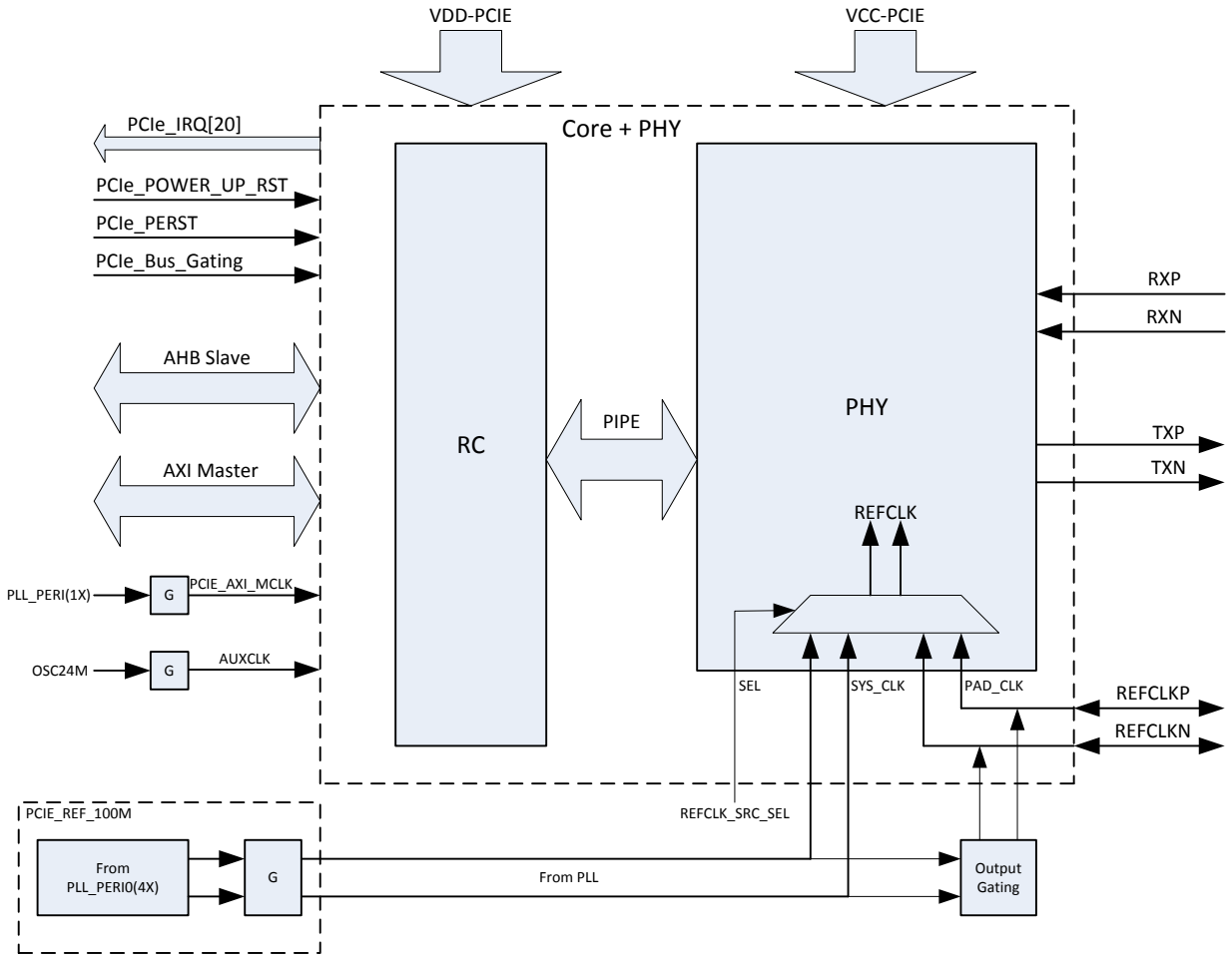


Figure 8-69. PCIe Controller Block Diagram

8.14.3. Operations and Functional Descriptions

8.14.3.1. External Signals

Table 8-32. PCIe External Signals

Signal	Description	Type
PCIE-REF-CLKP	PCIe differential signal REFCLK positive	AI/O
PCIE-REF-CLKM	PCIe differential signal REFCLK negative	AI/O
PCIE-RXP	PCIe differential signal RX positive	AI/O
PCIE-RXM	PCIe differential signal RX negative	AI/O
PCIE-TXP	PCIe differential signal TX positive	AI/O
PCIE-TXM	PCIe differential signal TX negative	AI/O

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8.14.3.2. Clock Sources

Table 8-33. PCIe Clock Sources

Clock Name	Clock Source	Description
PCIE_AXI_MCLK	PLL_PERI(1x)	AXI master interface clock
AUXCLK	OSC24M	Auxiliary Clock, the low-power clock
PCIE_REF_CLK	PLL_PERI(4x)/External PAD Clock	Reference Clock, the main clock

8.14.3.3. Typical Application

Figure 8-70 shows the PCIe application block diagram when using internal reference clock.

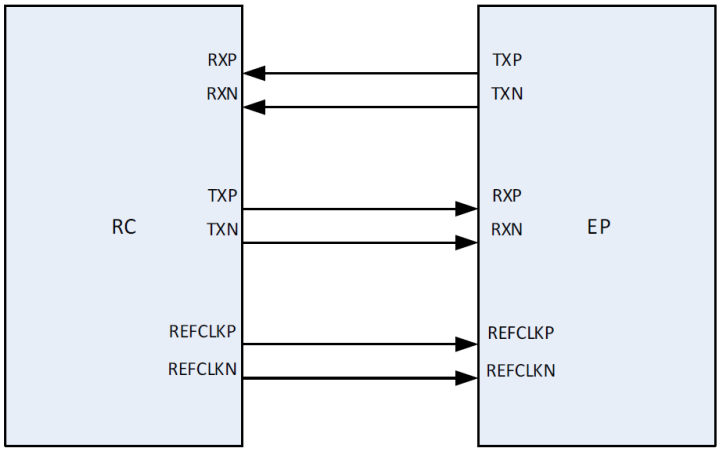


Figure 8-70. PCIe Application Block Diagram(internal reference clock)

Figure 8-71 shows the PCIe application block diagram when using external reference clock.

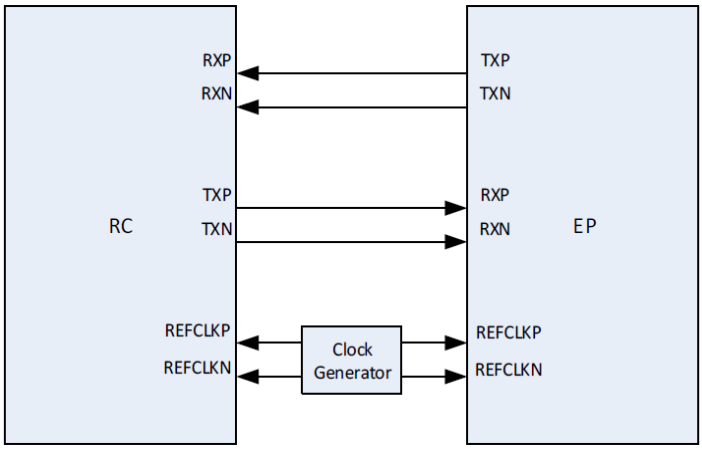


Figure 8-71. PCIe Application Block Diagram(external reference clock)

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