



**EN:** This Datasheet is presented by the manufacturer.

Please visit our website for pricing and availability at [www.hestore.hu](http://www.hestore.hu).

## 2.7V 4-Channel/8-Channel 12-Bit A/D Converters with SPI Serial Interface

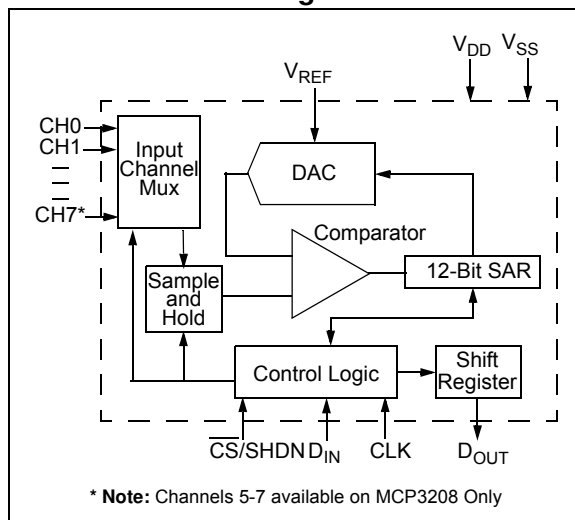
### Features

- 12-bit resolution
- $\pm 1$  LSB max DNL
- $\pm 1$  LSB max INL (MCP3204/3208-B)
- $\pm 2$  LSB max INL (MCP3204/3208-C)
- 4 (MCP3204) or 8 (MCP3208) input channels
- Analog inputs programmable as single-ended or pseudo-differential pairs
- On-chip sample and hold
- SPI serial interface (modes 0,0 and 1,1)
- Single supply operation: 2.7V - 5.5V
- 100 ksp/s max. sampling rate at  $V_{DD} = 5V$
- 50 ksp/s max. sampling rate at  $V_{DD} = 2.7V$
- Low power CMOS technology:
  - 500 nA typical standby current, 2  $\mu A$  max.
  - 400  $\mu A$  max. active current at 5V
- Industrial temp range:  $-40^{\circ}C$  to  $+85^{\circ}C$
- Available in PDIP, SOIC and TSSOP packages

### Applications

- Sensor Interface
- Process Control
- Data Acquisition
- Battery Operated Systems

### Functional Block Diagram



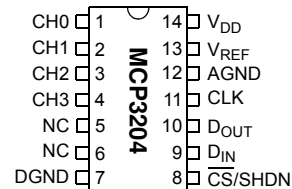
### Description

The Microchip Technology Inc. MCP3204/3208 devices are successive approximation 12-bit Analog-to-Digital (A/D) Converters with on-board sample and hold circuitry. The MCP3204 is programmable to provide two pseudo-differential input pairs or four single-ended inputs. The MCP3208 is programmable to provide four pseudo-differential input pairs or eight single-ended inputs. Differential Nonlinearity (DNL) is specified at  $\pm 1$  LSB, while Integral Nonlinearity (INL) is offered in  $\pm 1$  LSB (MCP3204/3208-B) and  $\pm 2$  LSB (MCP3204/3208-C) versions.

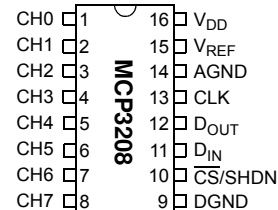
Communication with the devices is accomplished using a simple serial interface compatible with the SPI protocol. The devices are capable of conversion rates of up to 100 ksp/s. The MCP3204/3208 devices operate over a broad voltage range (2.7V - 5.5V). Low current design permits operation with typical standby and active currents of only 500 nA and 320  $\mu A$ , respectively. The MCP3204 is offered in 14-pin PDIP, 150 mil SOIC and TSSOP packages. The MCP3208 is offered in 16-pin PDIP and SOIC packages.

### Package Types

#### PDIP, SOIC, TSSOP



#### PDIP, SOIC



# MCP3204/3208

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

|                                                   |                          |
|---------------------------------------------------|--------------------------|
| $V_{DD}$ .....                                    | 7.0V                     |
| All inputs and outputs w.r.t. $V_{SS}$ .....      | -0.6V to $V_{DD} + 0.6V$ |
| Storage temperature .....                         | -65°C to +150°C          |
| Ambient temp. with power applied .....            | -65°C to +125°C          |
| Soldering temperature of leads (10 seconds) ..... | +300°C                   |
| ESD protection on all pins .....                  | > 4 kV                   |

†**Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL SPECIFICATIONS

| <b>Electrical Characteristics:</b> Unless otherwise noted, all parameters apply at $V_{DD} = 5V$ , $V_{SS} = 0V$ , $V_{REF} = 5V$ , $T_A = -40^\circ C$ to $+85^\circ C$ , $f_{SAMPLE} = 100$ ksp/s and $f_{CLK} = 20 \cdot f_{SAMPLE}$ |              |          |                         |                    |                    |                                                      |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|----------|-------------------------|--------------------|--------------------|------------------------------------------------------|
| Parameters                                                                                                                                                                                                                              | Sym          | Min      | Typ                     | Max                | Units              | Conditions                                           |
| <b>Conversion Rate</b>                                                                                                                                                                                                                  |              |          |                         |                    |                    |                                                      |
| Conversion Time                                                                                                                                                                                                                         | $t_{CONV}$   | —        | —                       | 12                 | clock cycles       |                                                      |
| Analog Input Sample Time                                                                                                                                                                                                                | $t_{SAMPLE}$ | 1.5      |                         |                    | clock cycles       |                                                      |
| Throughput Rate                                                                                                                                                                                                                         | $f_{SAMPLE}$ | —        | —                       | 100<br>50          | ksp/s<br>ksp/s     | $V_{DD} = V_{REF} = 5V$<br>$V_{DD} = V_{REF} = 2.7V$ |
| <b>DC Accuracy</b>                                                                                                                                                                                                                      |              |          |                         |                    |                    |                                                      |
| Resolution                                                                                                                                                                                                                              |              |          | 12                      |                    | bits               |                                                      |
| Integral Nonlinearity                                                                                                                                                                                                                   | INL          | —        | $\pm 0.75$<br>$\pm 1.0$ | $\pm 1$<br>$\pm 2$ | LSB                | MCP3204/3208-B<br>MCP3204/3208-C                     |
| Differential Nonlinearity                                                                                                                                                                                                               | DNL          | —        | $\pm 0.5$               | $\pm 1$            | LSB                | No missing codes over-temperature                    |
| Offset Error                                                                                                                                                                                                                            |              | —        | $\pm 1.25$              | $\pm 3$            | LSB                |                                                      |
| Gain Error                                                                                                                                                                                                                              |              | —        | $\pm 1.25$              | $\pm 5$            | LSB                |                                                      |
| <b>Dynamic Performance</b>                                                                                                                                                                                                              |              |          |                         |                    |                    |                                                      |
| Total Harmonic Distortion                                                                                                                                                                                                               |              | —        | -82                     | —                  | dB                 | $V_{IN} = 0.1V$ to $4.9V$ @1 kHz                     |
| Signal to Noise and Distortion (SINAD)                                                                                                                                                                                                  |              | —        | 72                      | —                  | dB                 | $V_{IN} = 0.1V$ to $4.9V$ @1 kHz                     |
| Spurious Free Dynamic Range                                                                                                                                                                                                             |              | —        | 86                      | —                  | dB                 | $V_{IN} = 0.1V$ to $4.9V$ @1 kHz                     |
| <b>Reference Input</b>                                                                                                                                                                                                                  |              |          |                         |                    |                    |                                                      |
| Voltage Range                                                                                                                                                                                                                           |              | 0.25     | —                       | $V_{DD}$           | V                  | <b>Note 2</b>                                        |
| Current Drain                                                                                                                                                                                                                           |              | —        | 100<br>0.001            | 150<br>3.0         | $\mu A$<br>$\mu A$ | $\overline{CS} = V_{DD} = 5V$                        |
| <b>Analog Inputs</b>                                                                                                                                                                                                                    |              |          |                         |                    |                    |                                                      |
| Input Voltage Range for CH0-CH7 in Single-Ended Mode                                                                                                                                                                                    |              | $V_{SS}$ | —                       | $V_{REF}$          | V                  |                                                      |
| Input Voltage Range for IN+ in pseudo-differential Mode                                                                                                                                                                                 |              | IN-      | —                       | $V_{REF} + IN-$    |                    |                                                      |

**Note 1:** This parameter is established by characterization and not 100% tested.

**2:** See graphs that relate linearity performance to  $V_{REF}$  levels.

**3:** Because the sample cap will eventually lose charge, effective clock rates below 10 kHz can affect linearity performance, particularly at elevated temperatures. See **Section 6.2 "Maintaining Minimum Clock Speed"**, "Maintaining Minimum Clock Speed", for more information.

**ELECTRICAL SPECIFICATIONS (CONTINUED)**

| <b>Electrical Characteristics:</b> Unless otherwise noted, all parameters apply at $V_{DD} = 5V$ , $V_{SS} = 0V$ , $V_{REF} = 5V$ , $T_A = -40^{\circ}C$ to $+85^{\circ}C$ , $f_{SAMPLE} = 100$ ksp/s and $f_{CLK} = 20 \cdot f_{SAMPLE}$ |                   |                 |            |              |            |                                                                                            |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|-----------------|------------|--------------|------------|--------------------------------------------------------------------------------------------|
| Parameters                                                                                                                                                                                                                                | Sym               | Min             | Typ        | Max          | Units      | Conditions                                                                                 |
| Input Voltage Range for IN- in pseudo-differential Mode                                                                                                                                                                                   |                   | $V_{SS}-100$    | —          | $V_{SS}+100$ | mV         |                                                                                            |
| Leakage Current                                                                                                                                                                                                                           |                   | —               | 0.001      | $\pm 1$      | $\mu A$    |                                                                                            |
| Switch Resistance                                                                                                                                                                                                                         |                   | —               | 1000       | —            | $\Omega$   | See Figure 4-1                                                                             |
| Sample Capacitor                                                                                                                                                                                                                          |                   | —               | 20         | —            | pF         | See Figure 4-1                                                                             |
| <b>Digital Input/Output</b>                                                                                                                                                                                                               |                   |                 |            |              |            |                                                                                            |
| Data Coding Format                                                                                                                                                                                                                        |                   | Straight Binary |            |              |            |                                                                                            |
| High Level Input Voltage                                                                                                                                                                                                                  | $V_{IH}$          | $0.7 V_{DD}$    | —          | —            | V          |                                                                                            |
| Low Level Input Voltage                                                                                                                                                                                                                   | $V_{IL}$          | —               | —          | $0.3 V_{DD}$ | V          |                                                                                            |
| High Level Output Voltage                                                                                                                                                                                                                 | $V_{OH}$          | 4.1             | —          | —            | V          | $I_{OH} = -1$ mA, $V_{DD} = 4.5V$                                                          |
| Low Level Output Voltage                                                                                                                                                                                                                  | $V_{OL}$          | —               | —          | 0.4          | V          | $I_{OL} = 1$ mA, $V_{DD} = 4.5V$                                                           |
| Input Leakage Current                                                                                                                                                                                                                     | $I_{LI}$          | -10             | —          | 10           | $\mu A$    | $V_{IN} = V_{SS}$ or $V_{DD}$                                                              |
| Output Leakage Current                                                                                                                                                                                                                    | $I_{LO}$          | -10             | —          | 10           | $\mu A$    | $V_{OUT} = V_{SS}$ or $V_{DD}$                                                             |
| Pin Capacitance (All Inputs/Outputs)                                                                                                                                                                                                      | $C_{IN}, C_{OUT}$ | —               | —          | 10           | pF         | $V_{DD} = 5.0V$ (Note 1)<br>$T_A = 25^{\circ}C$ , $f = 1$ MHz                              |
| <b>Timing Parameters</b>                                                                                                                                                                                                                  |                   |                 |            |              |            |                                                                                            |
| Clock Frequency                                                                                                                                                                                                                           | $f_{CLK}$         | —               | —          | 2.0<br>1.0   | MHz<br>MHz | $V_{DD} = 5V$ (Note 3)<br>$V_{DD} = 2.7V$ (Note 3)                                         |
| Clock High Time                                                                                                                                                                                                                           | $t_{HI}$          | 250             | —          | —            | ns         |                                                                                            |
| Clock Low Time                                                                                                                                                                                                                            | $t_{LO}$          | 250             | —          | —            | ns         |                                                                                            |
| CS Fall To First Rising CLK Edge                                                                                                                                                                                                          | $t_{SUCS}$        | 100             | —          | —            | ns         |                                                                                            |
| Data Input Setup Time                                                                                                                                                                                                                     | $t_{SU}$          | 50              | —          | —            | ns         |                                                                                            |
| Data Input Hold Time                                                                                                                                                                                                                      | $t_{HD}$          | 50              | —          | —            | ns         |                                                                                            |
| CLK Fall To Output Data Valid                                                                                                                                                                                                             | $t_{DO}$          | —               | —          | 200          | ns         | See Figures 1-2 and 1-3                                                                    |
| CLK Fall To Output Enable                                                                                                                                                                                                                 | $t_{EN}$          | —               | —          | 200          | ns         | See Figures 1-2 and 1-3                                                                    |
| CS Rise To Output Disable                                                                                                                                                                                                                 | $t_{DIS}$         | —               | —          | 100          | ns         | See Figures 1-2 and 1-3                                                                    |
| CS Disable Time                                                                                                                                                                                                                           | $t_{CSH}$         | 500             | —          | —            | ns         |                                                                                            |
| $D_{OUT}$ Rise Time                                                                                                                                                                                                                       | $t_R$             | —               | —          | 100          | ns         | See Figures 1-2 and 1-3 (Note 1)                                                           |
| $D_{OUT}$ Fall Time                                                                                                                                                                                                                       | $t_F$             | —               | —          | 100          | ns         | See Figures 1-2 and 1-3 (Note 1)                                                           |
| <b>Power Requirements</b>                                                                                                                                                                                                                 |                   |                 |            |              |            |                                                                                            |
| Operating Voltage                                                                                                                                                                                                                         | $V_{DD}$          | 2.7             | —          | 5.5          | V          |                                                                                            |
| Operating Current                                                                                                                                                                                                                         | $I_{DD}$          | —               | 320<br>225 | 400<br>—     | $\mu A$    | $V_{DD}=V_{REF} = 5V$ , $D_{OUT}$ unloaded<br>$V_{DD}=V_{REF} = 2.7V$ , $D_{OUT}$ unloaded |
| Standby Current                                                                                                                                                                                                                           | $I_{DDS}$         | —               | 0.5        | 2.0          | $\mu A$    | $\overline{CS} = V_{DD} = 5.0V$                                                            |

**Note 1:** This parameter is established by characterization and not 100% tested.

**2:** See graphs that relate linearity performance to  $V_{REF}$  levels.

**3:** Because the sample cap will eventually lose charge, effective clock rates below 10 kHz can affect linearity performance, particularly at elevated temperatures. See **Section 6.2 “Maintaining Minimum Clock Speed”**, “Maintaining Minimum Clock Speed”, for more information.

# MCP3204/3208

## TEMPERATURE CHARACTERISTICS

| Electrical Specifications: Unless otherwise indicated, V <sub>DD</sub> = 5V, V <sub>SS</sub> = 0V, V <sub>REF</sub> = 5V |                 |     |      |      |       |            |
|--------------------------------------------------------------------------------------------------------------------------|-----------------|-----|------|------|-------|------------|
| Parameters                                                                                                               | Sym             | Min | Typ  | Max  | Units | Conditions |
| Temperature Ranges                                                                                                       |                 |     |      |      |       |            |
| Specified Temperature Range                                                                                              | T <sub>A</sub>  | -40 | —    | +125 | °C    |            |
| Operating Temperature Range                                                                                              | T <sub>A</sub>  | -40 | —    | +125 | °C    |            |
| Storage Temperature Range                                                                                                | T <sub>A</sub>  | -65 | —    | +150 | °C    |            |
| Thermal Package Resistances                                                                                              |                 |     |      |      |       |            |
| Thermal Resistance, 14L-PDIP                                                                                             | θ <sub>JA</sub> | —   | 70   | —    | °C/W  |            |
| Thermal Resistance, 14L-SOIC                                                                                             | θ <sub>JA</sub> | —   | 95.3 | —    | °C/W  |            |
| Thermal Resistance, 14L-TSSOP                                                                                            | θ <sub>JA</sub> | —   | 100  | —    | °C/W  |            |
| Thermal Resistance, 16L-PDIP                                                                                             | θ <sub>JA</sub> | —   | 70   | —    | °C/W  |            |
| Thermal Resistance, 16L-SOIC                                                                                             | θ <sub>JA</sub> | —   | 86.1 | —    | °C/W  |            |

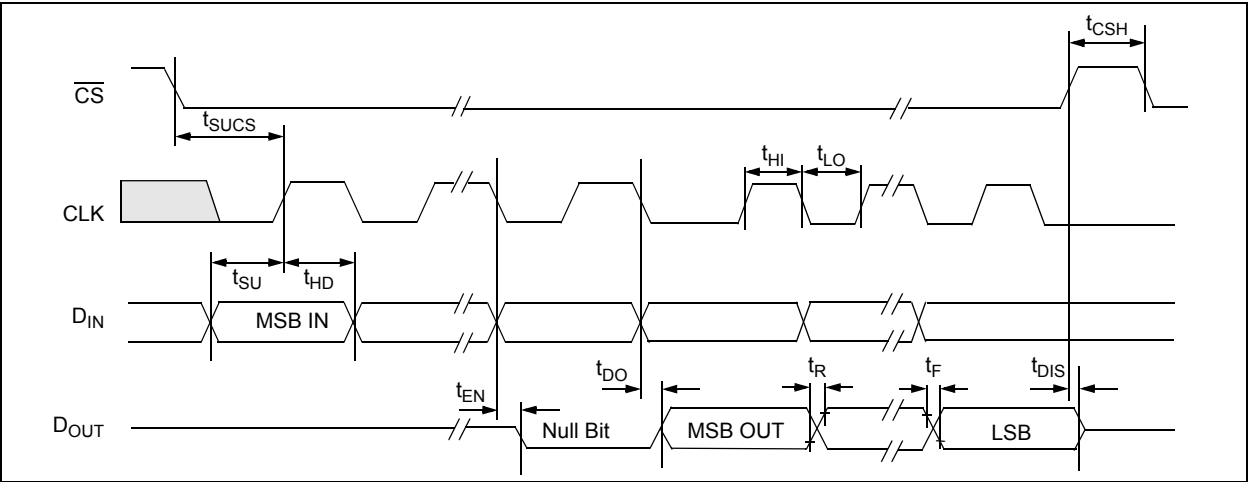
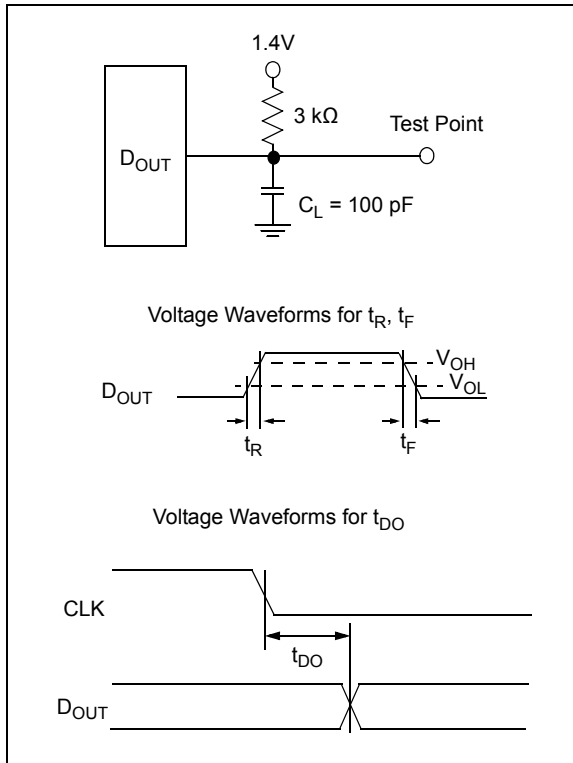
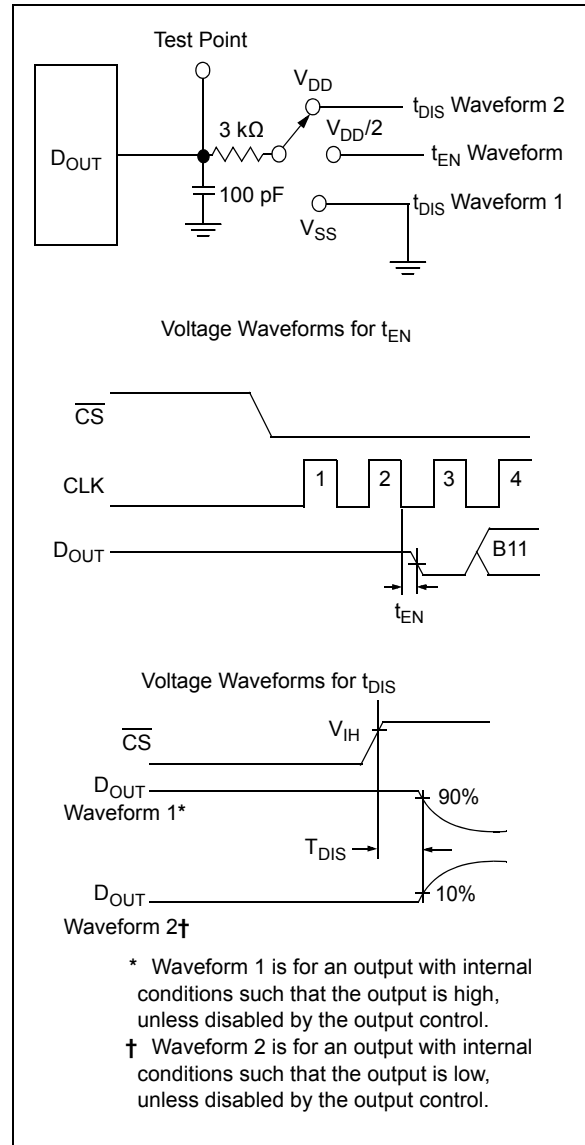


FIGURE 1-1: Serial Interface Timing.



**FIGURE 1-2:** Load Circuit for  $t_R, t_F, t_{DO}$ .



**FIGURE 1-3:** Load circuit for  $t_{DIS}$  and  $t_{EN}$ .

# MCP3204/3208

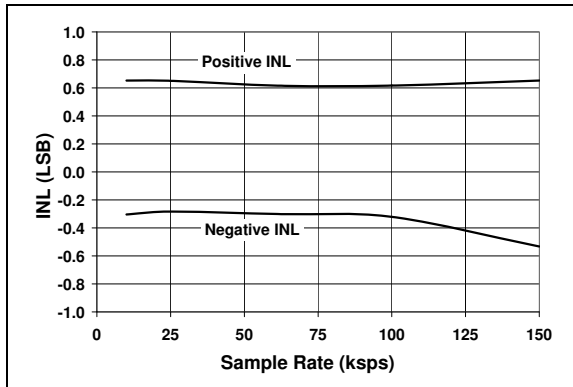
---

NOTES:

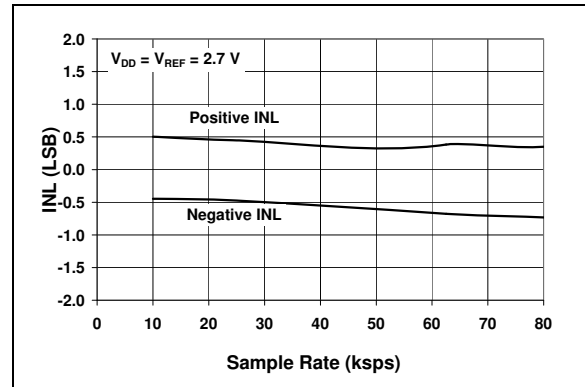
## 2.0 TYPICAL PERFORMANCE CHARACTERISTICS

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

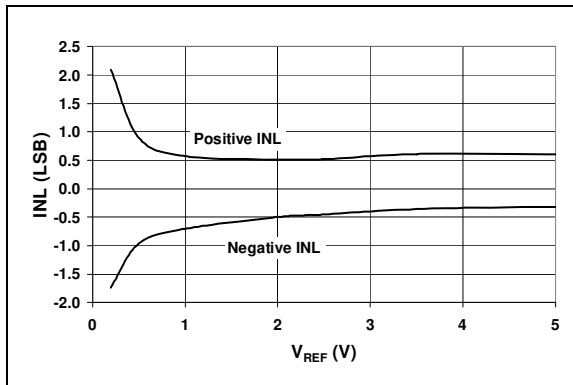
**Note:** Unless otherwise indicated,  $V_{DD} = V_{REF} = 5V$ ,  $V_{SS} = 0V$ ,  $f_{SAMPLE} = 100$  kps,  $f_{CLK} = 20 * f_{SAMPLE}$ ,  $T_A = +25^{\circ}C$ .



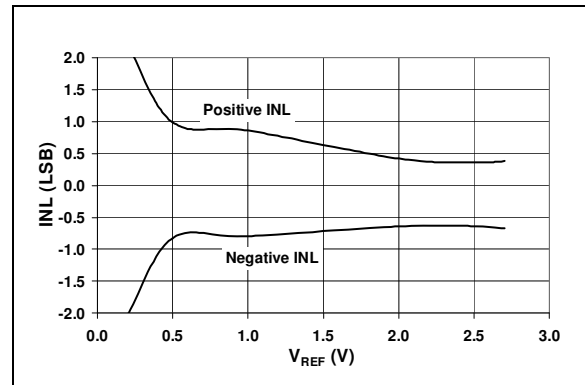
**FIGURE 2-1:** Integral Nonlinearity (INL) vs. Sample Rate.



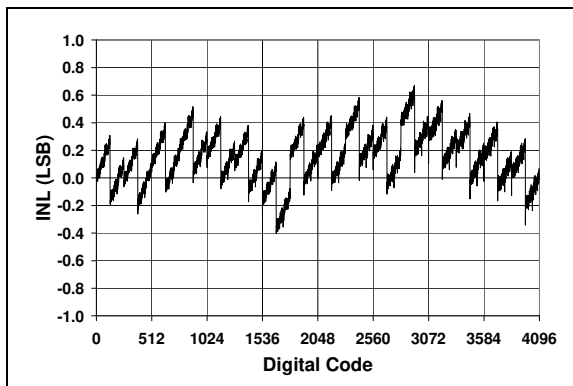
**FIGURE 2-4:** Integral Nonlinearity (INL) vs. Sample Rate ( $V_{DD} = 2.7V$ ).



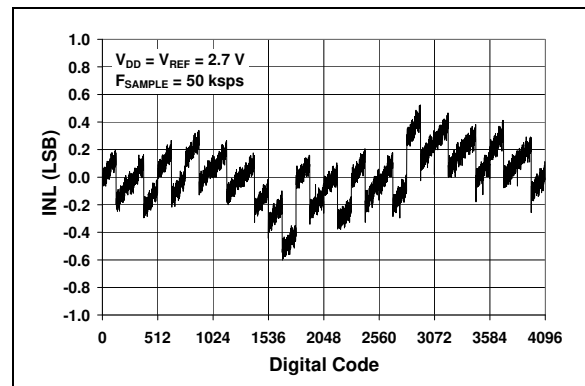
**FIGURE 2-2:** Integral Nonlinearity (INL) vs.  $V_{REF}$ .



**FIGURE 2-5:** Integral Nonlinearity (INL) vs.  $V_{REF}$  ( $V_{DD} = 2.7V$ ).



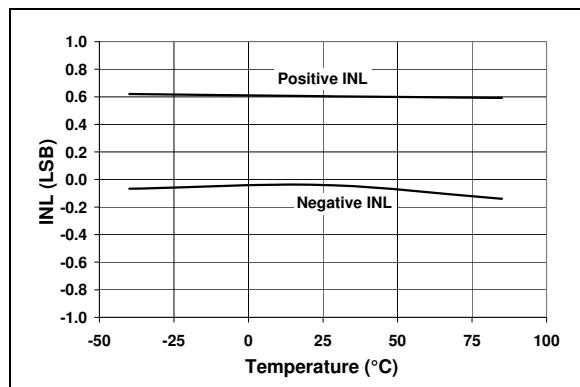
**FIGURE 2-3:** Integral Nonlinearity (INL) vs. Code (Representative Part).



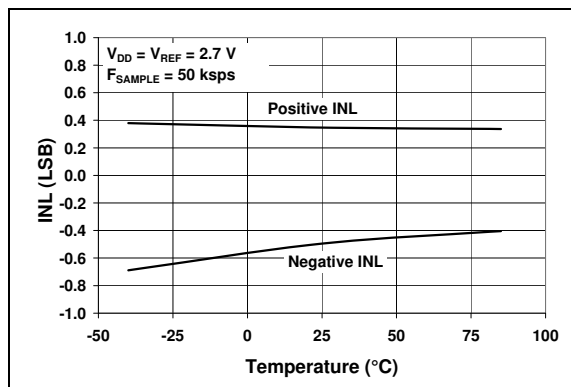
**FIGURE 2-6:** Integral Nonlinearity (INL) vs. Code (Representative Part,  $V_{DD} = 2.7V$ ).

# MCP3204/3208

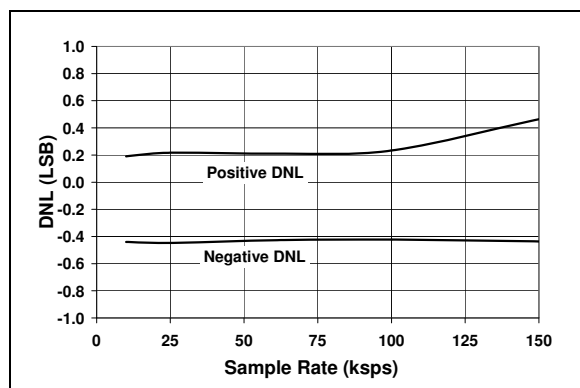
**Note:** Unless otherwise indicated,  $V_{DD} = V_{REF} = 5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $f_{SAMPLE} = 100\text{ kpsps}$ ,  $f_{CLK} = 20 * f_{SAMPLE}$ ,  $T_A = +25^\circ\text{C}$ .



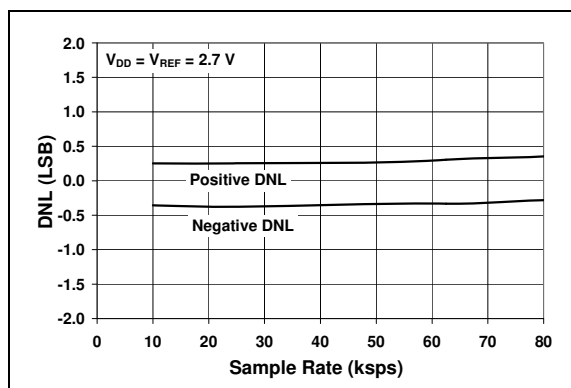
**FIGURE 2-7:** Integral Nonlinearity (INL) vs. Temperature.



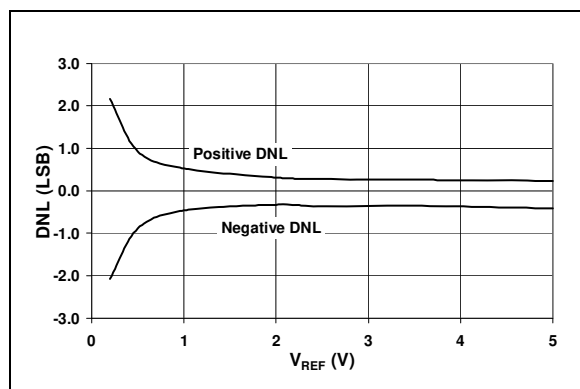
**FIGURE 2-10:** Integral Nonlinearity (INL) vs. Temperature ( $V_{DD} = 2.7\text{V}$ ).



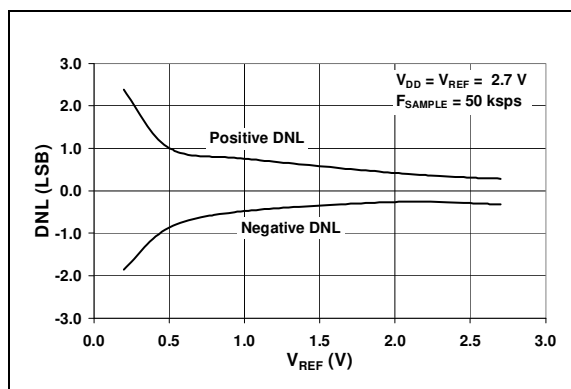
**FIGURE 2-8:** Differential Nonlinearity (DNL) vs. Sample Rate.



**FIGURE 2-11:** Differential Nonlinearity (DNL) vs. Sample Rate ( $V_{DD} = 2.7\text{V}$ ).

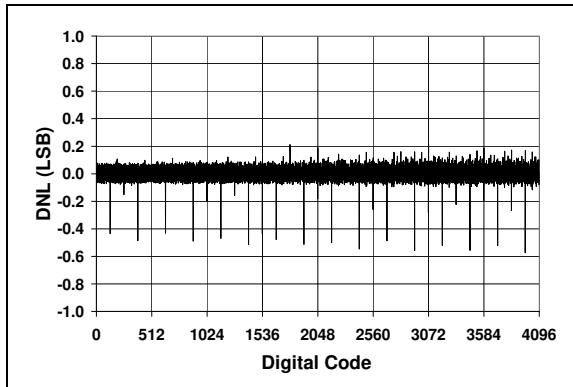


**FIGURE 2-9:** Differential Nonlinearity (DNL) vs.  $V_{REF}$ .

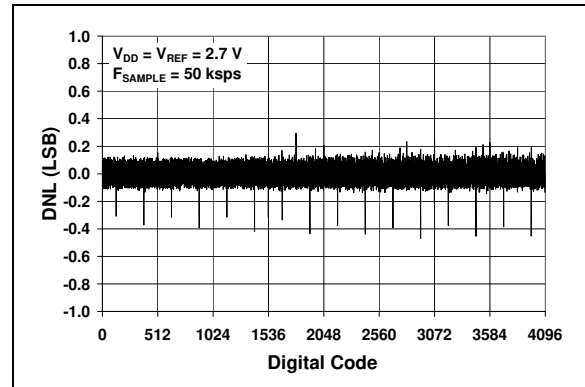


**FIGURE 2-12:** Differential Nonlinearity (DNL) vs.  $V_{REF}$  ( $V_{DD} = 2.7\text{V}$ ).

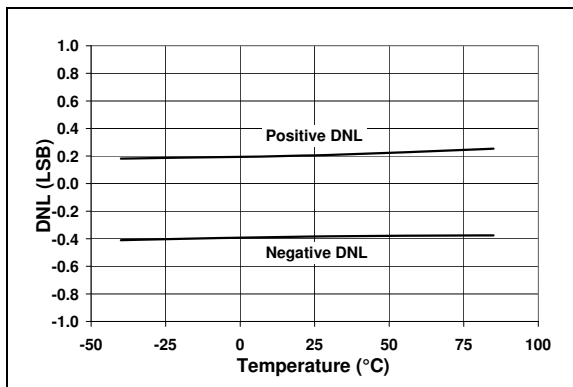
**Note:** Unless otherwise indicated,  $V_{DD} = V_{REF} = 5V$ ,  $V_{SS} = 0V$ ,  $f_{SAMPLE} = 100$  kps,  $f_{CLK} = 20 * f_{SAMPLE}$ ,  $T_A = +25^{\circ}C$ .



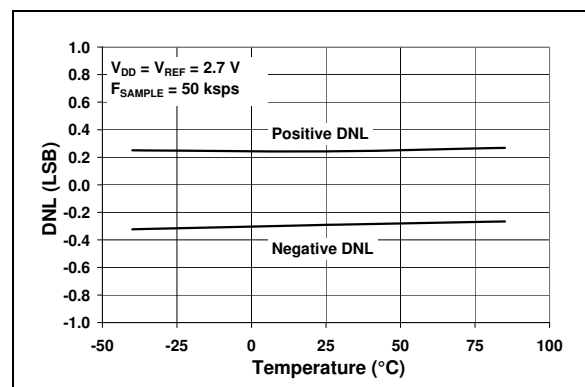
**FIGURE 2-13:** Differential Nonlinearity (DNL) vs. Code (Representative Part).



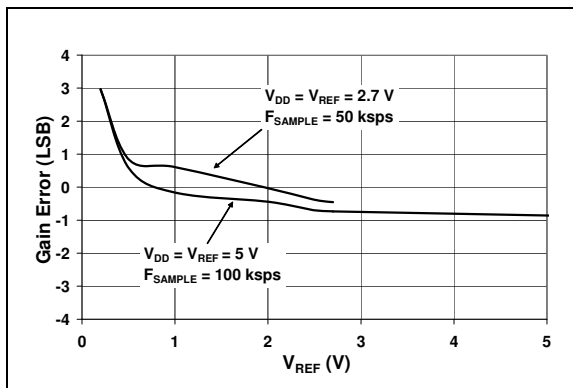
**FIGURE 2-16:** Differential Nonlinearity (DNL) vs. Code (Representative Part,  $V_{DD} = 2.7V$ ).



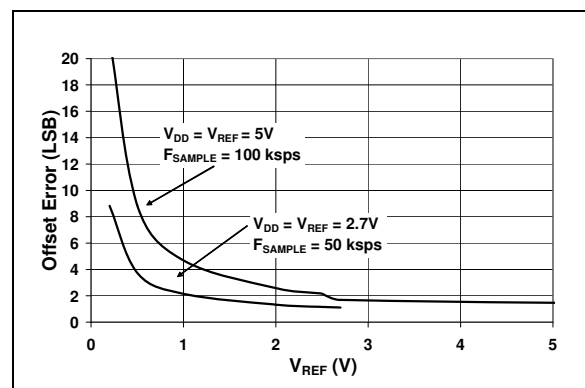
**FIGURE 2-14:** Differential Nonlinearity (DNL) vs. Temperature.



**FIGURE 2-17:** Differential Nonlinearity (DNL) vs. Temperature ( $V_{DD} = 2.7V$ ).



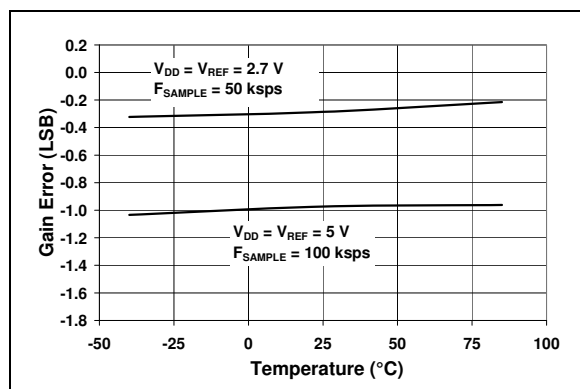
**FIGURE 2-15:** Gain Error vs.  $V_{REF}$ .



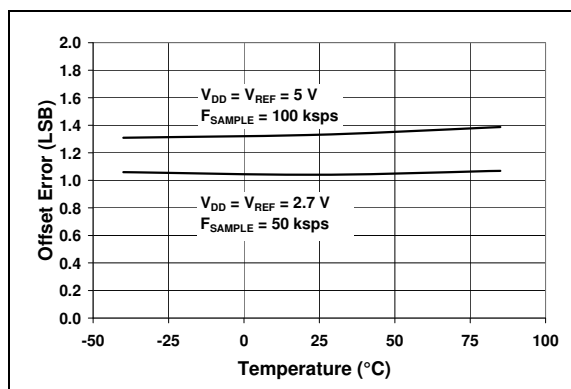
**FIGURE 2-18:** Offset Error vs.  $V_{REF}$ .

# MCP3204/3208

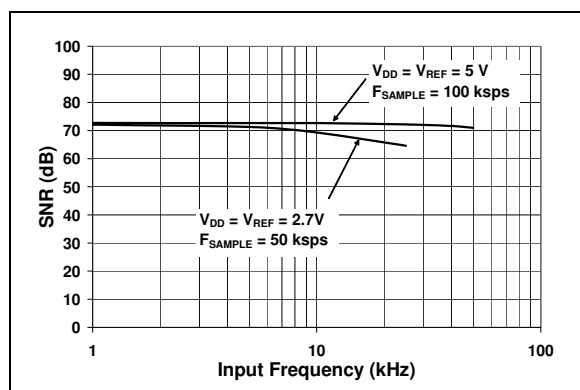
**Note:** Unless otherwise indicated,  $V_{DD} = V_{REF} = 5V$ ,  $V_{SS} = 0V$ ,  $f_{SAMPLE} = 100 \text{ kps}$ ,  $f_{CLK} = 20 * f_{SAMPLE}$ ,  $T_A = +25^\circ C$ .



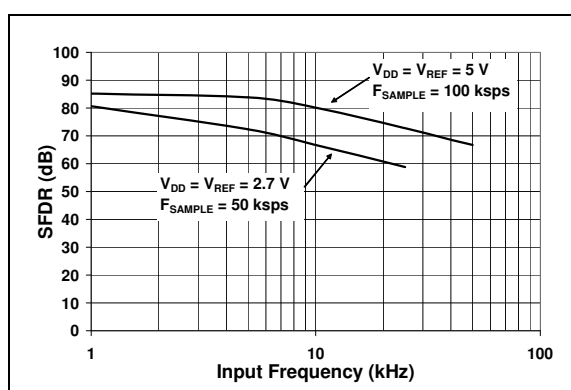
**FIGURE 2-19:** Gain Error vs. Temperature.



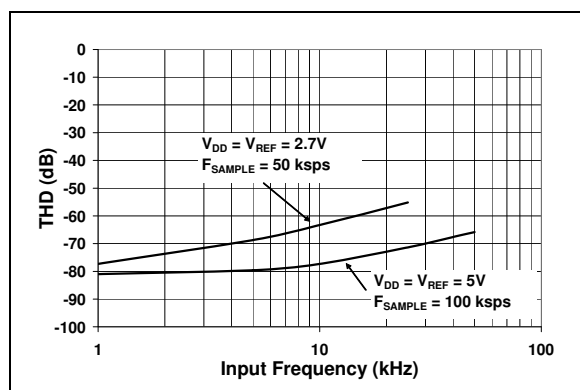
**FIGURE 2-22:** Offset Error vs. Temperature.



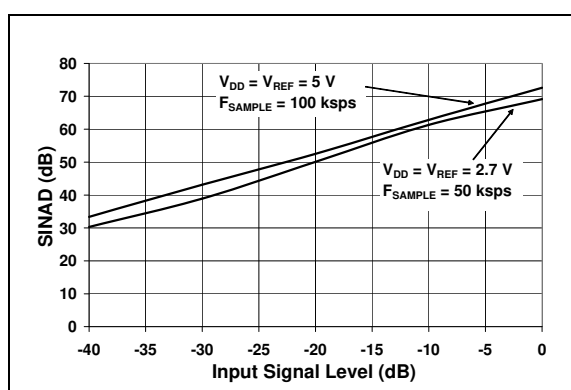
**FIGURE 2-20:** Signal-to-Noise (SNR) vs. Input Frequency.



**FIGURE 2-23:** Signal-to-Noise and Distortion (SINAD) vs. Input Frequency.

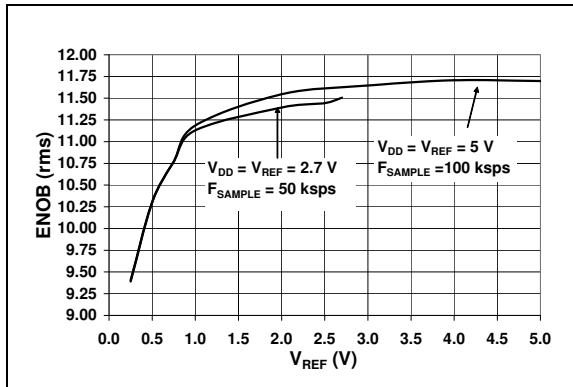


**FIGURE 2-21:** Total Harmonic Distortion (THD) vs. Input Frequency.

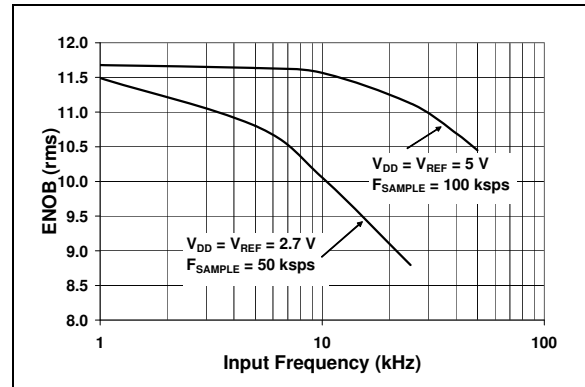


**FIGURE 2-24:** Signal-to-Noise and Distortion (SINAD) vs. Input Signal Level.

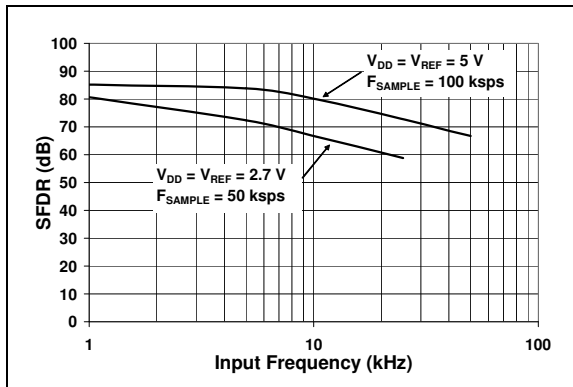
**Note:** Unless otherwise indicated,  $V_{DD} = V_{REF} = 5V$ ,  $V_{SS} = 0V$ ,  $f_{SAMPLE} = 100$  ksp/s,  $f_{CLK} = 20 * f_{SAMPLE}$ ,  $T_A = +25^{\circ}C$ .



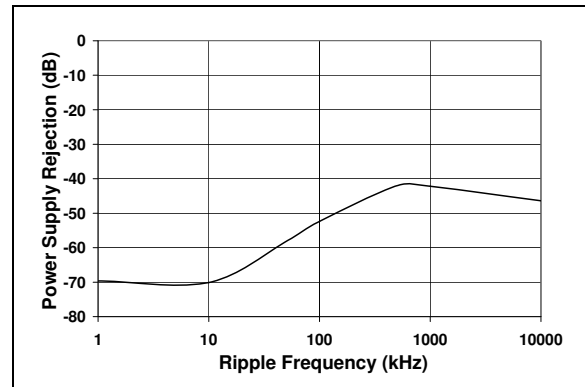
**FIGURE 2-25:** Effective Number of Bits (ENOB) vs.  $V_{REF}$



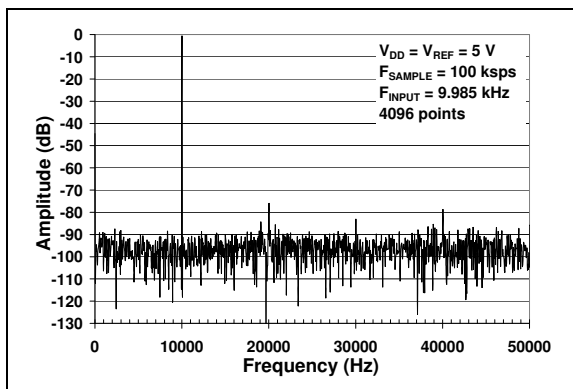
**FIGURE 2-28:** Effective Number of Bits (ENOB) vs. Input Frequency.



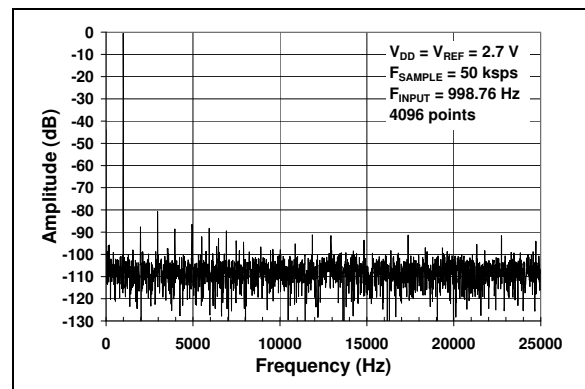
**FIGURE 2-26:** Spurious Free Dynamic Range (SFDR) vs. Input Frequency.



**FIGURE 2-29:** Power Supply Rejection (PSR) vs. Ripple Frequency.



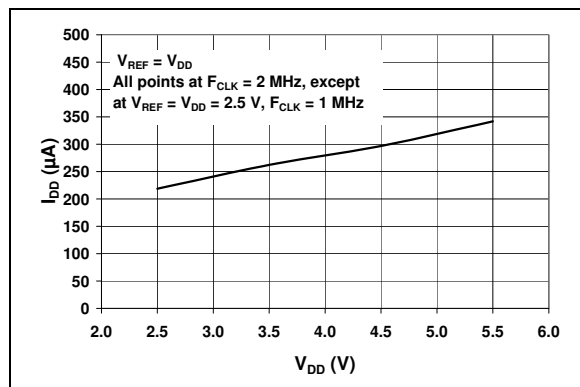
**FIGURE 2-27:** Frequency Spectrum of 10 kHz input (Representative Part).



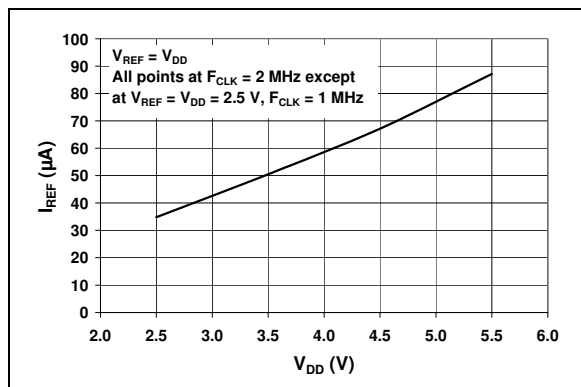
**FIGURE 2-30:** Frequency Spectrum of 1 kHz input (Representative Part,  $V_{DD} = 2.7V$ ).

# MCP3204/3208

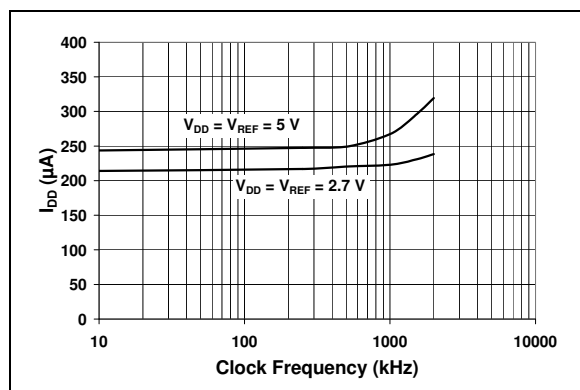
**Note:** Unless otherwise indicated,  $V_{DD} = V_{REF} = 5V$ ,  $V_{SS} = 0V$ ,  $f_{SAMPLE} = 100$  ksp/s,  $f_{CLK} = 20 * f_{SAMPLE}$ ,  $T_A = +25^{\circ}C$ .



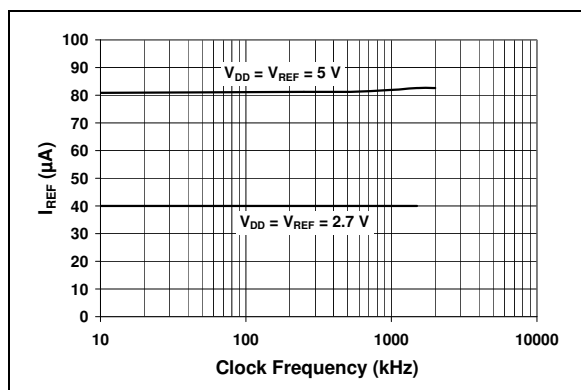
**FIGURE 2-31:**  $I_{DD}$  vs.  $V_{DD}$ .



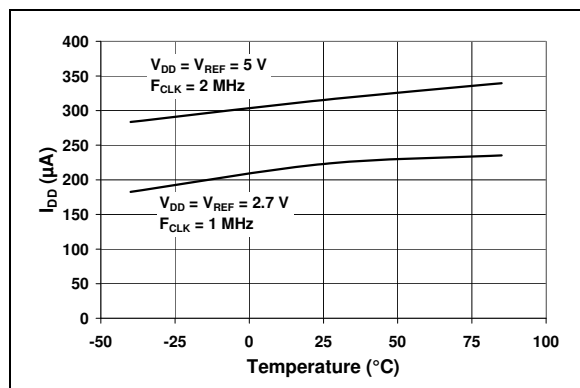
**FIGURE 2-34:**  $I_{REF}$  vs.  $V_{DD}$ .



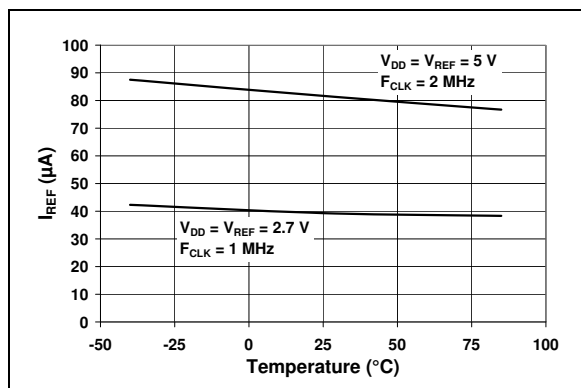
**FIGURE 2-32:**  $I_{DD}$  vs. Clock Frequency.



**FIGURE 2-35:**  $I_{REF}$  vs. Clock Frequency.

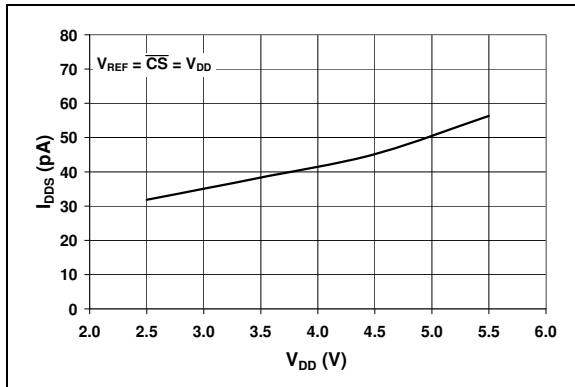


**FIGURE 2-33:**  $I_{DD}$  vs. Temperature.

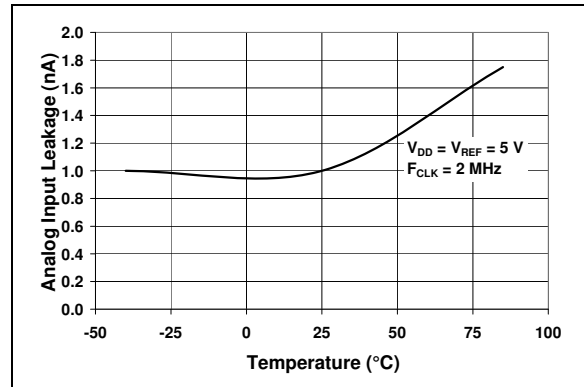


**FIGURE 2-36:**  $I_{REF}$  vs. Temperature.

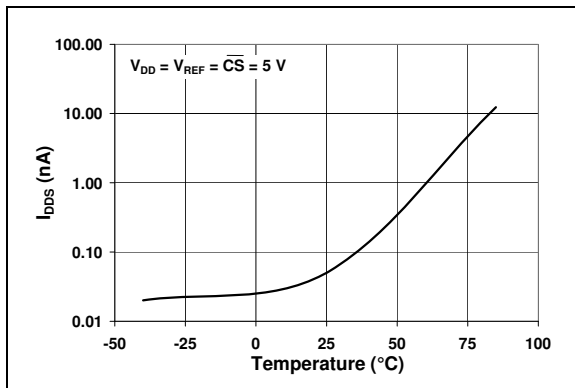
**Note:** Unless otherwise indicated,  $V_{DD} = V_{REF} = 5V$ ,  $V_{SS} = 0V$ ,  $f_{SAMPLE} = 100$  ksp/s,  $f_{CLK} = 20 * f_{SAMPLE}$ ,  $T_A = +25^{\circ}C$ .



**FIGURE 2-37:**  $I_{DDs}$  vs.  $V_{DD}$ .



**FIGURE 2-39:** Analog Input Leakage Current vs. Temperature.



**FIGURE 2-38:**  $I_{DDs}$  vs. Temperature.

# MCP3204/3208

---

NOTES:

## 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

**TABLE 3-1: PIN FUNCTION TABLE**

| MCP3204           | MCP3208    | Symbol                             | Definition                 |
|-------------------|------------|------------------------------------|----------------------------|
| PDIP, SOIC, TSSOP | PDIP, SOIC |                                    |                            |
| 1                 | 1          | CH0                                | Analog Input               |
| 2                 | 2          | CH1                                | Analog Input               |
| 3                 | 3          | CH2                                | Analog Input               |
| 4                 | 4          | CH3                                | Analog Input               |
| —                 | 5          | CH4                                | Analog Input               |
| —                 | 6          | CH5                                | Analog Input               |
| —                 | 7          | CH6                                | Analog Input               |
| —                 | 8          | CH7                                | Analog Input               |
| 7                 | 9          | DGND                               | Digital Ground             |
| 8                 | 10         | $\overline{\text{CS}}/\text{SHDN}$ | Chip Select/Shutdown Input |
| 9                 | 11         | D <sub>IN</sub>                    | Serial Data In             |
| 10                | 12         | D <sub>OUT</sub>                   | Serial Data Out            |
| 11                | 13         | CLK                                | Serial Clock               |
| 12                | 14         | AGND                               | Analog Ground              |
| 13                | 15         | V <sub>REF</sub>                   | Reference Voltage Input    |
| 14                | 16         | V <sub>DD</sub>                    | +2.7V to 5.5V Power Supply |
| 5, 6              | —          | NC                                 | No Connection              |

### 3.1 Digital Ground (DGND)

Digital ground connection to internal digital circuitry.

### 3.2 Analog Ground (AGND)

Analog ground connection to internal analog circuitry.

### 3.3 Analog Inputs (CH0 - CH7)

Analog inputs for channels 0 - 7 for the multiplexed inputs. Each pair of channels can be programmed to be used as two independent channels in single-ended mode or as a single pseudo-differential input, where one channel is IN+ and one channel is IN. See [Section 4.1 “Analog Inputs”](#), “Analog Inputs”, and [Section 5.0 “Serial communications”](#), “Serial Communications”, for information on programming the channel configuration.

### 3.4 Serial Clock (CLK)

The SPI clock pin is used to initiate a conversion and clock out each bit of the conversion as it takes place. See [Section 6.2 “Maintaining Minimum Clock Speed”](#), “Maintaining Minimum Clock Speed”, for constraints on clock speed.

### 3.5 Serial Data Input (D<sub>IN</sub>)

The SPI port serial data input pin is used to load channel configuration data into the device.

### 3.6 Serial Data Output (D<sub>OUT</sub>)

The SPI serial data output pin is used to shift out the results of the A/D conversion. Data will always change on the falling edge of each clock as the conversion takes place.

### 3.7 Chip Select/Shutdown ( $\overline{\text{CS}}/\text{SHDN}$ )

The  $\overline{\text{CS}}/\text{SHDN}$  pin is used to initiate communication with the device when pulled low and will end a conversion and put the device in low power standby when pulled high. The  $\overline{\text{CS}}/\text{SHDN}$  pin must be pulled high between conversions.

# MCP3204/3208

---

NOTES:

## 4.0 DEVICE OPERATION

The MCP3204/3208 A/D converters employ a conventional SAR architecture. With this architecture, a sample is acquired on an internal sample/hold capacitor for 1.5 clock cycles starting on the fourth rising edge of the serial clock after the start bit has been received. Following this sample time, the device uses the collected charge on the internal sample/hold capacitor to produce a serial 12-bit digital output code. Conversion rates of 100 ksp/s are possible on the MCP3204/3208. See **Section 6.2 “Maintaining Minimum Clock Speed”**, “Maintaining Minimum Clock Speed”, for information on minimum clock rates. Communication with the device is accomplished using a 4-wire SPI-compatible interface.

### 4.1 Analog Inputs

The MCP3204/3208 devices offer the choice of using the analog input channels configured as single-ended inputs or pseudo-differential pairs. The MCP3204 can be configured to provide two pseudo-differential input pairs or four single-ended inputs, while the MCP3208 can be configured to provide four pseudo-differential input pairs or eight single-ended inputs. Configuration is done as part of the serial command before each conversion begins. When used in the pseudo-differential mode, each channel pair (i.e., CH0 and CH1, CH2 and CH3 etc.) is programmed to be the IN+ and IN- inputs as part of the command string transmitted to the device. The IN+ input can range from IN- to ( $V_{REF} + IN-$ ). The IN- input is limited to  $\pm 100$  mV from the  $V_{SS}$  rail. The IN- input can be used to cancel small signal common-mode noise which is present on both the IN+ and IN- inputs.

When operating in the pseudo-differential mode, if the voltage level of IN+ is equal to or less than IN-, the resultant code will be 000h. If the voltage at IN+ is equal to or greater than  $\{[V_{REF} + (IN-)] - 1 \text{ LSB}\}$ , then the output code will be FFFh. If the voltage level at IN- is more than 1 LSB below  $V_{SS}$ , the voltage level at the IN+ input will have to go below  $V_{SS}$  to see the 000h output code. Conversely, if IN- is more than 1 LSB above  $V_{SS}$ , then the FFFh code will not be seen unless the IN+ input level goes above  $V_{REF}$  level.

For the A/D converter to meet specification, the charge holding capacitor ( $C_{SAMPLE}$ ) must be given enough time to acquire a 12-bit accurate voltage level during the 1.5 clock cycle sampling period. The analog input model is shown in [Figure 4-1](#).

This diagram illustrates that the source impedance ( $R_S$ ) adds to the internal sampling switch ( $R_{SS}$ ) impedance, directly effecting the time that is required to charge the capacitor ( $C_{SAMPLE}$ ). Consequently, larger source impedances increase the offset, gain and integral linearity errors of the conversion (see [Figure 4-2](#)).

### 4.2 Reference Input

For each device in the family, the reference input ( $V_{REF}$ ) determines the analog input voltage range. As the reference input is reduced, the LSB size is reduced accordingly. The theoretical digital output code produced by the A/D converter is a function of the analog input signal and the reference input, as shown below.

#### EQUATION 4-1:

$$\text{Digital Output Code} = \frac{4096 \times V_{IN}}{V_{REF}}$$

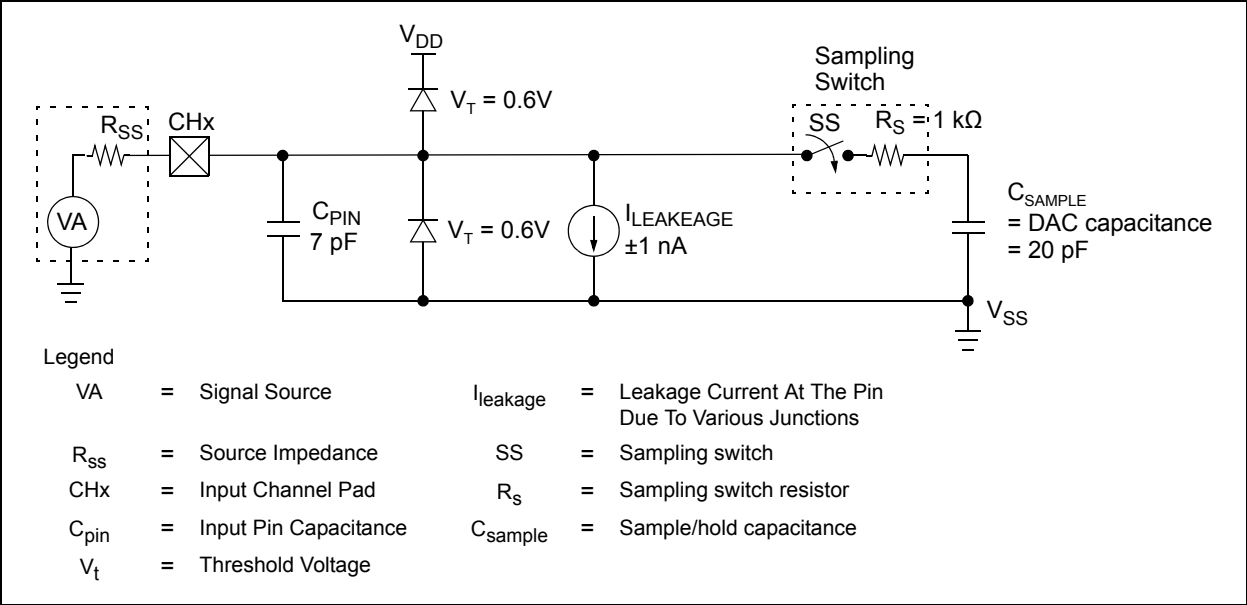
Where:

$V_{IN}$  = analog input voltage

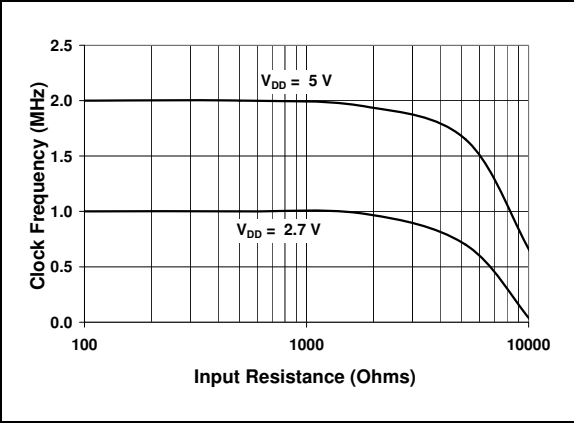
$V_{REF}$  = reference voltage

When using an external voltage reference device, the system designer should always refer to the manufacturer's recommendations for circuit layout. Any instability in the operation of the reference device will have a direct effect on the operation of the A/D converter.

# MCP3204/3208



**FIGURE 4-1:** Analog Input Model.



**FIGURE 4-2:** Maximum Clock Frequency vs. Input resistance (R<sub>S</sub>) to maintain less than a 0.1 LSB deviation in INL from nominal conditions.

## 5.0 SERIAL COMMUNICATIONS

Communication with the MCP3204/3208 devices is accomplished using a standard SPI-compatible serial interface. Initiating communication with either device is done by bringing the  $\overline{CS}$  line low (see Figure 5-1). If the device was powered up with the  $\overline{CS}$  pin low, it must be brought high and back low to initiate communication. The first clock received with  $\overline{CS}$  low and  $D_{IN}$  high will constitute a start bit. The SGL/DIFF bit follows the start bit and will determine if the conversion will be done using single-ended or differential input mode. The next three bits (D0, D1 and D2) are used to select the input channel configuration. Table 5-1 and Table 5-2 show the configuration bits for the MCP3204 and MCP3208, respectively. The device will begin to sample the analog input on the fourth rising edge of the clock after the start bit has been received. The sample period will end on the falling edge of the fifth clock following the start bit.

Once the D0 bit is input, one more clock is required to complete the sample and hold period ( $D_{IN}$  is a “don’t care” for this clock). On the falling edge of the next clock, the device will output a low null bit. The next 12 clocks will output the result of the conversion with MSB first, as shown in Figure 5-1. Data is always output from the device on the falling edge of the clock. If all 12 data bits have been transmitted and the device continues to receive clocks while the  $\overline{CS}$  is held low, the device will output the conversion result LSB first, as shown in Figure 5-2. If more clocks are provided to the device while  $\overline{CS}$  is still low (after the LSB first data has been transmitted), the device will clock out zeros indefinitely.

If necessary, it is possible to bring  $\overline{CS}$  low and clock in leading zeros on the  $D_{IN}$  line before the start bit. This is often done when dealing with microcontroller-based SPI ports that must send 8 bits at a time. Refer to Section 6.1 “Using the MCP3204/3208 with Microcontroller (MCU) SPI Ports” for more details on using the MCP3204/3208 devices with hardware SPI ports.

TABLE 5-1: CONFIGURATION BITS FOR THE MCP3204

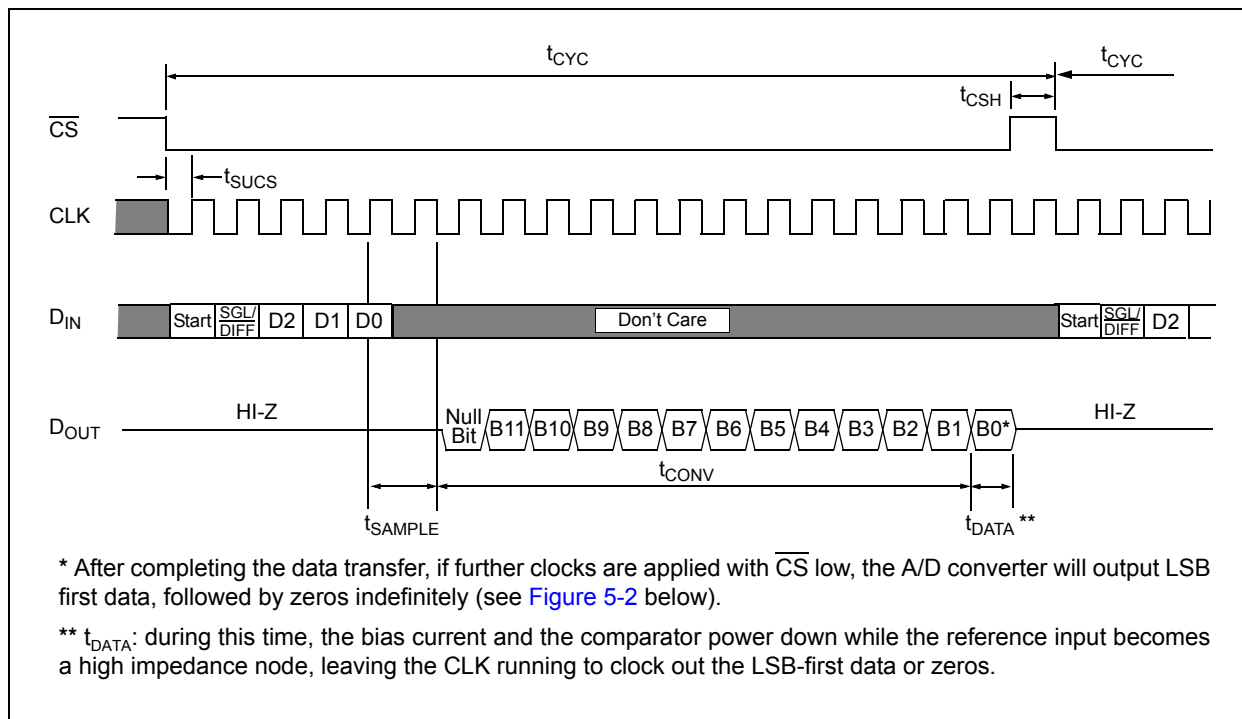
| Control Bit Selections |     |    |    | Input Configuration | Channel Selection      |
|------------------------|-----|----|----|---------------------|------------------------|
| Single/Diff            | D2* | D1 | D0 |                     |                        |
| 1                      | X   | 0  | 0  | single-ended        | CH0                    |
| 1                      | X   | 0  | 1  | single-ended        | CH1                    |
| 1                      | X   | 1  | 0  | single-ended        | CH2                    |
| 1                      | X   | 1  | 1  | single-ended        | CH3                    |
| 0                      | X   | 0  | 0  | differential        | CH0 = IN+<br>CH1 = IN- |
| 0                      | X   | 0  | 1  | differential        | CH0 = IN-<br>CH1 = IN+ |
| 0                      | X   | 1  | 0  | differential        | CH2 = IN+<br>CH3 = IN- |
| 0                      | X   | 1  | 1  | differential        | CH2 = IN-<br>CH3 = IN+ |

\* D2 is a “don’t care” for MCP3204

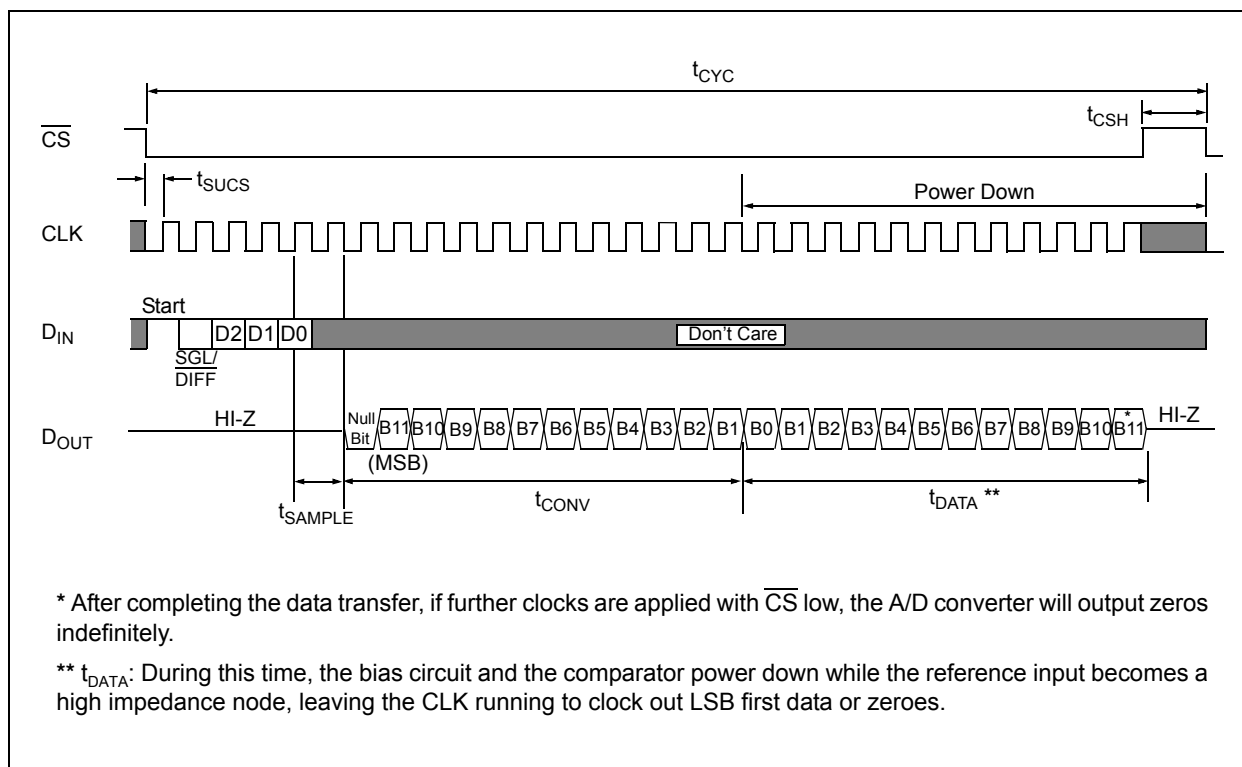
TABLE 5-2: CONFIGURATION BITS FOR THE MCP3208

| Control Bit Selections |    |    |    | Input Configuration | Channel Selection      |
|------------------------|----|----|----|---------------------|------------------------|
| Single/Diff            | D2 | D1 | D0 |                     |                        |
| 1                      | 0  | 0  | 0  | single-ended        | CH0                    |
| 1                      | 0  | 0  | 1  | single-ended        | CH1                    |
| 1                      | 0  | 1  | 0  | single-ended        | CH2                    |
| 1                      | 0  | 1  | 1  | single-ended        | CH3                    |
| 1                      | 1  | 0  | 0  | single-ended        | CH4                    |
| 1                      | 1  | 0  | 1  | single-ended        | CH5                    |
| 1                      | 1  | 1  | 0  | single-ended        | CH6                    |
| 1                      | 1  | 1  | 1  | single-ended        | CH7                    |
| 0                      | 0  | 0  | 0  | differential        | CH0 = IN+<br>CH1 = IN- |
| 0                      | 0  | 0  | 1  | differential        | CH0 = IN-<br>CH1 = IN+ |
| 0                      | 0  | 1  | 0  | differential        | CH2 = IN+<br>CH3 = IN- |
| 0                      | 0  | 1  | 1  | differential        | CH2 = IN-<br>CH3 = IN+ |
| 0                      | 1  | 0  | 0  | differential        | CH4 = IN+<br>CH5 = IN- |
| 0                      | 1  | 0  | 1  | differential        | CH4 = IN-<br>CH5 = IN+ |
| 0                      | 1  | 1  | 0  | differential        | CH6 = IN+<br>CH7 = IN- |
| 0                      | 1  | 1  | 1  | differential        | CH6 = IN-<br>CH7 = IN+ |

# MCP3204/3208



**FIGURE 5-1:** Communication with the MCP3204 or MCP3208.



**FIGURE 5-2:** Communication with MCP3204 or MCP3208 in LSB First Format.

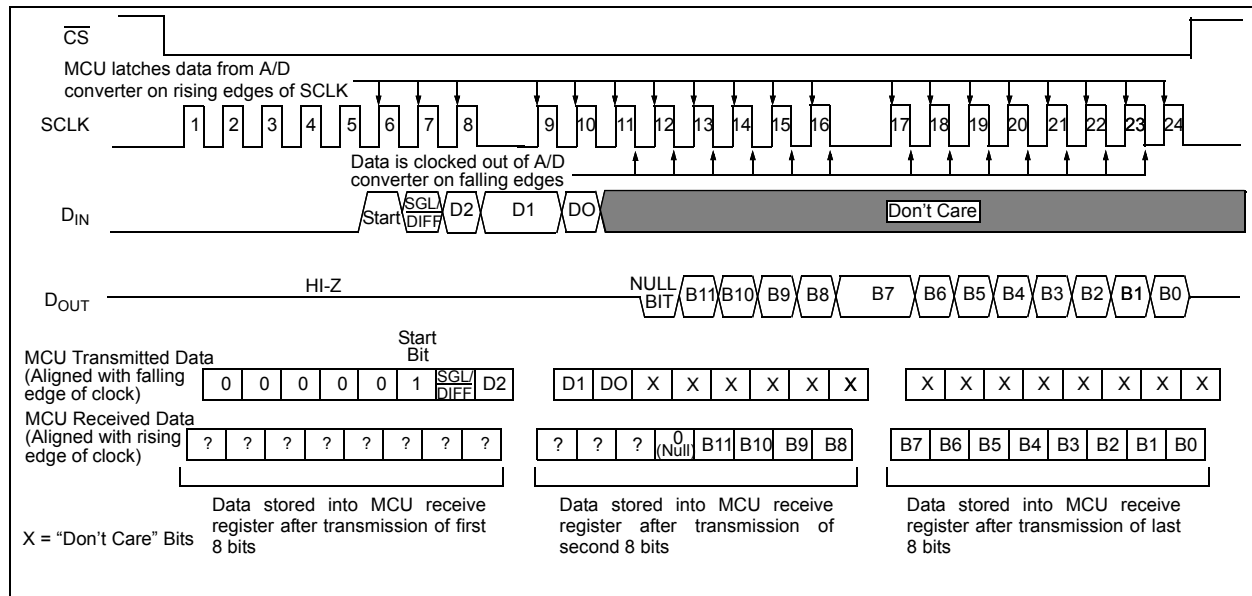
## 6.0 APPLICATIONS INFORMATION

### 6.1 Using the MCP3204/3208 with Microcontroller (MCU) SPI Ports

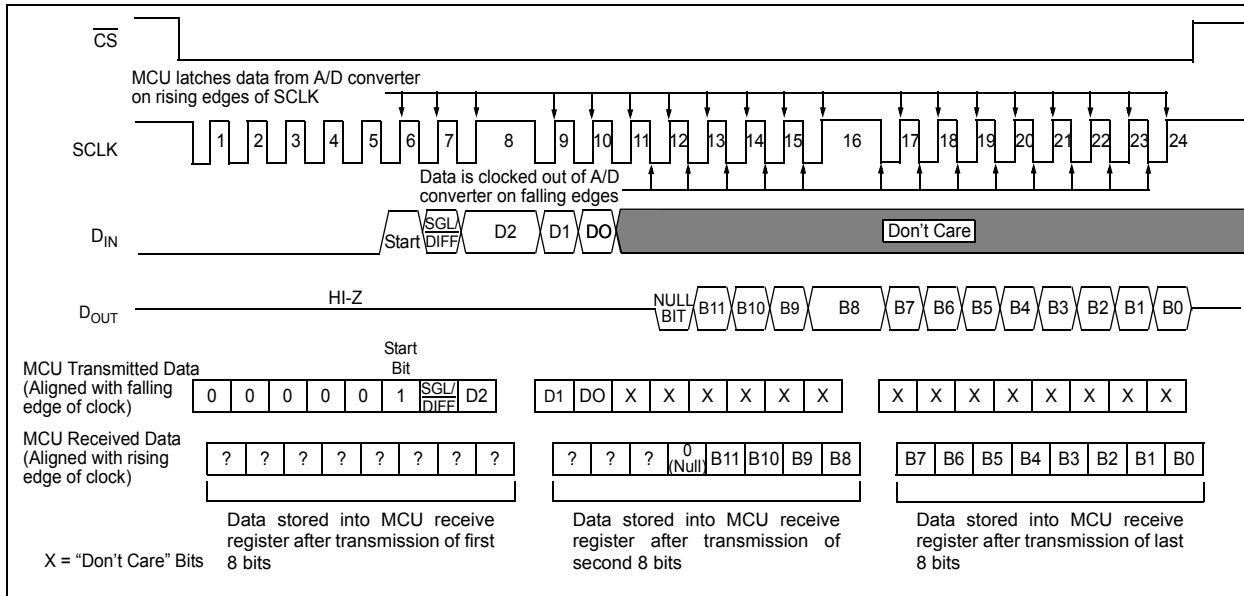
With most microcontroller SPI ports, it is required to send groups of eight bits. It is also required that the microcontroller SPI port be configured to clock out data on the falling edge of clock and latch data in on the rising edge. Because communication with the MCP3204/3208 devices may not need multiples of eight clocks, it will be necessary to provide more clocks than are required. This is usually done by sending 'leading zeros' before the start bit. As an example, [Figure 6-1](#) and [Figure 6-2](#) illustrate how the MCP3204/3208 can be interfaced to a MCU with a hardware SPI port. [Figure 6-1](#) depicts the operation shown in SPI Mode 0,0, which requires that the SCLK from the MCU idles in the 'low' state, while [Figure 6-2](#) shows the similar case of SPI Mode 1,1, where the clock idles in the 'high' state.

As is shown in [Figure 6-1](#), the first byte transmitted to the A/D converter contains five leading zeros before the start bit. Arranging the leading zeros this way allows the output 12 bits to fall in positions easily manipulated by the MCU. The MSB is clocked out of the A/D converter on the falling edge of clock number 12. Once the second eight clocks have been sent to the device, the MCU's receive buffer will contain three unknown bits (the output is at high impedance for the first two clocks), the null bit and the highest order four bits of the conversion. Once the third byte has been sent to the device, the receive register will contain the lowest order eight bits of the conversion results. Employing this method ensures simpler manipulation of the converted data.

[Figure 6-2](#) shows the same thing in SPI Mode 1,1, which requires that the clock idles in the high state. As with mode 0,0, the A/D converter outputs data on the falling edge of the clock and the MCU latches data from the A/D converter in on the rising edge of the clock.



**FIGURE 6-1:** SPI Communication using 8-bit segments (Mode 0,0: SCLK idles low).



**FIGURE 6-2:** SPI Communication using 8-bit segments (Mode 1, 1: SCLK idles high).

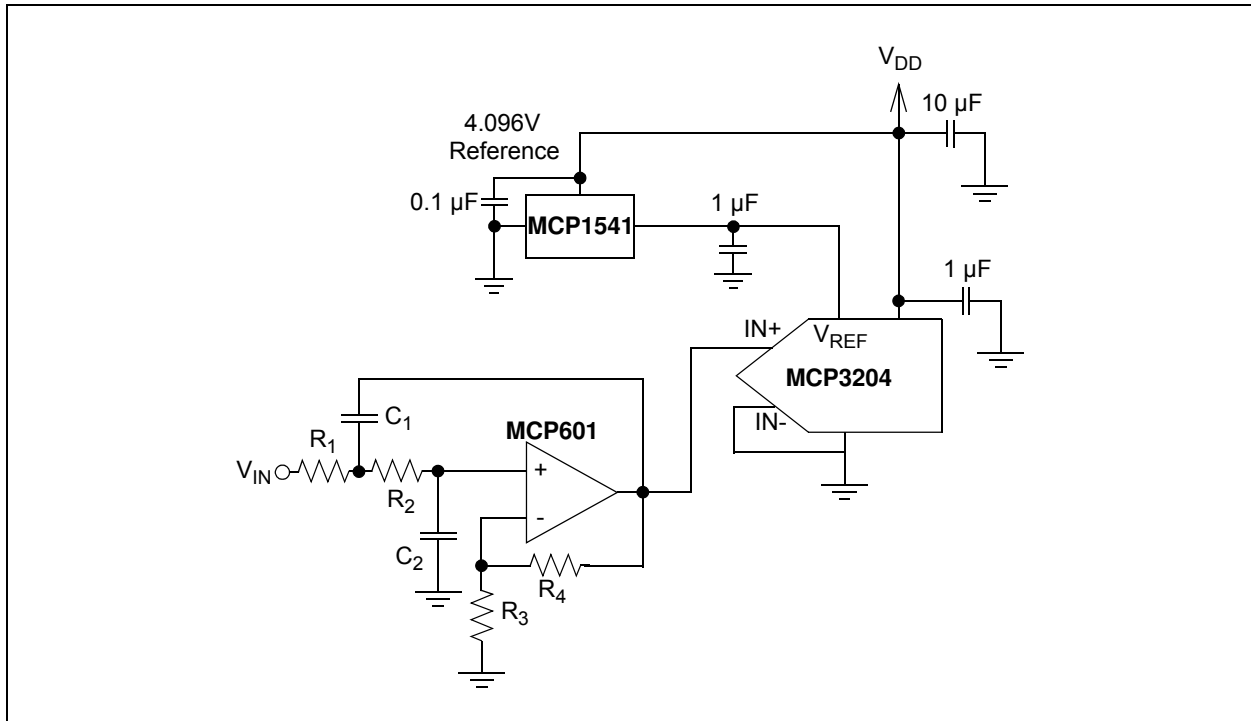
## 6.2 Maintaining Minimum Clock Speed

When the MCP3204/3208 initiates the sample period, charge is stored on the sample capacitor. When the sample period is complete, the device converts one bit for each clock that is received. It is important for the user to note that a slow clock rate will allow charge to bleed off the sample capacitor while the conversion is taking place. At 85°C (worst case condition), the part will maintain proper charge on the sample capacitor for at least 1.2 ms after the sample period has ended. This means that the time between the end of the sample period and the time that all 12 data bits have been clocked out must not exceed 1.2 ms (effective clock frequency of 10 kHz). Failure to meet this criterion may introduce linearity errors into the conversion outside the rated specifications. It should be noted that during the entire conversion cycle, the A/D converter does not require a constant clock speed or duty cycle, as long as all timing specifications are met.

## 6.3 Buffering/Filtering the Analog Inputs

If the signal source for the A/D converter is not a low impedance source, it will have to be buffered or inaccurate conversion results may occur (see [Figure 4-2](#)). It is also recommended that a filter be used to eliminate any signals that may be aliased back into the conversion results, as is illustrated in [Figure 6-3](#), where an op amp is used to drive the analog input of the MCP3204/3208. This amplifier provides a low impedance source for the converter input, and a low pass filter, which eliminates unwanted high frequency noise.

Low-pass (anti-aliasing) filters can be designed using Microchip's free interactive FilterLab® software. FilterLab will calculate capacitor and resistor values, as well as determine the number of poles that are required for the application. For more information on filtering signals, see AN699, "Anti-Aliasing Analog Filters for Data Acquisition Systems".



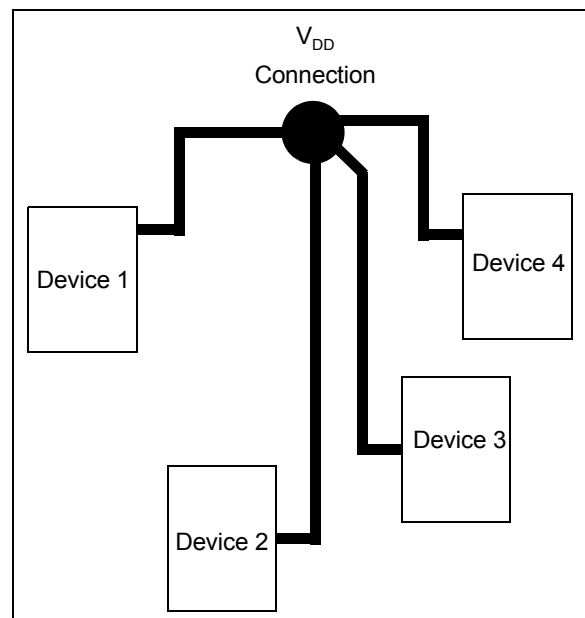
**FIGURE 6-3:** The MCP601 Operational Amplifier is used to implement a second order anti-aliasing filter for the signal being converted by the MCP3204.

## 6.4 Layout Considerations

When laying out a printed circuit board for use with analog components, care should be taken to reduce noise wherever possible. A bypass capacitor should always be used with this device, placed as close as possible to the device pin. A bypass capacitor value of 1  $\mu\text{F}$  is recommended.

Digital and analog traces should be separated as much as possible on the board, with no traces running underneath the device or the bypass capacitor. Extra precautions should be taken to keep traces with high frequency signals (such as clock lines) as far as possible from analog traces.

Use of an analog ground plane is recommended in order to keep the ground potential the same for all devices on the board. Providing  $V_{\text{DD}}$  connections to devices in a “star” configuration can also reduce noise by eliminating return current paths and associated errors (see Figure 6-4). For more information on layout tips when using A/D converters, refer to AN688, “Layout Tips for 12-Bit A/D converter Applications”.



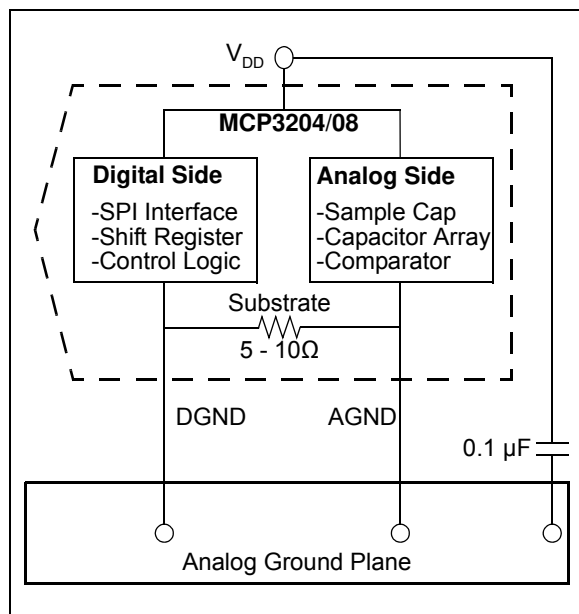
**FIGURE 6-4:**  $V_{\text{DD}}$  traces arranged in a ‘Star’ configuration in order to reduce errors caused by current return paths.

# MCP3204/3208

## 6.5 Utilizing the Digital and Analog Ground Pins

The MCP3204/3208 devices provide both digital and analog ground connections to provide another means of noise reduction. As shown in Figure 6-5, the analog and digital circuitry is separated internal to the device. This reduces noise from the digital portion of the device being coupled into the analog portion of the device. The two grounds are connected internally through the substrate, which has a resistance of 5 -10 $\Omega$ .

If no ground plane is utilized, then both grounds must be connected to  $V_{SS}$  on the board. If a ground plane is available, both digital and analog ground pins should be connected to the analog ground plane. If both an analog and a digital ground plane are available, both the digital and the analog ground pins should be connected to the analog ground plane. Following these steps will reduce the amount of digital noise from the rest of the board being coupled into the A/D converter.

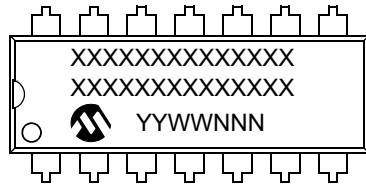


**FIGURE 6-5:** Separation of Analog and Digital Ground Pins.

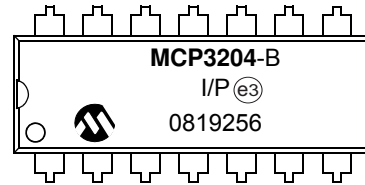
## 7.0 PACKAGING INFORMATION

### 7.1 Package Marking Information

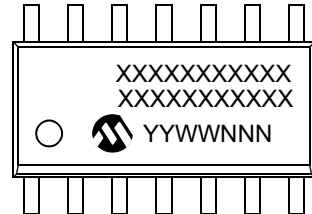
14-Lead PDIP (300 mil) (MCP3204)



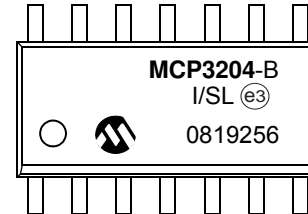
Example:



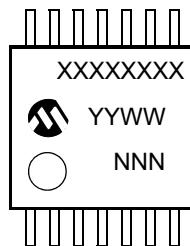
14-Lead SOIC (150 mil) (MCP3204)



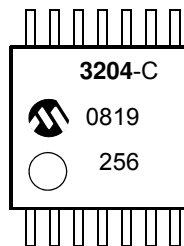
Example:



14-Lead TSSOP (4.4mm)\* (MCP3204)



Example:



|                |        |                                                                                                                  |
|----------------|--------|------------------------------------------------------------------------------------------------------------------|
| <b>Legend:</b> | XX...X | Customer-specific information                                                                                    |
|                | Y      | Year code (last digit of calendar year)                                                                          |
|                | YY     | Year code (last 2 digits of calendar year)                                                                       |
|                | WW     | Week code (week of January 1 is week '01')                                                                       |
|                | NNN    | Alphanumeric traceability code                                                                                   |
|                | (e3)   | Pb-free JEDEC designator for Matte Tin (Sn)                                                                      |
|                | *      | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |

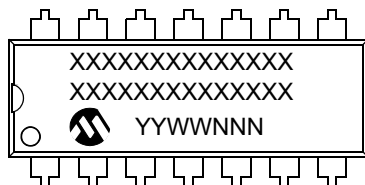
**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

# MCP3204/3208

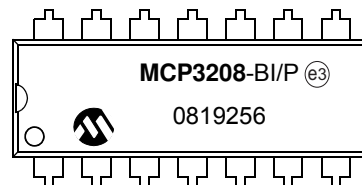
---

## Package Marking Information (Continued)

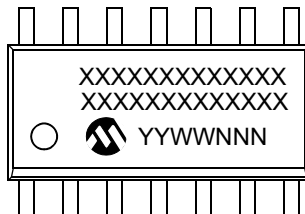
16-Lead PDIP (300 mil) (**MCP3208**)



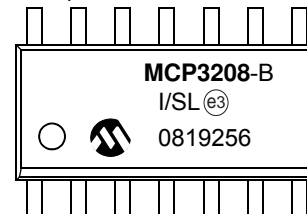
Example:



16-Lead SOIC (150 mil) (**MCP3208**)

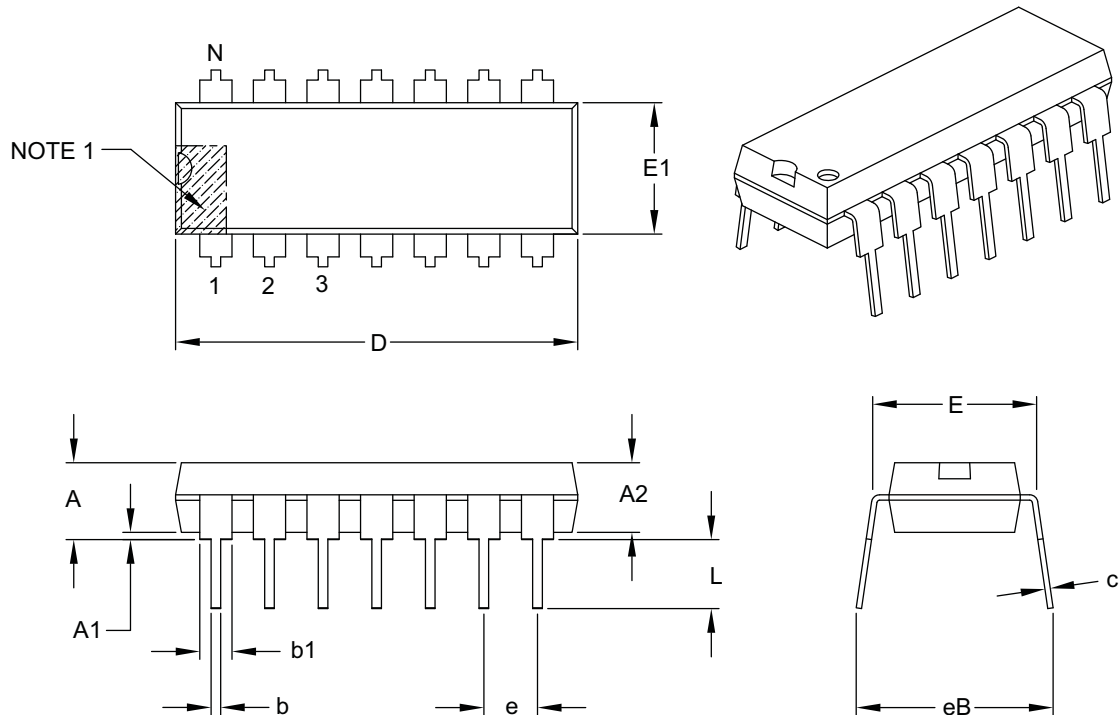


Example:



## 14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits           | Units | INCHES   |      |      |
|----------------------------|-------|----------|------|------|
|                            |       | MIN      | NOM  | MAX  |
| Number of Pins             | N     | 14       |      |      |
| Pitch                      | e     | .100 BSC |      |      |
| Top to Seating Plane       | A     | –        | –    | .210 |
| Molded Package Thickness   | A2    | .115     | .130 | .195 |
| Base to Seating Plane      | A1    | .015     | –    | –    |
| Shoulder to Shoulder Width | E     | .290     | .310 | .325 |
| Molded Package Width       | E1    | .240     | .250 | .280 |
| Overall Length             | D     | .735     | .750 | .775 |
| Tip to Seating Plane       | L     | .115     | .130 | .150 |
| Lead Thickness             | c     | .008     | .010 | .015 |
| Upper Lead Width           | b1    | .045     | .060 | .070 |
| Lower Lead Width           | b     | .014     | .018 | .022 |
| Overall Row Spacing §      | eB    | –        | –    | .430 |

### Notes:

- Pin 1 visual index feature may vary, but must be located with the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

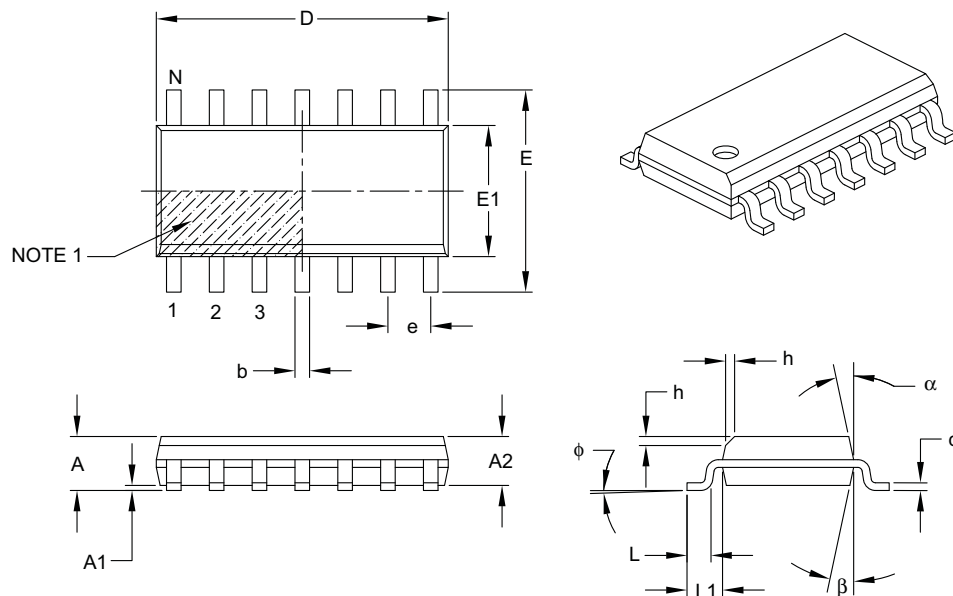
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

# MCP3204/3208

## 14-Lead Plastic Small Outline (SL) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units                    |    | MILLIMETERS |     |      |
|--------------------------|----|-------------|-----|------|
| Dimension Limits         |    | MIN         | NOM | MAX  |
| Number of Pins           | N  | 14          |     |      |
| Pitch                    | e  | 1.27 BSC    |     |      |
| Overall Height           | A  | –           | –   | 1.75 |
| Molded Package Thickness | A2 | 1.25        | –   | –    |
| Standoff §               | A1 | 0.10        | –   | 0.25 |
| Overall Width            | E  | 6.00 BSC    |     |      |
| Molded Package Width     | E1 | 3.90 BSC    |     |      |
| Overall Length           | D  | 8.65 BSC    |     |      |
| Chamfer (optional)       | h  | 0.25        | –   | 0.50 |
| Foot Length              | L  | 0.40        | –   | 1.27 |
| Footprint                | L1 | 1.04 REF    |     |      |
| Foot Angle               | φ  | 0°          | –   | 8°   |
| Lead Thickness           | c  | 0.17        | –   | 0.25 |
| Lead Width               | b  | 0.31        | –   | 0.51 |
| Mold Draft Angle Top     | α  | 5°          | –   | 15°  |
| Mold Draft Angle Bottom  | β  | 5°          | –   | 15°  |

### Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

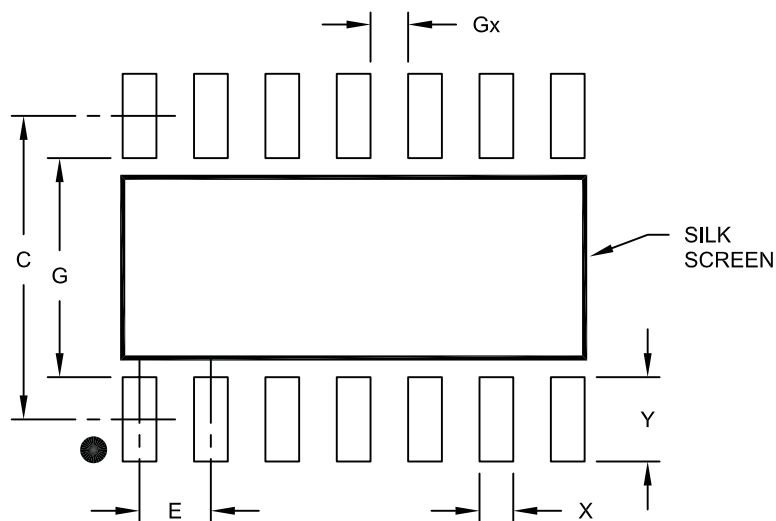
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-065B

## 14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

| Dimension Limits      | Units | MILLIMETERS |      |      |
|-----------------------|-------|-------------|------|------|
|                       |       | MIN         | NOM  | MAX  |
| Contact Pitch         | E     | 1.27 BSC    |      |      |
| Contact Pad Spacing   | C     |             | 5.40 |      |
| Contact Pad Width     | X     |             |      | 0.60 |
| Contact Pad Length    | Y     |             |      | 1.50 |
| Distance Between Pads | Gx    | 0.67        |      |      |
| Distance Between Pads | G     | 3.90        |      |      |

#### Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

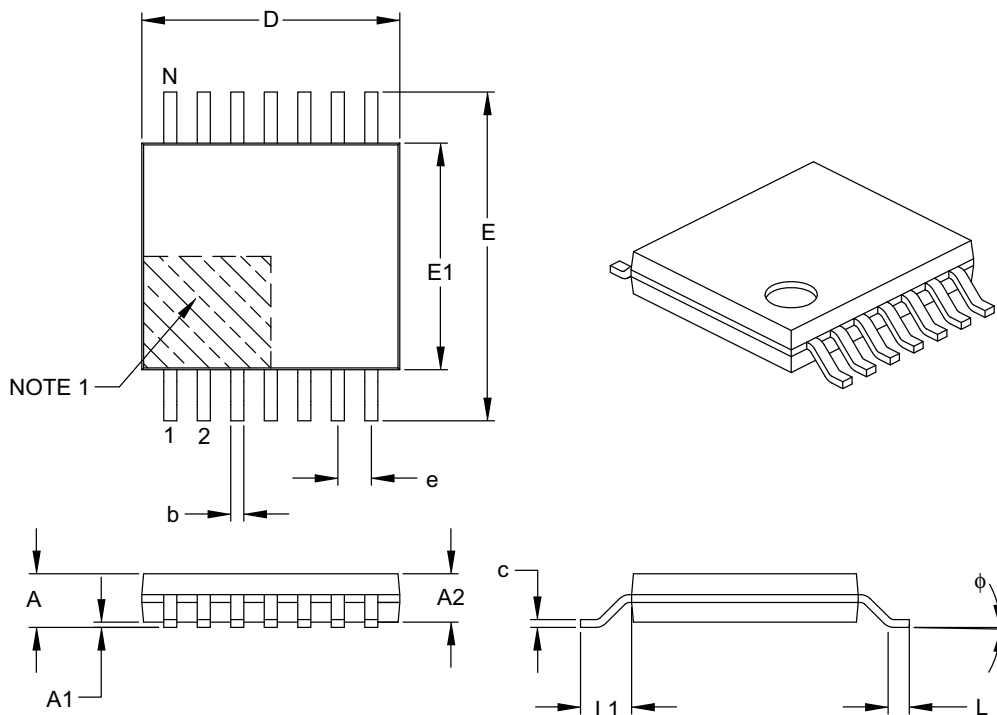
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

# MCP3204/3208

## 14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits         | Units | MILLIMETERS |      |      |
|--------------------------|-------|-------------|------|------|
|                          |       | MIN         | NOM  | MAX  |
| Number of Pins           | N     | 14          |      |      |
| Pitch                    | e     | 0.65 BSC    |      |      |
| Overall Height           | A     | –           | –    | 1.20 |
| Molded Package Thickness | A2    | 0.80        | 1.00 | 1.05 |
| Standoff                 | A1    | 0.05        | –    | 0.15 |
| Overall Width            | E     | 6.40 BSC    |      |      |
| Molded Package Width     | E1    | 4.30        | 4.40 | 4.50 |
| Molded Package Length    | D     | 4.90        | 5.00 | 5.10 |
| Foot Length              | L     | 0.45        | 0.60 | 0.75 |
| Footprint                | L1    | 1.00 REF    |      |      |
| Foot Angle               | φ     | 0°          | –    | 8°   |
| Lead Thickness           | c     | 0.09        | –    | 0.20 |
| Lead Width               | b     | 0.19        | –    | 0.30 |

### Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

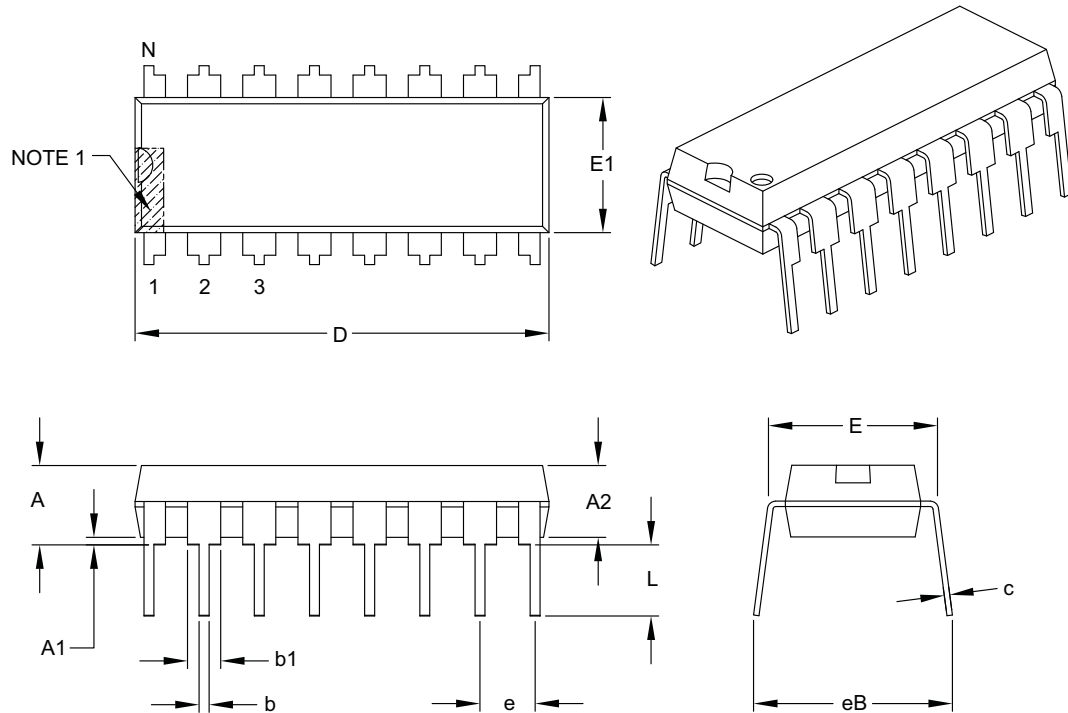
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087B

## 16-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units                      |    | INCHES   |      |      |
|----------------------------|----|----------|------|------|
| Dimension Limits           |    | MIN      | NOM  | MAX  |
| Number of Pins             | N  | 16       |      |      |
| Pitch                      | e  | .100 BSC |      |      |
| Top to Seating Plane       | A  | –        | –    | .210 |
| Molded Package Thickness   | A2 | .115     | .130 | .195 |
| Base to Seating Plane      | A1 | .015     | –    | –    |
| Shoulder to Shoulder Width | E  | .290     | .310 | .325 |
| Molded Package Width       | E1 | .240     | .250 | .280 |
| Overall Length             | D  | .735     | .755 | .775 |
| Tip to Seating Plane       | L  | .115     | .130 | .150 |
| Lead Thickness             | c  | .008     | .010 | .015 |
| Upper Lead Width           | b1 | .045     | .060 | .070 |
| Lower Lead Width           | b  | .014     | .018 | .022 |
| Overall Row Spacing §      | eB | –        | –    | .430 |

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

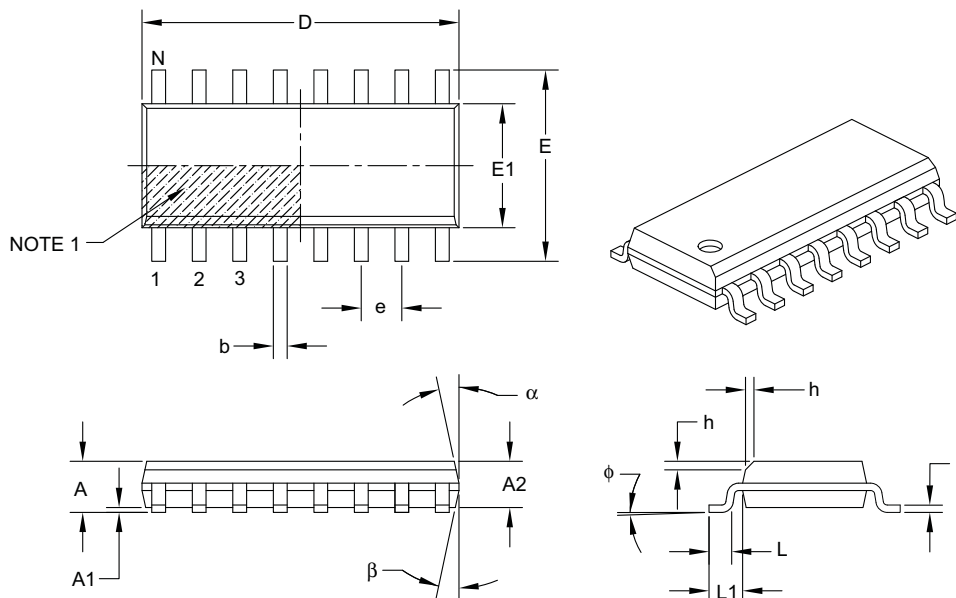
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-017B

# MCP3204/3208

## 16-Lead Plastic Small Outline (SL) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits         | Units | MILLIMETERS |     |      |
|--------------------------|-------|-------------|-----|------|
|                          |       | MIN         | NOM | MAX  |
| Number of Pins           | N     | 16          |     |      |
| Pitch                    | e     | 1.27 BSC    |     |      |
| Overall Height           | A     | –           | –   | 1.75 |
| Molded Package Thickness | A2    | 1.25        | –   | –    |
| Standoff §               | A1    | 0.10        | –   | 0.25 |
| Overall Width            | E     | 6.00 BSC    |     |      |
| Molded Package Width     | E1    | 3.90 BSC    |     |      |
| Overall Length           | D     | 9.90 BSC    |     |      |
| Chamfer (optional)       | h     | 0.25        | –   | 0.50 |
| Foot Length              | L     | 0.40        | –   | 1.27 |
| Footprint                | L1    | 1.04 REF    |     |      |
| Foot Angle               | φ     | 0°          | –   | 8°   |
| Lead Thickness           | c     | 0.17        | –   | 0.25 |
| Lead Width               | b     | 0.31        | –   | 0.51 |
| Mold Draft Angle Top     | α     | 5°          | –   | 15°  |
| Mold Draft Angle Bottom  | β     | 5°          | –   | 15°  |

### Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

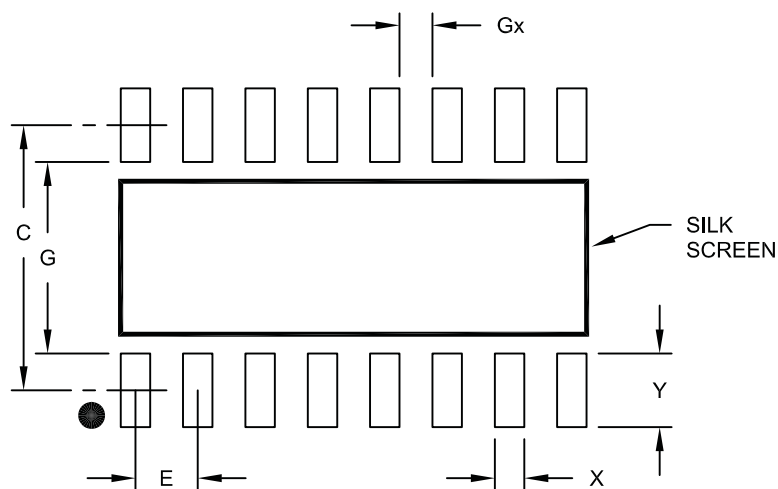
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-108B

## 16-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

| Units                 |    | MILLIMETERS |      |      |
|-----------------------|----|-------------|------|------|
| Dimension Limits      |    | MIN         | NOM  | MAX  |
| Contact Pitch         | E  | 1.27 BSC    |      |      |
| Contact Pad Spacing   | C  |             | 5.40 |      |
| Contact Pad Width     | X  |             |      | 0.60 |
| Contact Pad Length    | Y  |             |      | 1.50 |
| Distance Between Pads | Gx | 0.67        |      |      |
| Distance Between Pads | G  | 3.90        |      |      |

#### Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2108A

# MCP3204/3208

---

NOTES:

## **APPENDIX A: REVISION HISTORY**

### **Revision E (September 2008)**

The following is the list of modifications:

1. Updated package outline drawings in **Section 7.0 “Packaging Information”**.

### **Revision D (January 2007)**

The following is the list of modifications:

1. Undocumented changes

### **Revision C (May 2002)**

The following is the list of modifications:

1. Undocumented changes

### **Revision B (August 1999)**

The following is the list of modifications:

1. Undocumented changes

### **Revision A (November 1998)**

- Initial release of this document.

NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| <b>PART NO.</b>   |           | <b>=X</b>                                             | <b>X</b>                 | <b>/XX</b>     |
|-------------------|-----------|-------------------------------------------------------|--------------------------|----------------|
| <b>Device</b>     |           | <b>Grade</b>                                          | <b>Temperature Range</b> | <b>Package</b> |
| Device            | MCP3204:  | 4-Channel 12-Bit Serial A/D Converter                 |                          |                |
|                   | MCP3204T: | 4-Channel 12-Bit Serial A/D Converter (Tape and Reel) |                          |                |
|                   | MCP3208:  | 8-Channel 12-Bit Serial A/D Converter                 |                          |                |
|                   | MCP3208T: | 8-Channel 12-Bit Serial A/D Converter (Tape and Reel) |                          |                |
| Grade:            | B         | = $\pm 1$ LSB INL                                     |                          |                |
|                   | C         | = $\pm 2$ LSB INL                                     |                          |                |
| Temperature Range | I         | = -40°C to +85°C (Industrial)                         |                          |                |
| Package           | P         | = Plastic DIP (300 mil Body), 14-lead, 16-lead        |                          |                |
|                   | SL        | = Plastic SOIC (150 mil Body), 14-lead, 16-lead       |                          |                |
|                   | ST        | = Plastic TSSOP (4.4mm), 14-lead                      |                          |                |

**Examples:**

a) MCP3204-BI/P:  $\pm 1$  LSB INL, Industrial Temperature, PDIP package.

b) MCP3204-BI/SL:  $\pm 1$  LSB INL, Industrial Temperature, SOIC package.

c) MCP3204-CI/ST:  $\pm 2$  LSB INL, Industrial Temperature, TSSOP package.

a) MCP3208-BI/P:  $\pm 1$  LSB INL, Industrial Temperature, PDIP package.

b) MCP3208-BI/SL:  $\pm 1$  LSB INL, Industrial Temperature, SOIC package.

c) MCP3208-CI/ST:  $\pm 2$  LSB INL, Industrial Temperature, TSSOP package.

NOTES:

---

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

---

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

#### **Trademarks**

The Microchip name and logo, the Microchip logo, Accuron, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, rfPIC, SmartShunt and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL, SmartSensor and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, In-Circuit Serial Programming, ICSP, ICEPIC, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, PICkit, PICDEM, PICDEM.net, PICtail, PIC<sup>32</sup> logo, PowerCal, PowerInfo, PowerMate, PowerTool, REAL ICE, rfLAB, Select Mode, Total Endurance, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2008, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

**QUALITY MANAGEMENT SYSTEM**  
**CERTIFIED BY DNV**  
**== ISO/TS 16949:2002 ==**

*Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*



---

## WORLDWIDE SALES AND SERVICE

---

### AMERICAS

#### Corporate Office

2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200  
Fax: 480-792-7277  
Technical Support:  
<http://support.microchip.com>  
Web Address:  
[www.microchip.com](http://www.microchip.com)

#### Atlanta

Duluth, GA  
Tel: 678-957-9614  
Fax: 678-957-1455

#### Boston

Westborough, MA  
Tel: 774-760-0087  
Fax: 774-760-0088

#### Chicago

Itasca, IL  
Tel: 630-285-0071  
Fax: 630-285-0075

#### Dallas

Addison, TX  
Tel: 972-818-7423  
Fax: 972-818-2924

#### Detroit

Farmington Hills, MI  
Tel: 248-538-2250  
Fax: 248-538-2260

#### Kokomo

Kokomo, IN  
Tel: 765-864-8360  
Fax: 765-864-8387

#### Los Angeles

Mission Viejo, CA  
Tel: 949-462-9523  
Fax: 949-462-9608

#### Santa Clara

Santa Clara, CA  
Tel: 408-961-6444  
Fax: 408-961-6445

#### Toronto

Mississauga, Ontario,  
Canada  
Tel: 905-673-0699  
Fax: 905-673-6509

### ASIA/PACIFIC

#### Asia Pacific Office

Suites 3707-14, 37th Floor  
Tower 6, The Gateway  
Harbour City, Kowloon  
Hong Kong  
Tel: 852-2401-1200  
Fax: 852-2401-3431

#### Australia - Sydney

Tel: 61-2-9868-6733  
Fax: 61-2-9868-6755

#### China - Beijing

Tel: 86-10-8528-2100  
Fax: 86-10-8528-2104

#### China - Chengdu

Tel: 86-28-8665-5511  
Fax: 86-28-8665-7889

#### China - Hong Kong SAR

Tel: 852-2401-1200  
Fax: 852-2401-3431

#### China - Nanjing

Tel: 86-25-8473-2460  
Fax: 86-25-8473-2470

#### China - Qingdao

Tel: 86-532-8502-7355  
Fax: 86-532-8502-7205

#### China - Shanghai

Tel: 86-21-5407-5533  
Fax: 86-21-5407-5066

#### China - Shenyang

Tel: 86-24-2334-2829  
Fax: 86-24-2334-2393

#### China - Shenzhen

Tel: 86-755-8203-2660  
Fax: 86-755-8203-1760

#### China - Wuhan

Tel: 86-27-5980-5300  
Fax: 86-27-5980-5118

#### China - Xiamen

Tel: 86-592-2388138  
Fax: 86-592-2388130

#### China - Xian

Tel: 86-29-8833-7252  
Fax: 86-29-8833-7256

#### China - Zhuhai

Tel: 86-756-3210040  
Fax: 86-756-3210049

### ASIA/PACIFIC

#### India - Bangalore

Tel: 91-80-4182-8400  
Fax: 91-80-4182-8422

#### India - New Delhi

Tel: 91-11-4160-8631  
Fax: 91-11-4160-8632

#### India - Pune

Tel: 91-20-2566-1512  
Fax: 91-20-2566-1513

#### Japan - Yokohama

Tel: 81-45-471-6166  
Fax: 81-45-471-6122

#### Korea - Daegu

Tel: 82-53-744-4301  
Fax: 82-53-744-4302

#### Korea - Seoul

Tel: 82-2-554-7200  
Fax: 82-2-558-5932 or  
82-2-558-5934

#### Malaysia - Kuala Lumpur

Tel: 60-3-6201-9857  
Fax: 60-3-6201-9859

#### Malaysia - Penang

Tel: 60-4-227-8870  
Fax: 60-4-227-4068

#### Philippines - Manila

Tel: 63-2-634-9065  
Fax: 63-2-634-9069

#### Singapore

Tel: 65-6334-8870  
Fax: 65-6334-8850

#### Taiwan - Hsin Chu

Tel: 886-3-572-9526  
Fax: 886-3-572-6459

#### Taiwan - Kaohsiung

Tel: 886-7-536-4818  
Fax: 886-7-536-4803

#### Taiwan - Taipei

Tel: 886-2-2500-6610  
Fax: 886-2-2508-0102

#### Thailand - Bangkok

Tel: 66-2-694-1351  
Fax: 66-2-694-1350

### EUROPE

#### Austria - Wels

Tel: 43-7242-2244-39  
Fax: 43-7242-2244-393

#### Denmark - Copenhagen

Tel: 45-4450-2828  
Fax: 45-4485-2829

#### France - Paris

Tel: 33-1-69-53-63-20  
Fax: 33-1-69-30-90-79

#### Germany - Munich

Tel: 49-89-627-144-0  
Fax: 49-89-627-144-44

#### Italy - Milan

Tel: 39-0331-742611  
Fax: 39-0331-466781

#### Netherlands - Drunen

Tel: 31-416-690399  
Fax: 31-416-690340

#### Spain - Madrid

Tel: 34-91-708-08-90  
Fax: 34-91-708-08-91

#### UK - Wokingham

Tel: 44-118-921-5869  
Fax: 44-118-921-5820