Integrated Circuit True RMS-to-DC Converter

AD536A

FEATURES

True rms-to-dc conversion
Laser trimmed to high accuracy
- **0.2% maximum error (AD536AK)**
- **0.5% maximum error (AD536AJ)**

Wide response capability
- **Computes rms of ac and dc signals**
- **450 kHz bandwidth: V rms > 100 mV**
- **2 MHz bandwidth: V rms > 1 V**
- **Signal crest factor of 7 for 1% error**

dB output with 60 dB range
Low power: 1.2 mA quiescent current
Single or dual supply operation
Monolithic integrated circuit
−55°C to +125°C operation (AD536AS)

FUNCTIONAL BLOCK DIAGRAM

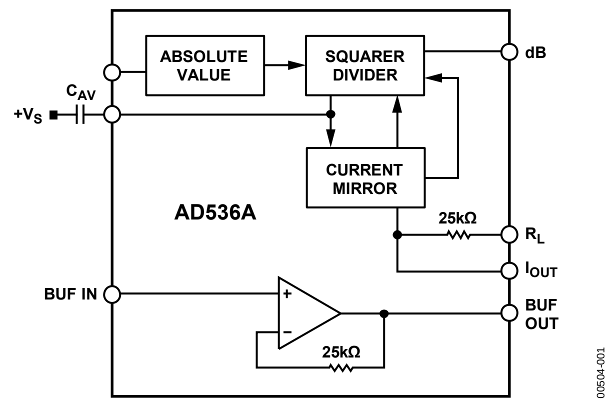

Figure 1.

GENERAL DESCRIPTION

The AD536A is a complete monolithic integrated circuit that performs true rms-to-dc conversion. It offers performance comparable or superior to that of hybrid or modular units costing much more. The AD536A directly computes the true rms value of any complex input waveform containing ac and dc components. A crest factor compensation scheme allows measurements with 1% error at crest factors up to 7. The wide bandwidth of the device extends the measurement capability to 300 kHz with less than 3 dB errors, for signal levels greater than 100 mV.

An important feature of the AD536A, not previously available in rms converters, is an auxiliary dB output pin. The logarithm of the rms output signal is brought out to a separate pin to allow the dB conversion, with a useful dynamic range of 60 dB. Using an externally supplied reference current, the 0 dB level can be conveniently set to correspond to any input level from 0.1 V to 2 V rms.

The AD536A is laser trimmed to minimize input and output offset voltage, to optimize positive and negative waveform symmetry (dc reversal error), and for full-scale accuracy at 7 V rms. As a result, no external trims are required to achieve the rated unit accuracy.

The input and output pins are fully protected. The input circuitry can take overload voltages well beyond the supply levels. Loss of supply voltage with the input connected to external circuitry does not cause the device to fail. The output is short-circuit protected.

The AD536A is available in two accuracy grades (J and K) for commercial temperature range (0°C to 70°C) applications, and one grade (S) rated for the −55°C to +125°C extended range. The AD536AK offers a maximum total error of ±2 mV ± 0.2% of reading while the AD536AJ and AD536AS have maximum errors of ±5 mV ± 0.5% of reading. All three versions are available in a hermetically sealed 14-lead DIP or a 10-lead TO-100 metal can. The AD536AS is also available in a 20-terminal leadless hermetically sealed ceramic chip carrier.

The AD536A computes the true root-mean-square level of a complex ac (or ac plus dc) input signal and provides an equivalent dc output level. The true rms value of a waveform is a more useful quantity than the average rectified value because it relates directly to the power of the signal. The rms value of a statistical signal also relates to its standard deviation.

An external capacitor is required to perform measurements to the fully specified accuracy. The value of this capacitor determines the low frequency ac accuracy, ripple amplitude, and settling time.

The AD536A operates equally well from split supplies or a single supply with total supply levels from 5 V to 36 V. With one milliampere quiescent supply current, the device is well suited for a wide variety of remote controllers and battery-powered instruments.

Rev. C

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TABLE OF CONTENTS

REVISION HISTORY

3/06—Rev. B to Rev. C

Updated Format ... Universal
Changed Product Description to General Description ... 1
Changes to General Description ... 1
Changes to Table 1 ... 3
Changes to Table 2 ... 5
Added Pin Configurations and Function Descriptions ... 6
Changed Standard Connection to Typical Connections ... 8
Changed Single Supply Connection to Single Supply Operation ... 9
Changes to Connections for dB Operation ... 11
Changes to Figure 17 ... 12
Updated Outline Dimensions ... 14
Changes to Ordering Guide ... 15

6/99—Rev. A to Rev. B

SPECIFICATIONS

@ +25°C and ±15 V dc, unless otherwise noted.

Table 1.

	AD536AJ			AD536AK			AD536AS			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
TRANSFER FUNCTION		$V_{OUT} = \sqrt{avg. (V_{IN})^2}$			$V_{OUT} = \sqrt{avg. (V_{IN})^2}$			$V_{OUT} = \sqrt{avg. (V_{IN})^2}$		
CONVERSION ACCURACY										
Total Error, Internal Trim[1] (Figure 6)			±5 ± 0.5			±2 ± 0.2			±5 ± 0.5	mV ± % of rdg
vs. Temperature, T_{MIN} to +70°C			±0.1 ± 0.01			±0.05 ± 0.005			±0.1 ± 0.005	mV ± % of rdg/°C
+70°C to +125°C									±0.3 ± 0.005	mV ± % of rdg/°C
vs. Supply Voltage		±0.1 ±0.01			±0.1 ± 0.01			±0.1 ±0.01		mV ± % of rdg/°C
dc Reversal Error		±0.2			±0.1			±0.2		mV ± % of rdg
Total Error, External Trim[1] (Figure 9)		±3 ± 0.3			±2 ± 0.1			±3 ± 0.3		mV ± % of rdg
ERROR VS. CREST FACTOR[2]										
Crest Factor 1 to 2		Specified Accuracy			Specified Accuracy			Specified Accuracy		
Crest Factor = 3		−0.1			−0.1			−0.1		% of rdg
Crest Factor = 7		−1.0			−1.0			−1.0		% of rdg
FREQUENCY RESPONSE[3]										
Bandwidth for 1% Additional Error (0.09 dB)										
V_{IN} = 10 mV		5			5			5		kHz
V_{IN} = 100 mV		45			45			45		kHz
V_{IN} = 1 V		120			120			120		kHz
±3 dB Bandwidth										
V_{IN} = 10 mV		90			90			90		kHz
V_{IN} = 100 mV		450			450			450		kHz
V_{IN} = 1 V		2.3			2.3			2.3		MHz
AVERAGING TIME CONSTANT (Figure 12)		25			25			25		ms/μF
INPUT CHARACTERISTICS										
Signal Range, ±15 V Supplies										
Continuous rms Level		0 to 7			0 to 7			0 to 7		V rms
Peak Transient Input			±20			±20			±20	V peak
Continuous rms Level, V_S = ±5 V		0 to 2			0 to 2			0 to 2		V rms
Peak Transient Input, V_S = ±5 V			±7			±7			±7	V peak
Maximum Continuous Nondestructive Input Level (All Supply Voltages)			±25			±25			±25	V peak
Input Resistance	13.33	16.67	20	13.33	16.67	20	13.33	16.67	20	kΩ
Input Offset Voltage		0.8	±2		0.5	±1		0.8	±2	mV
OUTPUT CHARACTERISTICS										
Offset Voltage, V_{IN} = COM (Figure 6)		±1	±2		±0.5	±1			±2	mV
vs. Temperature		±0.1			±0.1				±0.2	mV/°C
vs. Supply Voltage		±0.1			±0.1			±0.2		mV/V
Voltage Swing, ±15 V Supplies	0 to +11	+12.5		0 to +11	+12.5		0 to +11	+12.5		V
± 5 V Supply	0 to +2			0 to +2			0 to +2			V
dB OUTPUT, 0 dB = 1 V rms (Figure 17)										
Error, 7 mV < V_{IN} < 7 V rms		±0.4	±0.6		±0.2	±0.3		±0.5	±0.6	dB
Scale Factor		−3			−3			−3		mV/dB
Scale Factor Temperature Coefficient		−0.033			−0.033			−0.033		dB/°C
(Uncompensated)		+0.33			+0.33			+0.33		% of rdg/°C
I_{REF} for 0 dB = 1 V rms	5	20	80	5	20	80	5	20	80	μA
I_{REF} Range	1		100	1		100	1		100	μA

Parameter	AD536AJ Min	Typ	Max	AD536AK Min	Typ	Max	AD536AS Min	Typ	Max	Unit
I_{OUT} TERMINAL										
I_{OUT} Scale Factor		40			40			40		µA/V rms
I_{OUT} Scale Factor Tolerance		±10	±20		±10	±20		±10	±20	%
Output Resistance	20	25	30	20	25	30	20	25	30	kΩ
Voltage Compliance		$-V_S$ to ($+V_S - 2.5$ V)			$-V_S$ to ($+V_S - 2.5$ V)			$-V_S$ to ($+V_S - 2.5$ V)		V
BUFFER AMPLIFIER										
Input and Output Voltage Range	$-V_S$ to ($+V_S - 2.5$V)			$-V_S$ to ($+V_S - 2.5$V)			$-V_S$ to ($+V_S - 2.5$V)			V
Input Offset Voltage, $R_S = 25$ k		±0.5	±4		±0.5	±4		±0.5	±4	mV
Input Bias Current		20	60		20	60		20	60	nA
Input Resistance		10^8			10^8			10^8		Ω
Output Current	(+5 mA, −130 µA)			(+5 mA, −130 µA)			(+5 mA, −130 µA)			
Short-Circuit Current		20			20			20		mA
Output Resistance			0.5			0.5			0.5	Ω
Small Signal Bandwidth		1			1			1		MHz
Slew Rate[4]		5			5			5		V/µs
POWER SUPPLY										
Voltage Rated Performance		±15			±15			±15		V
Dual Supply	±3.0		±18	±3.0		±18	±3.0		±18	V
Single Supply	+5		+36	+5		+36	+5		+36	V
Quiescent Current										
Total V_S, 5 V to 36 V, T_{MIN} to T_{MAX}		1.2	2		1.2	2		1.2	2	mA
TEMPERATURE RANGE										
Rated Performance	0		+70	0		+70	−55		+125	°C
Storage	−55		+150	−55		+150	−55		+150	°C
NUMBER OF TRANSISTORS		65			65			65		

[1] Accuracy is specified for 0 V to 7 V rms, dc or 1 kHz sine wave input with the AD536A connected as in the figure referenced.
[2] Error vs. crest factor is specified as an additional error for 1 V rms rectangular pulse input, pulse width = 200 µs.
[3] Input voltages are expressed in volts rms, and error is percent of reading.
[4] With 2kΩ external pull-down resistor.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	
Dual Supply	±18 V
Single Supply	+36 V
Internal Power Dissipation	500 mW
Maximum Input Voltage	±25 V Peak
Buffer Maximum Input Voltage	$\pm V_S$
Maximum Input Voltage	±25 V Peak
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	
AD536AJ/AD536AK	0°C to +70°C
AD536AS	−55°C to +125°C
Lead Temperature (Soldering 60 seconds)	300°C
ESD Rating	1000 V
Thermal Resistance θ_{JA}[1]	
10-Lead Header	150°C/W
20-Lead LCC	95°C/W
14-Lead Side-Brazed CERDIP	95°C/W

[1] θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

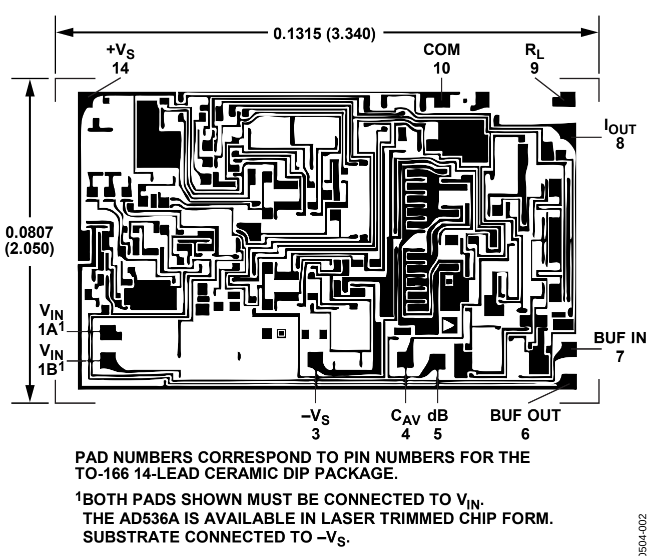


Figure 2. Die Dimensions and Pad Layout
Dimensions shown in inches and (millimeters)

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

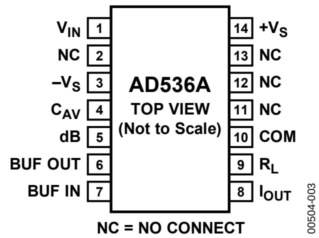


Figure 3. D-14 and Q-14 Packages Pin Configuration

Table 3. D-14 and Q-14 Packages Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{IN}	Input Voltage
2	NC	No Connection
3	$-V_S$	Negative Supply Voltage
4	C_{AV}	Averaging Capacitor
5	dB	Log (dB) Value of the RMS Output Voltage
6	BUF OUT	Buffer Output
7	BUF IN	Buffer Input
8	I_{OUT}	RMS Output Current
9	R_L	Load Resistor
10	COM	Common
11	NC	No Connection
12	NC	No Connection
13	NC	No Connection
14	$+V_S$	Positive Supply Voltage

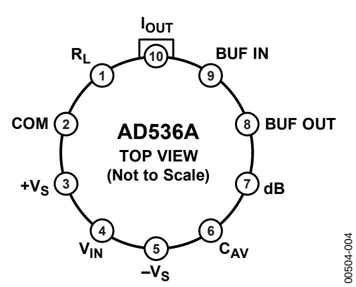


Figure 4. H-10 Package Pin Configuration

Table 4. H-10 Package Pin Function Descriptions

Pin No.	Mnemonic	Description
1	R_L	Load Resistor
2	COM	Common
3	$+V_S$	Positive Supply Voltage
4	V_{IN}	Input Voltage
5	$-V_S$	Negative Supply Voltage
6	C_{AV}	Averaging Capacitor
7	dB	Log (dB) Value of the RMS Output Voltage
8	BUF OUT	Buffer Output
9	BUF IN	Buffer Input
10	I_{OUT}	RMS Output Current

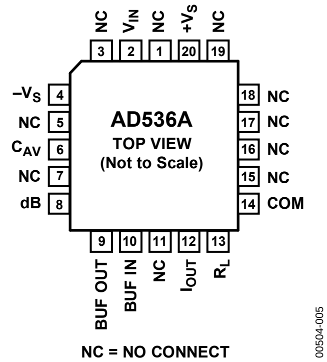


Figure 5. E-20 Package Pin Configuration

Table 5. E-20 Package Pin Function Description

Pin No.	Mnemonic	Description
1	NC	No Connection
2	V_{IN}	Input Voltage
3	NC	No Connection
4	$-V_S$	Negative Supply Voltage
5	NC	No Connection
6	C_{AV}	Averaging Capacitor
7	NC	No Connection
8	dB	Log (dB) Value of the RMS Output Voltage
9	BUF OUT	Buffer Output
10	BUF IN	Buffer Input
11	NC	No Connection
12	I_{OUT}	RMS Output Current
13	R_L	Load Resistor
14	COM	Common
15	NC	No Connection
16	NC	No Connection
17	NC	No Connection
18	NC	No Connection
19	NC	No Connection
20	$+V_S$	Positive Supply Voltage

APPLICATIONS

TYPICAL CONNECTIONS

The AD536A is simple to connect for the majority of high accuracy rms measurements, requiring only an external capacitor to set the averaging time constant. The standard connection is shown in Figure 6 through Figure 8. In this configuration, the AD536A measures the rms of the ac and dc level present at the input, but shows an error for low frequency input as a function of the filter capacitor, C_{AV}, as shown in Figure 12. Thus, if a 4 μF capacitor is used, the additional average error at 10 Hz is 0.1%; at 3 Hz, the additional average error is 1%.

The accuracy at higher frequencies is according to specification. To reject the dc input, add a capacitor in series with the input, as shown in Figure 10. Note that the capacitor must be nonpolar. If the AD536A supply rails contain a considerable amount of high frequency ripple, it is advisable to bypass both supply pins to ground with 0.1 μF ceramic capacitors, located as close to the device as possible.

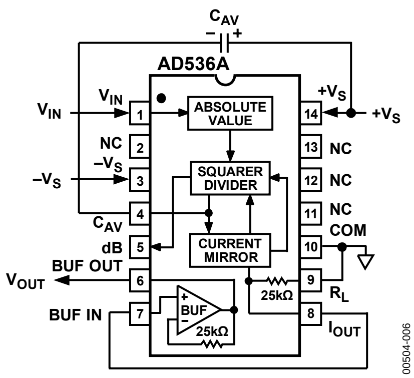


Figure 6. TO-116 and Q-14 Standard RMS Connection

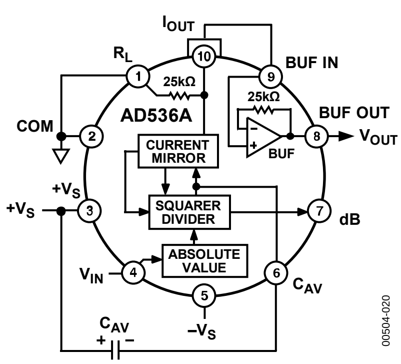


Figure 7. TO-100 Standard RMS Connection

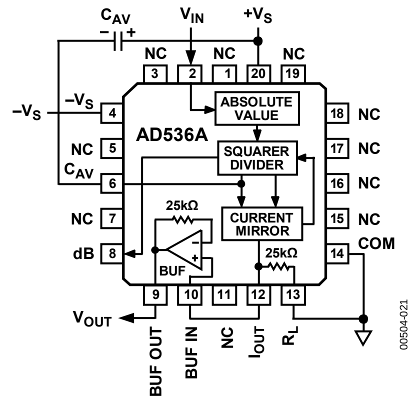


Figure 8. LCC Standard RMS Connection

The input and output signal ranges are a function of the supply voltages; these ranges are shown in Figure 21 and Figure 22. The AD536A can also be used in an unbuffered voltage output mode by disconnecting the input to the buffer. The output then appears unbuffered across the 25 kΩ resistor. The buffer amplifier can then be used for other purposes. Further, the AD536A can be used in a current output mode by disconnecting the 25 kΩ resistor from ground. The output current is available at Pin 8 (Pin 10 on the H-10 package) with a nominal scale of 40 μA per V rms input positive out.

OPTIONAL EXTERNAL TRIMS FOR HIGH ACCURACY

The accuracy and offset voltage of the AD536A is adjustable with external trims, as shown in Figure 9. R4 trims the offset. Note that the offset trim circuit adds 365 Ω in series with the internal 25 kΩ resistor. This causes a 1.5% increase in scale factor, which compensated by R1. The scale factor adjustment range is ±1.5%.

The trimming procedure is as follows:

1. Ground the input signal, V_{IN}, and adjust R4 to provide 0 V output from Pin 6. Alternatively, adjust R4 to provide the correct output with the lowest expected value of V_{IN}.
2. Connect the desired full-scale input level to V_{IN}, either dc or a calibrated ac signal (1 kHz is the optimum frequency).
3. Trim R1 to provide the correct output at Pin 6. For example, 1.000 V dc input provides 1.000 V dc output. A ±1.000 V peak-to-peak sine wave should provide a 0.707 V dc output. Any residual errors are caused by device nonlinearity.

The major advantage of external trimming is to optimize device performance for a reduced signal range; the AD536A is internally trimmed for a 7 V rms full-scale range.

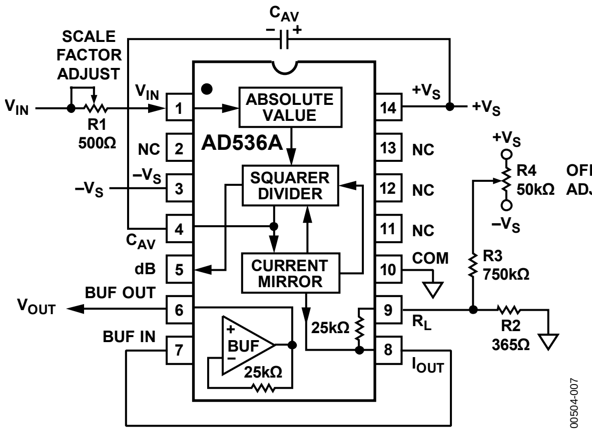


Figure 9. Optional External Gain and Output Offset Trims

SINGLE SUPPLY OPERATION

Dual power supplies are shown in Figure 6, Figure 7, Figure 8, and Figure 9. The AD536A may also be powered by a single supply greater than 5 V, as shown in Figure 10. When using the AD536A with a single supply, the differential input stage must be biased above ground, and the input must be ac coupled. Biasing the device between the supply and ground is simply a matter of connecting Pin 10 (COM, Pin 2 on the H10 package) to a resistor divider and bypassing the pin to ground. To minimize power consumption, the values of the resistors may be large as Pin 10 current is only 5 µA.

AC input coupling requires only Capacitor C2. A dc return is not necessary because it is provided internally. C2 is selected for the proper low frequency break point with the input resistance of 16.7 kΩ; for a cutoff at 10 Hz, C2 should be 1 µF. The signal ranges in this connection are slightly more restricted than in the dual supply connection. The input and output signal ranges are shown in Figure 21 and Figure 22. The load resistor, R_L, is necessary to provide output sink current.

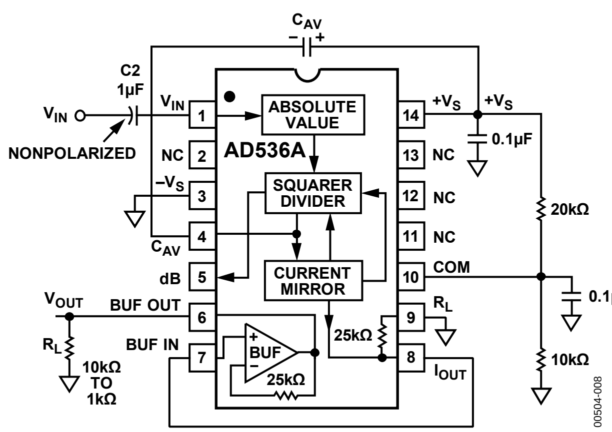


Figure 10. Single Supply Connection

CHOOSING THE AVERAGING TIME CONSTANT

The AD536A computes the rms of both ac and dc signals. If the input is a slowly varying dc signal, the output of the AD536A tracks the input exactly.

At higher frequencies, the average output of the AD536A approaches the rms value of the input signal. The actual output of the AD536A differs from the ideal output by a dc (or average) error and some amount of ripple, as shown in Figure 11.

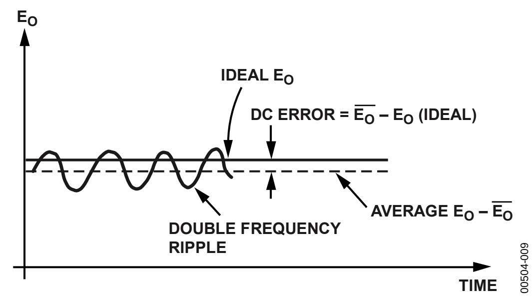


Figure 11. Typical Output Waveform for Sinusoidal Input

The dc error is dependent on the input signal frequency and the value of C_{AV}. Use Figure 12 to determine the minimum value of C_{AV}, which yields a given percent dc error above a given frequency using the standard rms connection.

The ac component of the output signal is the ripple. There are two ways to reduce the ripple. The first method involves using a large value of C_{AV}. Because the ripple is inversely proportional to C_{AV}, a tenfold increase in this capacitance affects a tenfold reduction in ripple.

When measuring waveforms with high crest factors, such as low duty cycle pulse trains, the averaging time constant should be at least 10 times the signal period. For example, a 100 Hz pulse rate requires a 100 ms time constant, which corresponds to a 4 µF capacitor (time constant = 25 ms per µF).

The primary disadvantage in using a large C_{AV} to remove ripple is that the settling time for a step change in input level is increased proportionately. Figure 12 illustrates that the relationship between C_{AV} and 1% settling time is 115 ms for each microfarad of C_{AV}. The settling time is twice as great for decreasing signals as for increasing signals. The values in Figure 12 are for decreasing signals. Settling time also increases for low signal levels, as shown in Figure 13.

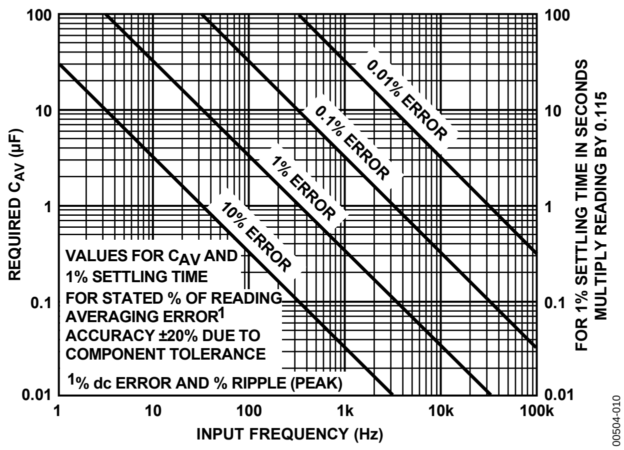


Figure 12. Error/Settling Time Graph for Use with the Standard RMS Connection (See Figure 6 Through Figure 8)

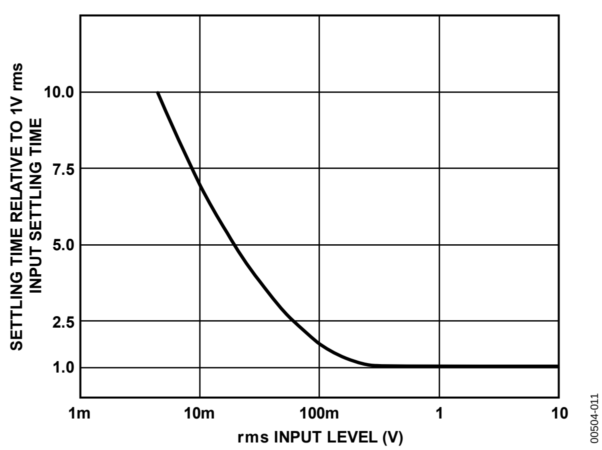


Figure 13. Settling Time vs. Input Level

A better method to reduce output ripple is the use of a post filter. Figure 14 shows a suggested circuit. If a single-pole filter is used (C3 removed, R_X shorted), and C2 is approximately twice the value of C_{AV}, the ripple is reduced, as shown in Figure 15, and settling time is increased. For example, with C_{AV} = 1 µF and C2 = 2.2 µF, the ripple for a 60 Hz input is reduced from 10% of reading to approximately 0.3% of reading.

The settling time, however, is increased by approximately a factor of 3. Therefore, the values of C_{AV} and C2 can be reduced to permit faster settling times while still providing substantial ripple reduction.

The two-pole post filter uses an active filter stage to provide even greater ripple reduction without substantially increasing the settling times over a circuit with a one-pole filter. The values of C_{AV}, C2, and C3 can then be reduced to allow extremely fast settling times for a constant amount of ripple. Caution should be exercised in choosing the value of C_{AV}, because the dc error is dependent upon this value and is independent of the post filter.

For a more detailed explanation of these topics, refer to the *RMS-to-DC Conversion Application Guide 2nd Edition*, available from Analog Devices, Inc.

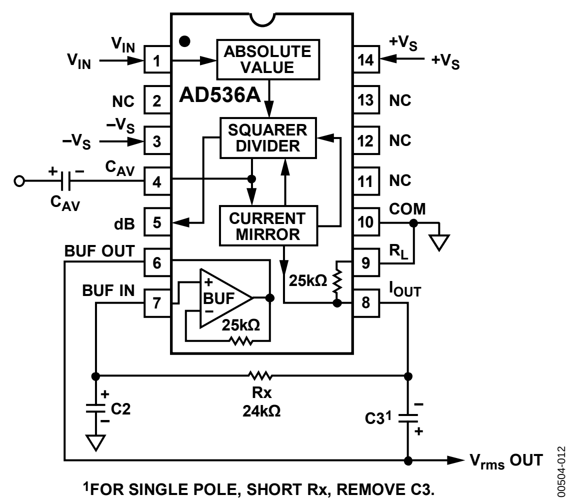


Figure 14. Two-Pole Post Filter

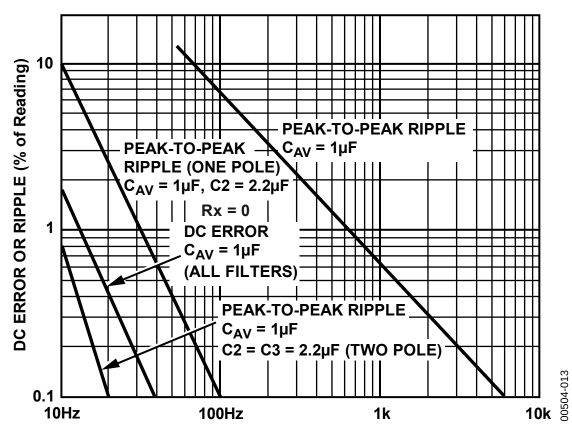


Figure 15. Performance Features of Various Filter Types (See Figure 7)

THEORY OF OPERATION

The AD536A embodies an implicit solution of the rms equation that overcomes the dynamic range as well as other limitations inherent in a straightforward computation of rms. The actual computation performed by the AD536A follows the equation

$$V\,rms = Avg.\left[\frac{V_{IN}^{\;2}}{V\,rms}\right]$$

Figure 16 is a simplified schematic of the AD536A. Note that it is subdivided into four major sections: absolute value circuit (active rectifier), squarer/divider, current mirror, and buffer amplifier. The input voltage (V_{IN}), which can be ac or dc, is converted to a unipolar current (I_1), by the active rectifier (A_1, A_2). I_1 drives one input of the squarer/divider, which has the transfer function

$$I_4 = I_I^2/I_3$$

The output current, I_4, of the squarer/divider drives the current mirror through a low-pass filter formed by R1 and the externally connected capacitor, C_{AV}. If the R1, C_{AV} time constant is much greater than the longest period of the input signal, then I_4 is effectively averaged. The current mirror returns a current I_3, which equals Avg. [I_4], back to the squarer/divider to complete the implicit rms computation. Thus

$$I_4 = Avg.\left[I_I^{\,2}/I_4\right] = I_I\,rms$$

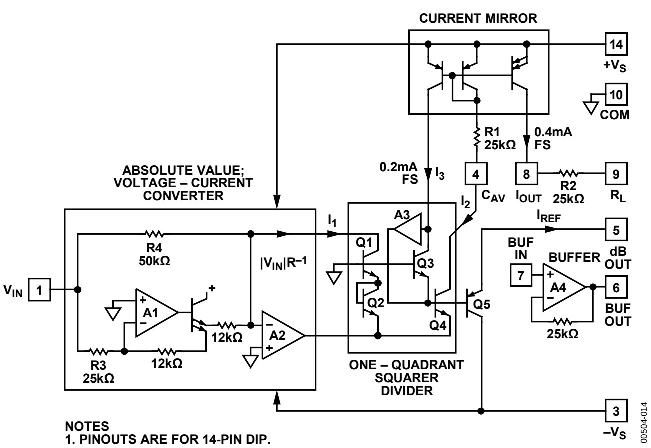


Figure 16. Simplified Schematic

The current mirror also produces the output current, I_{OUT}, which equals $2I_4$. I_{OUT} can be used directly or converted to a voltage with R2 and buffered by A4 to provide a low impedance voltage output. The transfer function of the AD536A results in the following:

$$V_{OUT} = 2R2 \times I\ rms = V_{IN}\ rms$$

The dB output is derived from the emitter of Q3 because the voltage at this point is proportional to –log V_{IN}. Emitter follower, Q5, buffers and level shifts this voltage, so that the dB output voltage is zero when the externally supplied emitter current (I_{REF}) to Q5 approximates I_3.

CONNECTIONS FOR dB OPERATION

The logarithmic (or decibel) output of the AD536A is one of its most powerful features. The internal circuit computing dB works accurately over a 60 dB range. The connections for dB measurements are shown in Figure 17.

Select the 0 dB level by adjusting R1 for the proper 0 dB reference current (which is set to cancel the log output current from the squarer/divider at the desired 0 dB point). The external op amp provides a more convenient scale and allows compensation of the +0.33%/°C scale factor drift of the dB output pin.

The temperature compensating resistor, R2, is available online in several styles from Precision Resistor Corporation. The average temperature coefficients of R2 and R3 result in the +3300 ppm required to compensate the dB output. The linear rms output is available at Pin 8 on the DIP or Pin 10 on the header device with an output impedance of 25 kΩ. Some applications require an additional buffer amplifier if this output is desired.

For dB calibration

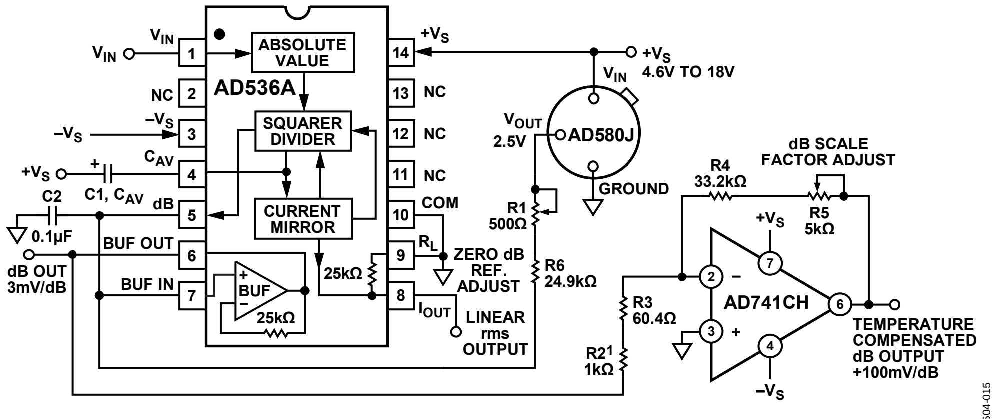
1. Set V_{IN} = 1.00 V dc or 1.00 V rms.

2. Adjust R1 for dB out = 0.00 V.

3. Set V_{IN} = +0.1 V dc or 0.10 V rms.

4. Adjust R5 for dB out = −2.00 V.

Any other desired 0 dB reference level can be used by setting V_{IN} and adjusting R1, accordingly. Note that adjusting R5 for the proper gain automatically provides the correct temperature compensation.



[1]SEE THE CONNECTIONS FOR dB OPERATION SECTION.

Figure 17. dB Connection

FREQUENCY RESPONSE

The AD536A utilizes a logarithmic circuit in performing the implicit rms computation. As with any log circuit, bandwidth is proportional to signal level. The solid lines in the graph below represent the frequency response of the AD536A at input levels from 10 mV to 7 V rms. The dashed lines indicate the upper frequency limits for 1%, 10%, and 3 dB of reading additional error. For example, note that a 1 V rms signal produces less than 1% of reading additional error up to 120 kHz. A 10 mV signal can be measured with 1% of reading additional error (100 µV) up to only 5 kHz.

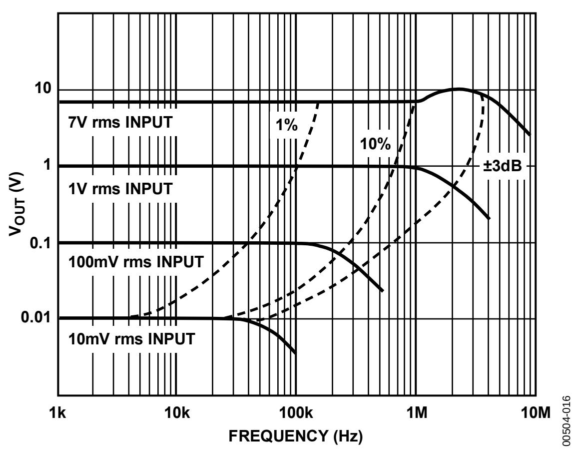


Figure 18. High Frequency Response

AC MEASUREMENT ACCURACY AND CREST FACTOR

Crest factor is often overlooked when determining the accuracy of an ac measurement. The definition of crest factor is the ratio of the peak signal amplitude to the rms value of the signal ($CF = V_P/V$ rms). Most common waveforms, such as sine and triangle waves, have relatively low crest factors (<2). Waveforms that resemble low duty cycle pulse trains, such as those occurring in switching power supplies and SCR circuits, have high crest factors. For example, a rectangular pulse train with a 1% duty cycle has a crest factor of 10 ($CF = 1\sqrt{n}$).

Figure 19 illustrates a curve of reading error for the AD536A for a 1 V rms input signal with crest factors from 1 to 11. A rectangular pulse train (pulse width 100 µs) was used for this test because it is the worst-case waveform for rms measurement (all of the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce crest factors from 1 to 11 while maintaining a constant 1 V rms input amplitude.

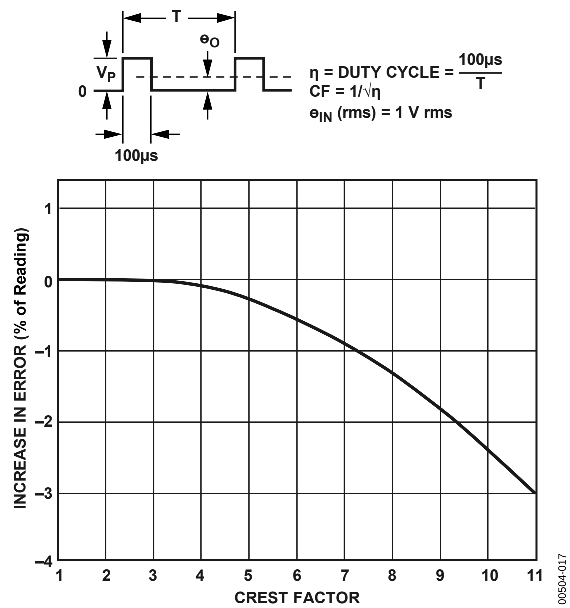


Figure 19. Error vs. Crest Factor

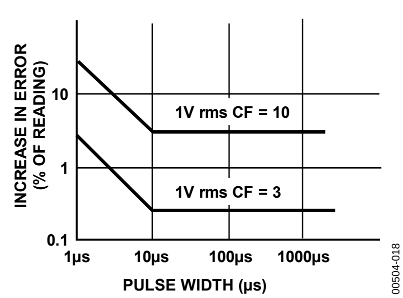


Figure 20. Error vs. Pulse Width Rectangular Pulse

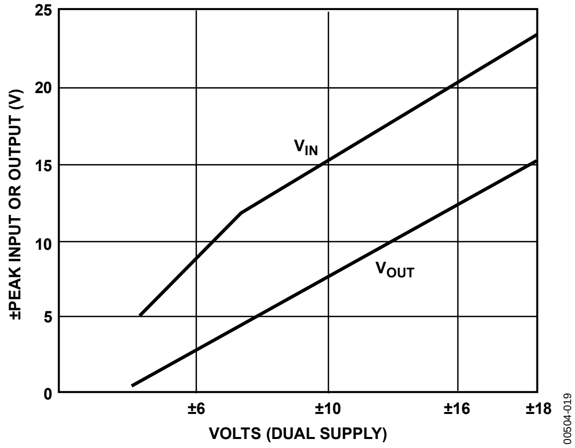


Figure 21. Input and Output Voltage Ranges vs. Dual Supply

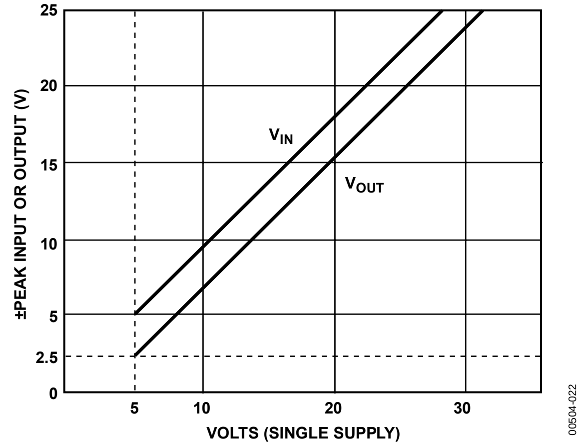
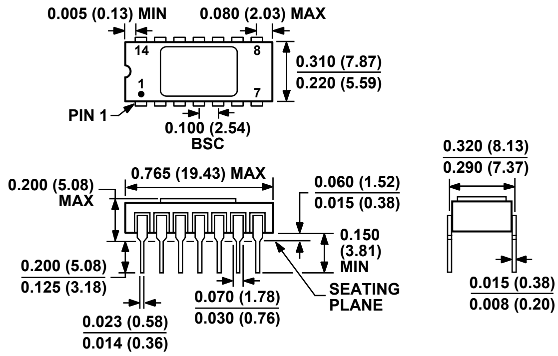


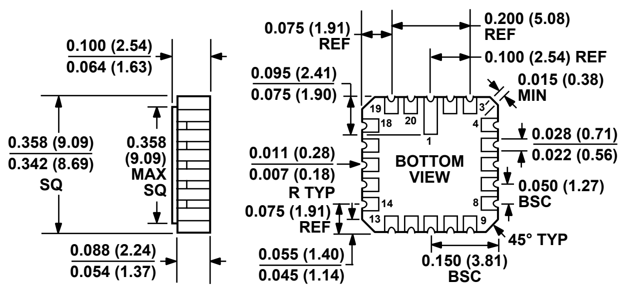
Figure 22. Input and Output Voltage Ranges vs. Single Supply

OUTLINE DIMENSIONS



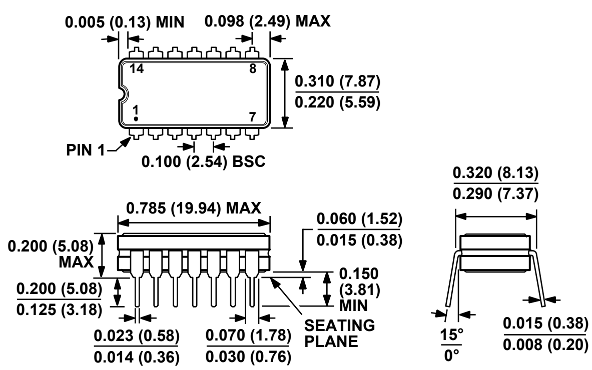
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 23. 14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP] (D-14)
Dimensions shown in inches and (millimeters)



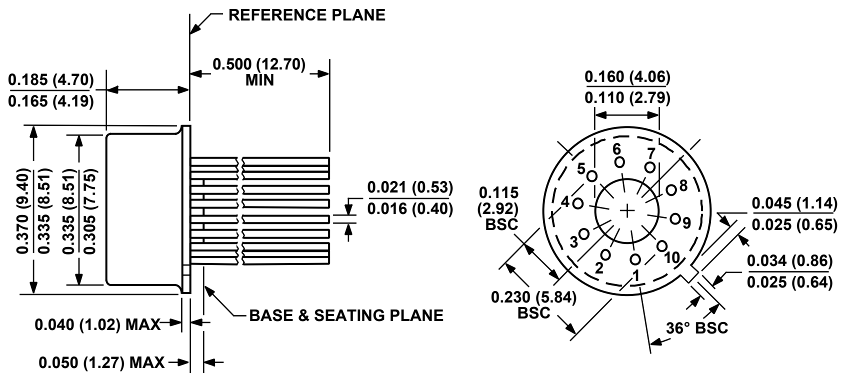
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 24. 20-Terminal Ceramic Leadless Chip Carrier [LCC] (E-20)
Dimensions shown in inches and (millimeter)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 25. 14-Lead Ceramic Dual In-Line Package [CERDIP] (Q-14)
Dimensions shown in inches and (millimeters)



DIMENSIONS PER JEDEC STANDARDS MO-006-AF
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 26. 10-Pin Metal Header Package [TO-100]
(H-10)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD536AJD	0°C to +70°C	14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-14
AD536AKD	0°C to +70°C	14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-14
AD536AJH	0°C to +70°C	10-Lead Metal Header Package [TO-100]	H-10
AD536AKH	0°C to +70°C	10-Lead Metal Header Package [TO-100]	H-10
AD536AJQ	0°C to +70°C	14-Lead Ceramic Dual In-Line Package [CERDIP]	Q-14
AD536AKQ	0°C to +70°C	14-Lead Ceramic Dual In-Line Package [CERDIP]	Q-14
AD536ASD	−55°C to +125°C	14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-14
AD536ASD/883B	−55°C to +125°C	14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-14
AD536ASE/883B	−55°C to +125°C	20-Terminal Ceramic Leadless Chip Carrier [LCC]	E-20
AD536ASH	−55°C to +125°C	10-Lead Metal Header Package [TO-100]	H-10
AD536ASH/883B	−55°C to +125°C	10-Lead Metal Header Package [TO-100]	H-10
AD536ASCHIPS	−55°C to +125°C	Die	
5962-89805012A	−55°C to +125°C	20-Terminal Ceramic Leadless Chip Carrier [LCC]	E-20
5962-8980501CA	−55°C to +125°C	14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-14
5962-8980501IA	−55°C to +125°C	10-Lead Metal Header Package [TO-100]	H-10

NOTES