DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT670

4 x 4 register file; 3-state

Product specification
File under Integrated Circuits, IC06

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Philips
Semiconductors

PHILIPS

4 x 4 register file; 3-state 74HC/HCT670

FEATURES

- Simultaneous and independent read and write operations
- Expandable to almost any word size and bit length
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT670 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT670 are 16-bit 3-state register files organized as 4 words of 4 bits each. Separated read and write address inputs (R_A, R_B and W_A, W_B) and enable inputs ($\overline{RE}$ and $\overline{WE}$) are available, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four data inputs (D_0 to D_3). The W_A and W_B inputs determine the location of the stored word. When the $\overline{WE}$ input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the $\overline{WE}$ input is LOW. Data supplied at the inputs will be read out in true (non-inverting) form from the 3-state outputs (Q_0 to Q_3). D_n and W_n inputs are inhibited when $\overline{WE}$ is HIGH.

Direct acquisition of data stored in any of the four registers is made possible by individual read address inputs (R_A and R_B). The addressed word appears at the four outputs when the $\overline{RE}$ is LOW. Data outputs are in the high impedance OFF-state when $\overline{RE}$ is HIGH. This permits outputs to be tied together to increase the word capacity to very large numbers.

Design of the read enable signals for the stacked devices must ensure that there is no overlap in the LOW levels which would cause more than one output to be active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the enable and address inputs of each device in parallel.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay D_n to Q_n	C_L = 15 pF; V_{CC} = 5 V	23	23	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	122	124	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$ where:

f_i = input frequency in MHz
f_o = output frequency in MHz
$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
C_L = output load capacitance in pF
V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC};
for HCT the condition is V_I = GND to V_{CC} −1.5 V

ORDERING INFORMATION

See *“74HC/HCT/HCU/HCMOS Logic Package Information”*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
5, 4	R_A, R_B	read address inputs
8	GND	ground (0 V)
10, 9, 7, 6	Q_0 to Q_3	data outputs
11	$\overline{RE}$	3-state output read enable input (active LOW)
12	$\overline{WE}$	write enable input (active LOW)
14, 13	W_A, W_B	write address inputs
15, 1, 2, 3	D_0 to D_3	data inputs
16	V_{CC}	positive supply voltage

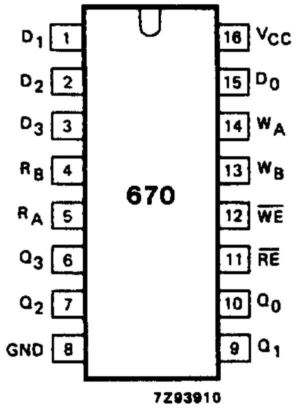


Fig.1 Pin configuration.

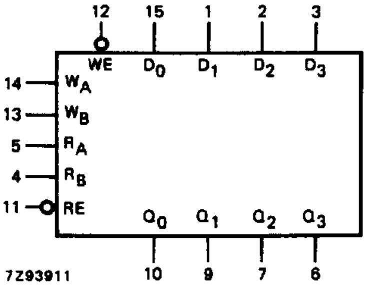


Fig.2 Logic symbol.

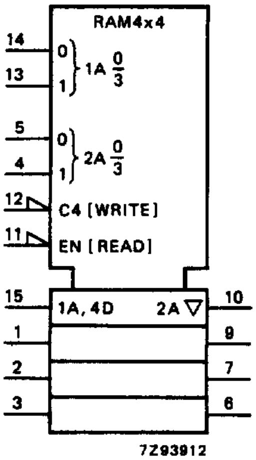


Fig.3 IEC logic symbol.

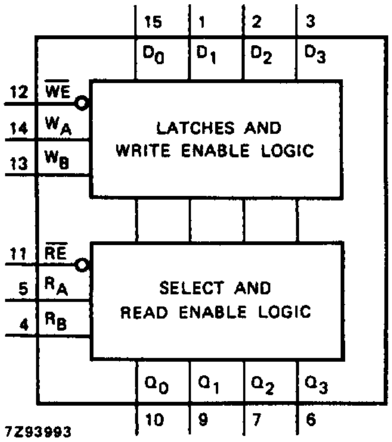


Fig.4 Functional diagram.

WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS		INTERNAL LATCHES(1)
	$\overline{WE}$	D_n	
write data	L L	L H	L H
data latched	H	X	no change

Note

1. The write address (W_A and W_B) to the “internal latches” must be stable while $\overline{WE}$ is LOW for conventional operation.

READ MODE SELECT TABLE

OPERATING MODE	INPUTS		OUTPUT
	$\overline{RE}$	INTERNAL LATCHES(1)	Q_n
read	L L	L H	L H
disabled	H	X	Z

Notes

1. The selection of the “internal latches” by read address (R_A and R_B) are not constrained by $\overline{WE}$ or $\overline{RE}$ operation.

H = HIGH voltage level
L = LOW voltage level
X = don’t care
Z = high impedance OFF-state

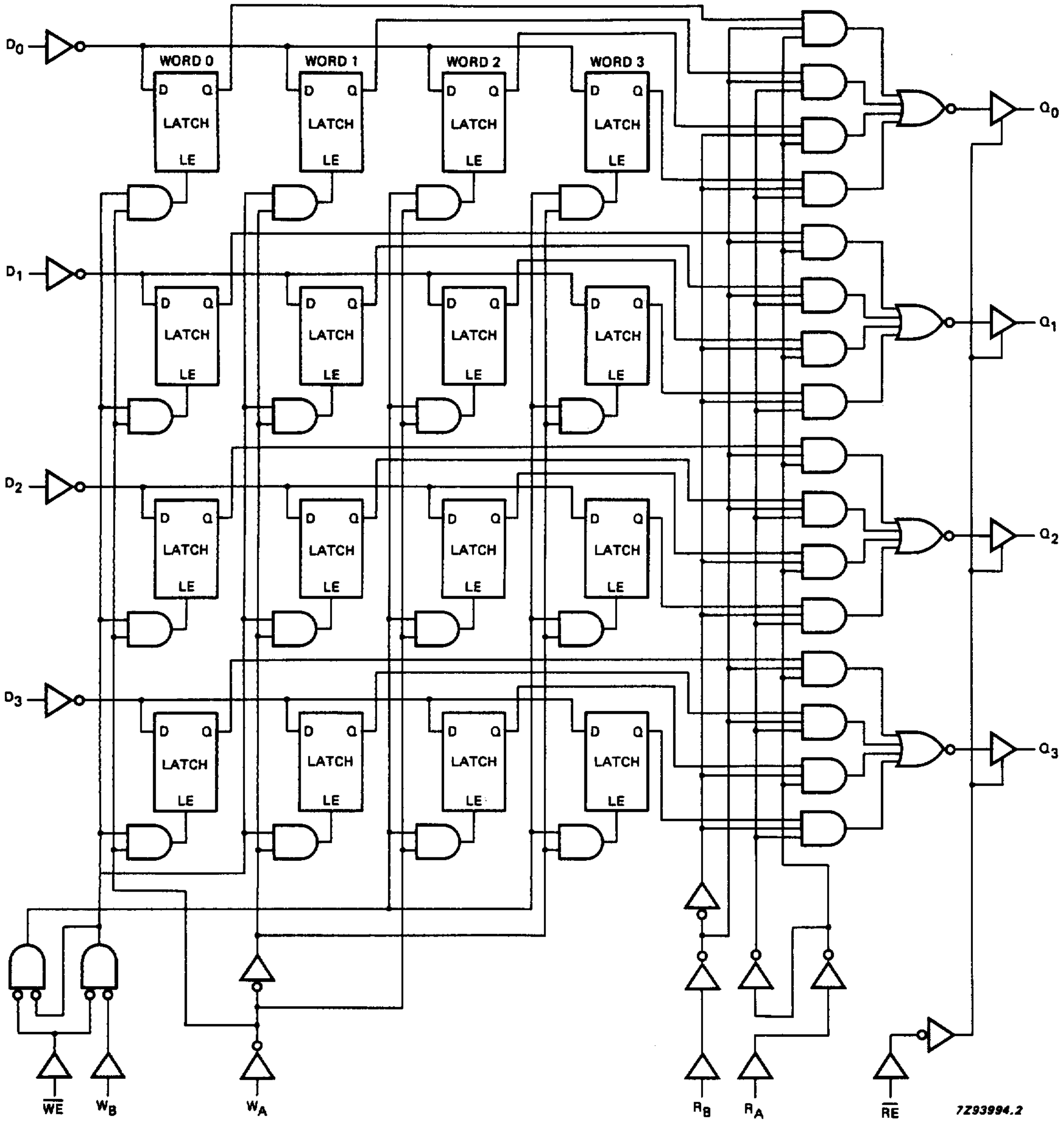


Fig.5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.
Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to+125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay R_A, R_B to Q_n		58 21 17	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $\overline{WE}$ to Q_n		77 28 22	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig.7
t_{PHL}/ t_{PLH}	propagation delay D_n to Q_n		74 27 22	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig.7
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{RE}$ to Q_n		39 14 11	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.9
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{RE}$ to Q_n		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.9
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.6
t_W	write enable pulse width LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t_{su}	set-up time D_n to $\overline{WE}$	60 12 10	3 1 1		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.8
t_{su}	set-up time W_A, W_B to $\overline{WE}$	60 12 10	6 2 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.8
t_h	hold time D_n to $\overline{WE}$	5 5 5	0 0 0		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig.8
t_h	hold time W_A, W_B to $\overline{WE}$	5 5 5	0 0 0		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig.8
t_{latch}	latch time $\overline{WE}$ to R_A, R_B	100 20 17	28 10 8		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.8

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *“74HC/HCT/HCU/HCMOS Logic Family Specifications”*.

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

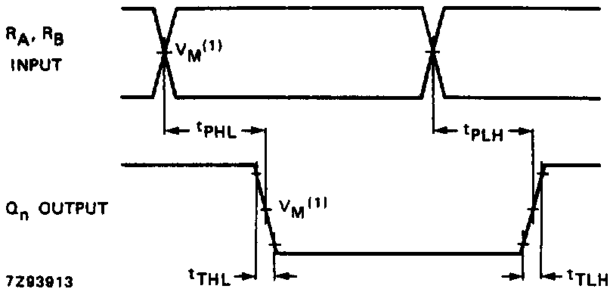
INPUT	UNIT LOAD COEFFICIENT
D_n	0.25
$\overline{WE}$, W_A	0.40
W_B	0.60
R_A	0.70
R_B	1.10
$\overline{RE}$	1.35

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

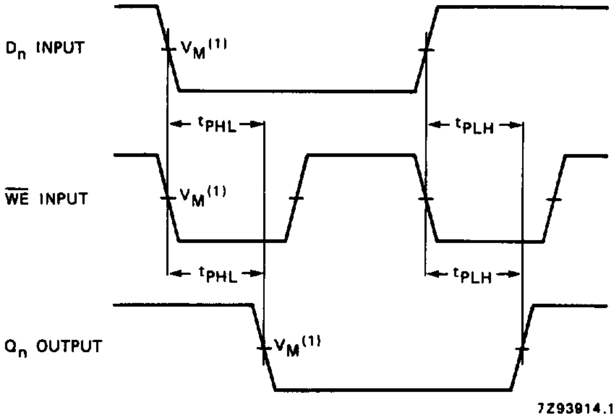
SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay R_A, R_B to Q_n		21	40		50		60	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $\overline{WE}$ to Q_n		28	50		63		75	ns	4.5	Fig.7
t_{PHL}/ t_{PLH}	propagation delay D_n to Q_n		27	50		63		75	ns	4.5	Fig.7
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{RE}$ to Q_n		18	35		44		53	ns	4.5	Fig.9
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{RE}$ to Q_n		19	35		44		53	ns	4.5	Fig.9
t_{THL}/ t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig.6
t_W	write enable pulse width LOW	18	9		23		27		ns	4.5	Fig.8
t_{su}	set-up time D_n to $\overline{WE}$	12	4		15		18		ns	4.5	Fig.8
t_{su}	set-up time W_A, W_B to $\overline{WE}$	12	−2		15		18		ns	4.5	Fig.8
t_h	hold time D_n to $\overline{WE}$	5	−1		5		5		ns	4.5	Fig.8
t_h	hold time W_A, W_B to $\overline{WE}$	5	0		5		5		ns	4.5	Fig.8
t_{latch}	latch time $\overline{WE}$ to R_A, R_B	25	11		31		38		ns	4.5	Fig.8

AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT : V_M = 1.3 V; V_I = GND to 3 V.

Fig.6 Waveforms showing the read address input (R_A, R_B) to output (Q_n) propagation delays and output transition times.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT : V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the write enable input ($\overline{WE}$) and data input (D_n) to output (Q_n) propagation delays, and the write enable pulse width.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT : V_M = 1.3 V; V_I = GND to 3 V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

The time allowed for the internal output of the latch to assume the state of the new data (t_{latch}) is important only when attempting to read from a location immediately after that location has received new data. This parameter is measured from the falling edge of $\overline{WE}$ to the rising edge of R_A or R_B, $\overline{RE}$ must be LOW.

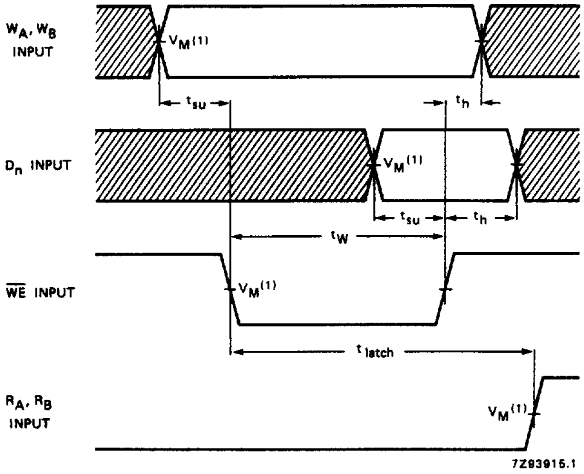
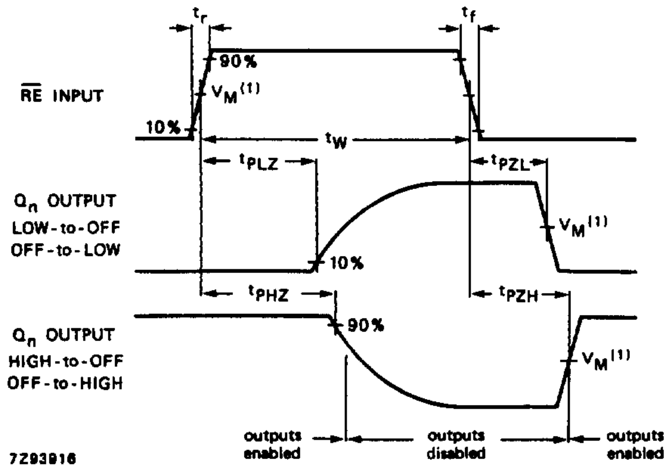


Fig.8 Waveforms showing the write address input (W_A, W_B) and data input (D_n) to write enable ($\overline{WE}$) set-up, hold and latch times.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT : V_M = 1.3 V; V_I = GND to 3 V.

Fig.9 Waveforms showing the read enable ($\overline{RE}$) to output (Q_n) enable and disable times, and the read enable pulse width.

PACKAGE OUTLINES

See *“74HC/HCT/HCU/HCMOS Logic Package Outlines”*.