74HC154; 74HCT154

4-to-16 line decoder/demultiplexer

Rev. 06 — 12 February 2007 | Product data sheet

1. General description

The 74HC154; 74HCT154 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL).

The 74HC154; 74HCT154 decoders accept four active HIGH binary address inputs and provide 16 mutually-exclusive active LOW outputs. The two-input enable gate can be used to strobe the decoder to eliminate the normal decoding ‘glitches’ on the outputs, or can be used for the expansion of the decoder.

The enable gate has two ANDed inputs which must be LOW to enable the outputs.

The 74HC154; 74HCT154 can be used as a 1-to-16 demultiplexer by using one of the enable inputs as the multiplexed data input.

When the other enable input is LOW, the addressed output will follow the state of the applied data.

2. Features

- 16-line demultiplexing capability
- Decodes 4 binary-coded inputs into 16 mutually-exclusive outputs
- Complies with JEDEC standard no. 7A
- Specified from –40 °C to +85 °C and –40 °C to +125 °C
- ESD protection:
  - HBM EIA/JESD22-A114D exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC154				
74HC154N	–40 °C to +125 °C	DIP24	plastic dual in-line package; 24 leads (600 mil)	SOT101-1
74HC154D	–40 °C to +125 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74HC154DB	–40 °C to +125 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
74HC154PW	–40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

Table 1. Ordering information *…continued*

Type number	Package			
	Temperature range	Name	Description	Version
74HC154BQ	–40 °C to +125 °C	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm	SOT815-1
74HCT154				
74HCT154N	–40 °C to +125 °C	DIP24	plastic dual in-line package; 24 leads (600 mil)	SOT101-1
74HCT154D	–40 °C to +125 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74HCT154DB	–40 °C to +125 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
74HCT154PW	–40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
74HCT154BQ	–40 °C to +125 °C	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm	SOT815-1

4. Functional diagram

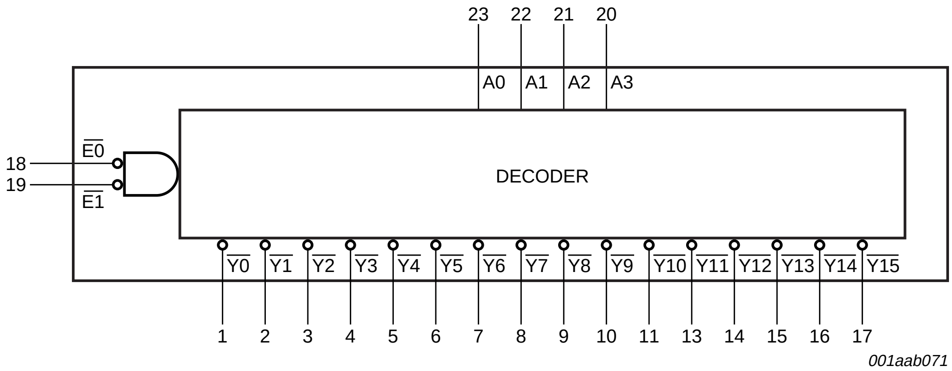


Fig 1. Functional diagram

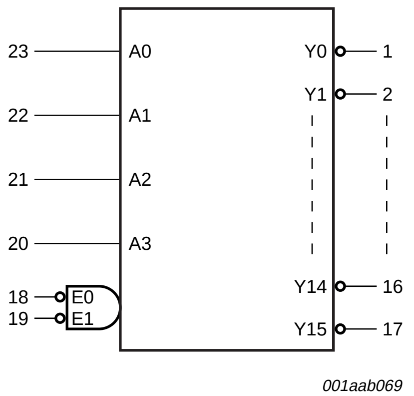


Fig 2. Logic symbol

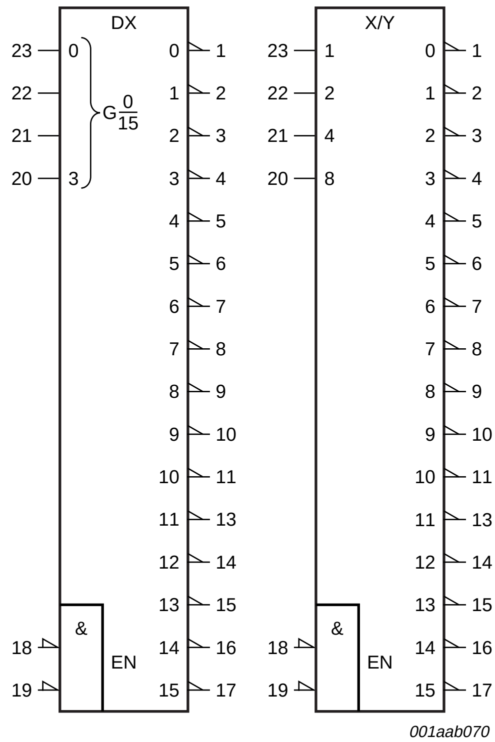


Fig 3. IEC logic symbol

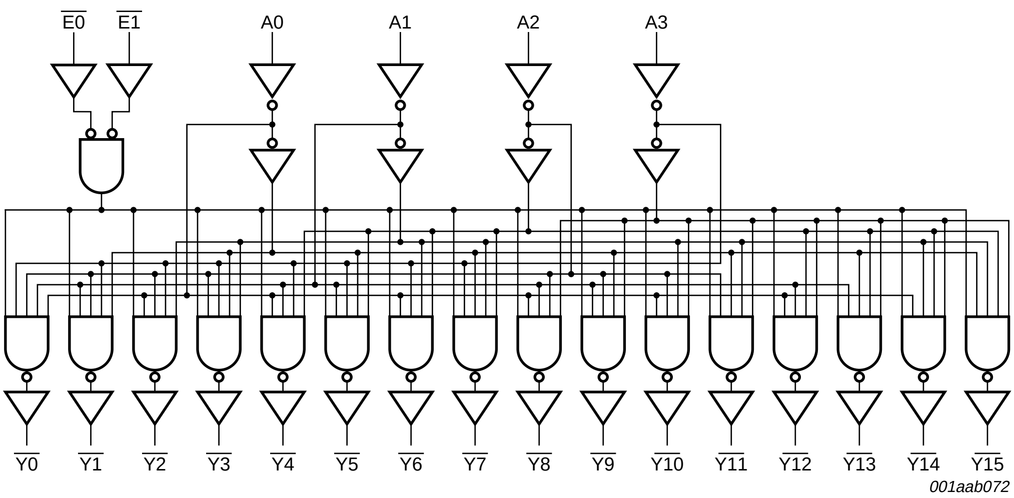


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

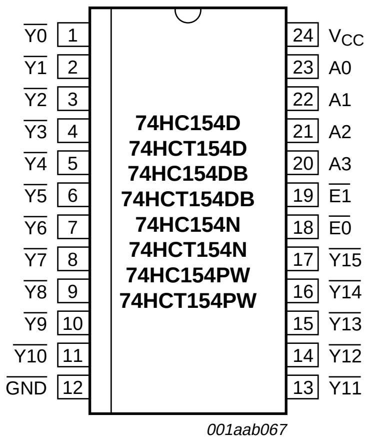
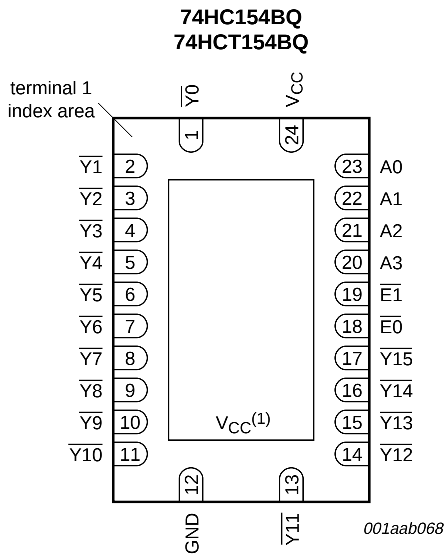


Fig 5. Pin configuration for SO24, DIP24, SSOP24 and TSSOP24



Transparent top view

(1) The die substrate is attached to this pad using conductive die attach material. It cannot be used as a supply pin or input.

Fig 6. Pin configuration for DHVQFN24

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{Y0}$	1	data output (active LOW)
$\overline{Y1}$	2	data output (active LOW)
$\overline{Y2}$	3	data output (active LOW)
$\overline{Y3}$	4	data output (active LOW)
$\overline{Y4}$	5	data output (active LOW)
$\overline{Y5}$	6	data output (active LOW)
$\overline{Y6}$	7	data output (active LOW)
$\overline{Y7}$	8	data output (active LOW)
$\overline{Y8}$	9	data output (active LOW)
$\overline{Y9}$	10	data output (active LOW)
$\overline{Y10}$	11	data output (active LOW)
GND	12	ground (0 V)
$\overline{Y11}$	13	data output (active LOW)
$\overline{Y12}$	14	data output (active LOW)

Table 2. Pin description *…continued*

Symbol	Pin	Description
$\overline{Y13}$	15	data output (active LOW)
$\overline{Y14}$	16	data output (active LOW)
$\overline{Y15}$	17	data output (active LOW)
$\overline{E0}$	18	enable input (active LOW)
$\overline{E1}$	19	enable input (active LOW)
A3	20	address input
A2	21	address input
A1	22	address input
A0	23	address input
V_{CC}	24	supply voltage

6. Functional description

Table 3. Function table[1]

Input						Output															
$\overline{E0}$	$\overline{E1}$	A0	A1	A2	A3	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	$\overline{Y8}$	$\overline{Y9}$	$\overline{Y10}$	$\overline{Y11}$	$\overline{Y12}$	$\overline{Y13}$	$\overline{Y14}$	$\overline{Y15}$
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
		H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
		L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
		H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
		L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
		H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
		L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
		H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
		L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
		H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
		L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
		H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
		L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
		H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
		L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
		H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

[1] H = HIGH voltage level
L = LOW voltage level
X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	$–0.5$ V $< V_O < V_{CC} + 0.5$ V	[1]	-	±25	mA
I_{CC}	supply current		[1]	-	50	mA
I_{GND}	ground current		[1]	-	–50	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[2]	-	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For DIP24 packages: P_{tot} derates linearly at 12 mW/K above 70 °C.
For SO24 packages: P_{tot} derates linearly at 8 mW/K above 70 °C.
For SSOP24 and TSSOP24 packages: P_{tot} derates linearly at 5.5 mW/K above 60 °C.
For DHVQFN24 packages: P_{tot} derates linearly at 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HC154						
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
t_r	rise time	V_{CC} = 2.0 V	-	-	1000	ns
		V_{CC} = 4.5 V	-	6.0	500	ns
		V_{CC} = 6.0 V	-	-	400	ns
t_f	fall time	V_{CC} = 2.0 V	-	-	1000	ns
		V_{CC} = 4.5 V	-	6.0	500	ns
		V_{CC} = 6.0 V	-	-	400	ns
74HCT154						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
t_r	input rise time	V_{CC} = 4.5 V	-	6.0	500	ns
t_f	input fall time	V_{CC} = 4.5 V	-	6.0	500	ns

9. Static characteristics

Table 6. Static characteristics 74HC154

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		V_{CC} = 2.0 V; I_O = –20 μA	1.9	2.0	-	V
		V_{CC} = 4.5 V; I_O = –20 μA	4.4	4.5	-	V
		V_{CC} = 6.0 V; I_O = –20 μA	5.9	6.0	-	V
		V_{CC} = 4.5 V; I_O = –4.0 mA	3.98	4.32	-	V
		V_{CC} = 6.0 V; I_O = –5.2 mA	5.48	5.81	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		V_{CC} = 2.0 V; I_O = 20 μA	-	0	0.1	V
		V_{CC} = 4.5 V; I_O = 20 μA	-	0	0.1	V
		V_{CC} = 6.0 V; I_O = 20 μA	-	0	0.1	V
		V_{CC} = 4.5 V; I_O = 4.0 mA	-	0.15	0.26	V
		V_{CC} = 6.0 V; I_O = 5.2 mA	-	0.16	0.26	V
I_I	input leakage current	V_{CC} = 6.0 V; $V_I = V_{CC}$ or GND	-	-	±0.1	μA
I_{CC}	supply current	V_{CC} = 6.0 V; $V_I = V_{CC}$ or GND; I_O = 0 A	-	-	8.0	μA
C_I	input capacitance		-	3.5	-	pF
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		V_{CC} = 2.0 V; I_O = –20 μA	1.9	-	-	V
		V_{CC} = 4.5 V; I_O = –20 μA	4.4	-	-	V
		V_{CC} = 6.0 V; I_O = –20 μA	5.9	-	-	V
		V_{CC} = 4.5 V; I_O = –4.0 mA	3.84	-	-	V
		V_{CC} = 6.0 V; I_O = –5.2 mA	5.34	-	-	V

Table 6. Static characteristics 74HC154 *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$V_{CC} = 2.0$ V; $I_O = 20$ μA	-	-	0.1	V
		$V_{CC} = 4.5$ V; $I_O = 20$ μA	-	-	0.1	V
		$V_{CC} = 6.0$ V; $I_O = 20$ μA	-	-	0.1	V
		$V_{CC} = 4.5$ V; $I_O = 4.0$ mA	-	-	0.33	V
		$V_{CC} = 6.0$ V; $I_O = 5.2$ mA	-	-	0.33	V
I_I	input leakage current	$V_{CC} = 6.0$ V; $V_I = V_{CC}$ or GND	-	-	±1.0	μA
I_{CC}	supply current	$V_{CC} = 6.0$ V; $V_I = V_{CC}$ or GND; $I_O = 0$ A	-	-	80	μA
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0$ V	1.5	-	-	V
		$V_{CC} = 4.5$ V	3.15	-	-	V
		$V_{CC} = 6.0$ V	4.2	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0$ V	-	-	0.5	V
		$V_{CC} = 4.5$ V	-	-	1.35	V
		$V_{CC} = 6.0$ V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$V_{CC} = 2.0$ V; $I_O = –20$ μA	1.9	-	-	V
		$V_{CC} = 4.5$ V; $I_O = –20$ μA	4.4	-	-	V
		$V_{CC} = 6.0$ V; $I_O = –20$ μA	5.9	-	-	V
		$V_{CC} = 4.5$ V; $I_O = –4.0$ mA	3.7	-	-	V
		$V_{CC} = 6.0$ V; $I_O = –5.2$ mA	5.2	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$V_{CC} = 2.0$ V; $I_O = 20$ μA	-	-	0.1	V
		$V_{CC} = 4.5$ V; $I_O = 20$ μA	-	-	0.1	V
		$V_{CC} = 6.0$ V; $I_O = 20$ μA	-	-	0.1	V
		$V_{CC} = 4.5$ V; $I_O = 4.0$ mA	-	-	0.4	V
		$V_{CC} = 6.0$ V; $I_O = 5.2$ mA	-	-	0.4	V
I_I	input leakage current	$V_{CC} = 6.0$ V; $V_I = V_{CC}$ or GND	-	-	±0.1	μA
I_{CC}	supply current	$V_{CC} = 6.0$ V; $V_I = V_{CC}$ or GND; $I_O = 0$ A	-	-	160	μA

Table 7. Static characteristics 74HCT154

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	1.6	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	1.2	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$V_{CC} = 4.5$ V; $I_O = –20$ μA	4.4	4.5	-	V
		$V_{CC} = 4.5$ V; $I_O = –4$ mA	3.98	4.32	-	V

Table 7. Static characteristics 74HCT154 *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$V_{CC} = 4.5$ V; $I_O = 20$ µA	-	0	0.1	V
		$V_{CC} = 4.5$ V; $I_O = 4$ mA	-	0.15	0.25	V
I_I	input leakage current	$V_{CC} = 5.5$ V; $V_I = V_{CC}$ or GND	-	-	±0.1	µA
I_{CC}	supply current	$V_{CC} = 5.5$ V; $V_I = V_{CC}$ or GND; $I_O = 0$ A	-	-	8.0	µA
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 4.5$ V to 5.5 V; $V_I = V_{CC} - 2.1$ V; $I_O = 0$ A	-	-	360	µA
C_I	input capacitance		-	3.5	-	pF
$T_{amb} = -40$ °C to +85 °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$V_{CC} = 4.5$ V; $I_O = -20$ µA	4.4	-	-	V
		$V_{CC} = 4.5$ V; $I_O = -4$ mA	3.84	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$V_{CC} = 4.5$ V; $I_O = 20$ µA	-	-	0.1	V
		$V_{CC} = 4.5$ V; $I_O = 4$ mA	-	-	0.33	V
I_I	input leakage current	$V_{CC} = 5.5$ V; $V_I = V_{CC}$ or GND	-	-	±1.0	µA
I_{CC}	supply current	$V_{CC} = 5.5$ V; $V_I = V_{CC}$ or GND; $I_O = 0$ A	-	-	80	µA
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 4.5$ V to 5.5 V; $V_I = V_{CC} - 2.1$ V; $I_O = 0$ A	-	-	450	µA
$T_{amb} = -40$ °C to +125 °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$V_{CC} = 4.5$ V; $I_O = -20$ µA	4.4	-	-	V
		$V_{CC} = 4.5$ V; $I_O = -4$ mA	3.7	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$V_{CC} = 4.5$ V; $I_O = 20$ µA	-	-	0.1	V
		$V_{CC} = 4.5$ V; $I_O = 4$ mA	-	-	0.4	V
I_I	input leakage current	$V_{CC} = 5.5$ V; $V_I = V_{CC}$ or GND	-	-	±1.0	µA
I_{CC}	supply current	$V_{CC} = 5.5$ V; $V_I = V_{CC}$ or GND; $I_O = 0$ A	-	-	160	µA
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 4.5$ V to 5.5 V; $V_I = V_{CC} - 2.1$ V; $I_O = 0$ A	-	-	490	µA

10. Dynamic characteristics

Table 8. Dynamic characteristics

GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Figure 9.

Symbol	Parameter	Conditions		25 °C			−40 °C to +125 °C			Unit
				Min	Typ	Max	Min	Max (85 °C)	Max (125 °C)	
74HC154										
t_{pd}	propagation delay	An to $\overline{Yn}$; see Figure 7	[1]							
		V_{CC} = 2.0 V		-	36	150	-	190	225	ns
		V_{CC} = 4.5 V		-	13	30	-	38	45	ns
		V_{CC} = 5 V; C_L = 15 pF		-	11	-	-	-	-	ns
		V_{CC} = 6.0 V		-	10	26	-	33	38	ns
		$\overline{En}$ to $\overline{Yn}$; see Figure 8								
		V_{CC} = 2.0 V		-	39	150	-	190	225	ns
		V_{CC} = 4.5 V		-	14	30	-	38	45	ns
		V_{CC} = 5 V; C_L = 15 pF		-	11	-	-	-	-	ns
		V_{CC} = 6.0 V		-	11	26	-	33	38	ns
t_t	transition time	see Figure 7 and 8	[2]							
		V_{CC} = 2.0 V		-	19	75	-	95	110	ns
		V_{CC} = 4.5 V		-	7	15	-	19	22	ns
		V_{CC} = 6.0 V		-	6	13	-	16	19	ns
C_{PD}	power dissipation capacitance	per gate; V_I = GND to V_{CC}	[3]	-	60	-	-	-	-	pF
74HCT154										
t_{pd}	propagation delay	An to $\overline{Yn}$; see Figure 7	[1]							
		V_{CC} = 4.5 V		-	16	35	-	44	53	ns
		V_{CC} = 5 V; C_L = 15 pF		-	13	-	-	-	-	ns
		$\overline{En}$ to $\overline{Yn}$; see Figure 8								
		V_{CC} = 4.5 V		-	15	32	-	40	48	ns
		V_{CC} = 5 V; C_L = 15 pF		-	13	-	-	-	-	ns
t_t	transition time	see Figure 7 and 8	[2]							
		V_{CC} = 4.5 V		-	7	15	-	19	22	ns
C_{PD}	power dissipation capacitance	per gate; V_I = GND to (V_{CC} − 1.5 V)	[3]	-	60	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}

[2] t_t is the same as t_{TLH} and t_{THL}

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

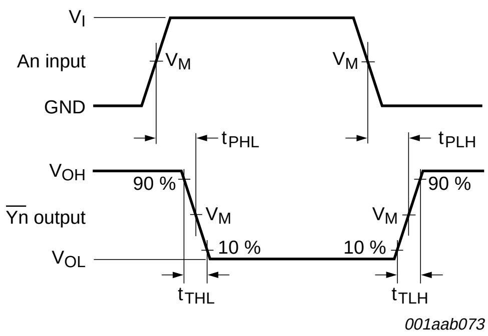
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of load switching outputs;

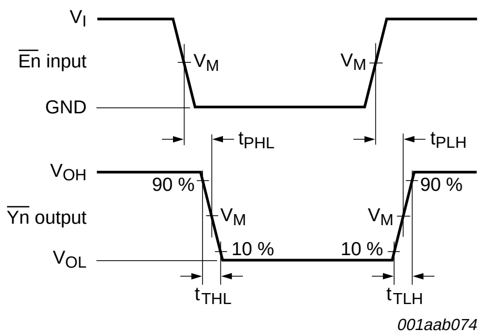
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11. Waveforms



Measurement points are given in Table 9.

Fig 7. Propagation delay address input (An) to output ($\overline{Yn}$) and transition time output ($\overline{Yn}$)

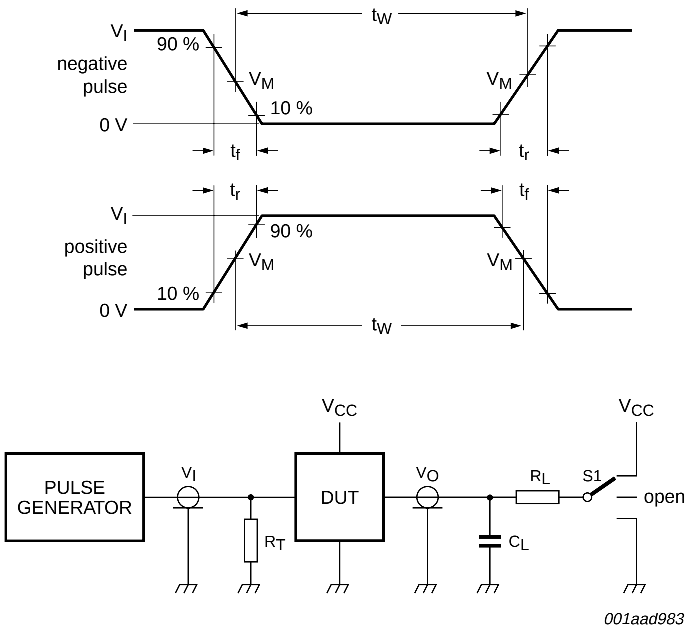


Measurement points are given in Table 9.

Fig 8. Propagation delay enable input ($\overline{En}$) to output ($\overline{Yn}$) and transition time output ($\overline{Yn}$)

Table 9. Measurement points

Type	Input	Output
	V_M	V_M
74HC154	$0.5V_{CC}$	$0.5V_{CC}$
74HCT154	1.3 V	1.3 V



Test data is given in Table 10.

Definitions for test circuit:

R_T = Termination resistance; should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistor.

S1 = Test selection switch.

Fig 9. Load circuitry for measuring switching times

Table 10. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
74HC154	V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open
74HCT154	3 V	6 ns	15 pF, 50 pF	1 kΩ	open

12. Application information

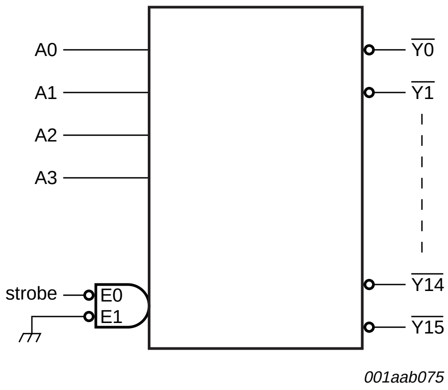


Fig 10. 1-of-16 decoder; LOW level output selected

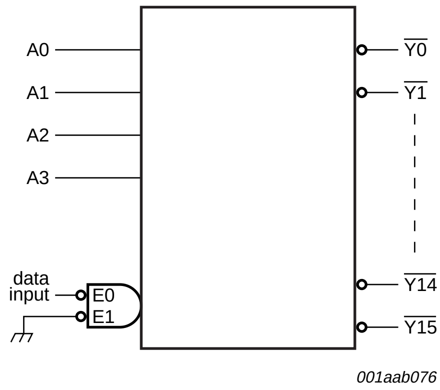
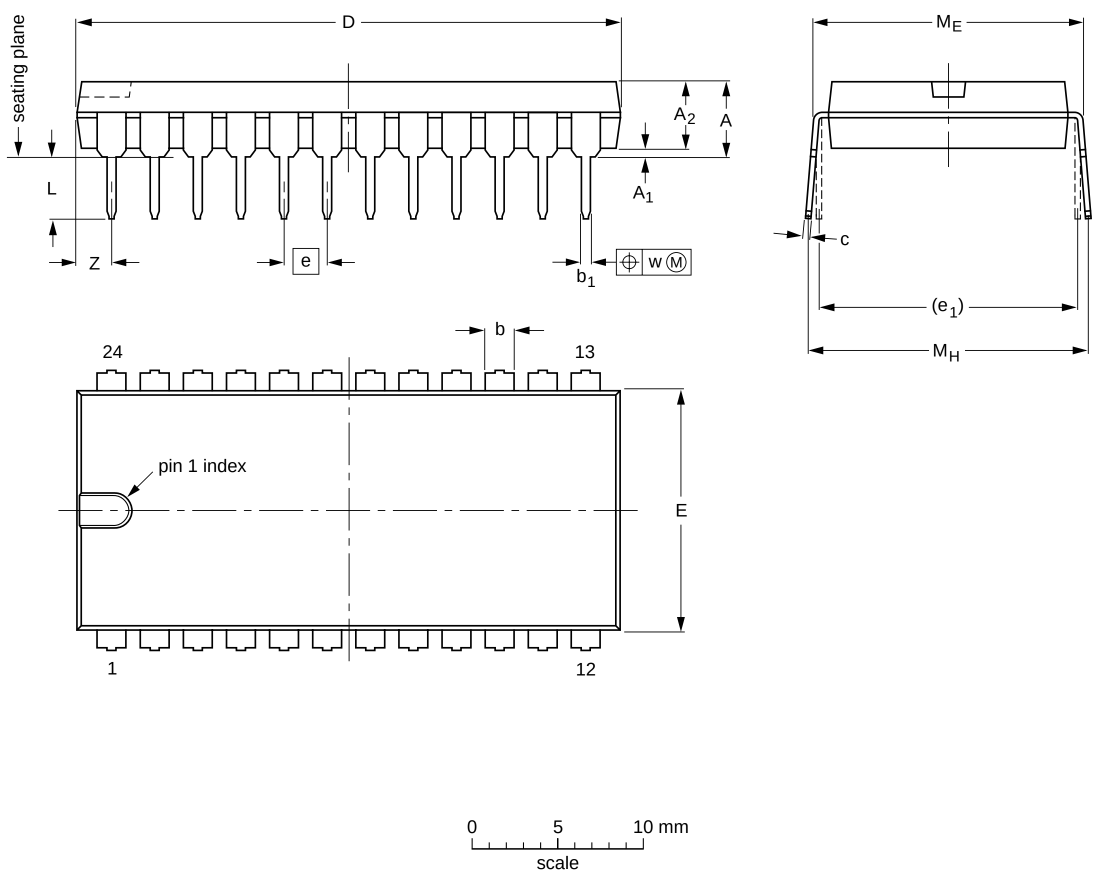


Fig 11. 1-of-16 demultiplexer; logic level on selected outputs follow the logic level on the data input

13. Package outline

DIP24: plastic dual in-line package; 24 leads (600 mil) **SOT101-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4	1.7 1.3	0.53 0.38	0.32 0.23	32.0 31.4	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	2.2
inches	0.2	0.02	0.16	0.066 0.051	0.021 0.015	0.013 0.009	1.26 1.24	0.56 0.54	0.1	0.6	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.087

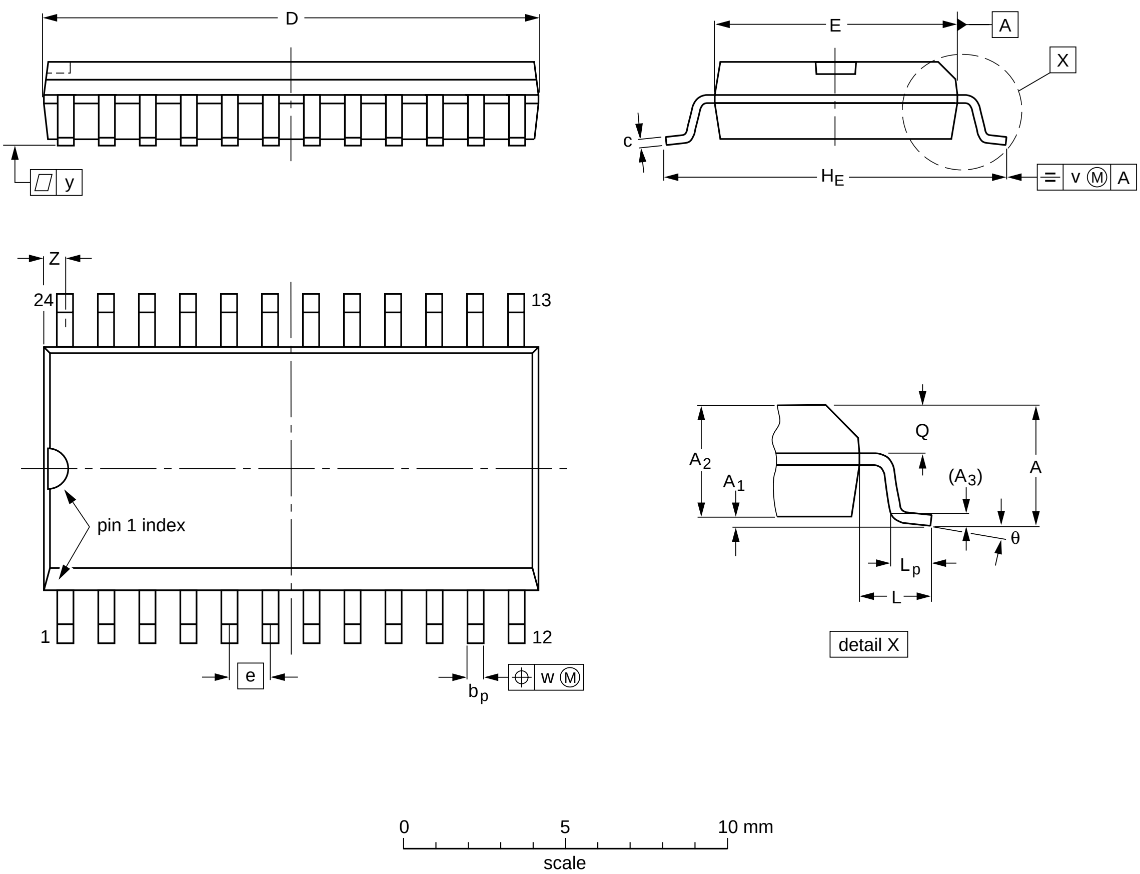
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT101-1	051G02	MO-015	SC-509-24			~~99-12-27~~ 03-02-13

Fig 12. Package outline SOT101-1 (DIP24)

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

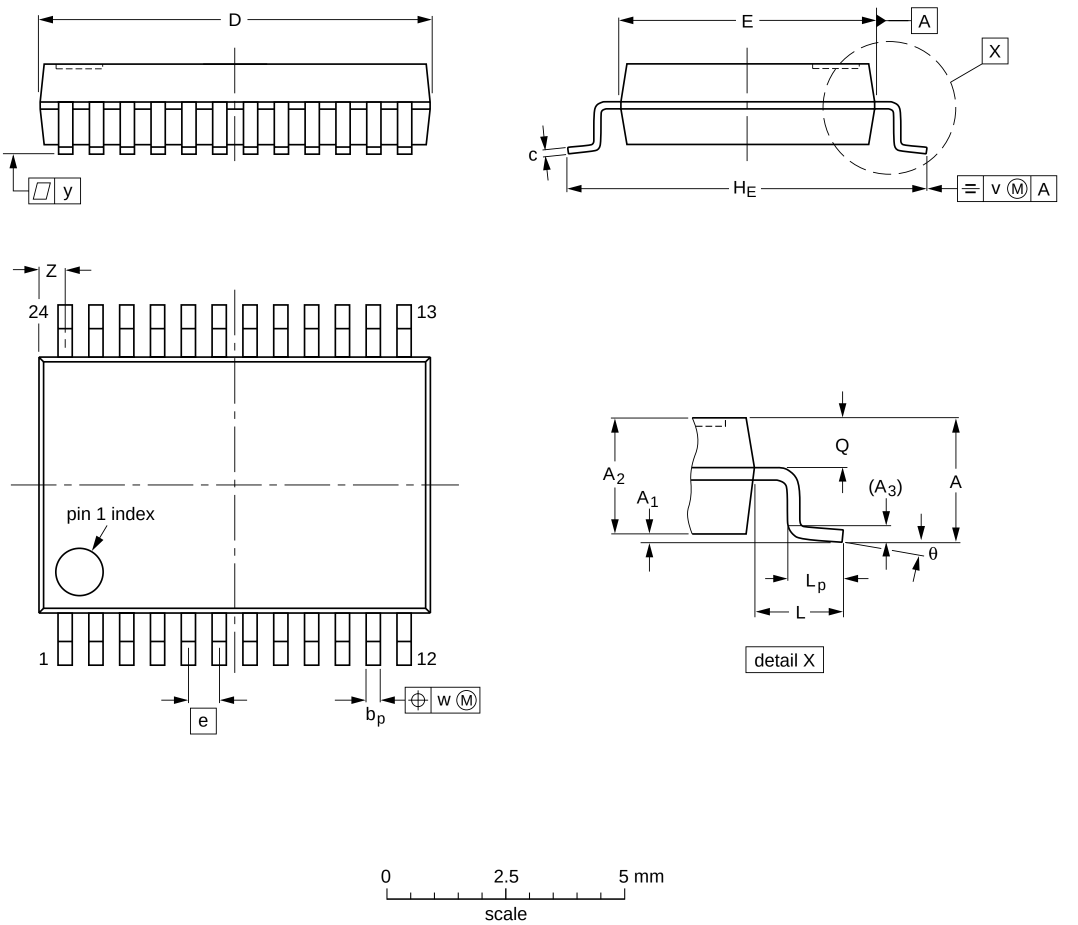
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT137-1 (SO24)

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

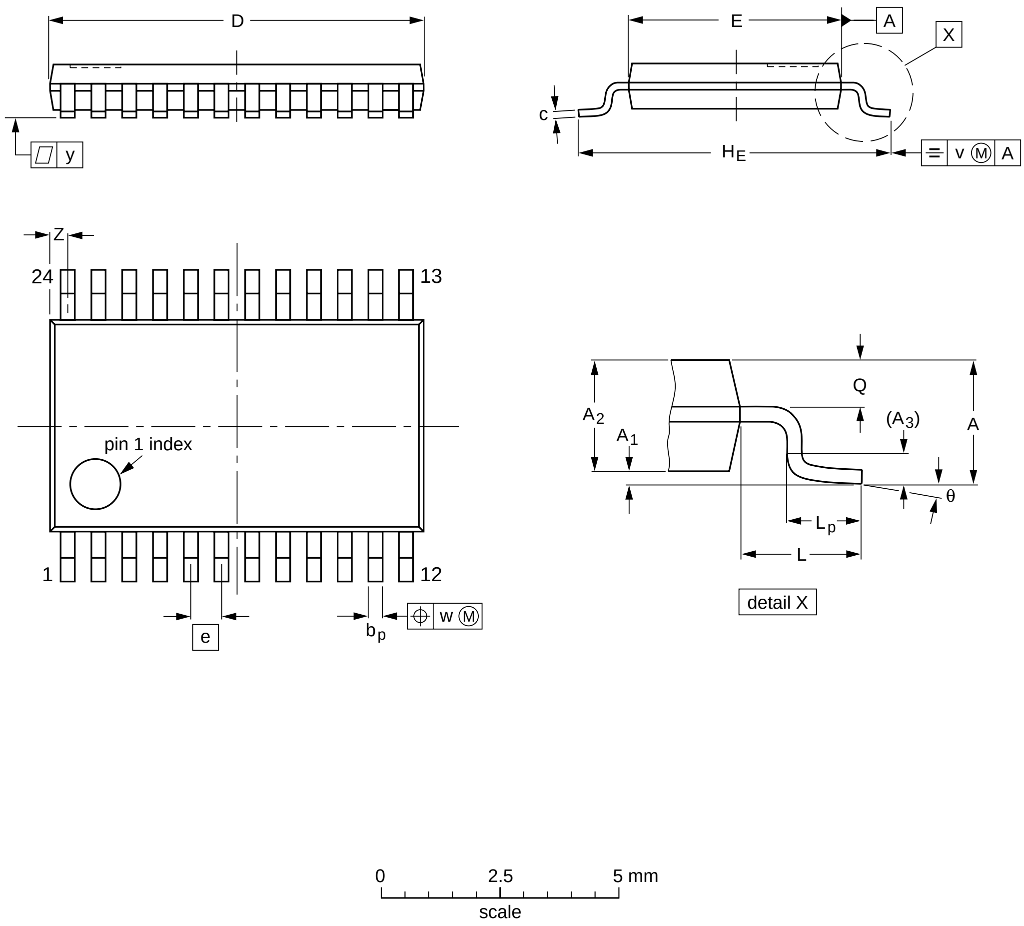
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19

Fig 14. Package outline SOT340-1 (SSOP24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

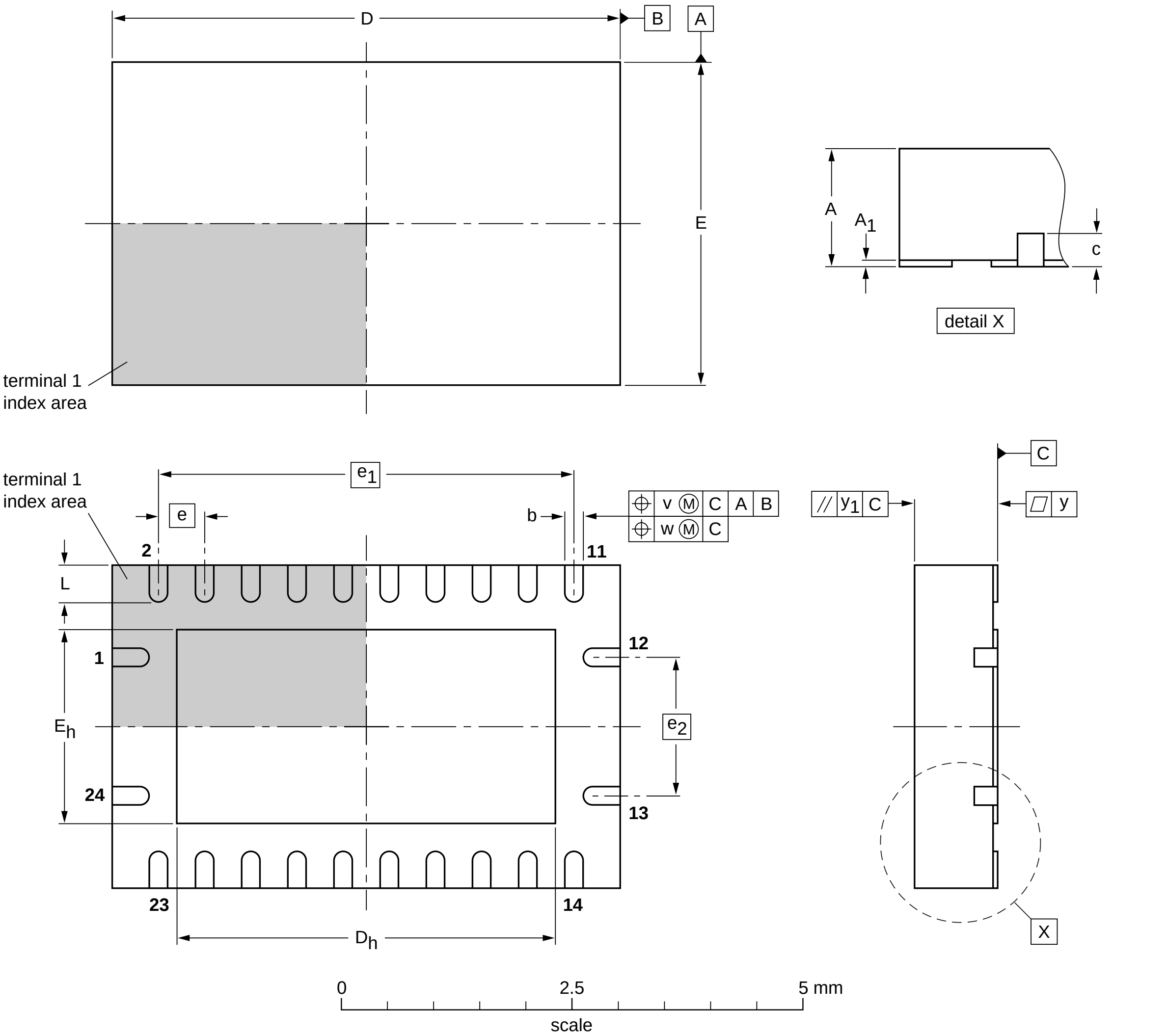
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig 15. Package outline SOT355-1 (TSSOP24)

DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm **SOT815-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
mm	1	0.05 0.00	0.30 0.18	0.2	5.6 5.4	4.25 3.95	3.6 3.4	2.25 1.95	0.5	4.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT815-1	- - -	- - -	- - -			03-04-29

Fig 16. Package outline SOT815-1 (DHVQFN24)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT154_6	20070212	Product data sheet	-	74HC_HCT154_5
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 3 on page 5: Corrected errors in output information.			
74HC_HCT154_5	20041012	Product specification	-	74HC_HCT154_4
74HC_HCT154_4	20041005	Product specification	-	74HC_HCT154_3
74HC_HCT154_3	20040601	Product specification	-	74HC_HCT154_CNV_2

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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