FAIRCHILD SEMICONDUCTOR™

September 1983
Revised February 1999

MM74HC251
8-Channel 3-STATE Multiplexer

General Description

The MM74HC251 8-channel digital multiplexer with 3-STATE outputs utilizes advanced silicon-gate CMOS technology. Along with the high noise immunity and low power consumption of standard CMOS integrated circuits, it possesses the ability to drive 10 LS-TTL loads. The large output drive capability and 3-STATE feature make this part ideally suited for interfacing with bus lines in a bus oriented system.

This multiplexer features both true (Y) and complement (W) outputs as well as a STROBE input. The STROBE must be at a low logic level to enable this device. When the STROBE input is HIGH, both outputs are in the high impedance state. When enabled, address information on the data select inputs determines which data input is routed to the Y and W outputs. The 74HC logic family is speed, function, as well as pinout compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay
  Data select to Y: 26 ns
- Wide supply range: 2–6V
- Low power supply quiescent current:
  80 μA maximum (74HC)
- 3-STATE outputs for interface to bus oriented systems

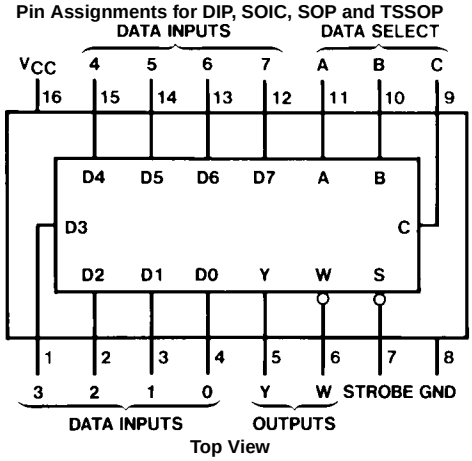
Ordering Code:

Order Number	Package Number	Package Description
MM74HC251M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
MM74HC251SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC251MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC251N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



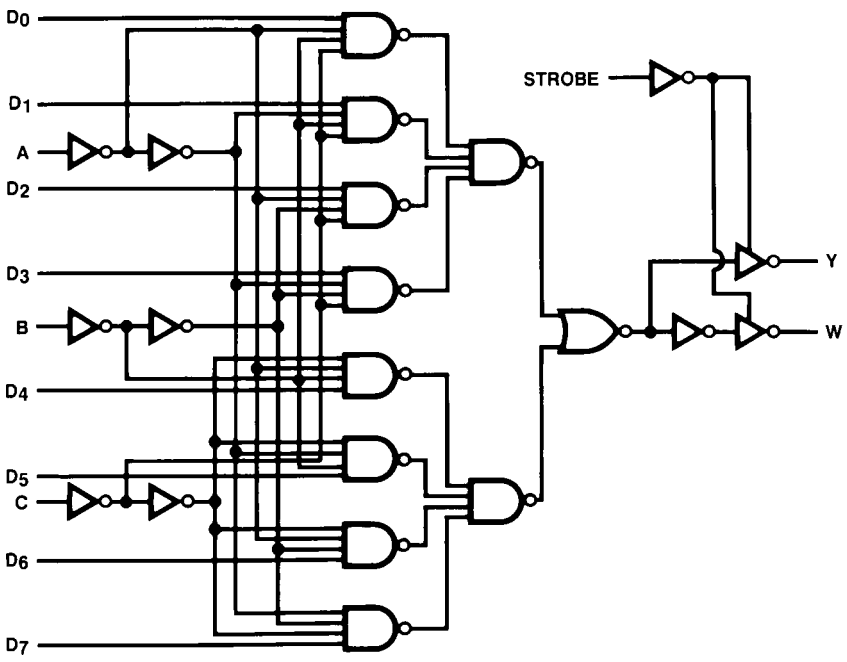
Top View

Truth Table

Inputs				Outputs	
Select			Strobe	Y	W
C	B	A	S		
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = HIGH Logic Level, L = LOW Logic Level
X = Irrelevant, Z = High Impedance (off)
D0, D1. . . D7 = The level of the respective D input

Logic Diagram



Absolute Maximum Ratings (Note 1)

(Note 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	−40	+85	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	T_A = −40 to 85°C	T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \le 20$ μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum LOW Level Output Voltage	V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \le 20$ μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum 3-STATE Leakage Current	Strobe = V_{CC}	6.0V		±0.5	±5	±10	μA
		V_{OUT} = V_{CC} or GND						
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	6.0V		8.0	80	160	μA
		I_{OUT} = 0 μA						

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, $t_r = t_f$ = 6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to Y		26	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A, B or C to W		27	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any D to Y		22	29	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any D to W		24	32	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time, W Output	R_L = 1 kΩ C_L = 50 pF	19	27	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time, Y Output	R_L = 1 kΩ C_L = 50 pF	19	26	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time W Output	R_L = 1 kΩ C_L = 5 pF	26	40	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time Y Output	R_L = 1 kΩ C_L = 5 pF	27	35	ns

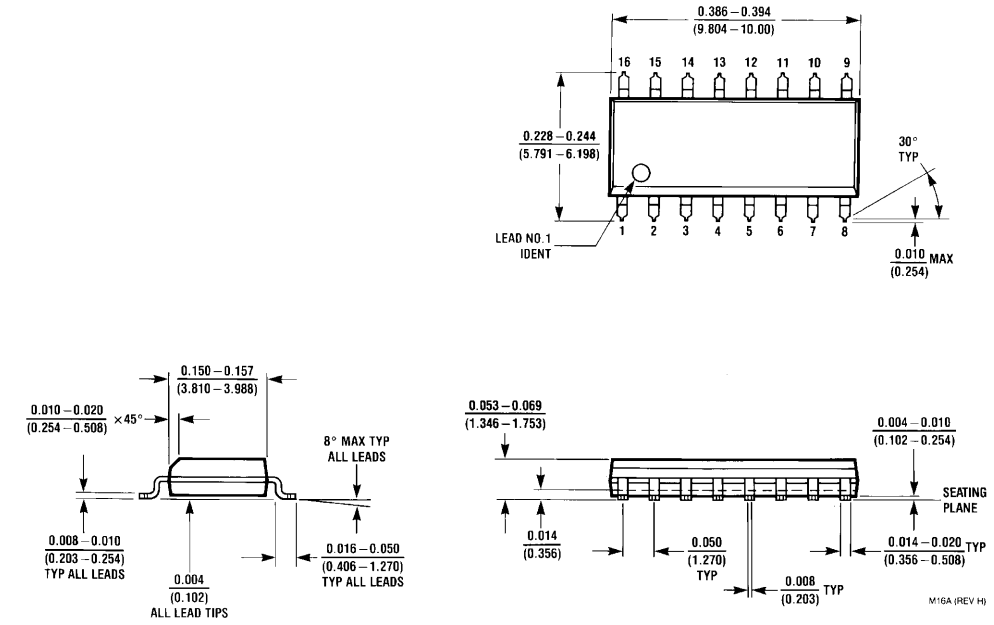
AC Electrical Characteristics

C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

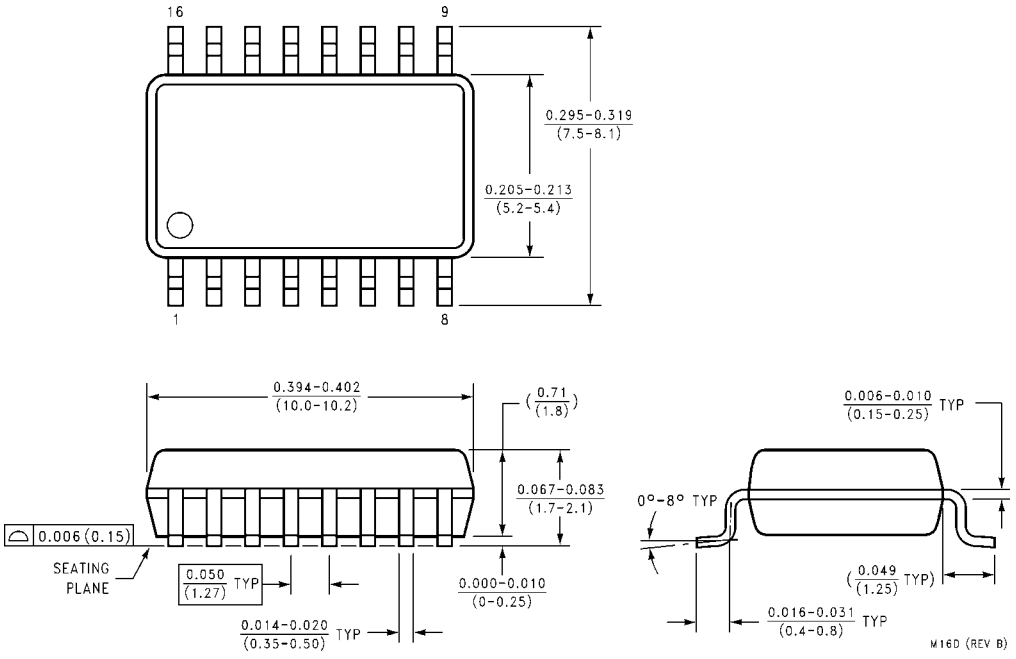
Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	T_A = −40 to 85°C	T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to Y		2.0V	90	205	256	300	ns
			4.5V	31	41	51	60	ns
			6.0V	26	35	44	51	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A, B or C to W		2.0V	95	205	256	300	ns
			4.5V	32	41	51	60	ns
			6.0V	27	35	44	51	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any D to Y		2.0V	70	195	244	283	ns
			4.5V	27	39	49	57	ns
			6.0V	23	33	41	48	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any D to W		2.0V	75	185	231	268	ns
			4.5V	29	37	46	54	ns
			6.0V	25	32	40	46	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time W Output	R_L = 1 kΩ	2.0V	45	150	188	218	ns
			4.5V	21	30	38	44	ns
			6.0V	18	26	33	38	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time Y Output	R_L = 1 kΩ	2.0V	45	145	181	210	ns
			4.5V	21	29	36	42	ns
			6.0V	18	25	31	36	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time W Output	R_L = 1 kΩ	2.0V	60	220	275	319	ns
			4.5V	29	44	55	64	ns
			6.0V	25	37	46	54	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time Y Output	R_L = 1 kΩ	2.0V	60	195	244	283	ns
			4.5V	30	39	49	57	ns
			6.0V	26	33	41	48	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		110				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Physical Dimensions inches (millimeters) unless otherwise noted

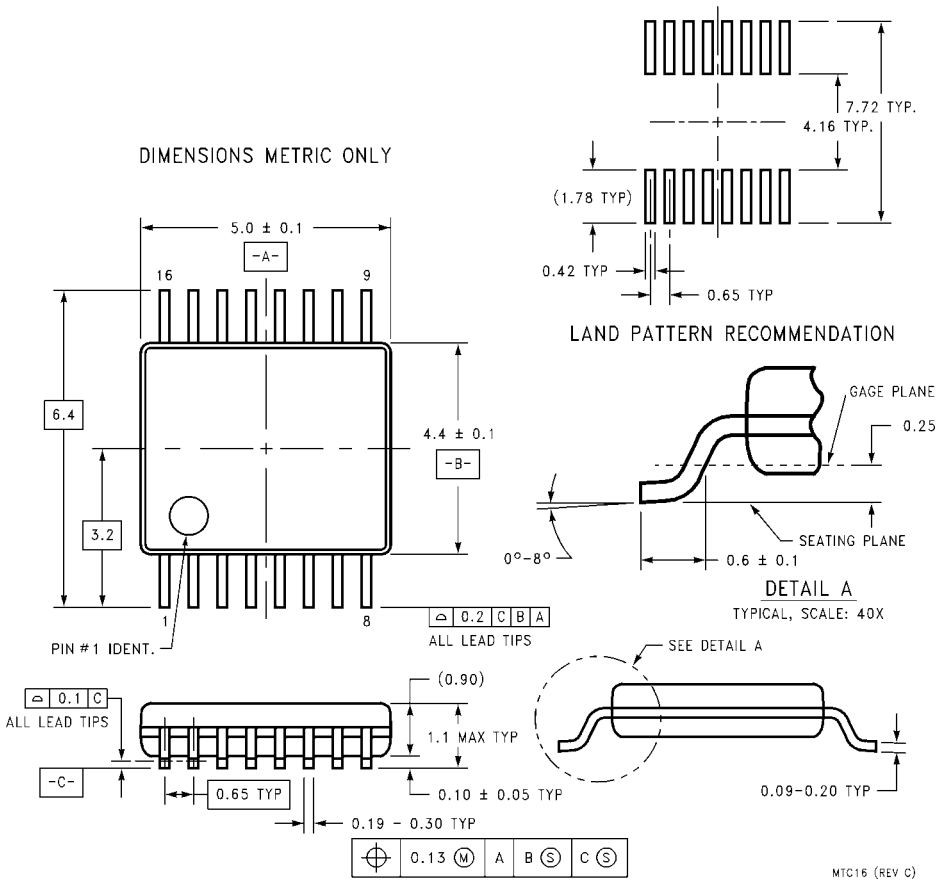


16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A



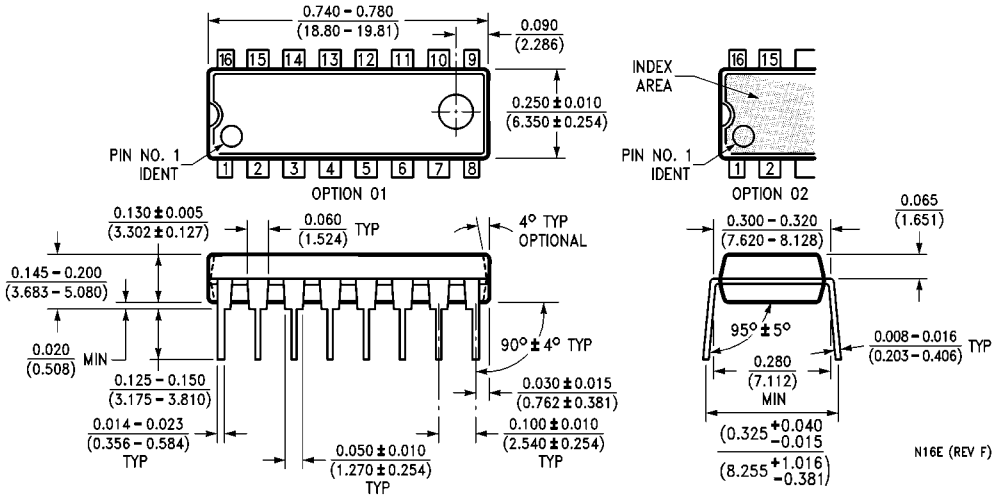
16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16A

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com