



HESTORE.HU

elektronikai alkatrész áruház

EN: This Datasheet is presented by the manufacturer.

Please visit our website for pricing and availability at www.hestore.hu.

74HC257; 74HCT257

Quad 2-input multiplexer; 3-state

Rev. 05 — 13 January 2010

Product data sheet

1. General description

The 74HC257; 74HCT257 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL).

The 74HC257 and 74HCT257 have four identical 2-input multiplexers with 3-state outputs, which select 4 bits of data from two sources and are controlled by a common data select input (S).

The data inputs from source 0 (1I0 to 4I0) are selected when input S is LOW and the data inputs from source 1 (1I1 to 4I1) are selected when S is HIGH. Data appears at the outputs (1Y to 4Y) in true (non-inverting) form from the selected inputs.

The 74HC257 and 74HCT257 are the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S. The outputs are forced to a high-impedance OFF-state when \overline{OE} is HIGH.

The logic equations for the outputs are:

$$1\bar{Y} = \overline{OE} \cdot (1I1 \cdot S \cdot 1I0 \cdot \bar{S})$$

$$2\bar{Y} = \overline{OE} \cdot (2I1 \cdot S \cdot 2I0 \cdot \bar{S})$$

$$3\bar{Y} = \overline{OE} \cdot (3I1 \cdot S \cdot 3I0 \cdot \bar{S})$$

$$4\bar{Y} = \overline{OE} \cdot (4I1 \cdot S \cdot 4I0 \cdot \bar{S})$$

Except for their non-inverting (true) outputs the 74HC257; 74HCT257 are identical to the 74HC258.

2. Features

- Non-inverting data path
- 3-state outputs interface directly with system bus
- Complies with JEDEC standard no. 7A
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC257N 74HCT257N	-40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HC257D 74HCT257D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC257DB 74HCT257DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC257PW 74HCT257PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

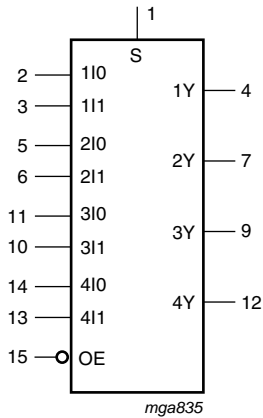


Fig 1. Logic symbol

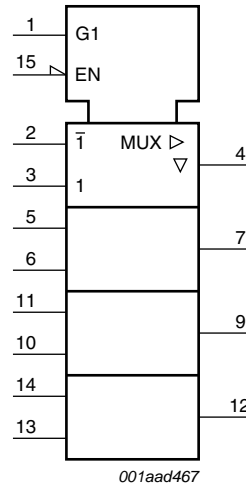


Fig 2. IEC logic symbol

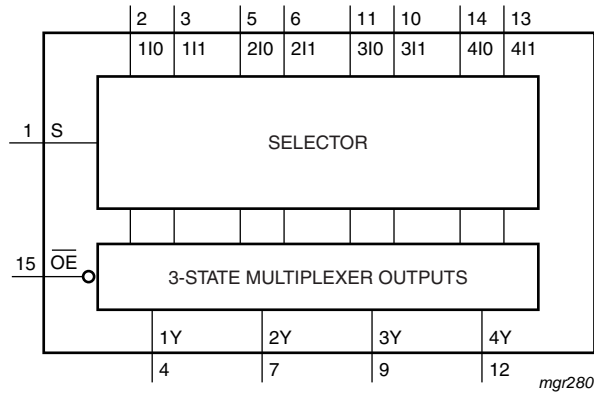


Fig 3. Functional diagram

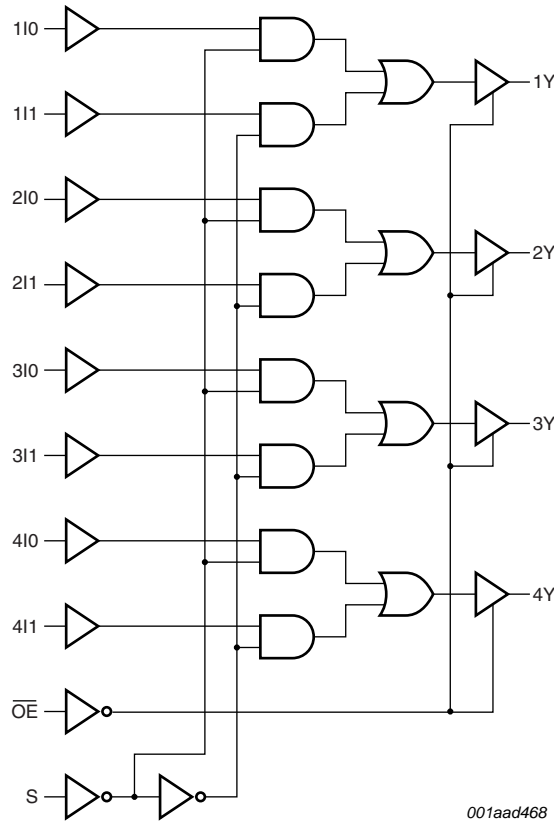


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

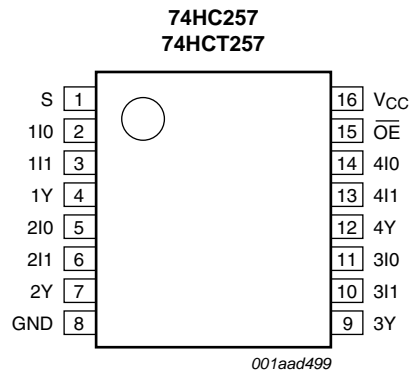


Fig 5. Pin configuration DIP16, SO16, SSOP16 and TSSOP16

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
S	1	common data select input
1I0 to 4I0	2, 5, 11, 14	data input from source 0
1I1 to 4I1	3, 6, 10, 13	data input from source 1
1Y to 4Y	4, 7, 9, 12	3-state multiplexer output
GND	8	ground (0 V)
\overline{OE}	15	3-state output enable input (active LOW)
V _{CC}	16	supply voltage

6. Functional description

6.1 Function table

Table 3. Function table^[1]

Control		Input		Output
\overline{OE}	S	nI0	nI1	nY
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	± 20	mA
I_O	output current	$V_O = -0.5$ V to $V_{CC} + 0.5$ V	-	± 35	mA
I_{CC}	supply current		-	+70	mA
I_{GND}	ground current		-	-70	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation				
	DIP16 package		[1] -	750	mW
	SO16 package		[2] -	500	mW
	SSOP16 package		[3] -	500	mW
	TSSOP16 package		[3] -	500	mW

[1] For DIP16 packages: above 70 °C, P_{tot} derates linearly with 12 mW/K.

[2] For SO16 packages: above 70 °C, P_{tot} derates linearly with 8 mW/K.

[3] For SSOP16 and TSSOP16 packages: above 60 °C, P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Type 74HC257						
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
$\Delta t/\Delta V$	input transition rise and fall rates	$V_{CC} = 2.0$ V	-	-	625	ns
		$V_{CC} = 4.5$ V	-	1.67	139	ns
		$V_{CC} = 6.0$ V	-	-	83	ns
T_{amb}	ambient temperature		-40	-	+125	°C
Type 74HCT257						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
$\Delta t/\Delta V$	input transition rise and fall rates	$V_{CC} = 4.5$ V	-	1.67	139	ns
T_{amb}	ambient temperature		-40	-	+125	°C

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC257										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -6.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 6.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1.0	±1.0	±1.0	μA
		V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.5	-	±5.0	±10.0	±10.0	μA
		V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	160	160	μA
			-	3.5	-					pF
74HCT257										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
V _{OL}	LOW-level output voltage	I _O = -6 mA	3.98	4.32	-	3.84	-	3.7	-	V
		V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V				-	0.1	-	0.1	
		I _O = 20 μA	-	0	0.1	-	0.33	-	0.4	V
I _I	input leakage current	I _O = 6.0 mA	-	0.15	0.26	-	±1.0	-	±1.0	V
		V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±5.0	-	±10	μA

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I _{oZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _{CC} = 5.5 V; V _O = V _{CC} or GND per input pin; other inputs at V _{CC} or GND; I _O = 0 A	-	-	±0.5	-	80	-	160	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0					μA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A								
		per input pin; nI0, nI1 inputs	-	40	144	-	180	-	196	μA
		per input pin; $\overline{\text{OE}}$ input	-	135	486	-	608	-	662	μA
		per input pin; S input	-	70	252	-	315	-	343	μA
C _I	input capacitance		-	3.5	-					pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	25 °C		-40 °C to +85 °C	-40 °C to +125 °C	Unit
			Typ	Max	Max	Max	

74HC257

t _{pd}	propagation delay	nI0 to nY or nI1 to nY; see Figure 6						
		V _{CC} = 2.0 V	36	110	140	165	ns	
		V _{CC} = 4.5 V	13	22	28	33	ns	
		V _{CC} = 5.0 V; C _L = 15 pF	11	-	-	-	ns	
		V _{CC} = 6.0 V	10	19	24	28	ns	
		S to nY; see Figure 6						
		V _{CC} = 2.0 V	47	150	190	225	ns	
		V _{CC} = 4.5 V	17	30	38	45	ns	
		V _{CC} = 5.0 V; C _L = 15 pF	14	-	-	-	ns	
		V _{CC} = 6.0 V	14	26	33	38	ns	
t _{en}	enable time	$\overline{\text{OE}}$ to nY; see Figure 7						
		V _{CC} = 2.0 V	33	150	190	225	ns	
		V _{CC} = 4.5 V	12	30	38	45	ns	
		V _{CC} = 6.0 V	10	26	33	38	ns	
t _{dis}	disable time	$\overline{\text{OE}}$ to nY; see Figure 7						
		V _{CC} = 2.0 V	41	150	190	225	ns	
		V _{CC} = 4.5 V	15	30	38	45	ns	
		V _{CC} = 6.0 V	12	26	33	38	ns	

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	25 °C		-40 °C to +85 °C	-40 °C to +125 °C	Unit
			Typ	Max	Max	Max	
t _t	transition time	see Figure 6 [4]					
		V _{CC} = 2.0 V	14	60	75	90	ns
		V _{CC} = 4.5 V	5	12	15	18	ns
		V _{CC} = 6.0 V	4	10	13	15	ns
C _{PD}	power dissipation capacitance	per multiplexer; V _I = GND to V _{CC} [5]	45	-			pF
74HCT257							
t _{pd}	propagation delay	nI0 to nY or nI1 to nY; see Figure 6 [1]					
		V _{CC} = 4.5 V	16	30	38	45	ns
		V _{CC} = 5.0 V; C _L = 15 pF	13	-	-		ns
		S to nY; see Figure 6					
		V _{CC} = 4.5 V	20	35	44	53	ns
		V _{CC} = 5.0 V; C _L = 15 pF	17	-			ns
t _{en}	enable time	\overline{OE} to nY; V _{CC} = 4.5 V; see Figure 7 [2]	15	30	38	45	ns
t _{dis}	disable time	\overline{OE} to nY; V _{CC} = 4.5 V; see Figure 7 [3]	16	30	38	45	ns
t _t	transition time	V _{CC} = 4.5 V; see Figure 6 [4]	5	12	15	18	ns
C _{PD}	power dissipation capacitance	per multiplexer; V _I = GND to V _{CC} [5]	45	-			pF

[1] t_{pd} is the same as t_{PHL}, t_{PLH}.

[2] t_{en} is the same as t_{PZH}, t_{PZL}.

[3] t_{dis} is the same as t_{PHZ}, t_{PLZ}.

[4] t_t is the same as t_{THL}, t_{TLH}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

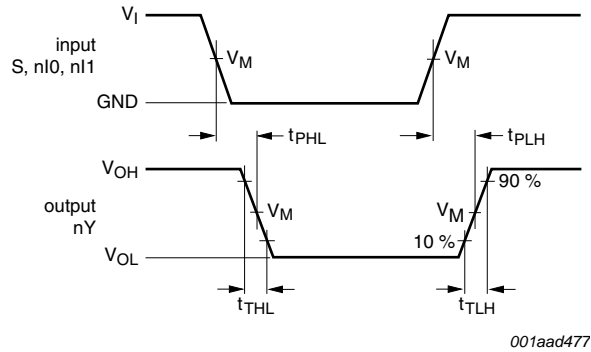
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

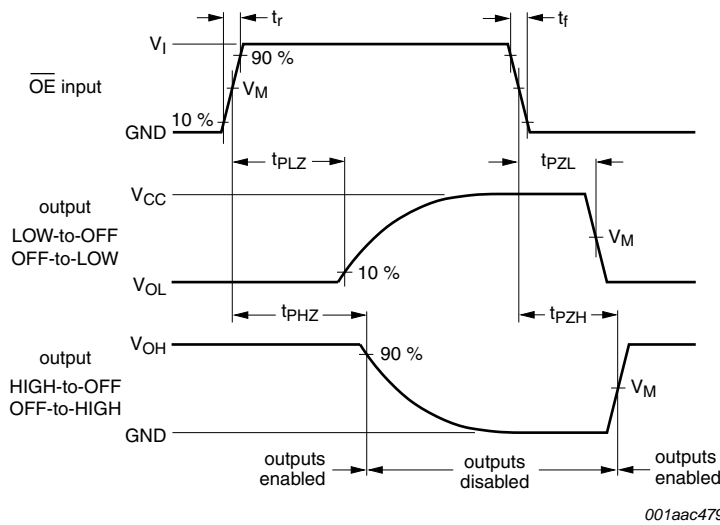
∑(C_L × V_{CC}² × f_o) = sum of outputs.

11. Waveforms



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Propagation delays input (S, nI0, nI1) to output (nY) and output (nY) transition times

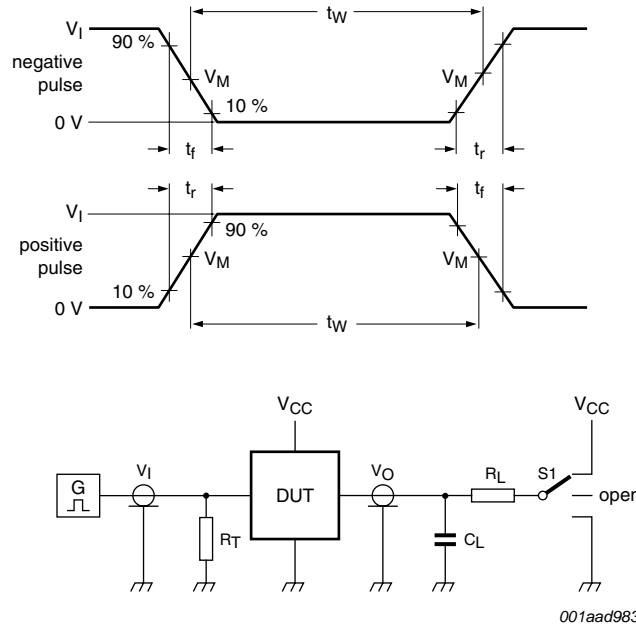


Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. 3-state output enable and disable times

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC257	$0.5V_{CC}$	$0.5V_{CC}$
74HCT257	1.3 V	1.3 V



Measurement points are given in [Table 8](#) and test data is given in [Table 9](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistor.

Fig 8. Test circuit for switching times

Table 9. Test data

Type	Input		Load		Switch position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC257	V_{CC}	6 ns	50 pF	1 k Ω	open	GND	V_{CC}
74HCT257	3 V	6 ns	50 pF	1 k Ω	open	GND	V_{CC}

12. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

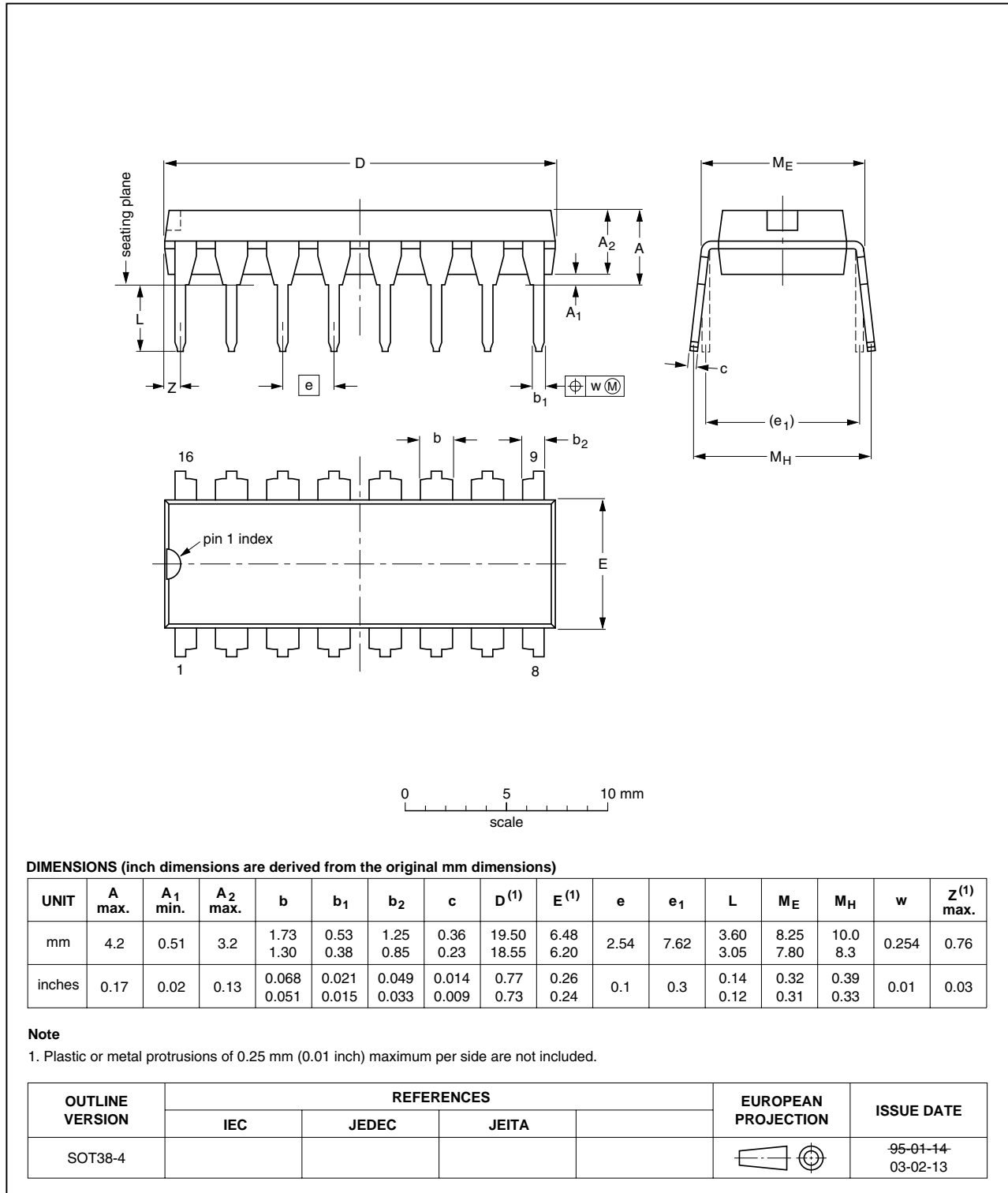


Fig 9. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

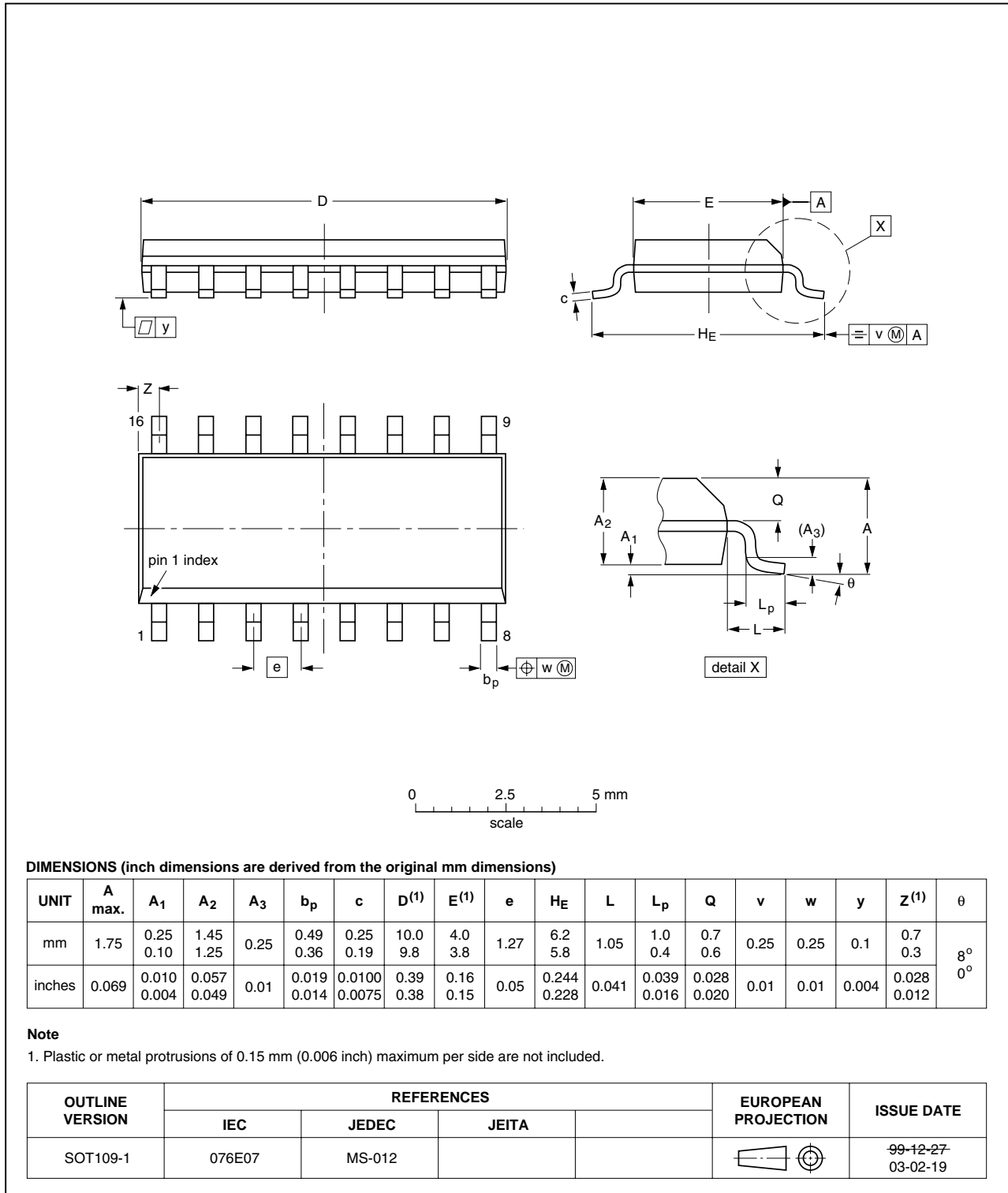


Fig 10. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

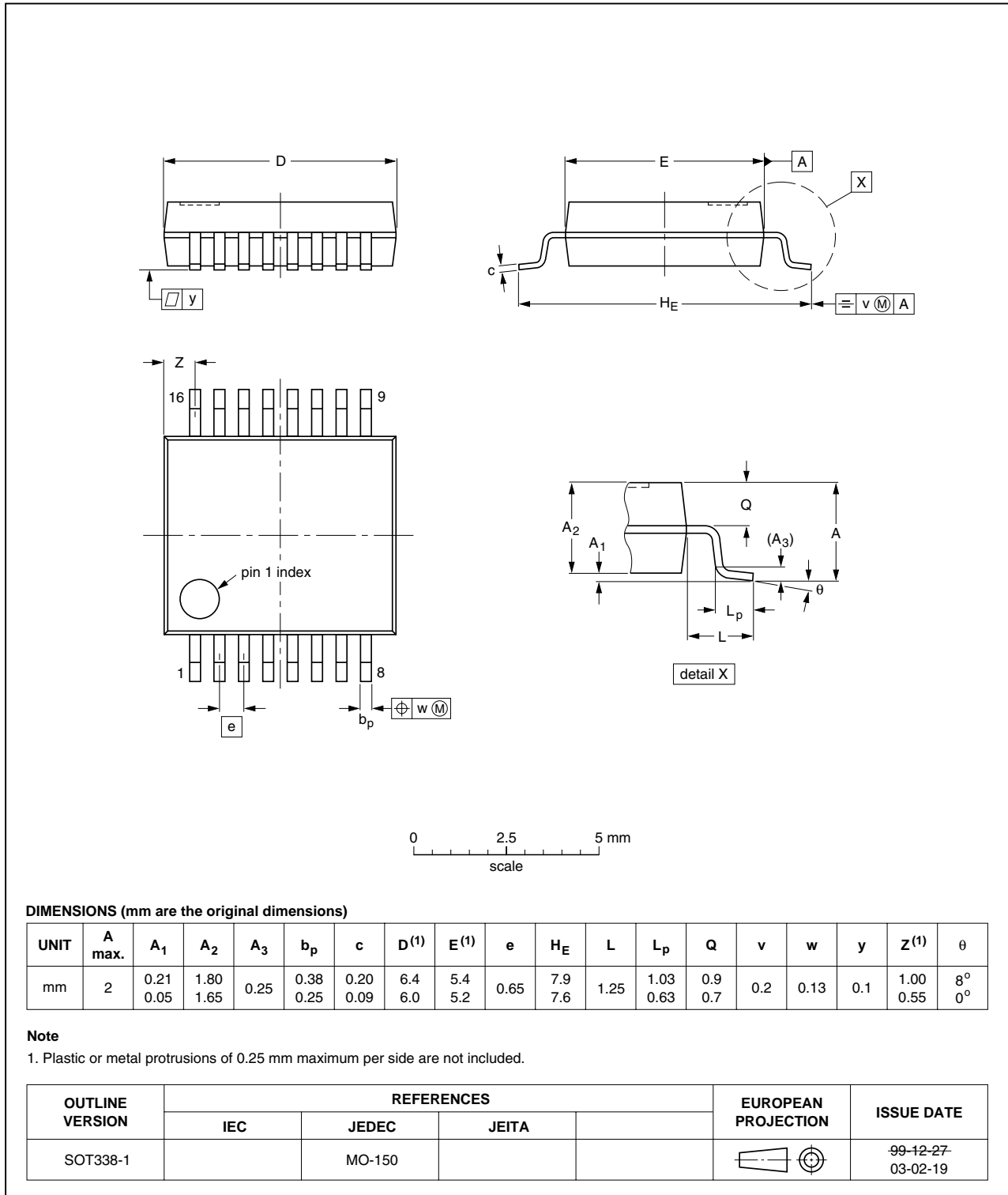


Fig 11. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

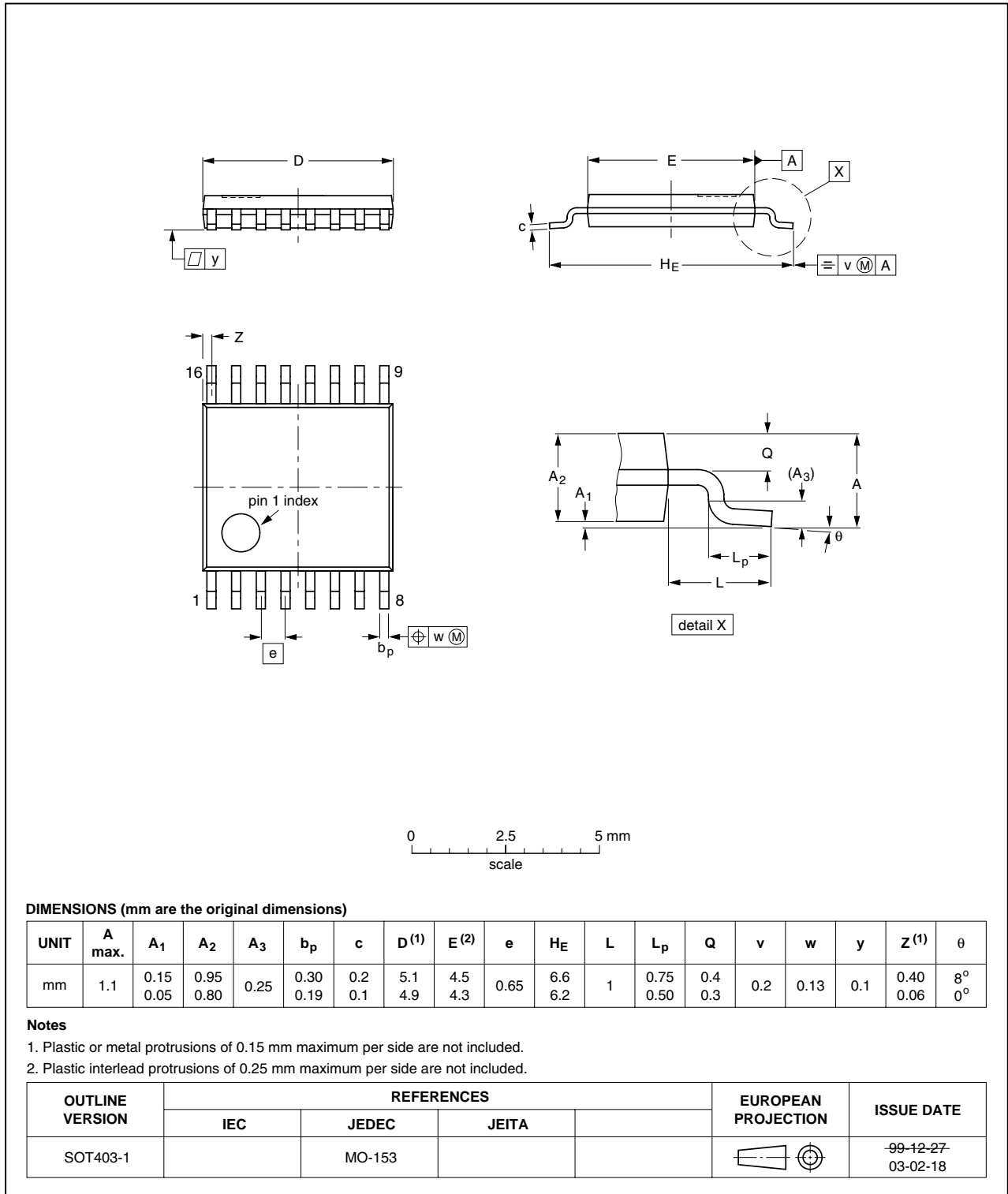


Fig 12. Package outline SOT403-1 (TSSOP16)

13. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT257_5	20100113	Product data sheet	-	74HC_HCT257_4
Modifications:	• Table 7 "Dynamic characteristics" : changed $\overline{3OE}$ to \overline{OE}			
74HC_HCT257_4	20090608	Product data sheet	-	74HC_HCT257_3
74HC_HCT257_3	20050920	Product data sheet	-	74HC_HCT257_CNV_2
74HC_HCT257_CNV_2	19980930	Product specification	-	-

14. Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

14.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

14.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental

damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

14.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

15. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

16. Contents

1	General description	1
2	Features	1
3	Ordering information	2
4	Functional diagram	2
5	Pinning information	4
5.1	Pinning	4
5.2	Pin description	4
6	Functional description	4
6.1	Function table	4
7	Limiting values	5
8	Recommended operating conditions	5
9	Static characteristics	6
10	Dynamic characteristics	7
11	Waveforms	9
12	Package outline	11
13	Revision history	15
14	Legal information	16
14.1	Data sheet status	16
14.2	Definitions	16
14.3	Disclaimers	16
14.4	Trademarks	16
15	Contact information	16
16	Contents	17

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2010.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 13 January 2010

Document identifier: 74HC_HCT257_5