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# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT75** Quad bistable transparent latch

Product specification  
File under Integrated Circuits, IC06

December 1990

## Quad bistable transparent latch

## 74HC/HCT75

## FEATURES

- Complementary Q and  $\bar{Q}$  outputs
- $V_{CC}$  and GND on the centre pins
- Output capability: standard
- $I_{CC}$  category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT75 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT75 have four bistable latches. The two latches are simultaneously controlled by one of two active HIGH enable inputs ( $LE_{1-2}$  and  $LE_{3-4}$ ). When  $LE_{n-n}$  is HIGH, the data enters the latches and appears at the nQ outputs. The nQ outputs follow the data inputs (nD) as long as  $LE_{n-n}$  is HIGH (transparent). The data on the nD inputs one set-up time prior to the HIGH-to-LOW transition of the  $LE_{n-n}$  will be stored in the latches. The latched outputs remain stable as long as the  $LE_{n-n}$  is LOW.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

| SYMBOL            | PARAMETER                                 | CONDITIONS                                   | TYPICAL |     | UNIT |
|-------------------|-------------------------------------------|----------------------------------------------|---------|-----|------|
|                   |                                           |                                              | HC      | HCT |      |
| $t_{PHL}/t_{PLH}$ | propagation delay<br>nD to nQ, $n\bar{Q}$ | $C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$ | 11      | 12  | ns   |
|                   | $LE_{n-n}$ to nQ, $n\bar{Q}$              |                                              | 11      | 11  | ns   |
| $C_I$             | input capacitance                         |                                              | 3.5     | 3.5 | pF   |
| $C_{PD}$          | power dissipation capacitance per latch   | notes 1 and 2                                | 42      | 42  | pF   |

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

## ORDERING INFORMATION

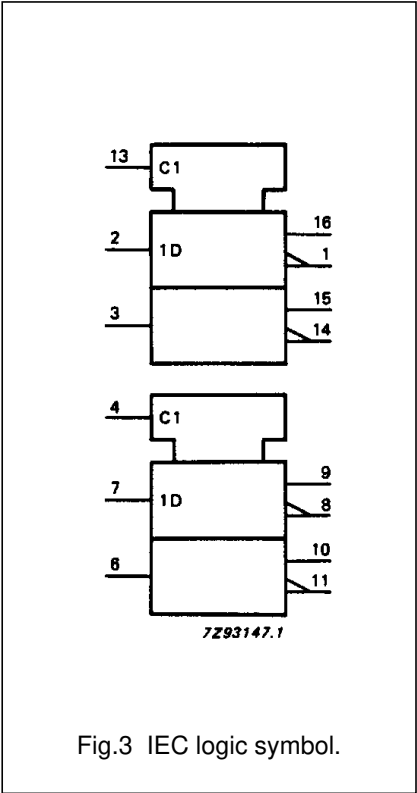
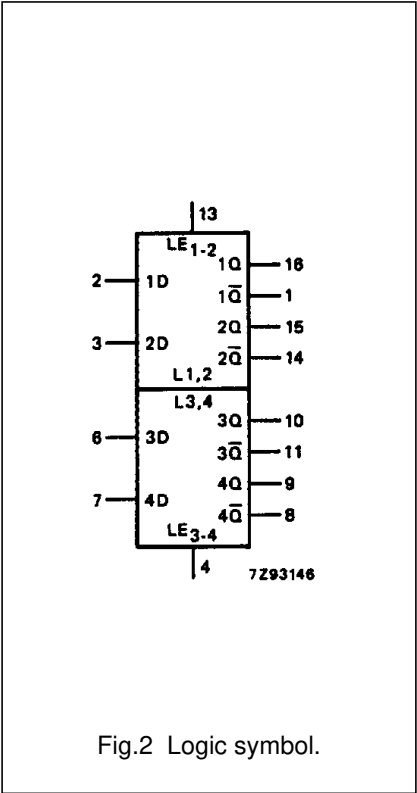
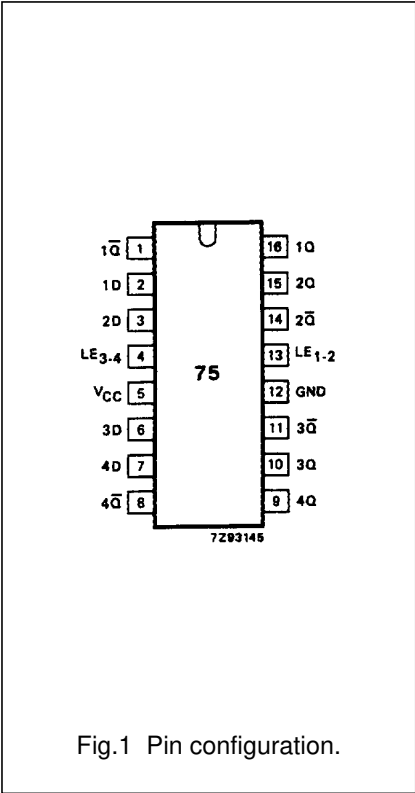
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

| PIN NO.       | SYMBOL                             | NAME AND FUNCTION                                 |
|---------------|------------------------------------|---------------------------------------------------|
| 1, 14, 11, 8  | $1\overline{Q}$ to $4\overline{Q}$ | complementary latch outputs                       |
| 2, 3, 6, 7    | 1D to 4D                           | data inputs                                       |
| 4             | $LE_{3-4}$                         | latch enable input, latches 3 and 4 (active HIGH) |
| 5             | $V_{CC}$                           | positive supply voltage                           |
| 12            | GND                                | ground (0 V)                                      |
| 13            | $LE_{1-2}$                         | latch enable input, latches 1 and 2 (active HIGH) |
| 16, 15, 10, 9 | 1Q to 4Q                           | latch outputs                                     |



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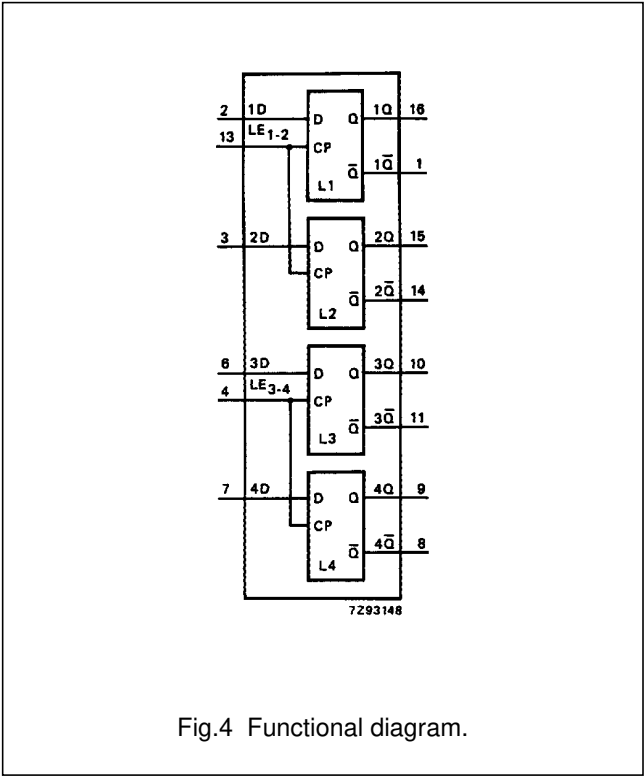
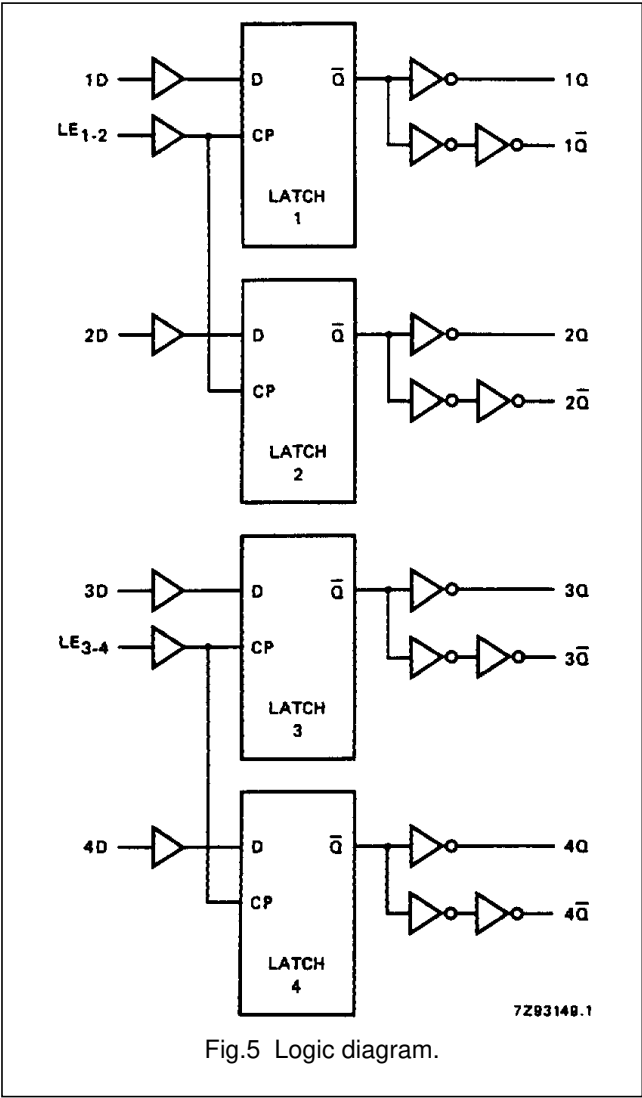
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FUNCTION TABLE

| OPERATING<br>MODES | INPUTS            |    | OUTPUTS |     |
|--------------------|-------------------|----|---------|-----|
|                    | LE <sub>n-n</sub> | nD | nQ      | nQ̄ |
| data enabled       | H                 | L  | L       | H   |
|                    | H                 | H  | H       | L   |
| data latched       | L                 | X  | q       | q̄  |

Notes

1. H = HIGH voltage level
- L = LOW voltage level
- q = lower case letters indicate the state of the  
referenced output one set-up time prior  
to the HIGH-to-LOW LE<sub>n-n</sub> transition
- X = don't care



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**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

| SYMBOL                              | PARAMETER                                     | T <sub>amb</sub> (°C) |                |                 |                 |                 |                 |                 | UNIT | TEST CONDITIONS        |              |
|-------------------------------------|-----------------------------------------------|-----------------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------|------------------------|--------------|
|                                     |                                               | 74HC                  |                |                 |                 |                 |                 |                 |      | V <sub>CC</sub><br>(V) | WAVEFORMS    |
|                                     |                                               | +25                   |                |                 | −40 to+85       |                 | −40 to+125      |                 |      |                        |              |
|                                     |                                               | min.                  | typ.           | max.            | min.            | max.            | min.            | max.            |      |                        |              |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>nD to nQ                 |                       | 33<br>12<br>10 | 110<br>22<br>19 |                 | 140<br>28<br>24 |                 | 165<br>33<br>28 | ns   | 2.0<br>4.5<br>6.0      | Fig.6        |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>nD to nQ̄                |                       | 39<br>14<br>11 | 120<br>24<br>20 |                 | 150<br>30<br>26 |                 | 180<br>36<br>31 | ns   | 2.0<br>4.5<br>6.0      | Fig.7        |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>LE <sub>n-n</sub> to nQ  |                       | 33<br>12<br>10 | 120<br>24<br>20 |                 | 150<br>30<br>26 |                 | 180<br>36<br>31 | ns   | 2.0<br>4.5<br>6.0      | Fig.8        |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>LE <sub>n-n</sub> to nQ̄ |                       | 39<br>14<br>11 | 125<br>25<br>21 |                 | 155<br>31<br>26 |                 | 190<br>38<br>32 | ns   | 2.0<br>4.5<br>6.0      | Fig.8        |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                        |                       | 19<br>7<br>6   | 75<br>15<br>13  |                 | 95<br>19<br>16  |                 | 110<br>22<br>19 | ns   | 2.0<br>4.5<br>6.0      | Figs 6 and 7 |
| t <sub>w</sub>                      | enable pulse width<br>HIGH                    | 80<br>16<br>14        | 17<br>6<br>5   |                 | 100<br>20<br>17 |                 | 120<br>24<br>20 |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.8        |
| t <sub>su</sub>                     | set-up time<br>nD to LE <sub>n-n</sub>        | 60<br>12<br>10        | 14<br>5<br>4   |                 | 75<br>15<br>13  |                 | 90<br>18<br>15  |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.9        |
| t <sub>h</sub>                      | hold time<br>nD to LE <sub>n-n</sub>          | 3<br>3<br>3           | −8<br>−3<br>−2 |                 | 3<br>3<br>3     |                 | 3<br>3<br>3     |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.9        |

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## 74HC/HCT75

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

$I_{CC}$  category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT             | UNIT LOAD COEFFICIENT |
|-------------------|-----------------------|
| nD                | 0.75                  |
| LE <sub>n-n</sub> | 1.00                  |

**AC CHARACTERISTICS FOR 74HCT**

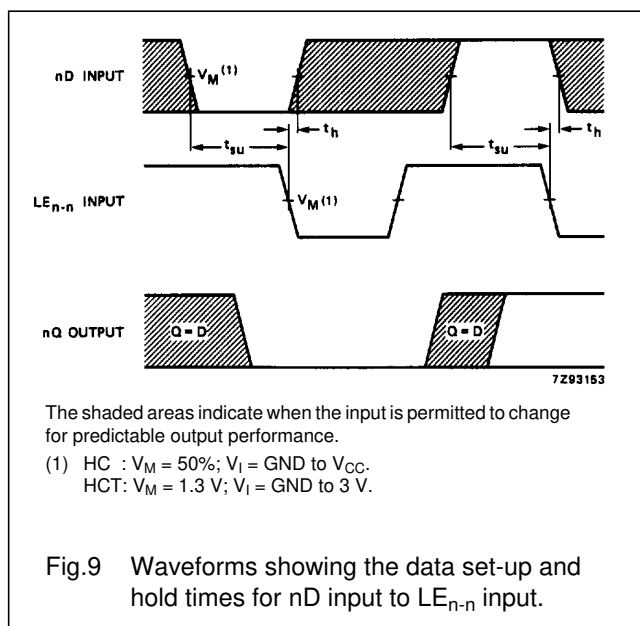
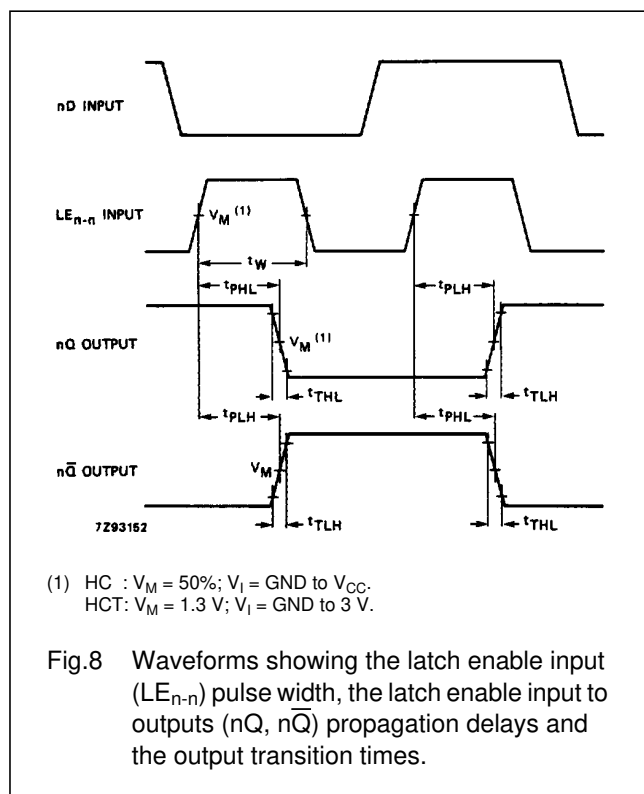
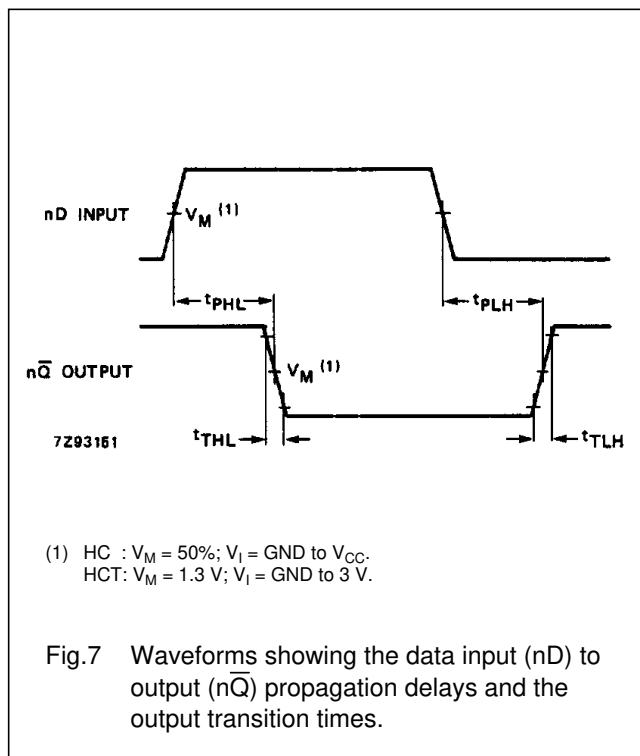
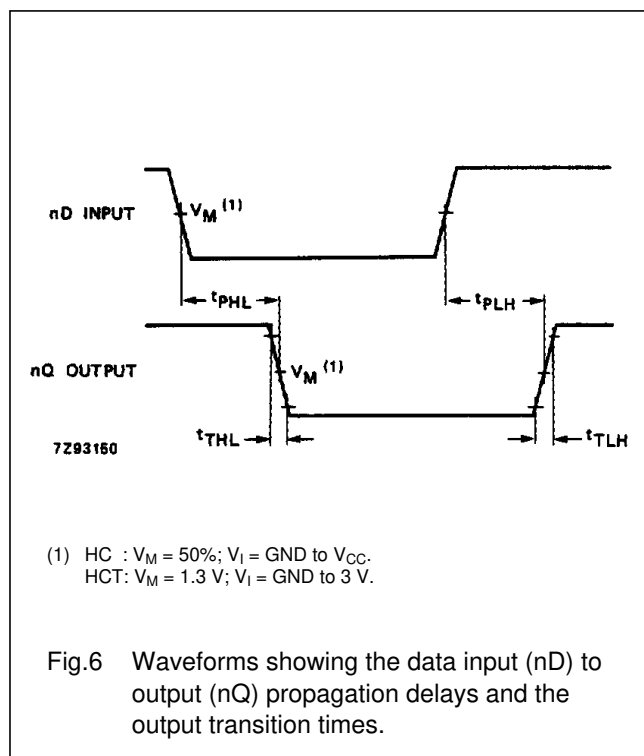
GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

| SYMBOL                              | PARAMETER                                     | T <sub>amb</sub> (°C) |      |      |            |      |             |      | UNIT | TEST CONDITIONS        |              |
|-------------------------------------|-----------------------------------------------|-----------------------|------|------|------------|------|-------------|------|------|------------------------|--------------|
|                                     |                                               | 74HCT                 |      |      |            |      |             |      |      | V <sub>CC</sub><br>(V) | WAVEFORMS    |
|                                     |                                               | +25                   |      |      | −40 to +85 |      | −40 to +125 |      |      |                        |              |
|                                     |                                               | min.                  | typ. | max. | min.       | max. | min.        | max. |      |                        |              |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>nD to nQ                 |                       | 15   | 28   |            | 35   |             | 42   | ns   | 4.5                    | Fig.6        |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>nD to nQ̄                |                       | 15   | 28   |            | 35   |             | 42   | ns   | 4.5                    | Fig.7        |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>LE <sub>n-n</sub> to nQ  |                       | 13   | 28   |            | 35   |             | 42   | ns   | 4.5                    | Fig.8        |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>LE <sub>n-n</sub> to nQ̄ |                       | 15   | 30   |            | 38   |             | 45   | ns   | 4.5                    | Fig.8        |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                        |                       | 7    | 15   |            | 19   |             | 22   | ns   | 4.5                    | Figs 6 and 7 |
| t <sub>W</sub>                      | enable pulse width<br>HIGH                    | 16                    | 4    |      | 20         |      | 24          |      | ns   | 4.5                    | Fig.8        |
| t <sub>su</sub>                     | set-up time<br>nD to LE <sub>n-n</sub>        | 12                    | 4    |      | 15         |      | 18          |      | ns   | 4.5                    | Fig.9        |
| t <sub>h</sub>                      | hold time<br>nD to LE <sub>n-n</sub>          | 3                     | −2   |      | 3          |      | 3           |      | ns   | 4.5                    | Fig.9        |

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## 74HC/HCT75

## AC WAVEFORMS



## PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".