TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS020

CD4009UB, CD4010B Types

CMOS Hex Buffers/Converters

High-Voltage Types (20-Volt Rating)

Inverting Type: CD4009UB
Non-Inverting Type: CD4010B

■ CD4009UB and CD4010B Hex Buffer/Converters may be used as CMOS to TTL or DTL logic-level converters or CMOS high-sink-current drivers.

The CD4049UB and CD4050B are preferred hex buffer replacements for the CD4009UB and CD4010B, respectively, in all applications except multiplexers. For applications not requiring high sink current or voltage conversion, the CD4069UB Hex Inverter is recommended.

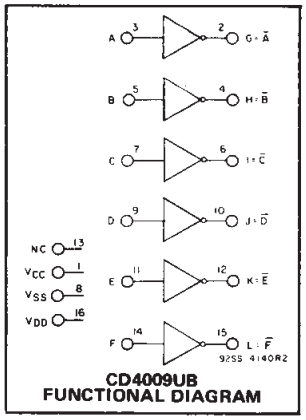
The CD4009UB and CD4010B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

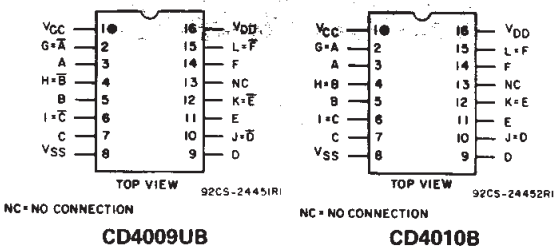
Features:

- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings

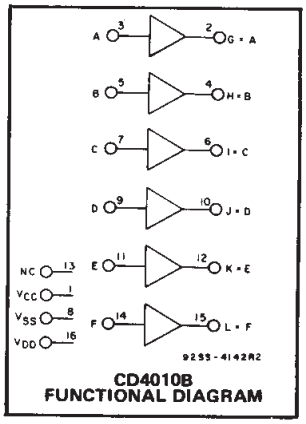
Applications:

- CMOS to DTL/TTL hex converter
- CMOS current "sink" or "source" driver
- CMOS high-to-low logic-level converter
- Multiplexer — 1 to 6 or 6 to 1





TERMINAL ASSIGNMENTS



MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

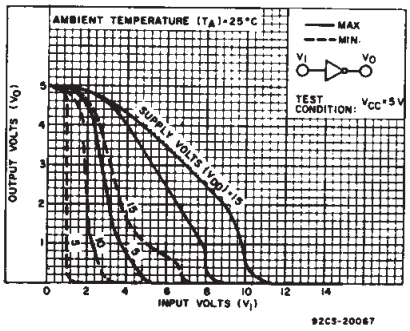


Fig. 3 — Minimum and maximum voltage transfer characteristics—CD4009UB.

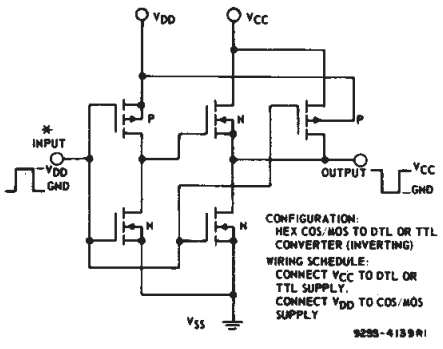


Fig. 1 — Schematic diagram of CD4009UB— 1 of 6 identical stages.

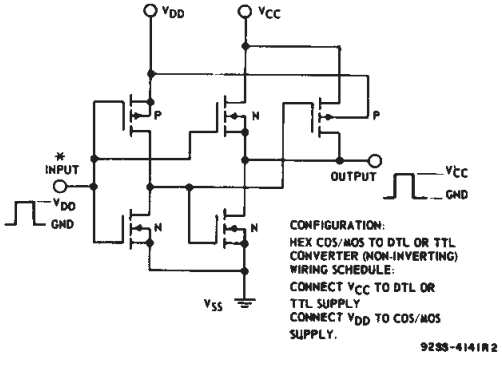
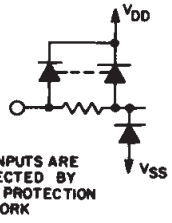


Fig. 2 — Schematic diagram of CD4010B— 1 of 6 identical stages.



RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range), V_{DD}	3	18	V
V_{CC}*	3	V_{DD}	
Input Voltage Range (V_I)	V_{CC}*	V_{DD}	V

*The CD4009UB and CD4010B have high-to-low level voltage conversion capability but not low-to-high level, therefore it is recommended that $V_{DD} \geq V_I \geq V_{CC}$.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	4.5	3.2	3.1	2.1	1.8	2.6	3.4	–	mA
	0.4	0,5	5	3.75	3.6	2.4	2.1	3	4	–	
	0.5	0,10	10	10	9.6	6.4	5.6	8	10	–	
	1.5	0,15	15	30	40	19	16	24	36	–	
Output High (Source) Current I_{OH} Min.	4.6	0,5	5	−0.25	−0.23	−0.18	−0.15	−0.2	−0.4	–	
	2.5	0,5	5	−1	−0.9	−0.65	−0.58	−0.8	−1.6	–	
	9.5	0,10	10	−0.55	−0.5	−0.38	−0.33	−0.45	−0.9	–	
	13.5	0,15	15	−1.65	−1.6	−1.25	−1.1	−1.5	−3	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05					0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage: V_{IL} Max. CD4009UB	4.5	–	5	1				–	–	1	V
	9	–	10	2				–	–	2	
	13.5	–	15	2.5				–	–	2.5	
Input Low Voltage: V_{IL} Max. CD4010B	0.5	–	5	1.5				–	–	1.5	
	1	–	10	3				–	–	3	
	1.5	–	15	4				–	–	4	
Input High Voltage: V_{IH} Min. CD4009UB	0.5	–	5	4				4	–	–	
	1	–	10	8				8	–	–	
	1.5	–	15	12.5				12.5	–	–	
Input High Voltage: V_{IH} Min. CD4010B	4.5	–	5	3.5				3.5	–	–	
	9	–	10	7				7	–	–	
	13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

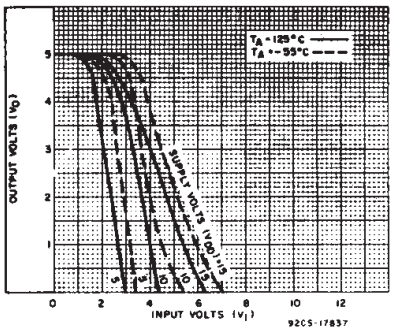


Fig. 4 – Typical voltage transfer characteristics as function of temp.–CD4009UB.

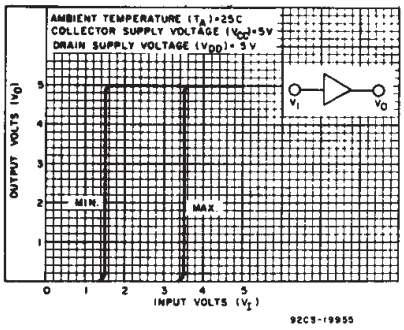


Fig. 5 – Minimum and maximum voltage transfer characteristics (V_{DD}=5)–CD4010B.

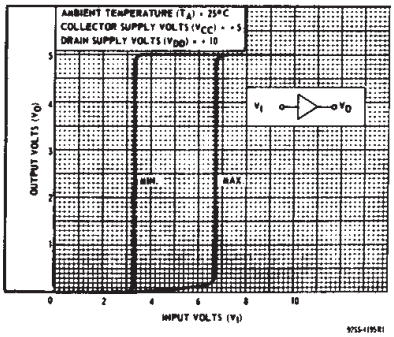


Fig. 6 – Minimum and maximum voltage transfer characteristics (V_{DD}=10)–CD4010B.

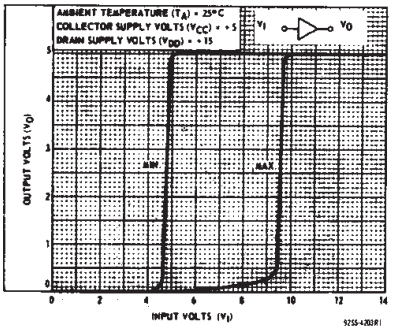


Fig. 7 – Minimum and maximum voltage transfer characteristics (V_{DD}=15)–CD4010B.

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A=25°C; Input t_r, t_f=20 ns, C_L=50 pF, R_L=200 KΩ*

CHARACTERISTIC	CONDITIONS			LIMITS ALL PKGS		UNIT
	V_{DD} (V)	V_I (V)	V_{CC} (V)	TYP.	MAX.	
Propagation Delay Time: Low-to-High, t_{PLH}	5	5	5	70	140	ns
	10	10	10	40	80	
CD4009UB	10	10	5	35	70	
	15	15	15	30	60	
	15	15	5	30	60	
	5	5	5	100	200	ns
	10	10	10	50	100	
CD4010B	10	10	5	50	100	
	15	15	15	35	70	
	15	15	5	35	70	
High-to-Low, t_{PHL}	5	5	5	30	60	ns
	10	10	10	20	40	
CD4009UB	10	10	5	15	30	
	15	15	15	15	30	
	15	15	5	10	20	
	5	5	5	65	130	ns
	10	10	10	35	70	
CD4010B	10	10	5	30	70	
	15	15	15	25	50	
	15	15	5	20	40	
Transition Time: Low-to-High, t_{TLH}	5	5	5	150	350	ns
	10	10	10	75	150	
	15	15	15	55	110	
High-to-Low, t_{THL}	5	5	5	35	70	ns
	10	10	10	20	40	
	15	15	15	15	30	
Input Capacitance, C_{IN} CD4009UB	–	–	–	15	22.5	pF
CD4010B	–	–	–	5	7.5	

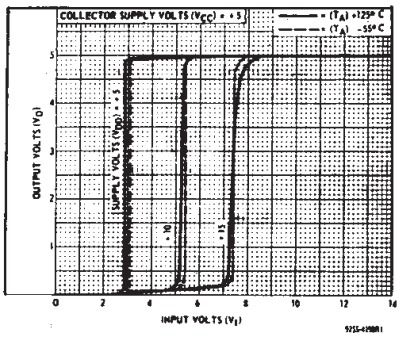


Fig. 8 – Typical voltage transfer characteristics as a function of temperature–CD4010B.

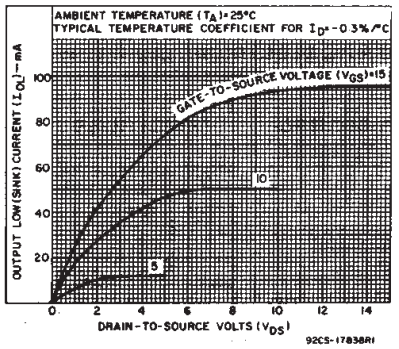


Fig. 9 – Typical output low (sink) current characteristics.

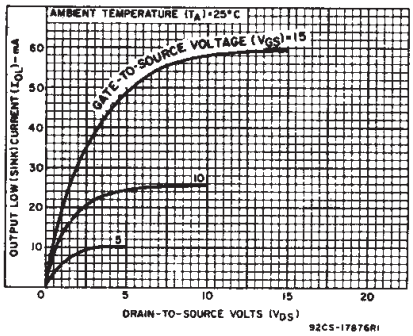


Fig. 10 – Minimum output low (sink) current characteristics.

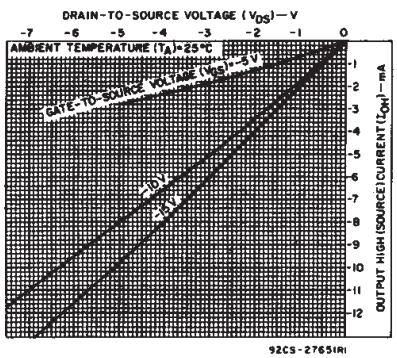


Fig. 11 – Typical output high (source) current characteristics.

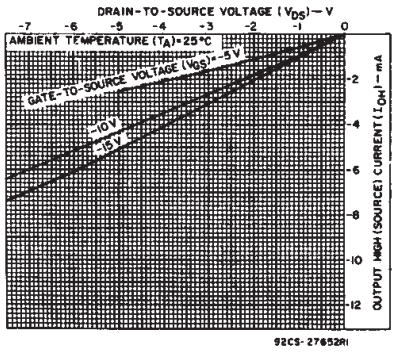


Fig. 12 – Minimum output high (source) current characteristics.

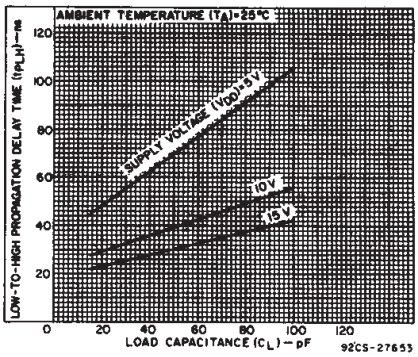


Fig. 13 – Typical low-to-high propagation delay time vs. load capacitance (CD4009UB).

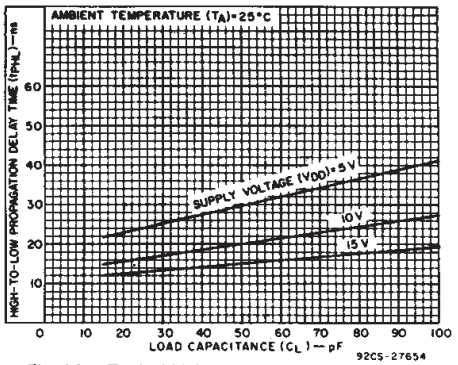


Fig. 14 — Typical high-to-low propagation delay time vs. load capacitance (CD4009UB).

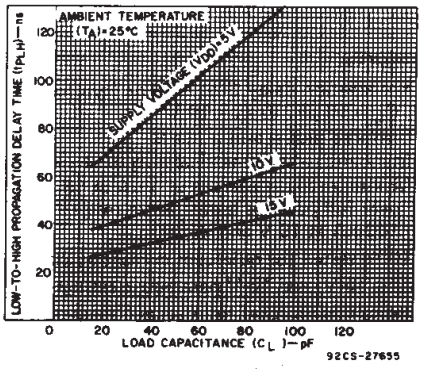


Fig. 15 — Typical low-to-high propagation delay time vs. load capacitance (CD4010B).

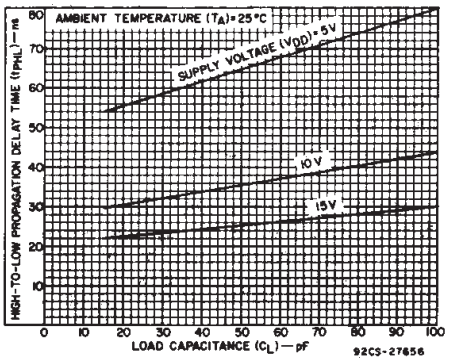


Fig. 16 — Typical high-to-low propagation delay time vs. load capacitance (CD4010B).

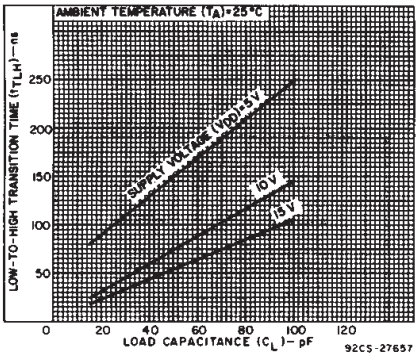


Fig. 17 — Typical low-to-high transition time vs. load capacitance.

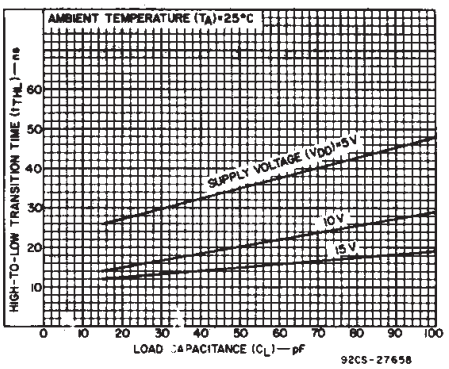


Fig. 18 — Typical high-to-low transition time vs. load capacitance.

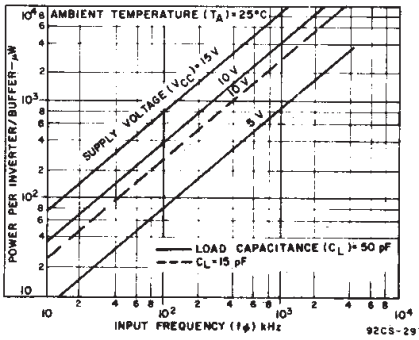


Fig. 19 — Typical dissipation characteristics.

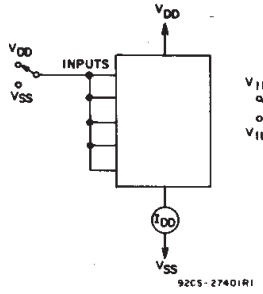


Fig. 20 — Quiescent device current test circuit.

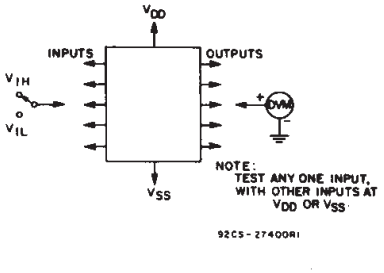
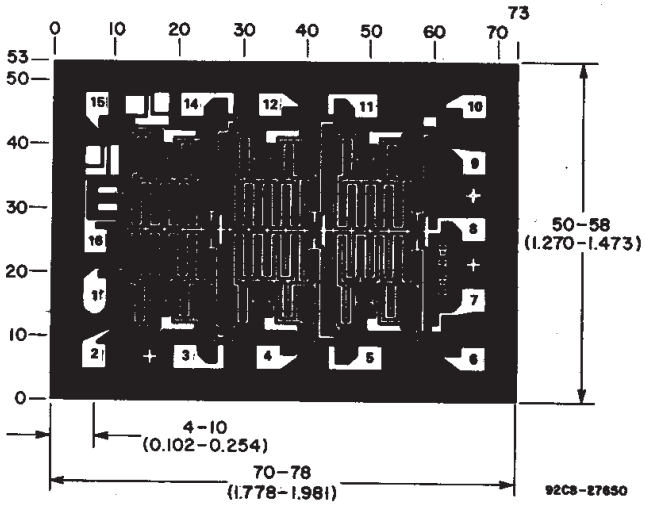


Fig. 21 — Noise immunity test circuit.



Photograph of chip for CD4009UB. Dimensions and pad layout for CD4010B are identical.

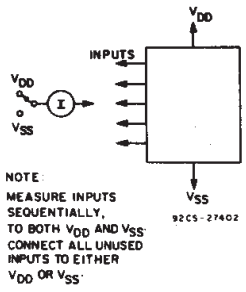


Fig. 22 — Input current test circuit.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid Graduations Are In Mils (10^{-3} Inch)

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.