National Semiconductor

November 8, 2010

LP2950/LP2951

Series of Adjustable Micropower Voltage Regulators

General Description

The LP2950 and LP2951 are micropower voltage regulators with very low quiescent current (75 6A typ.) and very low dropout voltage (typ. 40mV at light loads and 380mV at 100mA). They are ideally suited for use in battery-powered systems. Furthermore, the quiescent current of the LP2950/LP2951 increases only slightly in dropout, prolonging battery life.

The LP2950-5.0 is available in the surface-mount D-Pak package, and in the popular 3-pin TO-92 package for pin-compatibility with older 5V regulators. The 8-lead LP2951 is available in plastic, ceramic dual-in-line, LLP, or metal can packages and offers additional system functions.

One such feature is an error flag output which warns of a low output voltage, often due to falling batteries on the input. It may be used for a power-on reset. A second feature is the logic-compatible shutdown input which enables the regulator to be switched on and off. Also, the part may be pin-strapped for a 5V, 3V, or 3.3V output (depending on the version), or programmed from 1.24V to 29V with an external pair of resistors.

Careful design of the LP2950/LP2951 has minimized all contributions to the error budget. This includes a tight initial tolerance (.5% typ.), extremely good load and line regulation (.05% typ.) and a very low output voltage temperature coefficient, making the part useful as a low-power voltage reference.

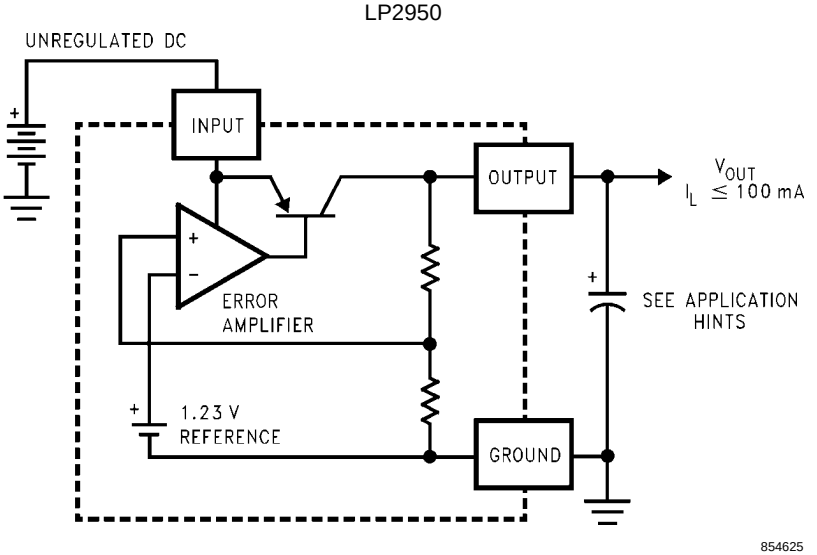
Features

- 5V, 3V, and 3.3V versions available
- High accuracy output voltage
- Guaranteed 100mA output current
- Extremely low quiescent current
- Low dropout voltage
- Extremely tight load and line regulation
- Very low temperature coefficient
- Use as Regulator or Reference
- Needs minimum capacitance for stability
- Current and Thermal Limiting
- Stable with low-ESR output capacitors (10m 5 to 6 5

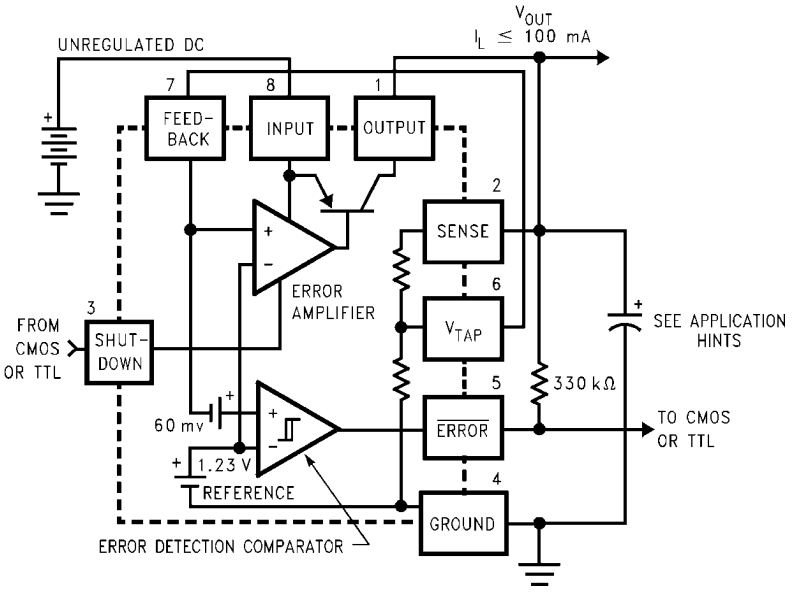
LP2951 versions only

- Error flag warns of output dropout
- Logic-controlled electronic shutdown
- Output programmable from 1.24 to 29V

Block Diagram and Typical Applications



LP2951



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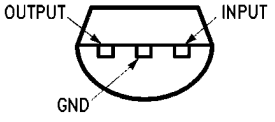
Connection Diagrams

TO-92 Plastic Package (Z)



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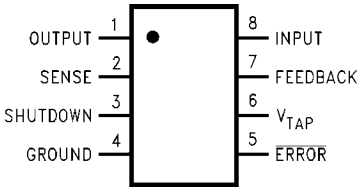
Bottom View

Dual-In-Line Packages (N, J)
Surface-Mount Package (M, MM)



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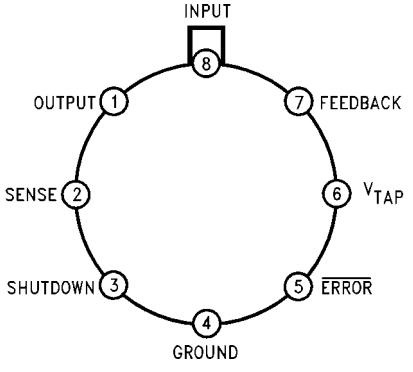
Top View

Metal Can Package (H)



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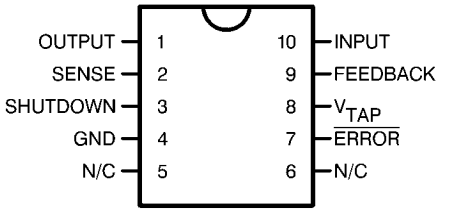
Top View

10-Lead Ceramic Surface-Mount Package (WG)



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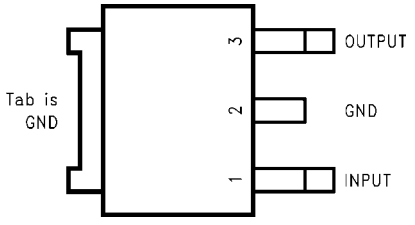
Top View

TO-252 (D-Pak)



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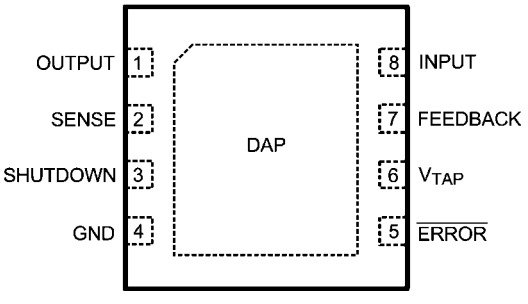
Front View

8-Lead LLP



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Connect DAP to GND at device pin 4.

Top View

Ordering Information

Package	Temperature Range	V_{OUT}	Part Number	Package Marking	Transport Media	NSC Drawing
TO-92 (Z)	40 < T_J < 125	3.0	LP2950ACZ-3.0	2950A CZ3.0	Bag	Z03A
			LP2950CZ-3.0	2950 CZ3.0	Bag	
		3.3	LP2950ACZ-3.3	2950A CZ3.3	Bag	
			LP2950CZ-3.3	2950 CZ3.3	Bag	
		5.0	LP2950ACZ-5.0	2950A CZ5.0	Bag	
			LP2950CZ-5.0	2950 CZ5.0	Bag	
TO-252 (D-Pak)	40 < T_J < 125	3.0	LP2950CDT-3.0	LP2950CDT-3.0	75 Units/Rail	TD03B
			LP2950CDTX-3.0		2.5k Units Tape and Reel	
		3.3	LP2950CDT-3.3	LP2950CDT-3.3	75 Units/Rail	
			LP2950CDTX-3.3		2.5k Units Tape and Reel	
		5.0	LP2950CDT-5.0	LP2950CDT-5.0	75 Units/Rail	
			LP2950CDTX-5.0		2.5k Units Tape and Reel	
N (N-08E)	40 < T_J < 125	3.0	LP2951ACN-3.0	LP2951ACN-3.0	40 Units/Rail	N08E
			LP2951CN-3.0	LP2951CN-3.0	40 Units/Rail	
		3.3	LP2951ACN-3.3	LP2951ACN-3.3	40 Units/Rail	
			LP2951CN-3.3	LP2951CN-3.3	40 Units/Rail	
		5.0	LP2951ACN	LP2951ACN	40 Units/Rail	
			LP2951CN	LP2951CN	40 Units/Rail	
M (M08A)	40 < T_J < 125	3.0	LP2951ACM-3.0	2951ACM30* (where * is die rev letter)	95 Units/Rail	M08A
			LP2951ACMX-3.0		2.5k Units Tape and Reel	
			LP2951CM-3.0	2951CM30* (where * is die rev letter)	95 Units/Rail	
			LP2951CMX-3.0		2.5k Units Tape and Reel	
		3.3	LP2951ACM-3.3	2951ACM33* (where * is die rev letter)	95 Units/Rail	
			LP2951ACMX-3.3		2.5k Units Tape and Reel	
			LP2951CM-3.3	2951CM33* (where * is die rev letter)	95 Units/Rail	
			LP2951CMX-3.3		2.5k Units Tape and Reel	
		5.0	LP2951ACM	2951ACM* (where * is die rev letter)	95 Units/Rail	
			LP2951ACMX		2.5k Units Tape and Reel	
			LP2951CM	2951CM* (where * is die rev letter)	95 Units/Rail	
			LP2951CMX		2.5k Units Tape and Reel	
MM (MUA08A)	40 < T_J < 125	3.0	LP2951ACMM-3.0	L0BA	1k Units Tape and Reel	MUA08A
			LP2951ACMMX-3.0		3.5k Units Tape and Reel	
			LP2951CMM-3.0	L0BB	1k Units Tape and Reel	
			LP2951CMMX-3.0		3.5k Units Tape and Reel	
		3.3	LP2951ACMM-3.3	L0CA	1k Units Tape and Reel	
			LP2951ACMMX-3.3		3.5k Units Tape and Reel	
			LP2951CMM-3.3	L0CB	1k Units Tape and Reel	
			LP2951CMMX-3.3		3.5k Units Tape and Reel	
		5.0	LP2951ACMM	L0DA	1k Units Tape and Reel	
			LP2951ACMMX		3.5k Units Tape and Reel	
			LP2951CMM	L0DB	1k Units Tape and Reel	
			LP2951CMMX		3.5k Units Tape and Reel	
J (J08A)	55 < T_J < 150	5.0	LP2951J/883	See MIL/AERO Datasheet	40 Units/Rail	J08A
H (H08C)	55 < T_J < 150	5.0	LP2951H/883	See MIL/AERO Datasheet	Tray	H08C
WG (WG10A)	55 < T_J < 150	5.0	LP2951WG/883	See MIL/AERO Datasheet	Tray	WG10A

Package	Temperature Range	V_{OUT}	Part Number	Package Marking	Transport Media	NSC Drawing
8-lead LLP	$40 < T_J < 125$	3.0	LP2951ACSD-3.0	51AC30	1k Units Tape and Reel	SDC08A
			LP2951ACSDX-3.0		4.5k Units Tape and Reel	
			LP2951CSD-3.0	51AC30B	1k Units Tape and Reel	
			LP2951CSDX-3.0		4.5k Units Tape and Reel	
		3.3	LP2951ACSD-3.3	51AC33	1k Units Tape and Reel	
			LP2951ACSDX-3.3		4.5k Units Tape and Reel	
			LP2951CSD-3.3	51AC33B	1k Units Tape and Reel	
			LP2951CSDX-3.3		4.5k Units Tape and Reel	
		5.0	LP2951ACSD	2951AC	1k Units Tape and Reel	
			LP2951ACSDX		4.5k Units Tape and Reel	
			LP2951CSD	2951ACB	1k Units Tape and Reel	
			LP2951CSDX		4.5k Units Tape and Reel	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Input Supply Voltage	0.3 to +30V
SHUTDOWN Input Voltage, Error Comparator Output Voltage, (Note 9)	
FEEDBACK Input Voltage ˜ (Note 9, Note 10)	1.5 to +30V
Power Dissipation	Internally Limited
Junction Temperature (T_J)	+150 C
Ambient Storage Temperature	65 to +150 C
Soldering Dwell Time, Temperature	
Wave	4 seconds, 260 C
Infrared	10 seconds, 240 C
Vapor Phase	75 seconds, 219 C
ESD Rating	
Human Body Model(Note 18)	2500V

Operating Ratings (Note 1)

Maximum Input Supply Voltage	30V
Junction Temperature Range (T_J) (Note 8)	
LP2951	55 to +150 C
LP2950AC-XX, LP2950C-XX, LP2951AC-XX, LP2951C-XX	40 to +125 C

Electrical Characteristics (Note 2)

Parameter	Conditions (Note 2)	LP2951		LP2950AC-XX LP2951AC-XX			LP2950C-XX LP2951C-XX			Units
		Typ	Tested Limit (Note 3) (Note 16)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	
3V Versions (Note 17)										
Output Voltage	T_J = 25 C	3.0	3.015 2.985	3.0	3.015 2.985		3.0	3.030 2.970		V max V min
	25 C 7T_J 785 C	3.0		3.0		3.030 2.970	3.0		3.045 2.955	V max V min
	Full Operating Temperature Range	3.0	3.036 2.964	3.0		3.036 2.964	3.0		3.060 2.940	V max V min
Output Voltage	éA 7I_L 7100mA T_J 7T_{JMAX}	3.0	3.045 2.955	3.0		3.042 2.958	3.0		3.072 2.928	V max V min
3.3V Versions (Note 17)										
Output Voltage	T_J = 25 C	3.3	3.317 3.284	3.3	3.317 3.284		3.3	3.333 3.267		V max V min
	25 C 7T_J 785 C	3.3		3.3		3.333 3.267	3.3		3.350 3.251	V max V min
	Full Operating Temperature Range	3.3	3.340 3.260	3.3		3.340 3.260	3.3		3.366 3.234	V max V min
Output Voltage	éA 7I_L 7100mA T_J 7T_{JMAX}	3.3	3.350 3.251	3.3		3.346 3.254	3.3		3.379 3.221	V max V min
5V Versions (Note 17)										
Output Voltage	T_J = 25 C	5.0	5.025 4.975	5.0	5.025 4.975		5.0	5.05 4.95		V max V min
	25 C 7T_J 785 C	5.0		5.0		5.05 4.95	5.0		5.075 4.925	V max V min
	Full Operating Temperature Range	5.0	5.06 4.94	5.0		5.06 4.94	5.0		5.1 4.9	V max V min
Output Voltage	éA 7I_L 7100mA T_J 7T_{JMAX}	5.0	5.075 4.925	5.0		5.075 4.925	5.0		5.12 4.88	V max V min

Parameter	Conditions (Note 2)	LP2951		LP2950AC-XX LP2951AC-XX			LP2950C-XX LP2951C-XX			Units
		Typ	Tested Limit (Note 3) (Note 16)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	
All Voltage Options										
Output Voltage Temperature Coefficient	(Note 12)	20	120	20		100	50		150	ppm/ C
Line Regulation (Note 14)	(V_ONOM + 1)V 7V_{in} 730V (Note 15)	0.03	0.1 0.5	0.03	0.1	 0.2	0.04	0.2	 0.4	% max % max
Load Regulation (Note 14)	éA 7I_L 7100mA	0.04	0.1 0.3	0.04	0.1	 0.2	0.1	0.2	 0.3	% max % max
Dropout Voltage (Note 5)	I_L Æ	 50	80 150	 50	80	 150	 50	80	 150	mV max mV max
	I_L = 100mA	 380	450 600	 380	450	 600	 380	450	 600	mV max mV max
Ground Current	I_L Æ	75	120 140	75	120	 140	75	120	 140	éA max éA max
	I_L = 100mA	8	12 14	8	12	 14	8	12	 14	mA max mA max
Dropout Ground Current	V_{in} = (V_ONOM 0.5) V I_L Æ	110	170 200	110	170	 200	110	170	 200	éA max éA max
Current Limit	V_{out} = 0	160	200 220	160	200	 220	160	200	 220	mA max mA max
Thermal Regulation	(Note 13)	0.05	0.2	0.05	0.2		0.05	0.2		%/W max
Output Noise, 10 Hz to 100 kHz	C_L Fé (5V Only)	430		430			430			é/ rms
	C_L Fé	160		160			160			é/ rms
	C_L Fé (Bypass = 0.01 éF Pins 7 to 1 (LP2951)	100		100			100			é/ rms
8-pin Versions Only		LP2951		LP2951AC-XX			LP2951C-XX			
Reference Voltage		1.235 1.26 1.22 1.2	1.25 	1.235 	1.25 1.22 	 1.26 1.2	1.235 	1.26 1.21 	 1.27 1.2	V max V max V min V min
Reference Voltage	(Note 7)		1.27 1.19			1.27 1.19			1.285 1.185	V max V min
Feedback Pin Bias Current		20	40 60	20	40	 60	20	40	 60	nA max nA max
Reference Voltage Temperature Coefficient	(Note 12)	20		20			50			ppm/ C
Feedback Pin Bias Current Temperature Coefficient		0.1		0.1			0.1			nA/ C

Parameter	Conditions (Note 2)	LP2951		LP2950AC-XX LP2951AC-XX			LP2950C-XX LP2951C-XX			Units
		Typ	Tested Limit (Note 3) (Note 16)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	
Error Comparator										
Output Leakage Current	V_{OH} = 30V	0.01	1 2	0.01	1	 2	0.01	1	 2	µA max µA max
Output Low Voltage	V_{in} = (V_ONOM 0.5) V I_{OL} µA	150	250 400	150	250	 400	150	250	 400	mV max mV max
Upper Threshold Voltage	(Note 6)	60	40 25	60	40	 25	60	40	 25	mV min mV min
Lower Threshold Voltage	(Note 6)	75	95 140	75	95	 140	75	95	 140	mV max mV max
Hysteresis	(Note 6)	15		15			15			mV
Shutdown Input										
Input Logic Voltage	 Low (Regulator ON) High (Regulator OFF)	1.3	 0.6 2.0	1.3		 0.7 2.0	1.3		 0.7 2.0	V V max V min
Shutdown Pin Input Current	$V_{shutdown}$ = 2.4V	30	50 100	30	50	 100	30	50	 100	µA max µA max
	$V_{shutdown}$ = 30V	450	600 750	450	600	 750	450	600	 750	µA max µA max
Regulator Output Current in Shutdown	(Note 11)	3	10 20	3	10	 20	3	10	 20	µA max µA max

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: Unless otherwise specified all limits guaranteed for V_{IN} = (V_{ONOM} + 1)V, I_L µA and C_L F for 5V versions and 2.2 µF for 3V and 3.3V versions. Limits appearing in boldface type apply over the entire junction temperature range for operation. Limits appearing in normal type apply for T_A = T_J = 25 C. Additional conditions for the 8-pin versions are FEEDBACK tied to V_{TAP}, OUTPUT tied to SENSE, and $V_{SHUTDOWN}$ 0.8V.

Note 3: Guaranteed and 100% production tested.

Note 4: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing AQL levels.

Note 5: Dropout Voltage is defined as the input to output differential at which the output voltage drops 100 mV below its nominal value measured at 1V differential. At very low values of programmed output voltage, the minimum input supply voltage of 2V (2.3V over temperature) must be taken into account.

Note 6: Comparator thresholds are expressed in terms of a voltage differential at the Feedback terminal below the nominal reference voltage measured at V_{in} = (V_ONOM + 1)V. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = V_{out}/V_{ref} = (R1 + R2)/R2.For example, at a programmed output voltage of 5V, the Error output is guaranteed to go low when the output drops by 95mV 5V/1.235V = 384 mV. Thresholds remain constant as a percent of V_{out} as V_{out} is varied, with the dropout warning occurring at typically 5% below nominal, 7.5% guaranteed.

Note 7: V_{ref} V_{out} (V_{in} 1V), 2.3V V_{in} 30V, 100 µA I_L 100mA, T_J T_{JMAX}.

Note 8: The junction-to-ambient thermal resistances are as follows: 180 C/W and 160 C/W for the TO-92 package with 0.40 inch and 0.25 inch leads to the printed circuit board (PCB) respectively, 105 C/W for the molded plastic DIP (N), 130 C/W for the ceramic DIP (J), 160 C/W for the molded plastic SOP (M), 200 C/W for the molded plastic MSOP (MM), and 160 C/W for the metal can package (H). The above thermal resistances for the N, J, M, and MM packages apply when the package is soldered directly to the PCB. Junction-to-case thermal resistance for the H package is 20 C/W. Junction-to-case thermal resistance for the TO-252 package is 5.4 C/W. The value of θ_{JA} for the LLP package is typically 51 C/W but is dependent on the PCB trace area, trace material, and the number of layers and thermal vias. For details of thermal resistance and power dissipation for the LLP package, refer to Application Note AN-1187.

Note 9: May exceed input supply voltage.

Note 10: When used in dual-supply systems where the output terminal sees loads returned to a negative supply, the output voltage should be diode-clamped to ground.

Note 11: $V_{shutdown}$ 2V, V_{in} 30V, V_{out} = 0, Feedback pin tied to V_{TAP}.

Note 12: Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

Note 13: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 50mA load pulse at V_{IN} = 30V (1.25W pulse) for T = 10ms.

Note 14: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

Note 15: Line regulation for the LP2951 is tested at 150 C for I_L = 1mA. For I_L µA and T_J = 125 C, line regulation is guaranteed by design to 0.2%. See Typical Performance Characteristics for line regulation versus temperature and load current.

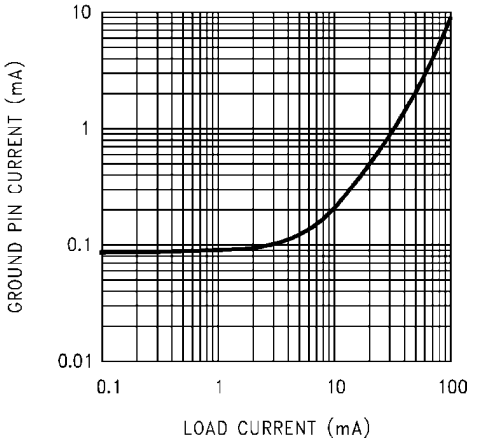
Note 16: A Military RETS specification is available on request. At time of printing, the LP2951 RETS specification complied with the boldface limits in this column. The LP2951H, WG, or J may also be procured as Standard Military Drawing Spec #5962-3870501MGA, MXA, or MPA.

Note 17: All LP2950 devices have the nominal output voltage coded as the last two digits of the part number. In the LP2951 products, the 3.0V and 3.3V versions are designated by the last two digits, but the 5V version is denoted with no code at this location of the part number (refer to ordering information table).

Note 18: Human Body Model 1.5k Öin series with 100pF.

Typical Performance Characteristics

Quiescent Current



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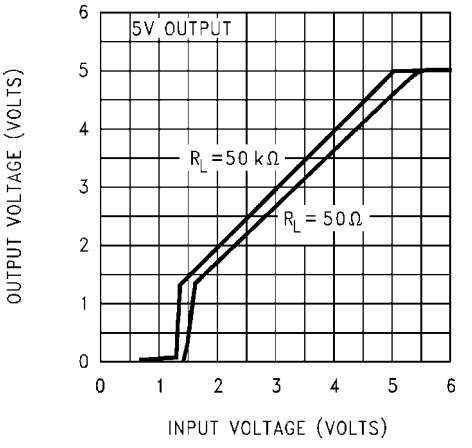
Dropout Characteristics



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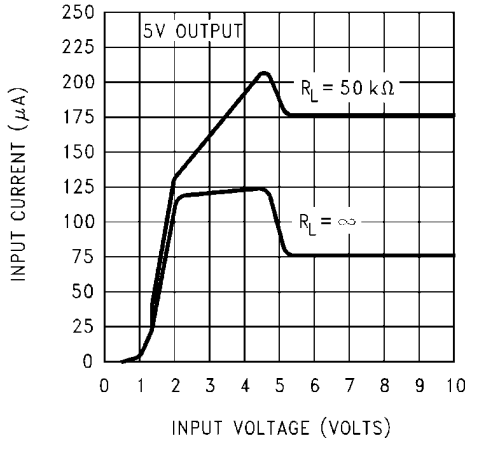
Input Current



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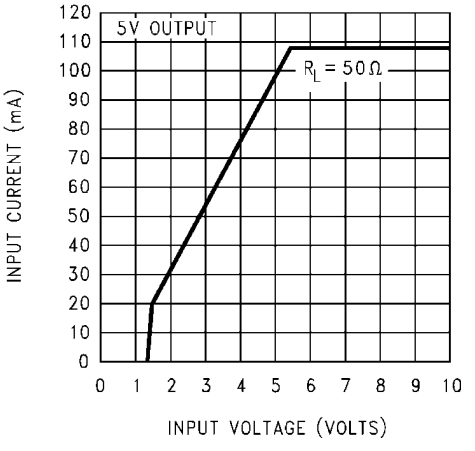
Input Current



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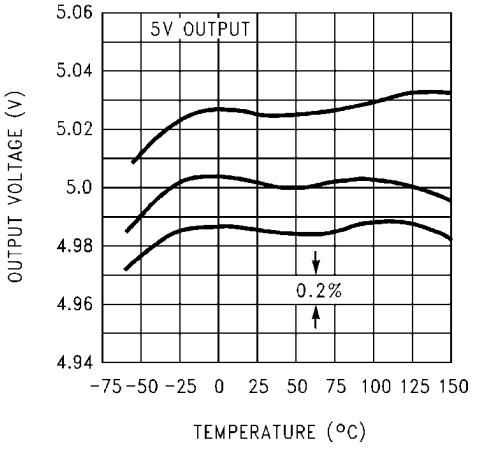
Output Voltage vs. Temperature of 3 Representative Units



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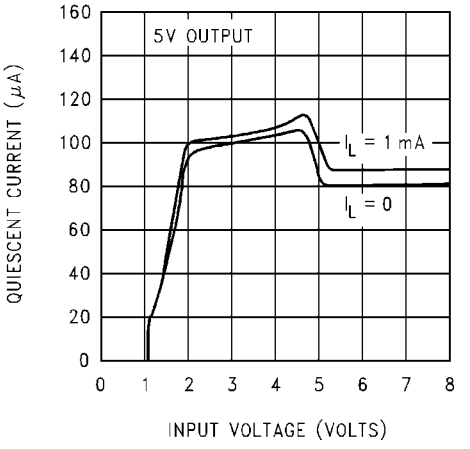
Quiescent Current



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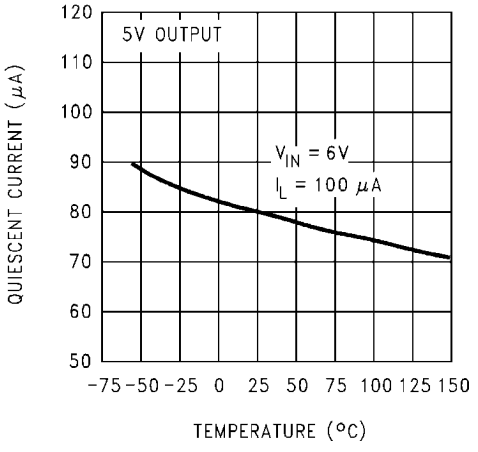
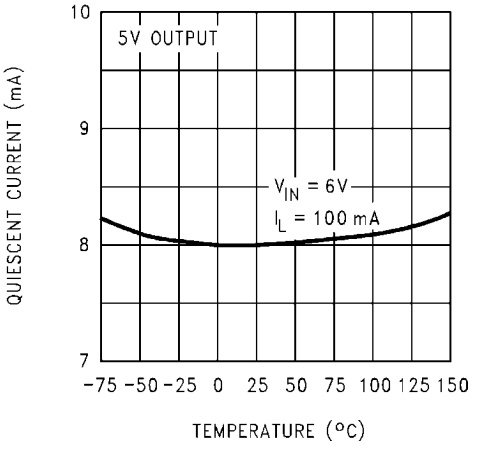
Quiescent Current



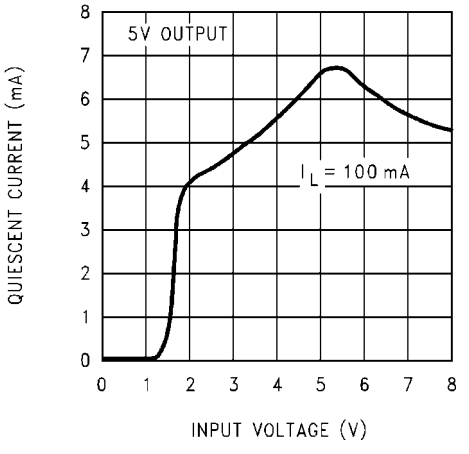
854633

Quiescent Current



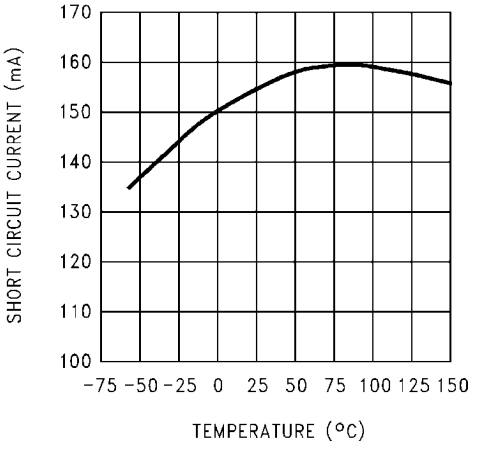
854634

Quiescent Current



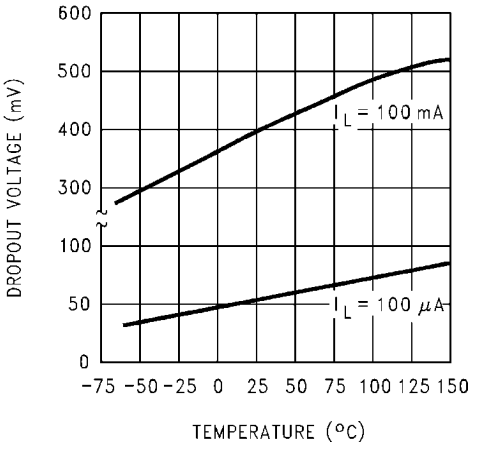
854635

Short Circuit Current



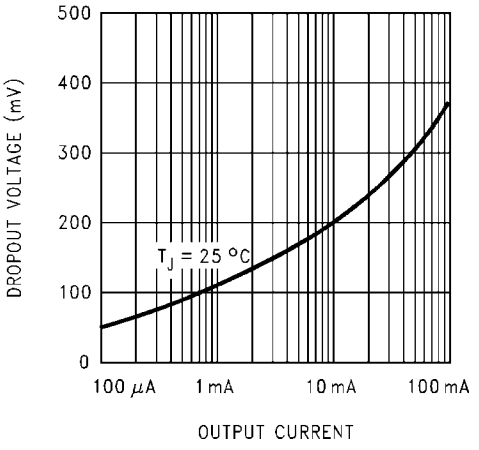
854636

Dropout Voltage



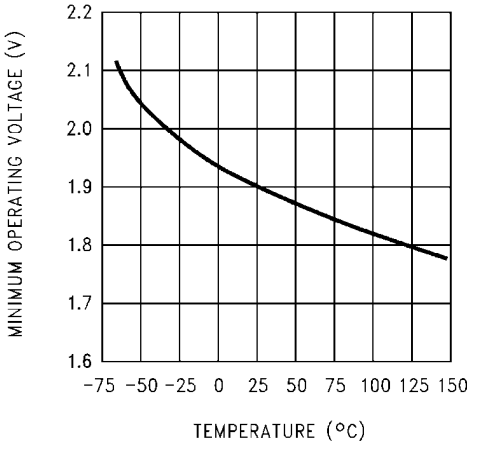
854637

Dropout Voltage



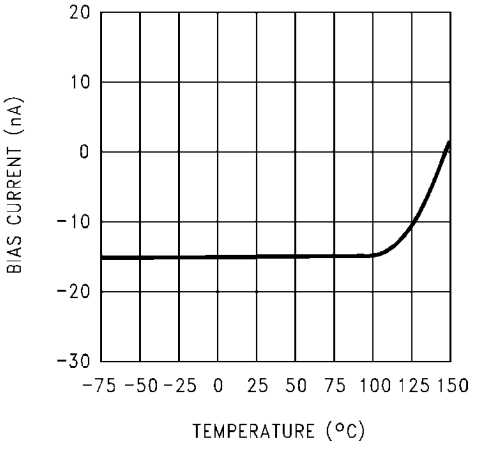
854638

LP2951 Minimum Operating Voltage



854639

LP2951 Feedback Bias Current



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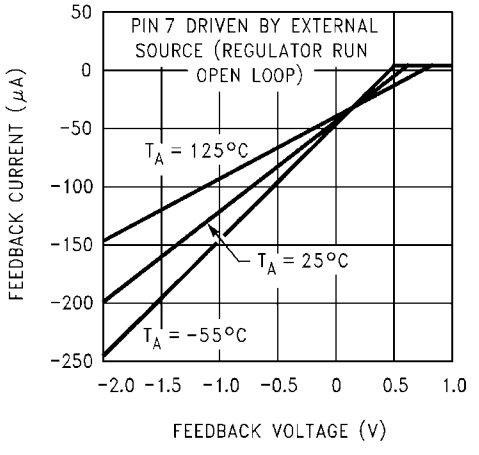
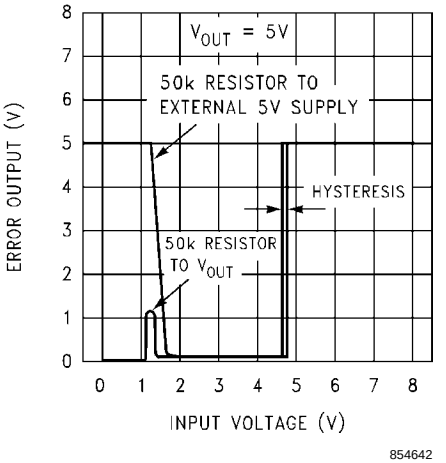
LP2951 Feedback Pin Current



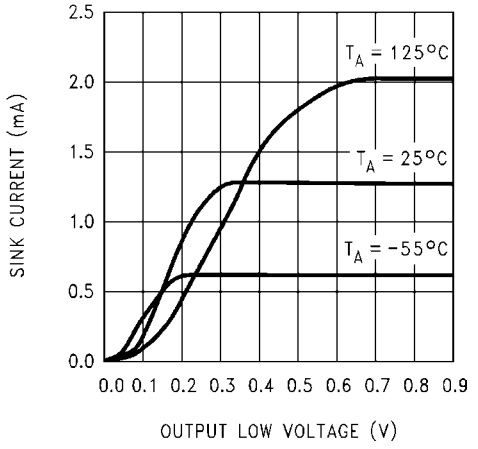
854641

LP2951 Error Comparator Output



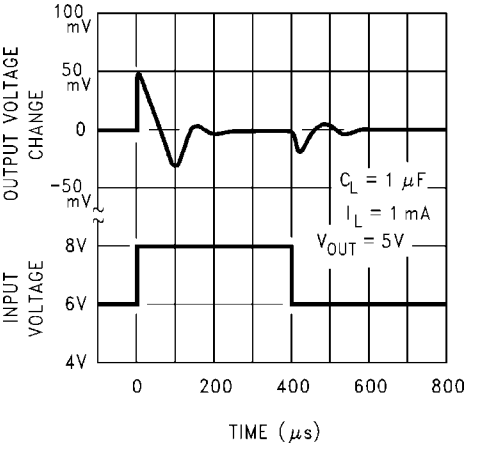
854642

LP2951 Comparator Sink Current



854643

Line Transient Response



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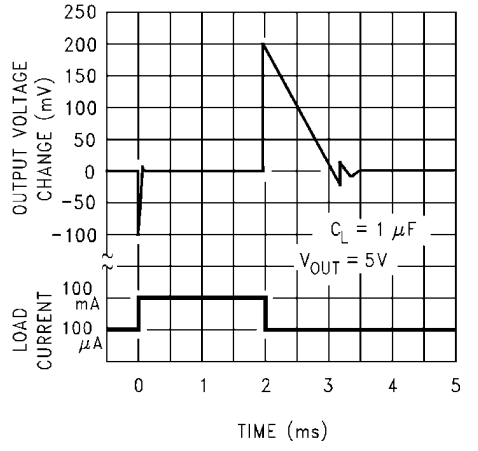
Load Transient Response



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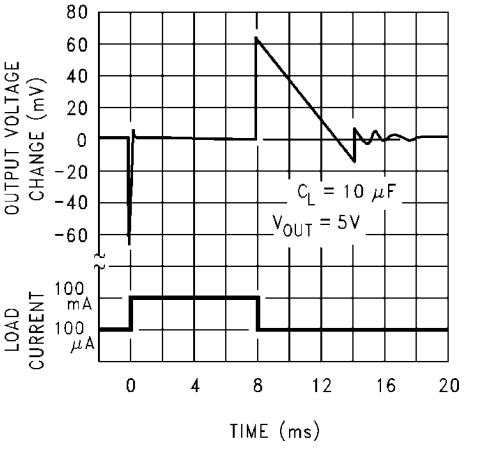
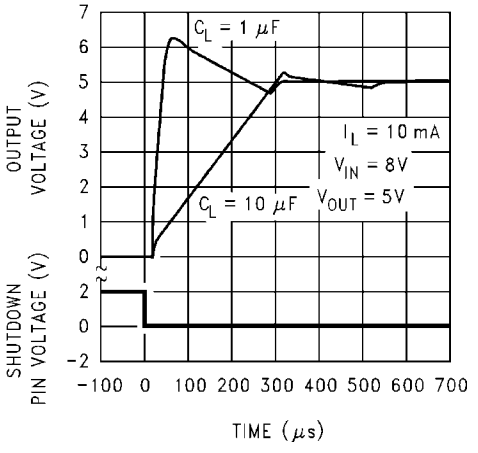
Load Transient Response



854646

LP2951 Enable Transient



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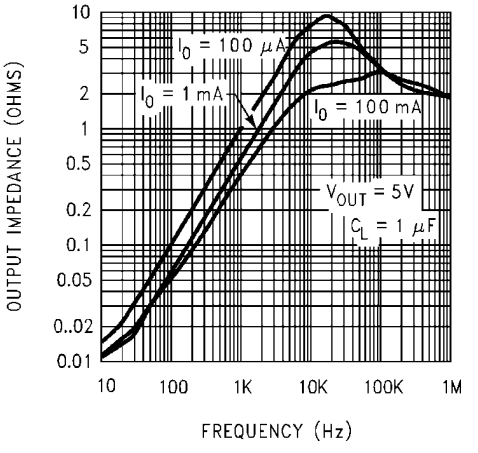
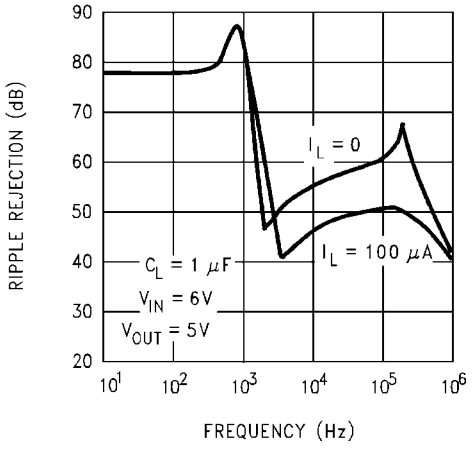
Output Impedance



854648

Ripple Rejection



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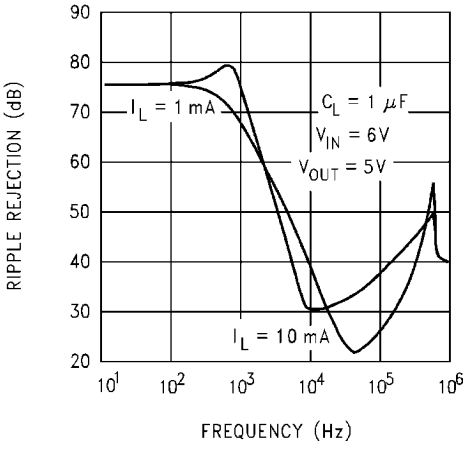
Ripple Rejection



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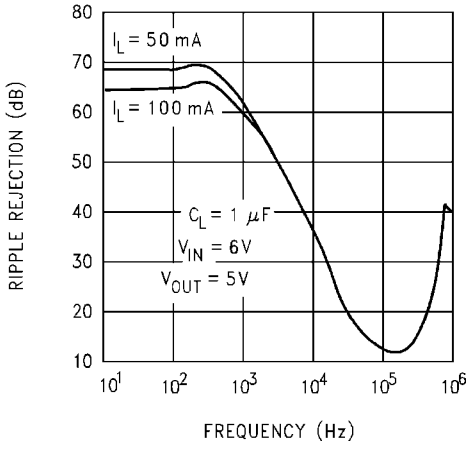
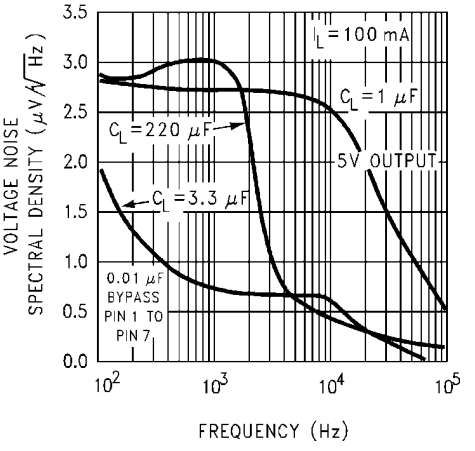
Ripple Rejection



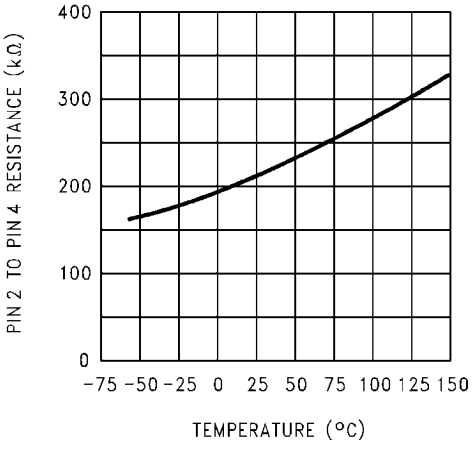
854651

LP2951 Output Noise



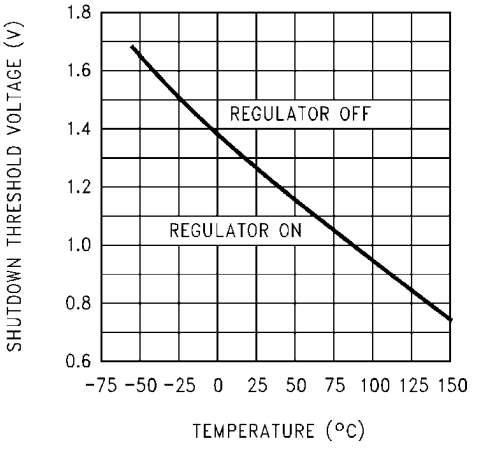
854652

LP2951 Divider Resistance



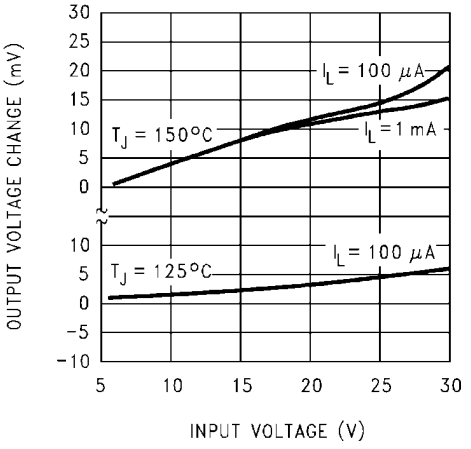
854653

Shutdown Threshold Voltage



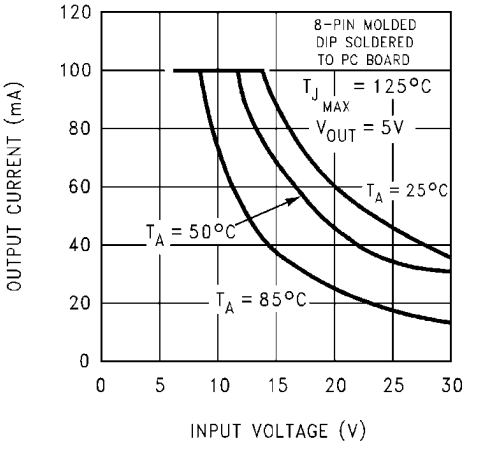
854654

Line Regulation



854655

LP2951 Maximum Rated Output Current



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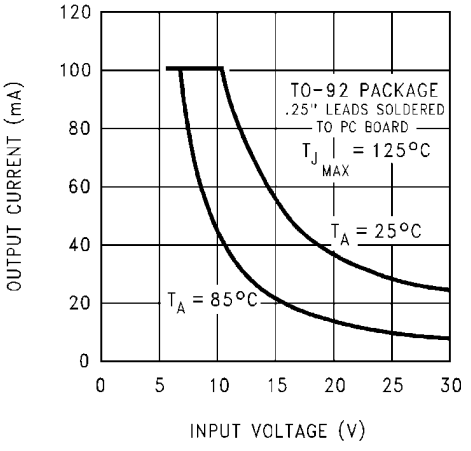
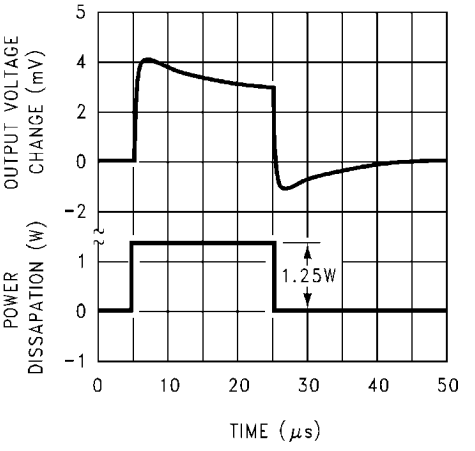
LP2950 Maximum Rated Output Current



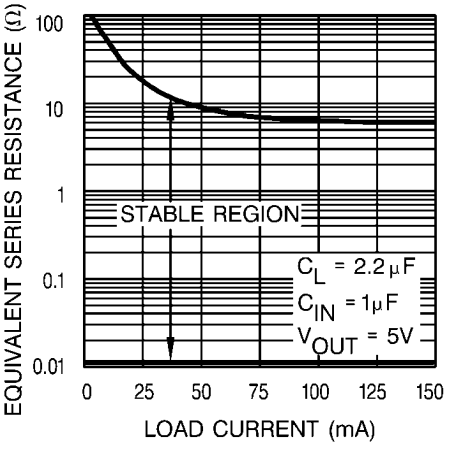
854657

Thermal Response



854658

Output Capacitor ESR Range



854663

Application Hints

EXTERNAL CAPACITORS

A 1.0 µF (or greater) capacitor is required between the output and ground for stability at output voltages of 5V or more. At lower output voltages, more capacitance is required (µF or more is recommended for 3V and 3.3V versions). Without this capacitor the part will oscillate. Most types of tantalum or aluminum electrolytics work fine here; even film types work but are not recommended for reasons of cost. Many aluminum electrolytics have electrolytes that freeze at about 30 C, so solid tantalums are recommended for operation below 25 C. The important parameters of the capacitor are an ESR of about 5 Ωor less and a resonant frequency above 500kHz. The value of this capacitor may be increased without limit.

Ceramic capacitors whose value is greater than 1000pF should not be connected directly from the LP2951 output to ground. Ceramic capacitors typically have ESR values in the range of 5 to 10m 5, a value below the lower limit for stable operation (see curve Output Capacitor ESR Range).

The reason for the lower ESR limit is that the loop compensation of the part relies on the ESR of the output capacitor to provide the zero that gives added phase lead. The ESR of ceramic capacitors is so low that this phase lead does not occur, significantly reducing phase margin. A ceramic output capacitor can be used if a series resistance is added (recommended value of resistance about 0.1 5 to 2 5

At lower values of output current, less output capacitance is required for stability. The capacitor can be reduced to µF for currents below 10mA or 0.1 µF for currents below 1mA. Using the adjustable versions at voltages below 5V runs the error amplifier at lower gains so that more output capacitance is needed. For the worst-case situation of a 100mA load at 1.23V output (Output shorted to Feedback) a µF (or greater) capacitor should be used.

Unlike many other regulators, the LP2950 will remain stable and in regulation with no load in addition to the internal voltage divider. This is especially important in CMOS RAM keep-alive applications. When setting the output voltage of the LP2951 versions with external resistors, a minimum load of 1 µA is recommended.

A 1 µF tantalum, ceramic or aluminum electrolytic capacitor should be placed from the LP2950/LP2951 input to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

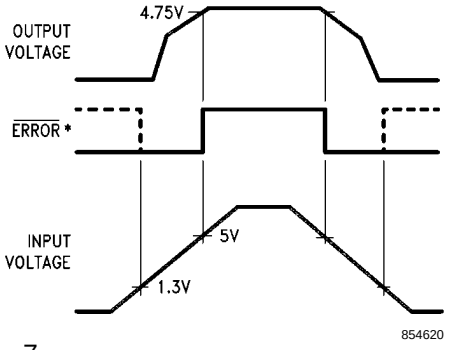
Stray capacitance to the LP2951 Feedback terminal can cause instability. This may especially be a problem when using high value external resistors to set the output voltage. Adding a 100pF capacitor between Output and Feedback and increasing the output capacitor to at least 3.3 µF will fix this problem.

ERROR DETECTION COMPARATOR OUTPUT

The comparator produces a logic low output whenever the LP2951 output falls out of regulation by more than approximately 5%. This figure is the comparator©s built-in offset of about 60mV divided by the 1.235 reference voltage. (Refer to the block diagram in the front of the datasheet.) This trip level remains ª5% below normalº regardless of the programmed output voltage of the 2951. For example, the error flag trip level is typically 4.75V for a 5V output or 11.4V for a 12V output. The out of regulation condition may be due either to low input voltage, current limiting, or thermal limiting.

Figure 1 below gives a timing diagram depicting the $\overline{\text{ERROR}}$ signal and the regulated output voltage as the LP2951 input is ramped up and down. For 5V versions, the $\overline{\text{ERROR}}$ signal becomes valid (low) at about 1.3V input. It goes high at about 5V input (the input voltage at which V_{OUT} = 4.75V). Since the LP2951©s dropout voltage is load-dependent (see curve in typical performance characteristics), the input voltage trip point (about 5V) will vary with the load current. The output voltage trip point (approx. 4.75V) does not vary with load.

The error comparator has an open-collector output which requires an external pull up resistor. This resistor may be returned to the output or some other supply voltage depending on system requirements. In determining a value for this resistor, note that while the output is rated to sink 400 µA, this sink current adds to battery drain in a low battery condition. Suggested values range from 100k to 1 M Ω The resistor is not required if this output is unused.



*When V_{IN} 7 1.3V, the error flag pin becomes a high impedance, and the error flag voltage rises to its pull-up voltage. Using V_{OUT} as the pull-up voltage (see Figure 2), rather than an external 5V source, will keep the error flag voltage under 1.2V (typ.) in this condition. The user may wish to divide down the error flag voltage using equal-value resistors (10k 5 suggested), to ensure a low-level logic signal during any fault condition, while still allowing a valid high logic level during normal operation.

FIGURE 1. $\overline{\text{ERROR}}$ Output Timing

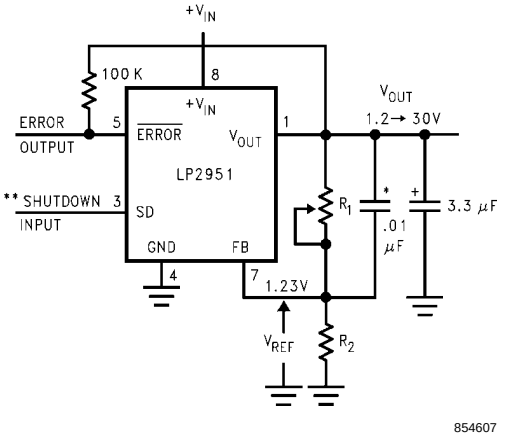
PROGRAMMING THE OUTPUT VOLTAGE (LP2951)

The LP2951 may be pin-strapped for the nominal fixed output voltage using its internal voltage divider by tying the output and sense pins together, and also tying the feedback and V_{TAP} pins together. Alternatively, it may be programmed for any output voltage between its 1.235V reference and its 30V maximum rating. As seen in Figure 2, an external pair of resistors is required.

The complete equation for the output voltage is

$$V_{OUT} = V_{REF} \bullet \left(1 + \frac{R_1}{R_2}\right) + I_{FB}R_1$$

where V_{REF} is the nominal 1.235 reference voltage and I_{FB} is the feedback pin bias current, nominally 20nA. The minimum recommended load current of 1 µA forces an upper limit of 1.2 M Ωon the value of R_2, if the regulator must work with no load (a condition often found in CMOS in standby). I_{FB} will produce a 2% typical error in V_{OUT} which may be eliminated at room temperature by trimming R_1. For better accuracy, choosing R_2 = 100k reduces this error to 0.17% while increasing the resistor program current to 12 µA. Since the LP2951 typically draws 60 µA at no load with Pin 2 open-circuited, this is a small price to pay.



*See Application Hints

$$V_{out} = V_{Ref}\left(1 + \frac{R_1}{R_2}\right)$$

**Drive with TTL-high to shut down. Ground or leave open if shutdown feature is not to be used.

Note: Pins 2 and 6 are left open.

FIGURE 2. Adjustable Regulator

REDUCING OUTPUT NOISE

In reference applications it may be advantageous to reduce the AC noise present at the output. One method is to reduce the regulator bandwidth by increasing the size of the output capacitor. This is the only way noise can be reduced on the 3 lead LP2950 but is relatively inefficient, as increasing the capacitor from 1 µF to 220 µF only decreases the noise from 430 µV to 160 µV rms for a 100kHz bandwidth at 5V output.

Noise can be reduced fourfold by a bypass capacitor across R_1, since it reduces the high frequency gain from 4 to unity. Pick

$$C_{BYPASS} \cong \frac{1}{2\pi R_1 \bullet 200\ Hz}$$

or about 0.01 µF. When doing this, the output capacitor must be increased to 3.3 µF to maintain stability. These changes reduce the output noise from 430 µV to 100 µV rms for a 100kHz bandwidth at 5V output. With the bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.

LLP MOUNTING

The SDC08A (No Pullback) 8-Lead LLP package requires specific mounting techniques which are detailed in National Semiconductor Application Note # 1187. Referring to the section PCB Design Recommendations in AN-1187 (Page 5), it should be noted that the pad style which should be used with the LLP package is the NSMD (non-solder mask defined) type. Additionally, it is recommended the PCB terminal pads to be 0.2 mm longer than the package pads to create a solder fillet to improve reliability and inspection.

The thermal dissipation of the LLP package is directly related to the printed circuit board construction and the amount of additional copper area connected to the DAP.

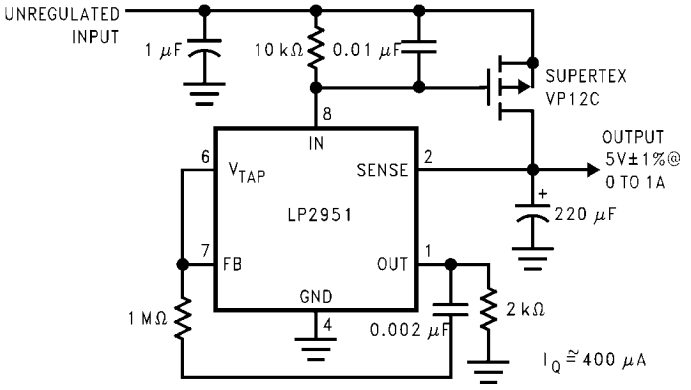
The DAP (exposed pad) on the bottom of the LLP package is connected to the die substrate with a conductive die attach adhesive. The DAP has no direct electrical (wire) connection to any of the eight pins. There is a parasitic PN junction between the die substrate and the device ground. As such, it is strongly recommend that the DAP be connected directly to the ground at device lead 4 (i.e. GND). Alternately, but not recommended, the DAP may be left floating (i.e. no electrical connection). The DAP must not be connected to any potential other than ground.

For the LP2951 in the SDC08A 8-Lead LLP package, the junction-to-case thermal rating, θ_{JC}, is 14.2 C/W, where the case is the bottom of the package at the center of the DAP. The junction-to-ambient thermal performance for the LP2951 in the SDC08A 8-Lead LLP package, using the JEDEC JESD51 standards is summarized in the following table:

Board Type	Thermal Vias	θ_{JC}	θ_{JA}
JEDEC 2-Layer JESD 51-3	None	14.2 C/W	185 C/W
JEDEC 4-Layer JESD 51-7	1	14.2 C/W	68 C/W
	2	14.2 C/W	60 C/W
	4	14.2 C/W	51 C/W
	6	14.2 C/W	48 C/W

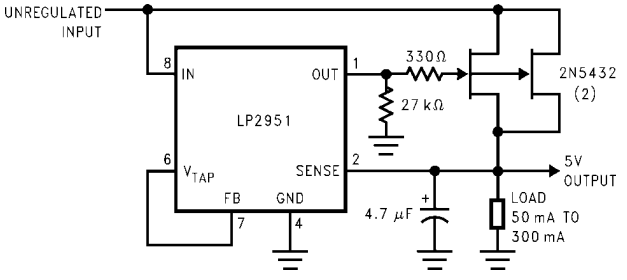
Typical Applications

1A Regulator with 1.2V Dropout



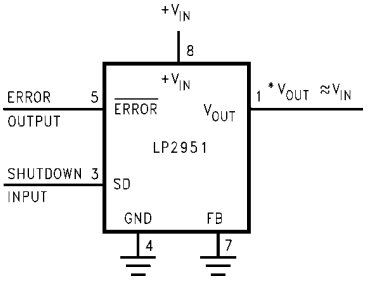
854622

300mA Regulator with 0.75V Dropout



854621

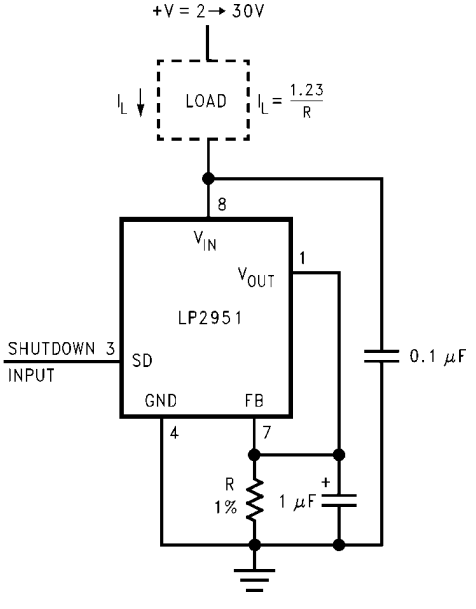
Wide Input Voltage Range Current Limiter



854609

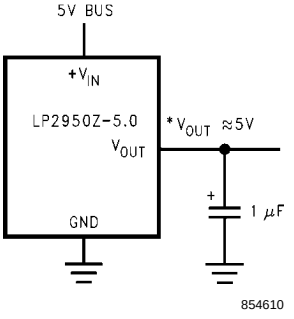
*Minimum input-output voltage ranges from 40mV to 400mV, depending on load current. Current limit is typically 160mA.

Low Drift Current Source



854608

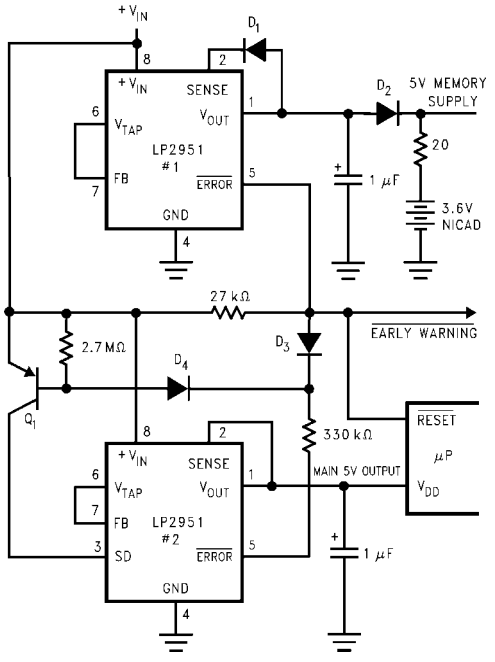
5 Volt Current Limiter



854610

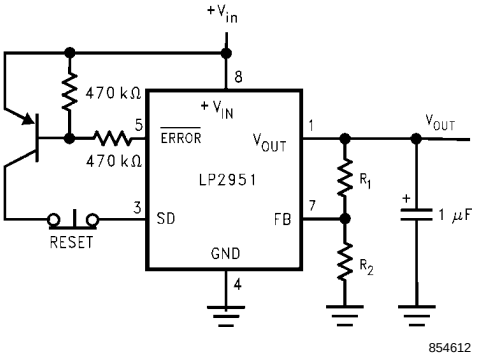
*Minimum input-output voltage ranges from 40mV to 400mV, depending on load current. Current limit is typically 160mA.

Regulator with Early Warning and Auxiliary Output

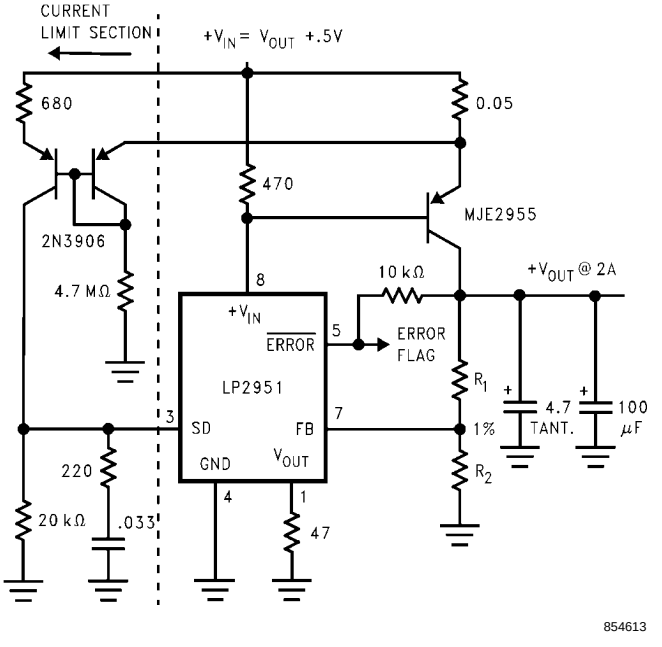


- Early warning flag on low input voltage
- Main output latches off at lower input voltages
- Battery backup on auxiliary output
- Operation: Reg. #1©s V_{out} is programmed one diode drop above 5V. Its error flag becomes active when V_{in} 7 5.7V. When V_{in} drops below 5.3V, the error flag of Reg. #2 becomes active and via Q1 latches the main output off. When V_{in} again exceeds 5.7V Reg. #1 is back in regulation and the early warning signal rises, unlatching Reg. #2 via D3.

Latch Off When Error Flag Occurs



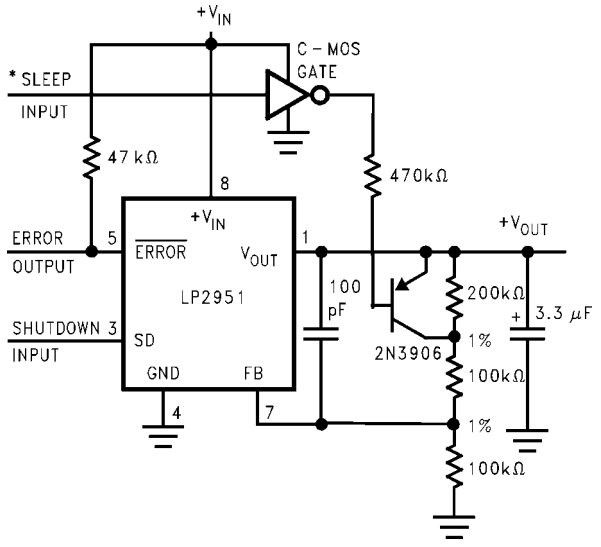
2 Ampere Low Dropout Regulator



$$V_{out} = 1.23V \left(1 + \frac{R_1}{R_2}\right)$$

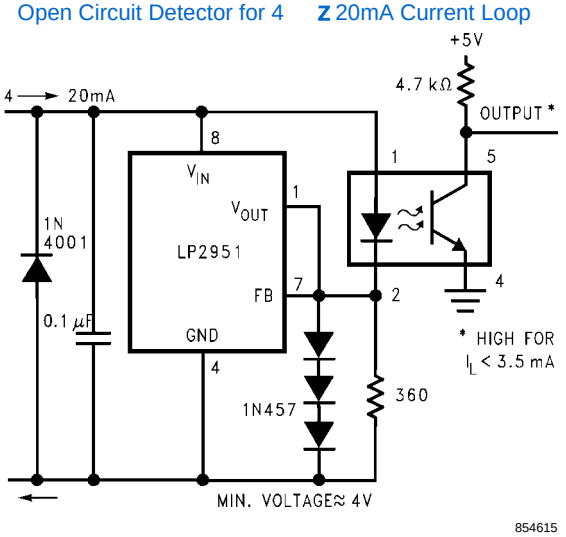
For $5V_{out}$, use internal resistors. Wire pin 6 to 7, & wire pin 2 to $+V_{out}$ Bus.

5V Regulator with 2.5V Sleep Function

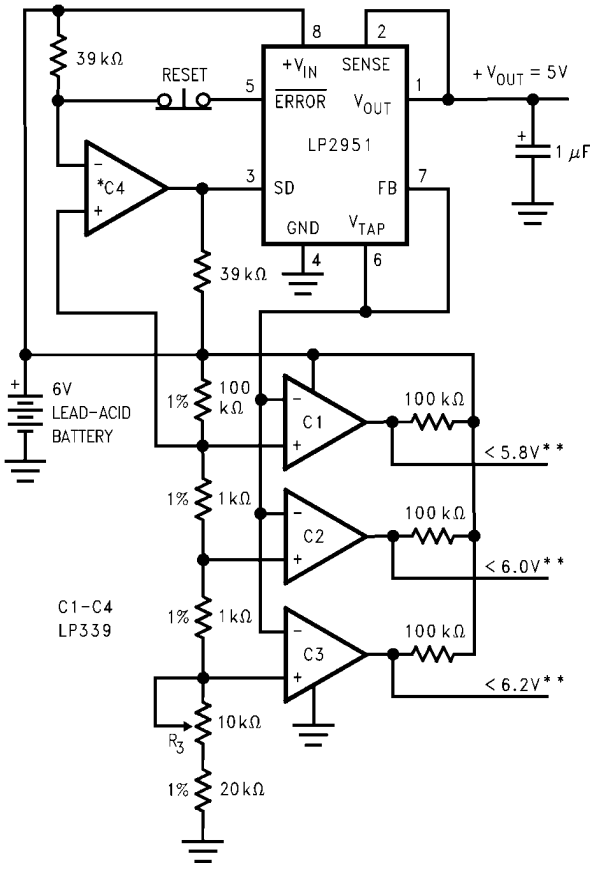


*High input lowers V_{out} to 2.5V

Open Circuit Detector for 4 ≤ 20mA Current Loop



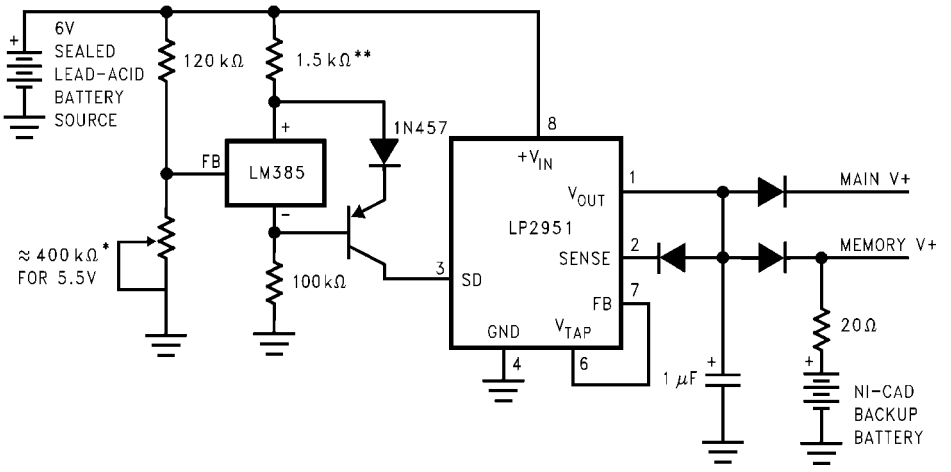
Regulator with State-of-Charge Indicator



*Optional Latch off when drop out occurs. Adjust R3 for C2 Switching when V_{in} is 6.0V.

**Outputs go low when V_{in} drops below designated thresholds.

Low Battery Disconnect



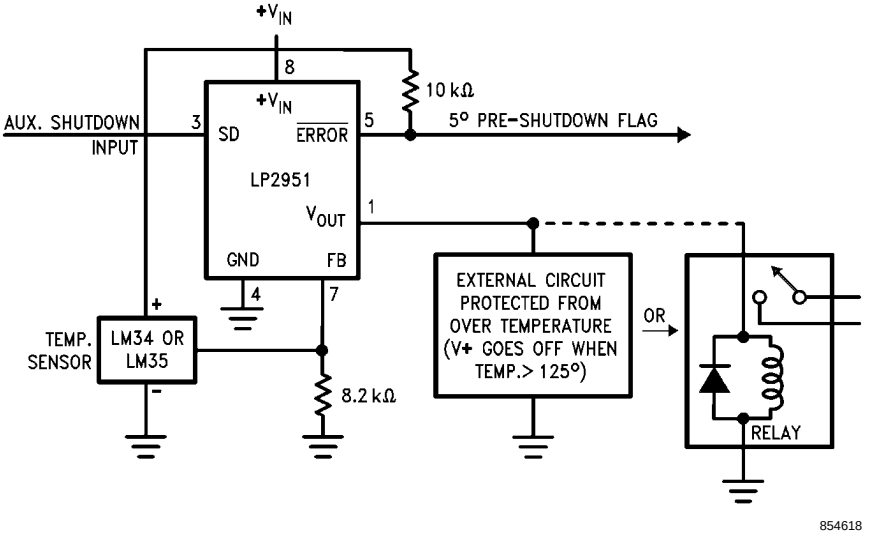
854617

For values shown, Regulator shuts down when V_{in} < 5.5V and turns on again at 6.0V. Current drain in disconnected mode is ~~A~~.

*Sets disconnect Voltage

**Sets disconnect Hysteresis

System Overtemperature Protection Circuit

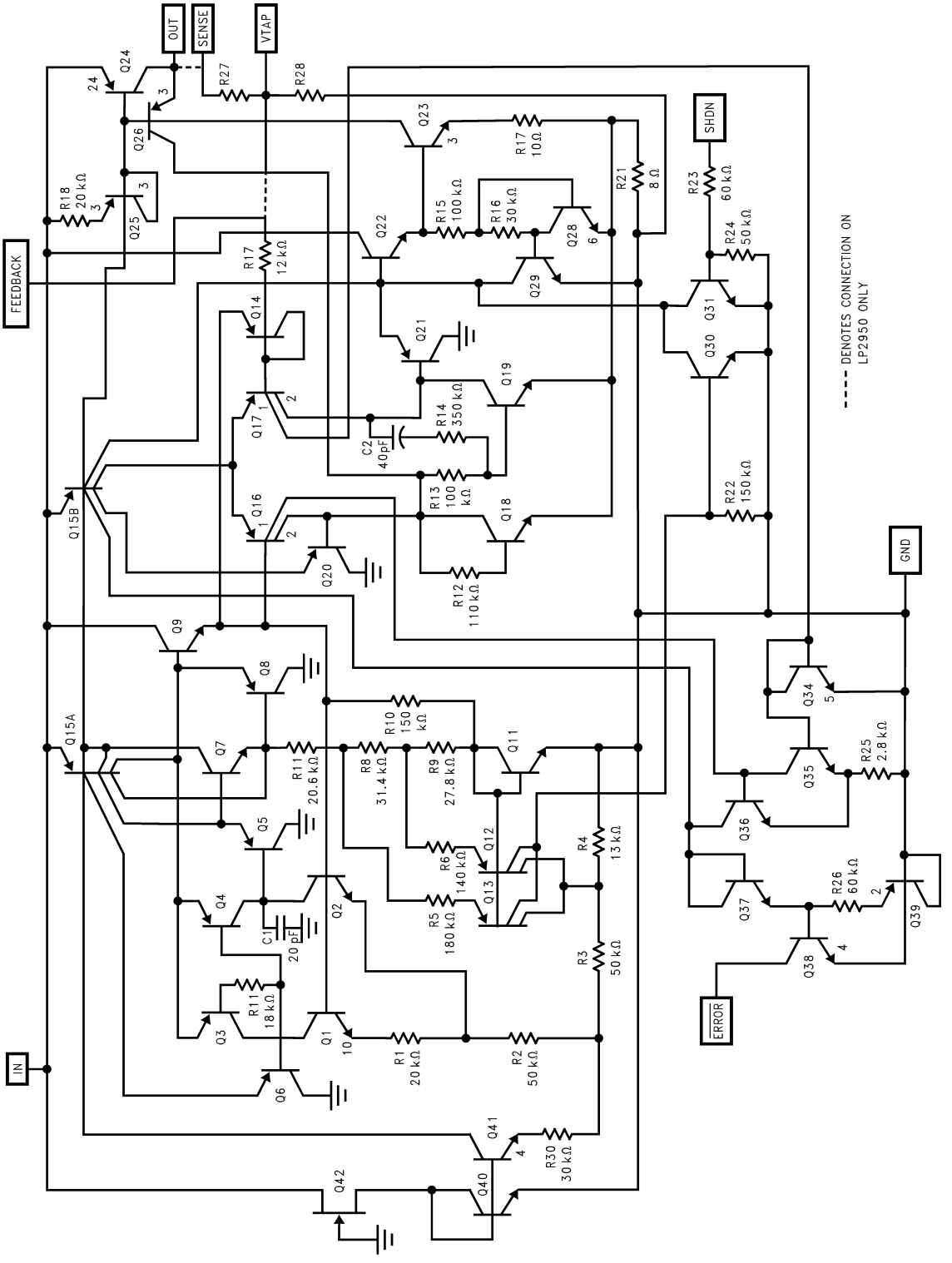


854618

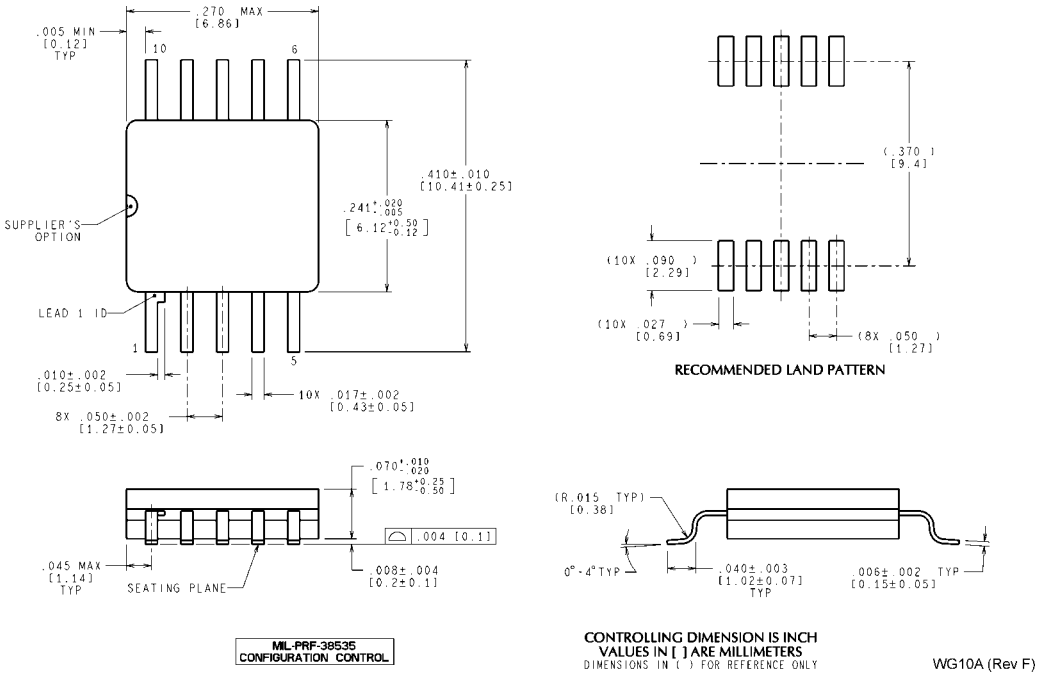
LM34 for 125 F Shutdown

LM35 for 125 C Shutdown

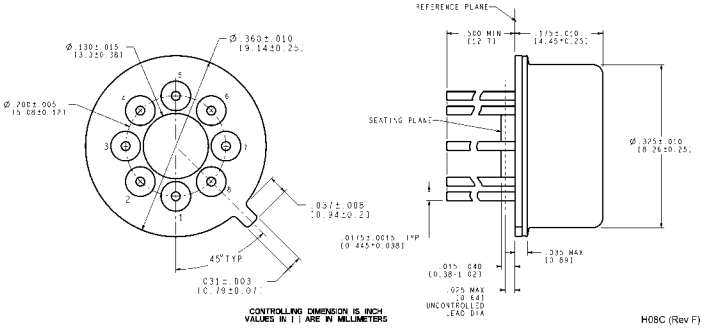
Schematic Diagram



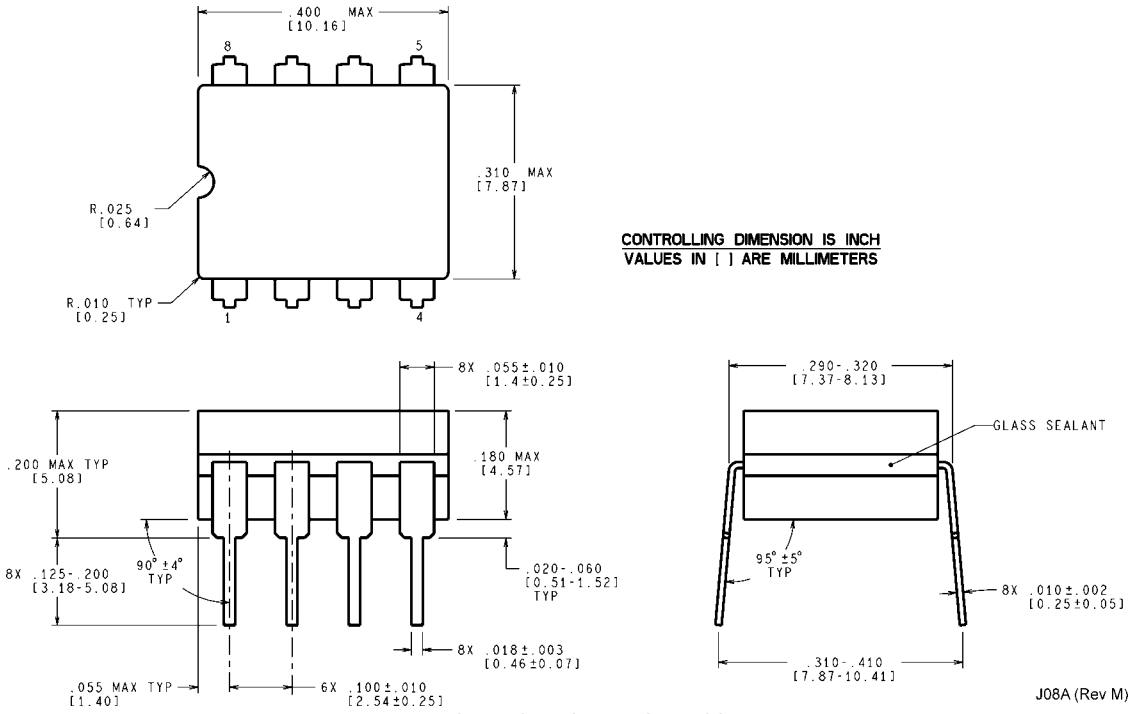
Physical Dimensions inches (millimeters) unless otherwise noted



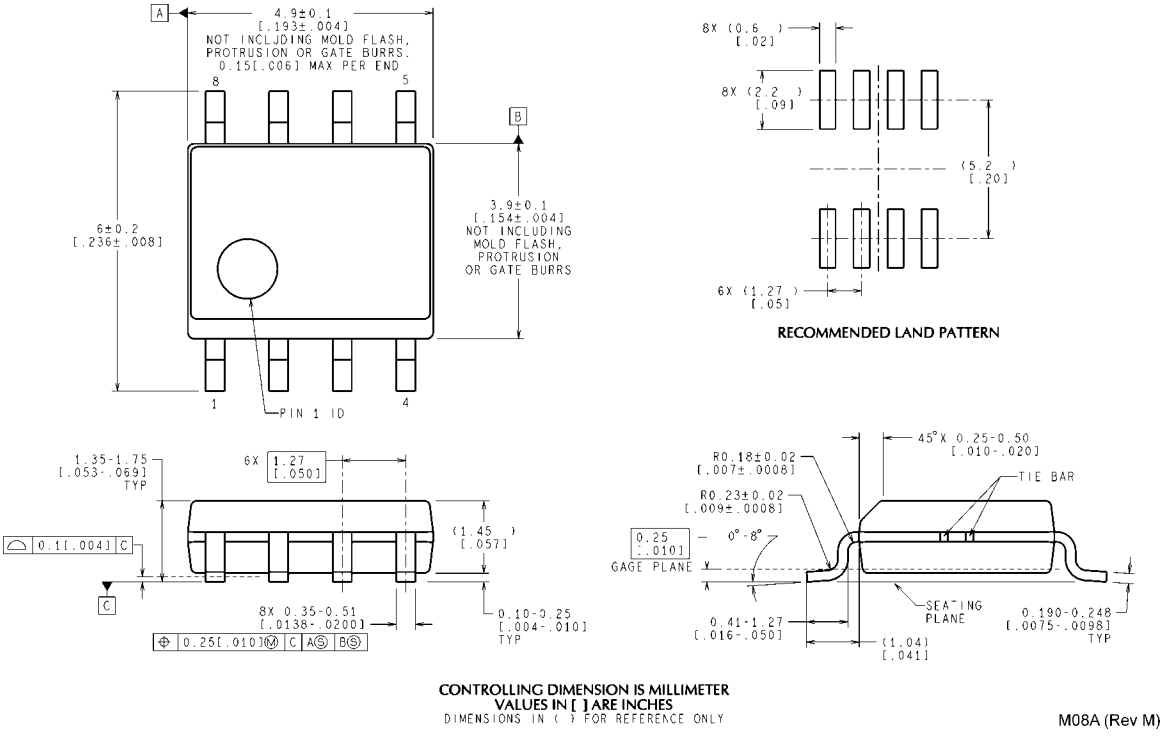
Order Number LP2951WG/883
NS Package Number WG10A



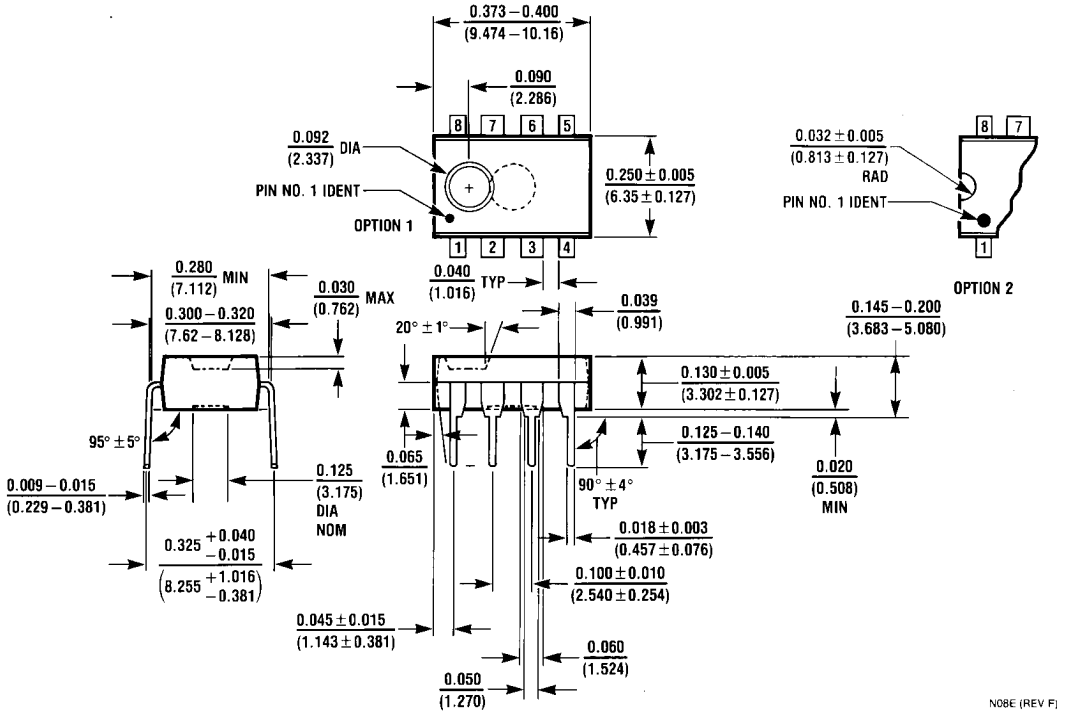
Metal Can Package (H)
NS Package Number H08C



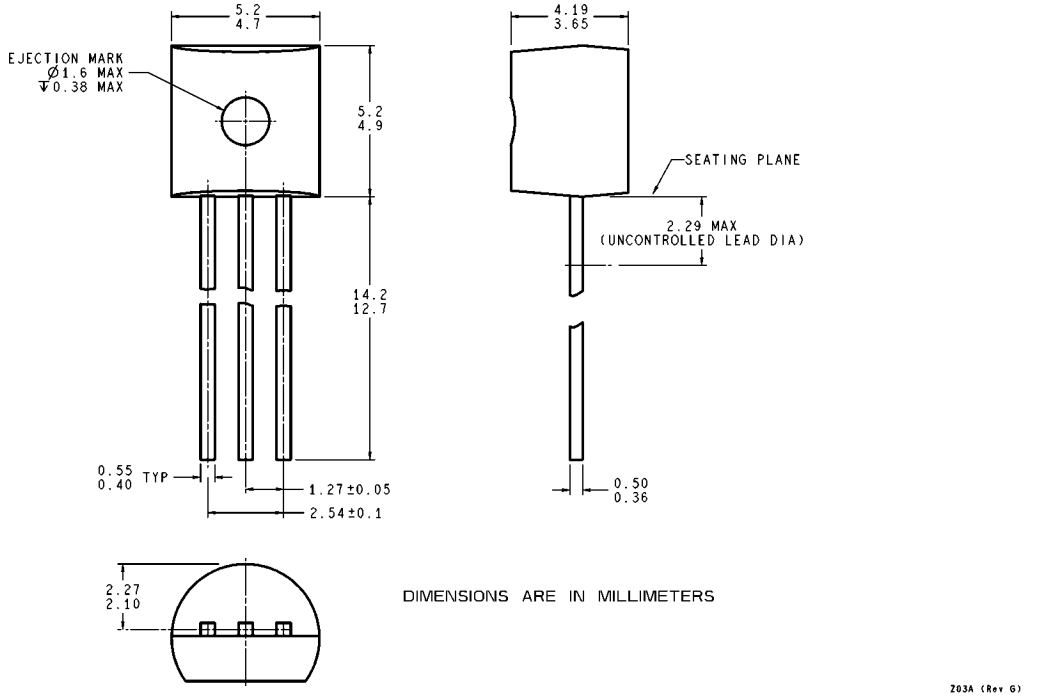
Ceramic Dual-In-Line Package (J)
NS Package Number J08A



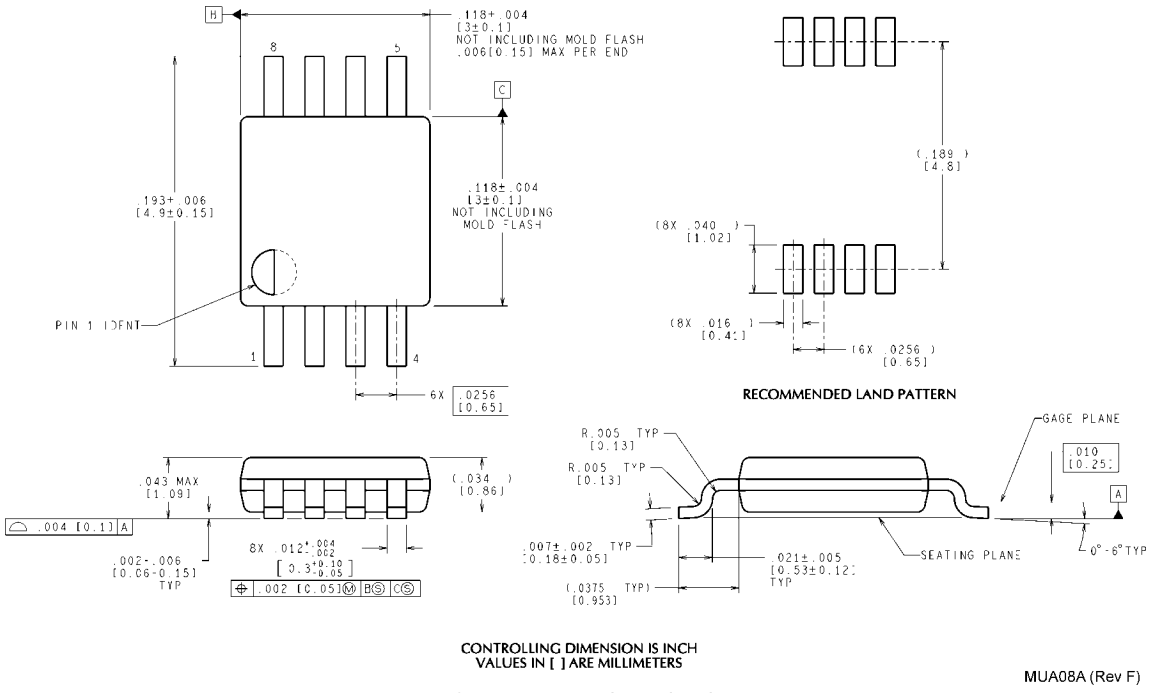
Surface Mount Package (M)
NS Package Number M08A



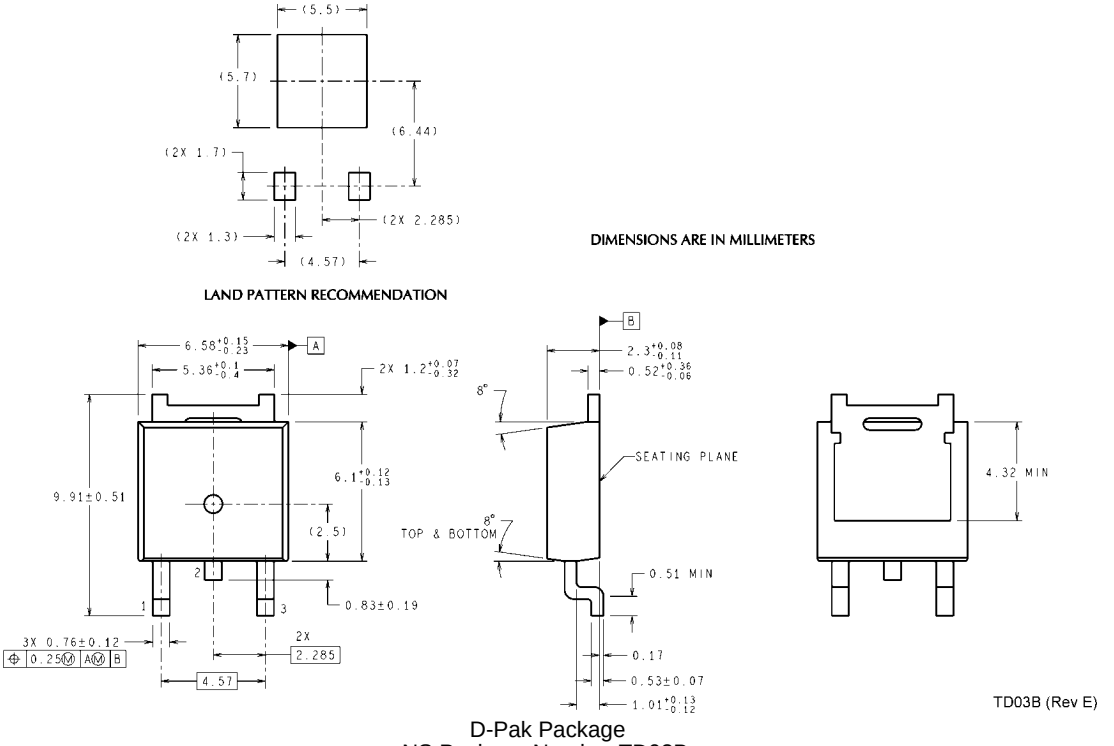
Molded Dual-In-Line Package (N)
NS Package Number N08E



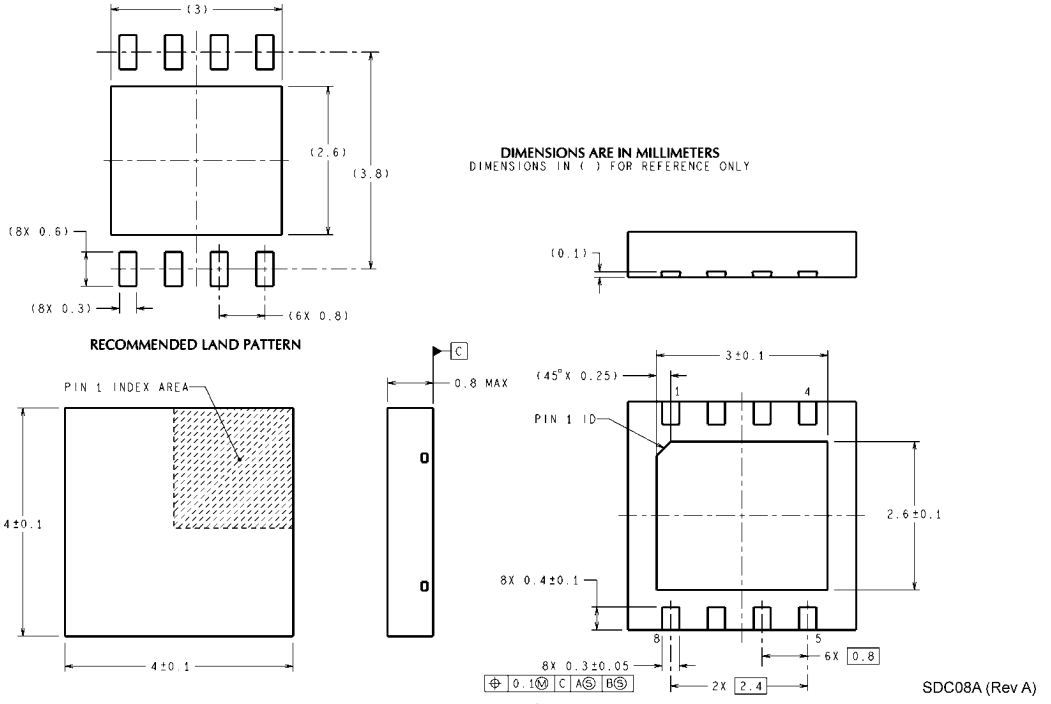
Molded TO-92 Package (Z)
NS Package Number Z03A



Surface Mount Package (MM)
NS Package Number MUA08A



D-Pak Package
NS Package Number TD03B



LLP Package
NS Package Number SDC08A

Notes

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