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# TLC7528C, TLC7528E, TLC7528I DUAL 8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTERS

SLAS062D – JANUARY 1987 – REVISED JUNE 2007

- Easily Interfaced to Microprocessors
- On-Chip Data Latches
- Monotonic Over the Entire A/D Conversion Range
- Interchangeable With Analog Devices AD7528 and PMI PM-7528
- Fast Control Signaling for Digital Signal Processor (DSP) Applications Including Interface With TMS320
- Voltage-Mode Operation
- CMOS Technology

| KEY PERFORMANCE SPECIFICATIONS          |        |
|-----------------------------------------|--------|
| Resolution                              | 8 bits |
| Linearity Error                         | 1/2LSB |
| Power Dissipation at $V_{DD} = 5V$      | 20mW   |
| Settling Time at $V_{DD} = 5V$          | 100ns  |
| Propagation Delay Time at $V_{DD} = 5V$ | 80ns   |

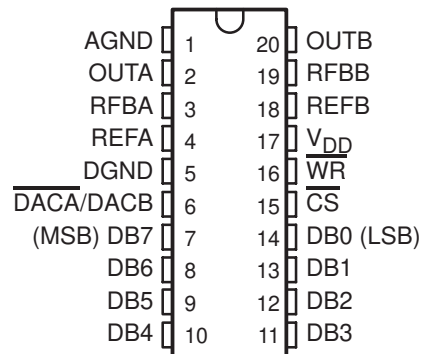
## description

The TLC7528C, TLC7528E, and TLC7528I are dual, 8-bit, digital-to-analog converters designed with separate on-chip data latches and feature exceptionally close DAC-to-DAC matching. Data is transferred to either of the two DAC data latches through a common, 8-bit, input port. Control input  $\overline{DACA/DACB}$  determines which DAC is to be loaded. The load cycle of these devices is similar to the write cycle of a random-access memory, allowing easy interface to most popular microprocessor buses and output ports. Segmenting the high-order bits minimizes glitches during changes in the most significant bits, where glitch impulse is typically the strongest.

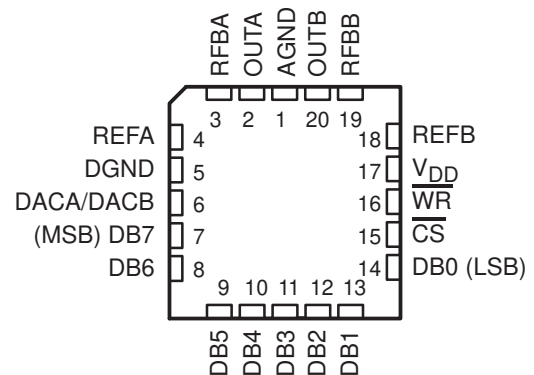
These devices operate from a 5V to 15V power supply and dissipates less than 15mW (typical). The 2- or 4-quadrant multiplying makes these devices a sound choice for many microprocessor-controlled gain-setting and signal-control applications. It can be operated in voltage mode, which produces a voltage output rather than a current output. Refer to the typical application information in this data sheet.

The TLC7528C is characterized for operation from 0°C to +70°C. The TLC7528I is characterized for operation from –25°C to +85°C. The TLC7528E is characterized for operation from –40°C to +85°C.

DW, N OR PW PACKAGE  
(TOP VIEW)



FN PACKAGE  
(TOP VIEW)



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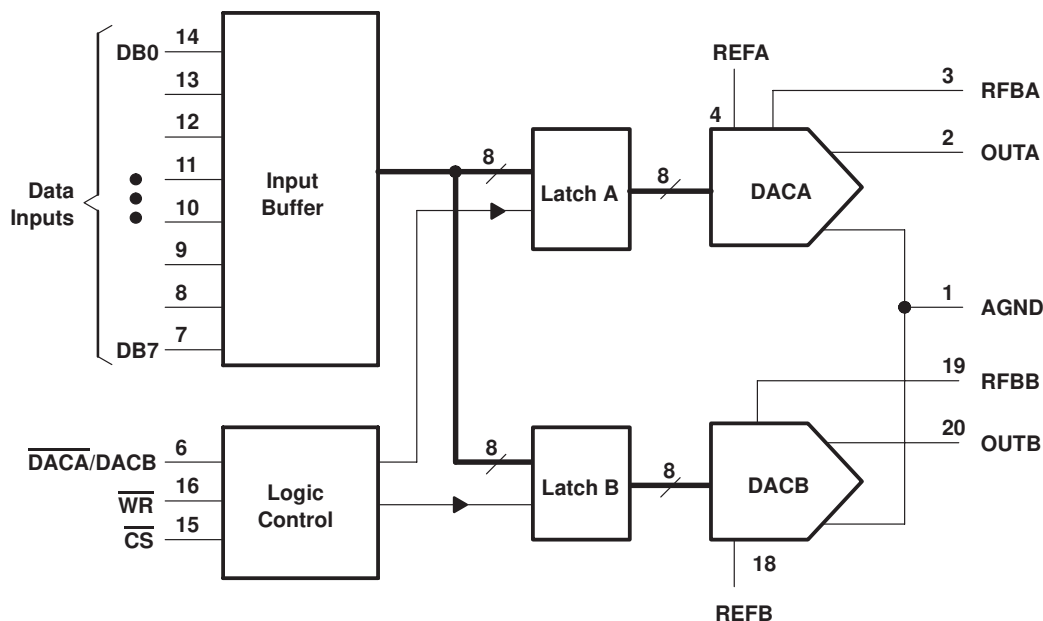
# TLC7528C, TLC7528E, TLC7528I

## DUAL 8-BIT MULTIPLYING

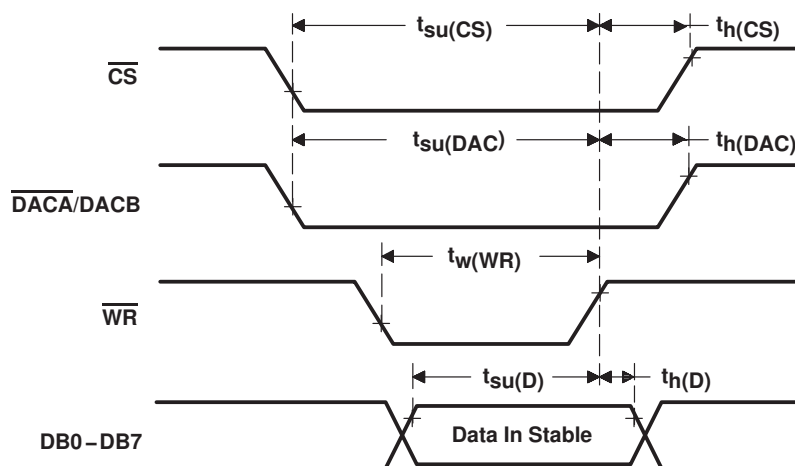
## DIGITAL-TO-ANALOG CONVERTERS

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### functional block diagram



### operating sequence



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

|                                                                              |                         |
|------------------------------------------------------------------------------|-------------------------|
| Supply voltage range, $V_{DD}$ (to AGND or DGND)                             | –0.3V to 16.5V          |
| Voltage between AGND and DGND                                                | $\pm V_{DD}$            |
| Input voltage range, $V_I$ (to DGND)                                         | –0.3V to $V_{DD} + 0.3$ |
| Reference voltage, $V_{refA}$ or $V_{refB}$ (to AGND)                        | $\pm 25V$               |
| Feedback voltage $V_{RFBA}$ or $V_{RFBB}$ (to AGND)                          | $\pm 25V$               |
| Input voltage (voltage mode out A, out B to AGND)                            | –0.3V to $V_{DD} + 0.3$ |
| Output voltage, $V_{OA}$ or $V_{OB}$ (to AGND)                               | $\pm 25V$               |
| Peak input current                                                           | 10 $\mu$ A              |
| Operating free-air temperature range, $T_A$ : TLC7528C                       | 0°C to +70°C            |
| TLC7528I                                                                     | –25°C to +85°C          |
| TLC7528E                                                                     | –40°C to +85°C          |
| Storage temperature range, $T_{stg}$                                         | –65°C to +150°C         |
| Case temperature for 10 seconds, $T_C$ : FN package                          | +260°C                  |
| Lead temperature 1,6mm (1/16 inch) from case for 10 seconds: DW or N package | +260°C                  |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**package/ordering information**

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

**recommended operating conditions**

|                                                           |          | V <sub>DD</sub> = 4.75V to 5.25V |     |     | V <sub>DD</sub> = 14.5V to 15.5V |     |     | UNIT |
|-----------------------------------------------------------|----------|----------------------------------|-----|-----|----------------------------------|-----|-----|------|
|                                                           |          | MIN                              | NOM | MAX | MIN                              | NOM | MAX |      |
| Reference voltage, V <sub>refA</sub> or V <sub>refB</sub> |          | ±10                              |     |     | ±10                              |     |     | V    |
| High-level input voltage, V <sub>IH</sub>                 |          | 2.4                              |     |     | 13.5                             |     |     | V    |
| Low-level input voltage, V <sub>IL</sub>                  |          | 0.8                              |     |     | 1.5                              |     |     | V    |
| $\overline{CS}$ setup time, t <sub>su</sub> (CS)          |          | 50                               |     |     | 50                               |     |     | ns   |
| $\overline{CS}$ hold time, t <sub>h</sub> (CS)            |          | 0                                |     |     | 0                                |     |     | ns   |
| DAC select setup time, t <sub>su</sub> (DAC)              |          | 50                               |     |     | 50                               |     |     | ns   |
| DAC select hold time, t <sub>h</sub> (DAC)                |          | 10                               |     |     | 10                               |     |     | ns   |
| Data bus input setup time t <sub>su</sub> (D)             |          | 25                               |     |     | 25                               |     |     | ns   |
| Data bus input hold time t <sub>h</sub> (D)               |          | 10                               |     |     | 10                               |     |     | ns   |
| Pulse duration, $\overline{WR}$ low, t <sub>w</sub> (WR)  |          | 50                               |     |     | 50                               |     |     | ns   |
| Operating free-air temperature, T <sub>A</sub>            | TLC7628C | 0                                |     |     | +70                              |     |     | °C   |
|                                                           | TLC7628I | −25                              |     |     | +85                              |     |     |      |
|                                                           | TLC7628E | −40                              |     |     | +85                              |     |     |      |

# TLC7528C, TLC7528E, TLC7528I

## DUAL 8-BIT MULTIPLYING

## DIGITAL-TO-ANALOG CONVERTERS

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electrical characteristics over recommended operating free-air temperature range,  
 $V_{\text{refA}} = V_{\text{refB}} = 10\text{V}$ ,  $V_{\text{OA}}$  and  $V_{\text{OB}}$  at 0V (unless otherwise noted)

| PARAMETER                                         |                                 | TEST CONDITIONS                                                          | V <sub>DD</sub> = 5V |      |     | V <sub>DD</sub> = 15V |      |     | UNIT |
|---------------------------------------------------|---------------------------------|--------------------------------------------------------------------------|----------------------|------|-----|-----------------------|------|-----|------|
|                                                   |                                 |                                                                          | MIN                  | TYP† | MAX | MIN                   | TYP† | MAX |      |
| I <sub>IH</sub>                                   | High-level input current        | V <sub>I</sub> = V <sub>DD</sub>                                         | 10                   |      |     | 10                    |      |     | μA   |
| I <sub>IL</sub>                                   | Low-level input current         | V <sub>I</sub> = 0                                                       | 5                    | 12   | −10 | 5                     | 12   | −10 | μA   |
| Reference input impedance<br>REFA or REFB to AGND |                                 |                                                                          | 20                   |      |     | 20                    |      |     | kΩ   |
| I <sub>Ikg</sub>                                  | Output leakage current          | OUTA<br>DAC data latch loaded with<br>00000000, V <sub>refA</sub> = ±10V | ±400                 |      |     | ±200                  |      |     | nA   |
|                                                   |                                 | OUTB<br>DAC data latch loaded with<br>00000000, V <sub>refB</sub> = ±10V | ±400                 |      |     | ±200                  |      |     |      |
| Input resistance match<br>(REFA to REFB)          |                                 |                                                                          | ±1%                  |      |     | ±1%                   |      |     |      |
| DC supply sensitivity, Δgain/ΔV <sub>DD</sub>     |                                 | ΔV <sub>DD</sub> = ±10%                                                  | 0.04                 |      |     | 0.02                  |      |     | %/%  |
| I <sub>DD</sub>                                   | Supply current (quiescent)      | All digital inputs at V <sub>IHmin</sub> or<br>V <sub>ILmax</sub>        | 2                    |      |     | 2                     |      |     | mA   |
| I <sub>DD</sub>                                   | Supply current (standby)        | All digital inputs at 0V or V <sub>DD</sub>                              | 0.5                  |      |     | 0.5                   |      |     | mA   |
| C <sub>i</sub>                                    | Input capacitance               | DB0–DB7                                                                  | 10                   |      |     | 10                    |      |     | pF   |
|                                                   |                                 | WR, CS,<br>DACA/DACB                                                     | 15                   |      |     | 15                    |      |     | pF   |
| C <sub>O</sub>                                    | Output capacitance (OUTA, OUTB) | DAC data latches loaded with<br>00000000                                 | 50                   |      |     | 50                    |      |     | pF   |
|                                                   |                                 | DAC data latches loaded with<br>11111111                                 | 120                  |      |     | 120                   |      |     |      |

† All typical values are at  $T_{\text{A}} = +25^{\circ}\text{C}$ .

operating characteristics over recommended operating free-air temperature range,  
 $V_{refA} = V_{refB} = 10V$ ,  $V_{OA}$  and  $V_{OB}$  at 0V (unless otherwise noted)

| PARAMETER                                                                    |              | TEST CONDITIONS                                                             | $V_{DD} = 5V$ |     |           | $V_{DD} = 15V$ |     |           | UNIT    |
|------------------------------------------------------------------------------|--------------|-----------------------------------------------------------------------------|---------------|-----|-----------|----------------|-----|-----------|---------|
|                                                                              |              |                                                                             | MIN           | TYP | MAX       | MIN            | TYP | MAX       |         |
| Linearity error                                                              |              |                                                                             |               |     | $\pm 1/2$ |                |     | $\pm 1/2$ | LSB     |
| Settling time (to 1/2LSB)                                                    |              | See Note 1                                                                  |               |     | 100       |                |     | 100       | ns      |
| Gain error                                                                   |              | See Note 2                                                                  |               |     | 2.5       |                |     | 2.5       | LSB     |
| AC feedthrough                                                               | REFA to OUTA | See Note 3                                                                  |               |     | -65       |                |     | -65       | dB      |
|                                                                              | REFB to OUTB |                                                                             |               |     | -65       |                |     | -65       |         |
| Temperature coefficient of gain                                              |              | See Note 4                                                                  |               |     | 0.007     |                |     | 0.0035    | %FSR/°C |
| Propagation delay (from digital input to 90% of final analog output current) |              | See Note 5                                                                  |               |     | 80        |                |     | 80        | ns      |
| Channel-to-channel isolation                                                 | REFA to OUTB | See Note 6                                                                  |               | 77  |           |                | 77  |           | dB      |
|                                                                              | REFB to OUTA | See Note 7                                                                  |               | 77  |           |                | 77  |           |         |
| Digital-to-analog glitch impulse area                                        |              | Measured for code transition from 00000000 to 11111111, $T_A = +25^\circ C$ |               | 160 |           |                | 440 |           | nV-s    |
| Digital crosstalk                                                            |              | Measured for code transition from 00000000 to 11111111, $T_A = +25^\circ C$ |               | 30  |           |                | 60  |           | nV-s    |
| Harmonic distortion                                                          |              | $V_i = 6V$ , $f = 1kHz$ , $T_A = +25^\circ C$                               |               | -85 |           |                | -85 |           | dB      |

- NOTES: 1. OUTA, OUTB load = 100Ω,  $C_{ext} = 13pF$ ;  $\overline{WR}$  and  $\overline{CS}$  at 0V; DB0-DB7 at 0V to  $V_{DD}$  or  $V_{DD}$  to 0V.  
 2. Gain error is measured using an internal feedback resistor. Nominal full scale range (FSR) =  $V_{ref} - 1LSB$ .  
 3.  $V_{ref} = 20V$  peak-to-peak, 100kHz sine wave; DAC data latches loaded with 00000000.  
 4. Temperature coefficient of gain measured from 0°C to +25°C or from +25°C to +70°C.  
 5.  $V_{refA} = V_{refB} = 10V$ ; OUTA/OUTB load = 100Ω,  $C_{ext} = 13pF$ ;  $\overline{WR}$  and  $\overline{CS}$  at 0V; DB0-DB7 at 0V to  $V_{DD}$  or  $V_{DD}$  to 0V.  
 6. Both DAC latches loaded with 11111111;  $V_{refA} = 20V$  peak-to-peak, 100kHz sine wave;  $V_{refB} = 0$ ;  $T_A = +25^\circ C$ .  
 7. Both DAC latches loaded with 11111111;  $V_{refB} = 20V$  peak-to-peak, 100kHz sine wave;  $V_{refA} = 0$ ;  $T_A = +25^\circ C$ .

## PRINCIPLES OF OPERATION

These devices contain two identical, 8-bit-multiplying D/A converters, DACA and DACB. Each DAC consists of an inverted R-2R ladder, analog switches, and input data latches. Binary-weighted currents are switched between DAC output and AGND, thus maintaining a constant current in each ladder leg independent of the switch state. Most applications require only the addition of an external operational amplifier and voltage reference. A simplified D/A circuit for DACA with all digital inputs low is shown in Figure 1.

Figure 2 shows the DACA equivalent circuit. A similar equivalent circuit can be drawn for DACB. Both DACs share the analog ground terminal 1 (AGND). With all digital inputs high, the entire reference current flows to OUTA. A small leakage current ( $I_{lkg}$ ) flows across internal junctions, and as with most semiconductor devices, doubles every 10°C.  $C_O$  is due to the parallel combination of the NMOS switches and has a value that depends on the number of switches connected to the output. The range of  $C_O$  is 50pF to 120pF maximum. The equivalent output resistance ( $r_O$ ) varies with the input code from 0.8R to 3R where R is the nominal value of the ladder resistor in the R-2R network.

These devices interface to a microprocessor through the data bus,  $\overline{CS}$ ,  $\overline{WR}$ , and  $\overline{DACA}/\overline{DACB}$  control signals. When  $\overline{CS}$  and  $\overline{WR}$  are both low, the TLC7528 analog output, specified by the  $\overline{DACA}/\overline{DACB}$  control line, responds to the activity on the DB0-DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the  $\overline{CS}$  signal or  $\overline{WR}$  signal goes high, the data on the DB0-DB7 inputs is latched until the  $\overline{CS}$  and  $\overline{WR}$  signals go low again. When  $\overline{CS}$  is high, the data inputs are disabled regardless of the state of the  $\overline{WR}$  signal.

# TLC7528C, TLC7528E, TLC7528I

## DUAL 8-BIT MULTIPLYING

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### PRINCIPLES OF OPERATION

The digital inputs of these devices provide TTL compatibility when operated from a supply voltage of 5V. These devices can operate with any supply voltage in the range from 5V to 15V; however, input logic levels are not TTL compatible above 5V.

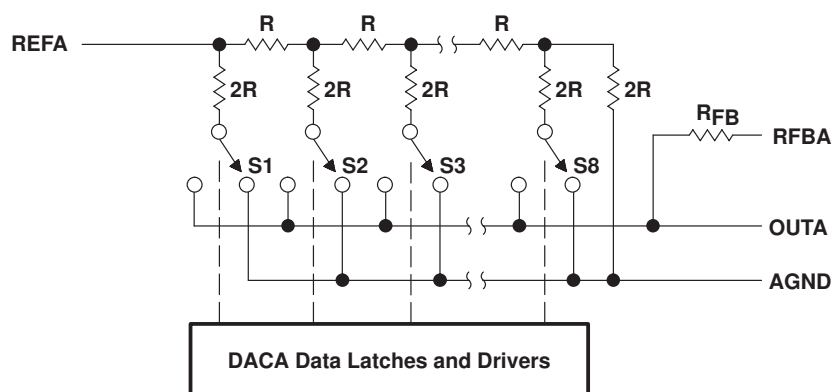


Figure 1. Simplified Functional Circuit for DACA

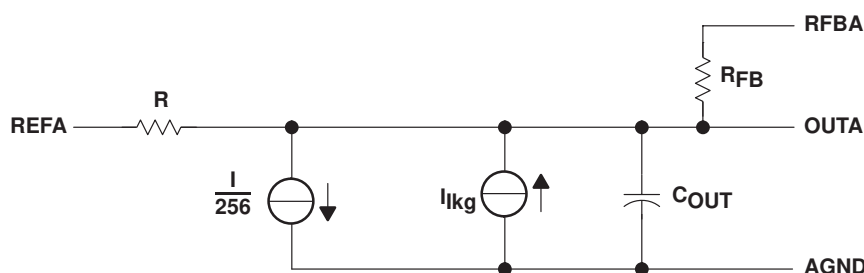


Figure 2. TLC7528 Equivalent Circuit, DACA Latch Loaded With 11111111

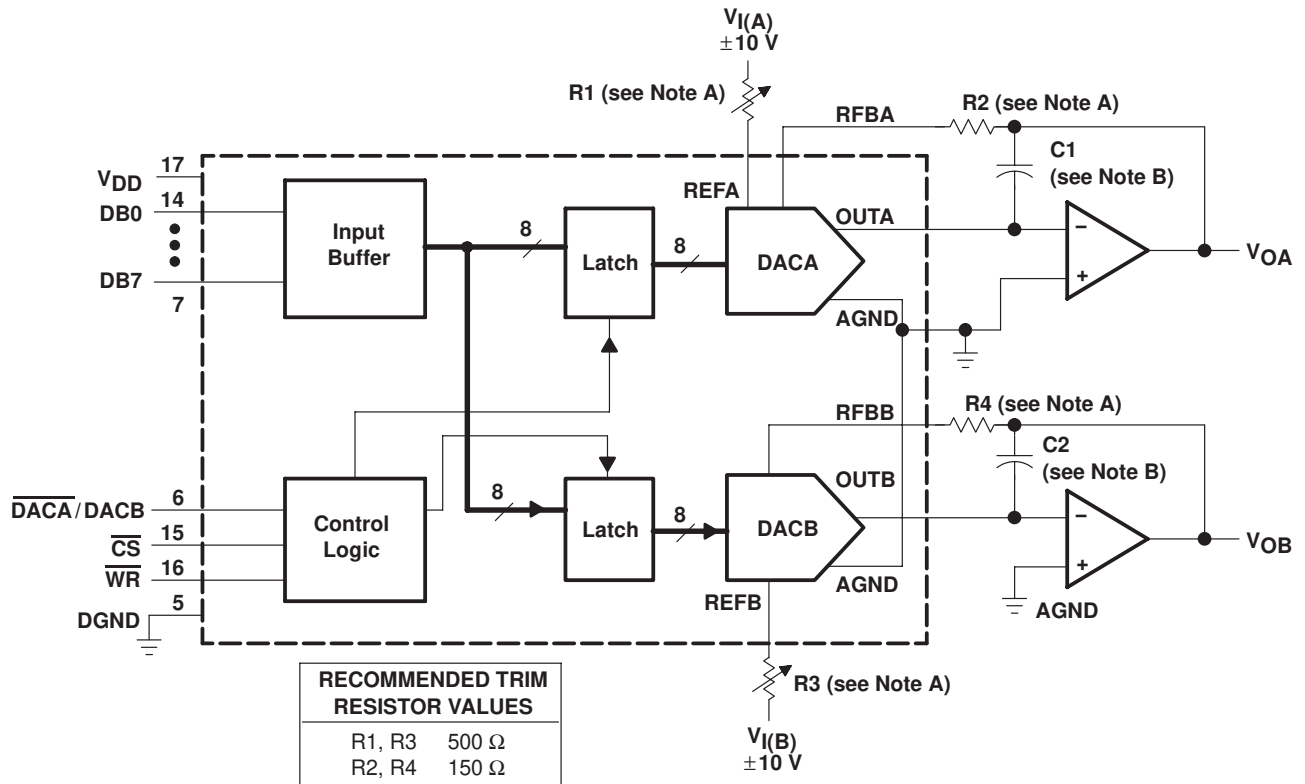
MODE SELECTION TABLE

| DACA/DACB | $\overline{CS}$ | $\overline{WR}$ | DACA  | DACB  |
|-----------|-----------------|-----------------|-------|-------|
| L         | L               | L               | Write | Hold  |
| H         | L               | L               | Hold  | Write |
| X         | H               | X               | Hold  | Hold  |
| X         | X               | H               | Hold  | Hold  |

L = low level, H = high level, X = don't care

## APPLICATION INFORMATION

These devices are capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant and 4-quadrant multiplication are shown in Figures 3 and 4. Tables 1 and 2 summarize input coding for unipolar and bipolar operation.



- NOTES: A. R1, R2, R3, and R4 are used only if gain adjustment is required. See table for recommended values. Make gain adjustment with digital input of 255.
- B. C1 and C2 phase compensation capacitors (10pF to 15pF) are required when using high-speed amplifiers to prevent ringing or oscillation.

**Figure 3. Unipolar Operation (2-Quadrant Multiplication)**



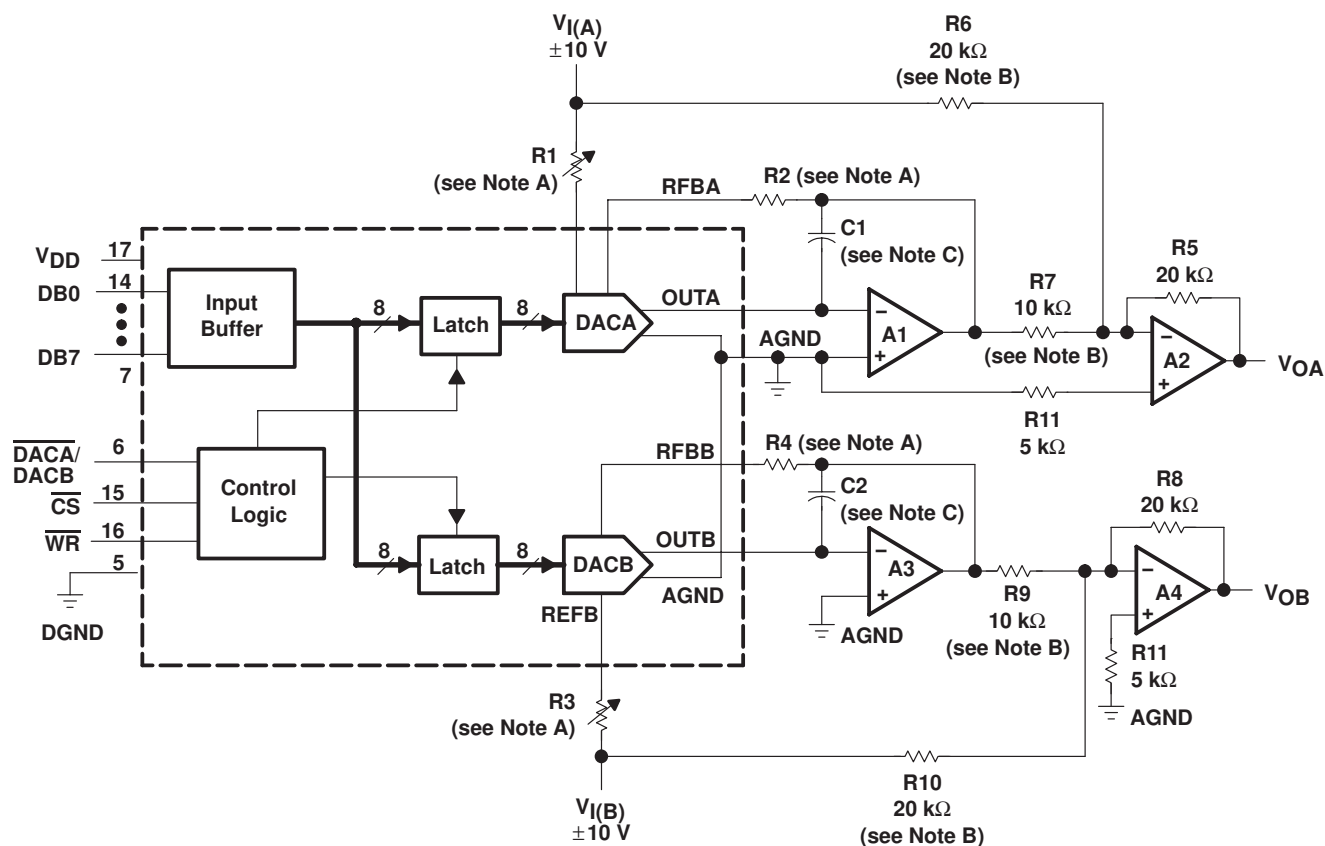
# TLC7528C, TLC7528E, TLC7528I

## DUAL 8-BIT MULTIPLYING

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### APPLICATION INFORMATION



- NOTES: A. R1, R2, R3, and R4 are used only if gain adjustment is required. See table in Figure 3 for recommended values. Adjust R1 for  $V_{OA} = 0V$  with code 10000000 in DACA latch. Adjust R3 for  $V_{OB} = 0V$  with 10000000 in DACB latch.
- B. Matching and tracking are essential for resistor pairs R6, R7, R9, and R10.
- C. C1 and C2 phase compensation capacitors (10pF to 15pF) may be required if A1 and A3 are high-speed amplifiers.

Figure 4. Bipolar Operation (4-Quadrant Operation)

Table 1. Unipolar Binary Code

| DAC LATCH CONTENTS |      | ANALOG OUTPUT             |
|--------------------|------|---------------------------|
| MSB                | LSB† |                           |
| 1                  | 1    | $-V_I (255/256)$          |
| 1                  | 0    | $-V_I (129/256)$          |
| 1                  | 0    | $-V_I (128/256) = -V_I/2$ |
| 0                  | 1    | $-V_I (127/256)$          |
| 0                  | 0    | $-V_I (1/256)$            |
| 0                  | 0    | $-V_I (0/256) = 0$        |

†1LSB =  $(2^{-8})V_I$

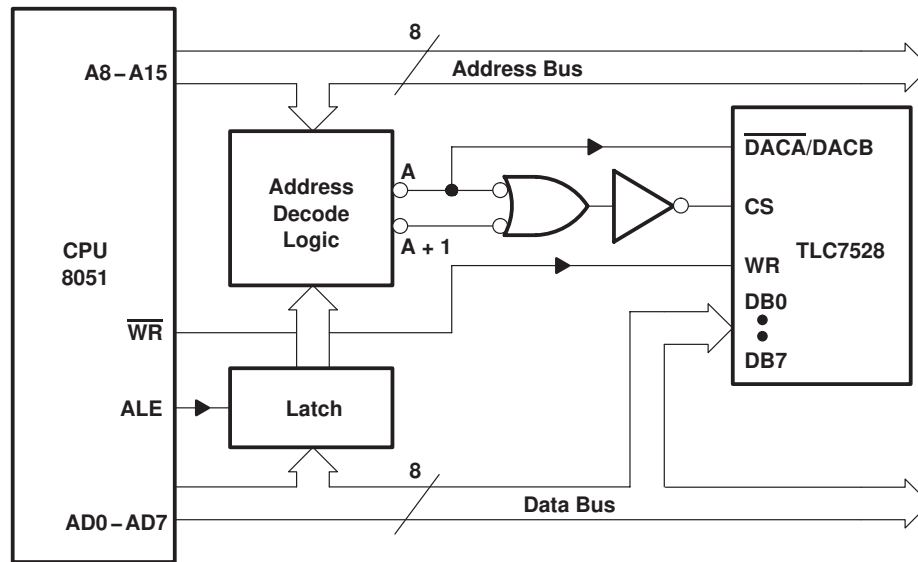
Table 2. Bipolar (Offset Binary) Code

| DAC LATCH CONTENTS |      | ANALOG OUTPUT    |
|--------------------|------|------------------|
| MSB                | LSB‡ |                  |
| 1                  | 1    | $V_I (127/128)$  |
| 1                  | 0    | $V_I (1/128)$    |
| 1                  | 0    | 0V               |
| 0                  | 1    | $-V_I (1/128)$   |
| 0                  | 0    | $-V_I (127/128)$ |
| 0                  | 0    | $-V_I (128/128)$ |

‡1LSB =  $(2^{-7})V_I$

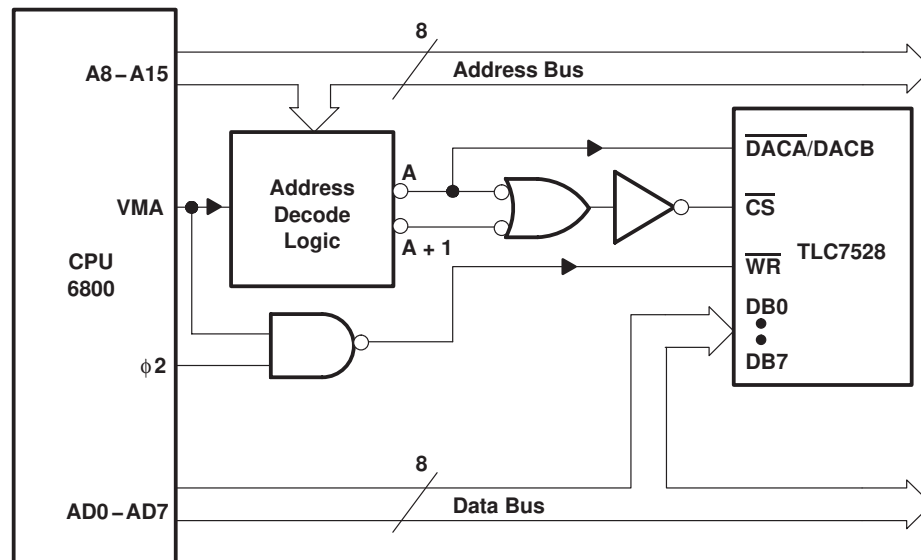
## APPLICATION INFORMATION

### microprocessor interface information



NOTE A: A = decoded address for TLC7528 DACA  
 A + 1 = decoded address for TLC7528 DACB

**Figure 5. TLC7528: Intel 8051 Interface**



NOTE A: A = decoded address for TLC7528 DACA  
 A + 1 = decoded address for TLC7528 DACB

**Figure 6. TLC7528: 6800 Interface**

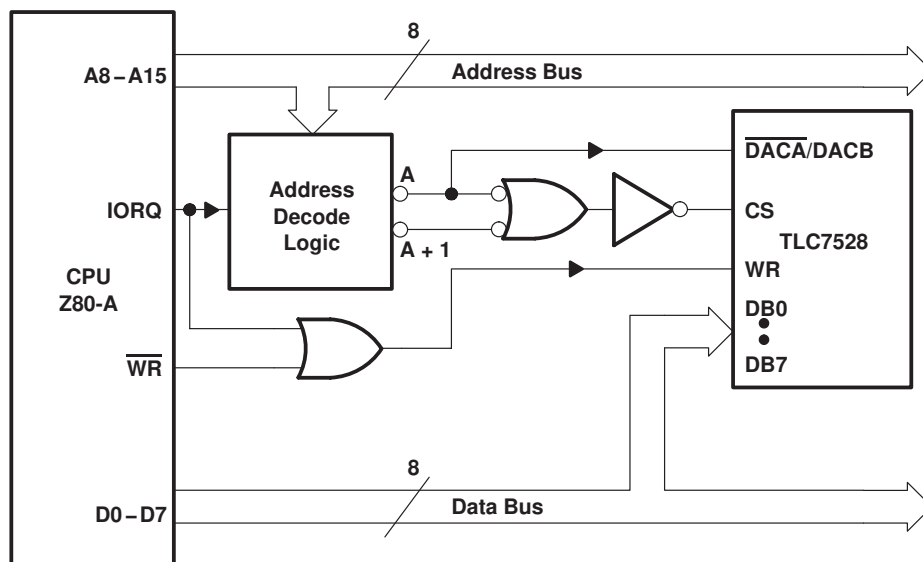
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### APPLICATION INFORMATION



NOTE A: A = decoded address for TLC7528 DACA  
A + 1 = decoded address for TLC7528 DACB

**Figure 7. TLC7528 To Z-80A Interface**

### programmable window detector

The programmable window comparator shown in Figure 8 determines if voltage applied to the DAC feedback resistors are within the limits programmed into the data latches of these devices. Input signal range depends on the reference and polarity, that is, the test input range is 0 to  $-V_{ref}$ . The DACA and DACB data latches are programmed with the upper and lower test limits. A signal within the programmed limits drives the output high.

## APPLICATION INFORMATION

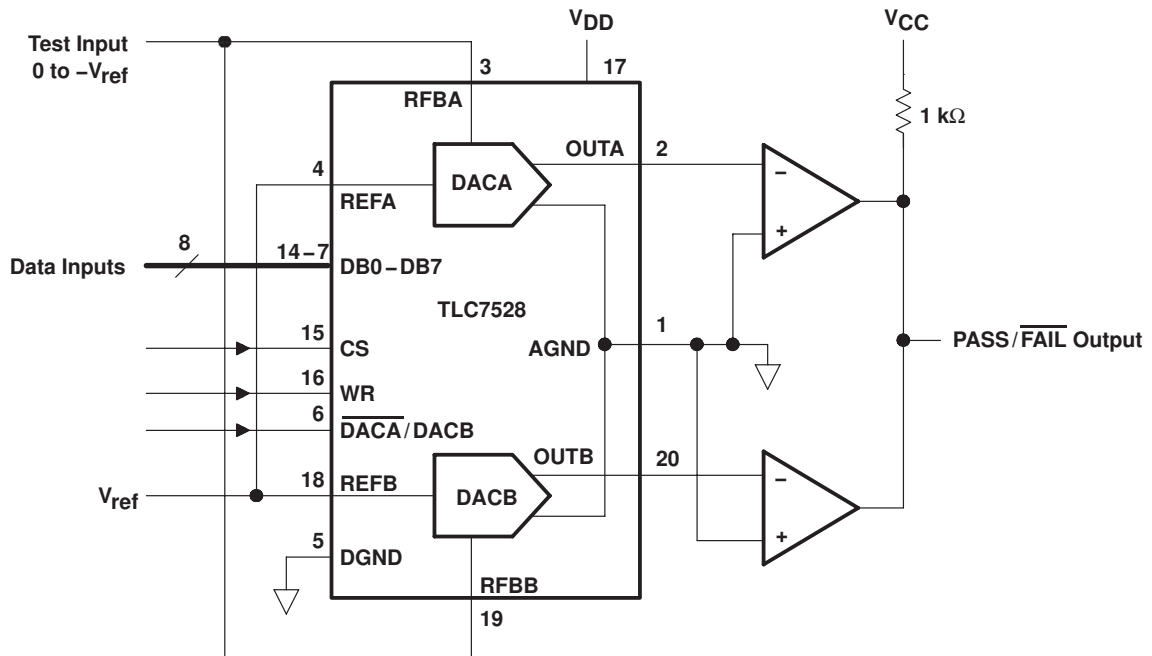


Figure 8. Digitally-Programmable Window Comparator (Upper- and Lower-Limit Tester)

### digitally controlled signal attenuator

Figure 9 shows a TLC7528 configured as a two-channel programmable attenuator. Applications include stereo audio and telephone signal level control. Table 3 shows input codes vs attenuation for a 0 to 15.5dB range.

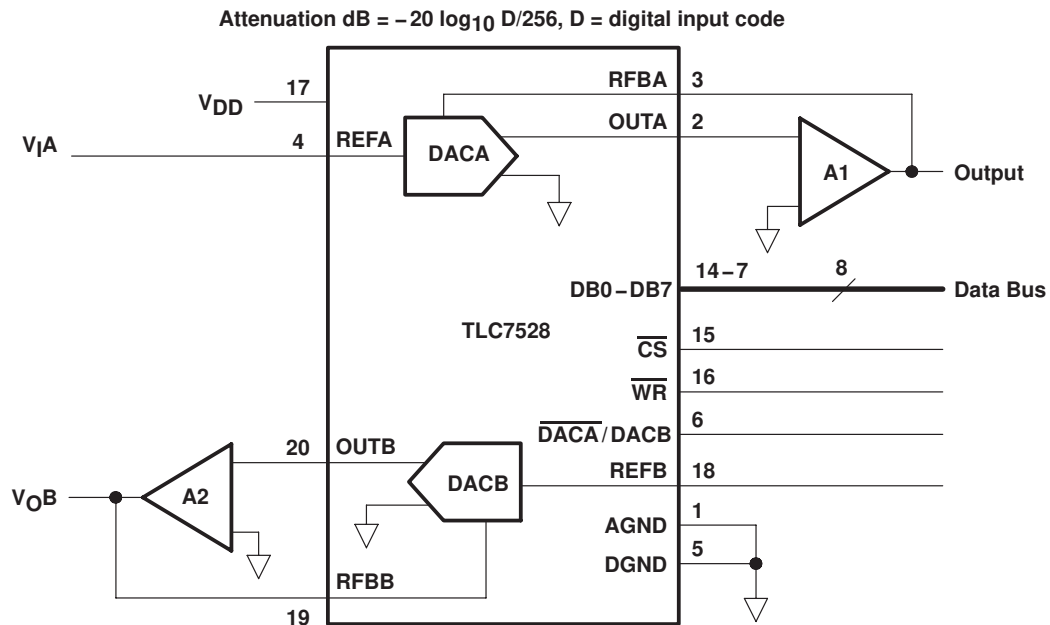


Figure 9. Digitally Controlled Dual Telephone Attenuator

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## DUAL 8-BIT MULTIPLYING

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### APPLICATION INFORMATION

Table 3. Attenuation vs DACA, DACB Code

| ATTN (dB) | DAC INPUT CODE  | CODE IN DECIMAL | ATTN (dB) | DAC INPUT CODE  | CODE IN DECIMAL |
|-----------|-----------------|-----------------|-----------|-----------------|-----------------|
| 0         | 1 1 1 1 1 1 1 1 | 255             | 8.0       | 0 1 1 0 0 1 1 0 | 102             |
| 0.5       | 1 1 1 1 0 0 1 0 | 242             | 8.5       | 0 1 1 0 0 0 0 0 | 96              |
| 1.0       | 1 1 1 0 0 1 0 0 | 228             | 9.0       | 0 1 0 1 1 0 1 1 | 91              |
| 1.5       | 1 1 0 1 0 1 1 1 | 215             | 9.5       | 0 1 0 1 0 1 1 0 | 86              |
| 2.0       | 1 1 0 0 1 0 1 1 | 203             | 10.0      | 0 1 0 1 0 0 0 1 | 81              |
| 2.5       | 1 1 0 0 0 0 0 0 | 192             | 10.5      | 0 1 0 0 1 1 0 0 | 76              |
| 3.0       | 1 0 1 1 0 1 0 1 | 181             | 11.0      | 0 1 0 0 1 0 0 0 | 72              |
| 3.5       | 1 0 1 0 1 0 1 1 | 171             | 11.5      | 0 1 0 0 0 1 0 0 | 68              |
| 4.0       | 1 0 1 0 0 0 1 0 | 162             | 12.0      | 0 1 0 0 0 0 0 0 | 64              |
| 4.5       | 1 0 0 1 1 0 0 0 | 152             | 12.5      | 0 0 1 1 1 1 0 1 | 61              |
| 5.0       | 1 0 0 1 1 1 1 1 | 144             | 13.0      | 0 0 1 1 1 0 0 1 | 57              |
| 5.5       | 1 0 0 0 1 0 0 0 | 136             | 13.5      | 0 0 1 1 0 1 1 0 | 54              |
| 6.0       | 1 0 0 0 0 0 0 0 | 128             | 14.0      | 0 0 1 1 0 0 1 1 | 51              |
| 6.5       | 0 1 1 1 1 0 0 1 | 121             | 14.5      | 0 0 1 1 0 0 0 0 | 48              |
| 7.0       | 0 1 1 1 0 0 1 0 | 114             | 15.0      | 0 0 1 0 1 1 1 0 | 46              |
| 7.5       | 0 1 1 0 1 1 0 0 | 108             | 15.5      | 0 0 1 0 1 0 1 1 | 43              |

### programmable state-variable filter

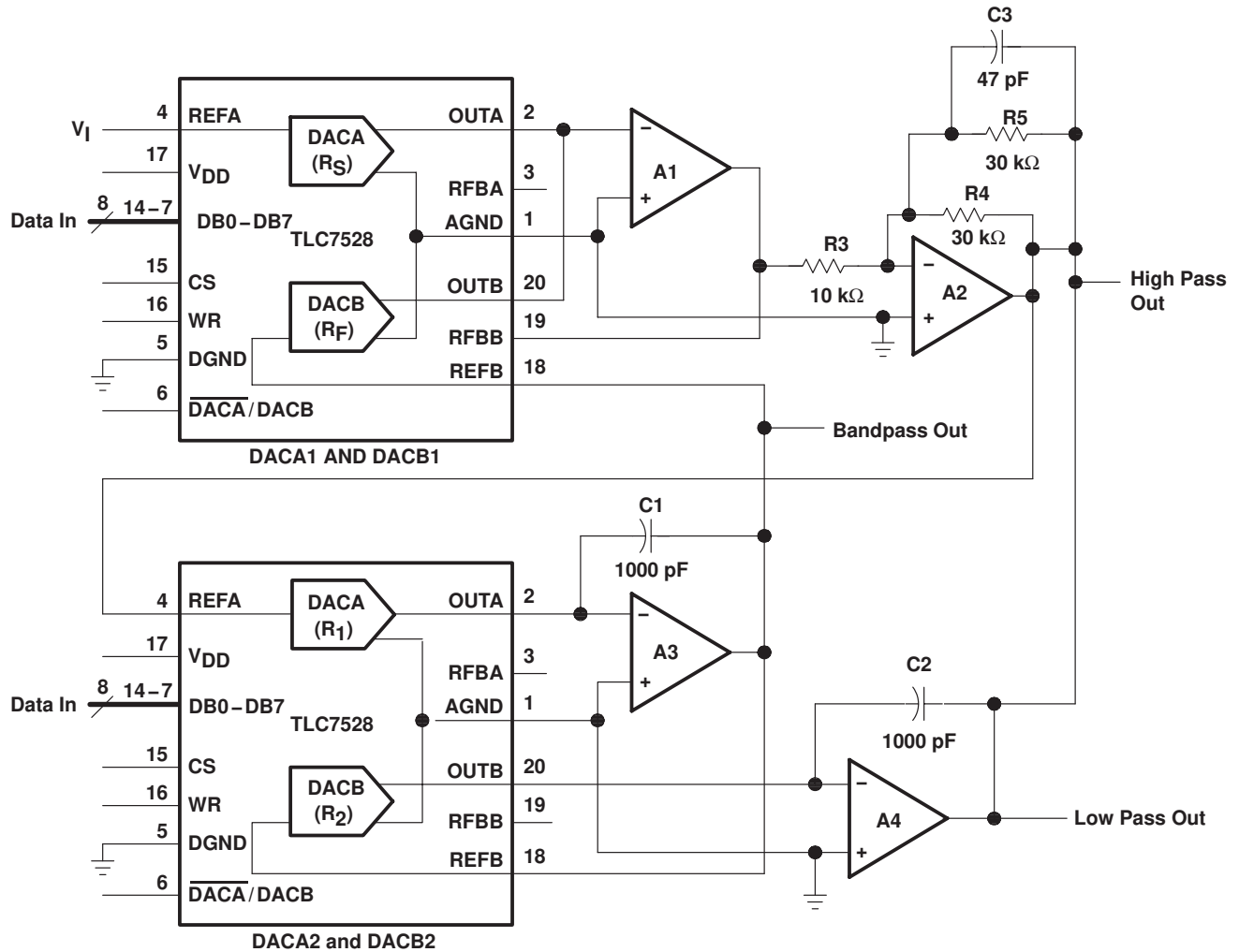
This programmable state-variable or universal filter configuration provides low-pass, high-pass, and bandpass outputs, and is suitable for applications requiring microprocessor control of filter parameters.

As shown in Figure 10, DACA1 and DACB1 control the gain and Q of the filter while DACA2 and DACB2 control the cutoff frequency. Both halves of the DACA2 and DACB2 must track accurately in order for the cutoff-frequency equation to be true. With the TLC7528, this is easy to achieve.

$$f_c = \frac{1}{2\pi R1C1}$$

The programmable range for the cutoff or center frequency is 0 to 15kHz with a Q ranging from 0.3 to 4.5. This defines the limits of the component values.

## APPLICATION INFORMATION



### Circuit Equations:

$$C_1 = C_2, R_1 = R_2, R_4 = R_5$$

$$Q = \frac{R_3}{R_4} \times \frac{R_F}{R_{fb}(\text{DACB1})}$$

### Where:

$R_{fb}$  is the internal resistor connected between OUTB and RFBB

$$G = -\frac{R_F}{R_S}$$

- NOTES: A. Op-amps A1, A2, A3, and A4 are TL287.  
 B. CS compensates for the op-amp gain-bandwidth limitations.  
 C. DAC equivalent resistance equals  $\frac{256 \times (\text{DAC ladder resistance})}{\text{DAC digital code}}$

**Figure 10. Digitally Controlled State-Variable Filter**

# TLC7528C, TLC7528E, TLC7528I

## DUAL 8-BIT MULTIPLYING

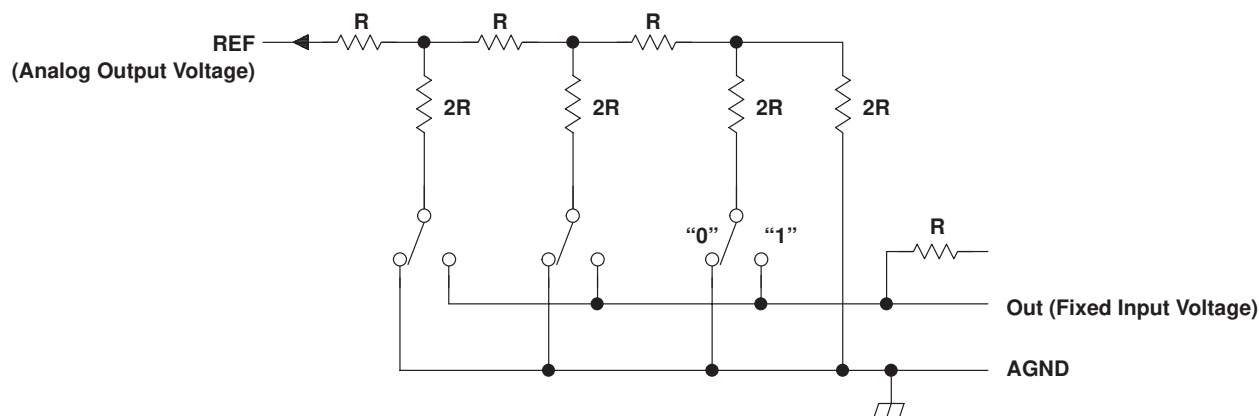
## DIGITAL-TO-ANALOG CONVERTERS

SLAS062D – JANUARY 1987 – REVISED JUNE 2007

### APPLICATION INFORMATION

#### voltage-mode operation

It is possible to operate the current multiplying D/A converter of these devices in a voltage mode. In the voltage mode, a fixed voltage is placed on the current output terminal. The analog output voltage is then available at the reference voltage terminal. Figure 11 is an example of a current multiplying D/A, that operates in the voltage mode.



**Figure 11. Voltage-Mode Operation**

The following equation shows the relationship between the fixed input voltage and the analog output voltage:

$$V_O = V_I (D/256)$$

Where:

$V_O$  = analog output voltage

$V_I$  = fixed input voltage (must not be forced below 0V.)

$D$  = digital input code converted to decimal

In voltage-mode operation, these devices meet the following specification:

| PARAMETER                       | TEST CONDITIONS                                               | MIN | MAX | UNIT |
|---------------------------------|---------------------------------------------------------------|-----|-----|------|
| Linearity error at REFA or REFB | $V_{DD} = 5V$ , $OUTA$ or $OUTB$ at 2.5V, $T_A = +25^\circ C$ |     | 1   | LSB  |

**Revision History**

| DATE | REV | PAGE       | SECTION | DESCRIPTION                            |
|------|-----|------------|---------|----------------------------------------|
| 6/07 | D   | Front Page | —       | Deleted Available Options table.       |
|      |     | 3          | —       | Inserted Package/Ordering information. |

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.



**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| TLC7528CDW       | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TLC7528CDWG4     | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TLC7528CDWR      | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TLC7528CDWRG4    | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TLC7528CFN       | ACTIVE                | PLCC         | FN              | 20   | 46          | Green (RoHS & no Sb/Br) | CU SN            | Level-1-260C-UNLIM           |
| TLC7528CFNG3     | ACTIVE                | PLCC         | FN              | 20   | 46          | Green (RoHS & no Sb/Br) | CU SN            | Level-1-260C-UNLIM           |
| TLC7528CFNR      | ACTIVE                | PLCC         | FN              | 20   | 1000        | Green (RoHS & no Sb/Br) | CU SN            | Level-1-260C-UNLIM           |
| TLC7528CFNRG3    | ACTIVE                | PLCC         | FN              | 20   | 1000        | Green (RoHS & no Sb/Br) | CU SN            | Level-1-260C-UNLIM           |
| TLC7528CN        | ACTIVE                | PDIP         | N               | 20   | 20          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| TLC7528CNE4      | ACTIVE                | PDIP         | N               | 20   | 20          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| TLC7528CNS       | ACTIVE                | SO           | NS              | 20   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TLC7528CNSG4     | ACTIVE                | SO           | NS              | 20   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TLC7528CNSR      | ACTIVE                | SO           | NS              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TLC7528CNSRG4    | ACTIVE                | SO           | NS              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TLC7528CPW       | ACTIVE                | TSSOP        | PW              | 20   | 70          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TLC7528CPWG4     | ACTIVE                | TSSOP        | PW              | 20   | 70          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TLC7528CPWR      | ACTIVE                | TSSOP        | PW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TLC7528CPWRG4    | ACTIVE                | TSSOP        | PW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TLC7528EDW       | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TLC7528EDWG4     | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TLC7528EDWR      | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TLC7528EDWRG4    | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TLC7528EN        | ACTIVE                | PDIP         | N               | 20   | 20          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| TLC7528ENE4      | ACTIVE                | PDIP         | N               | 20   | 20          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| TLC7528IDW       | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| TLC7528IDWG4     | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TLC7528IDWR      | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TLC7528IDWRG4    | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TLC7528IFN       | ACTIVE                | PLCC         | FN              | 20   | 46          | Green (RoHS & no Sb/Br) | CU SN            | Level-1-260C-UNLIM           |
| TLC7528IFNG3     | ACTIVE                | PLCC         | FN              | 20   | 46          | Green (RoHS & no Sb/Br) | CU SN            | Level-1-260C-UNLIM           |
| TLC7528IFNR      | ACTIVE                | PLCC         | FN              | 20   | 1000        | Green (RoHS & no Sb/Br) | CU SN            | Level-1-260C-UNLIM           |
| TLC7528IFNRG3    | ACTIVE                | PLCC         | FN              | 20   | 1000        | Green (RoHS & no Sb/Br) | CU SN            | Level-1-260C-UNLIM           |
| TLC7528IN        | ACTIVE                | PDIP         | N               | 20   | 20          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| TLC7528INE4      | ACTIVE                | PDIP         | N               | 20   | 20          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| TLC7528IPW       | ACTIVE                | TSSOP        | PW              | 20   | 70          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TLC7528IPWG4     | ACTIVE                | TSSOP        | PW              | 20   | 70          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TLC7528IPWR      | ACTIVE                | TSSOP        | PW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| TLC7528IPWRG4    | ACTIVE                | TSSOP        | PW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

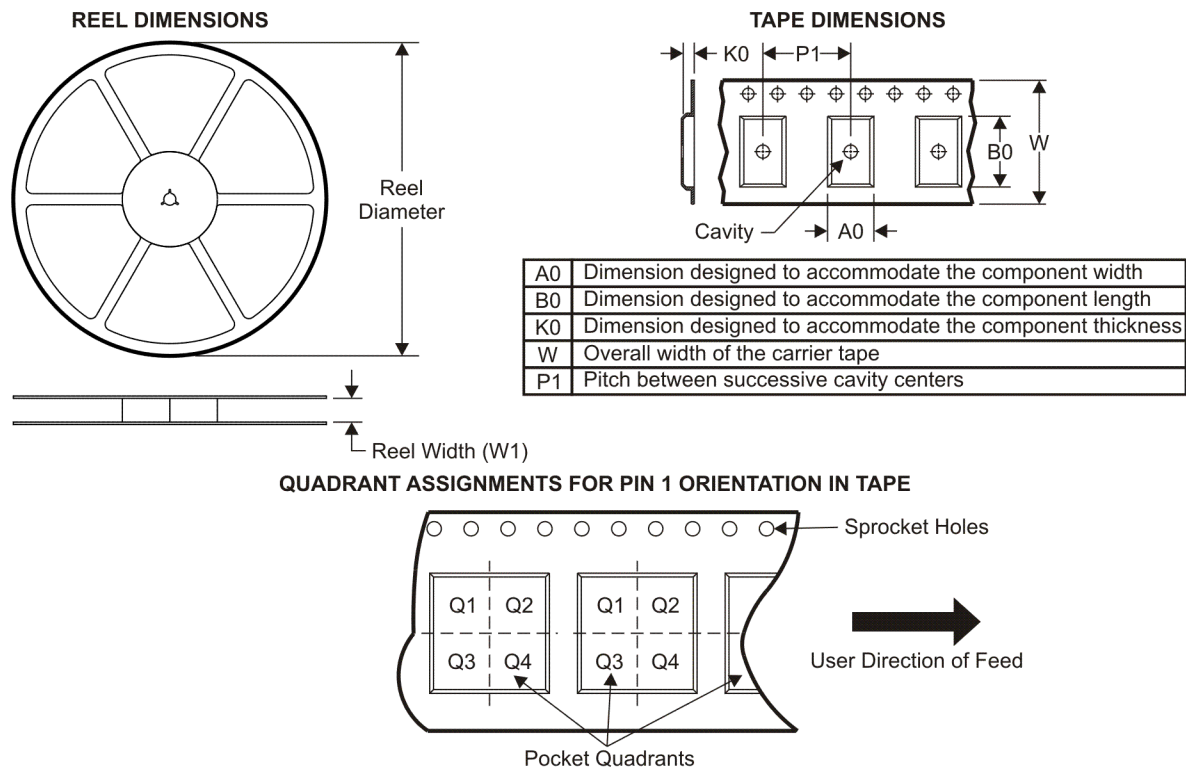
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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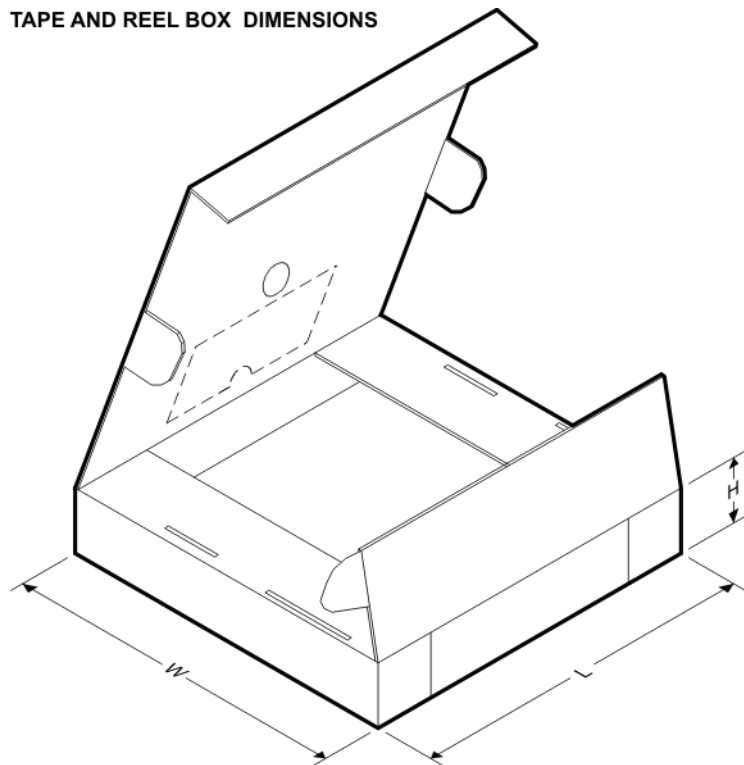
**TAPE AND REEL INFORMATION**



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLC7528CDWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.1    | 2.65    | 12.0    | 24.0   | Q1            |
| TLC7528CPWR | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |
| TLC7528EDWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.1    | 2.65    | 12.0    | 24.0   | Q1            |
| TLC7528IDWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.1    | 2.65    | 12.0    | 24.0   | Q1            |
| TLC7528IPWR | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



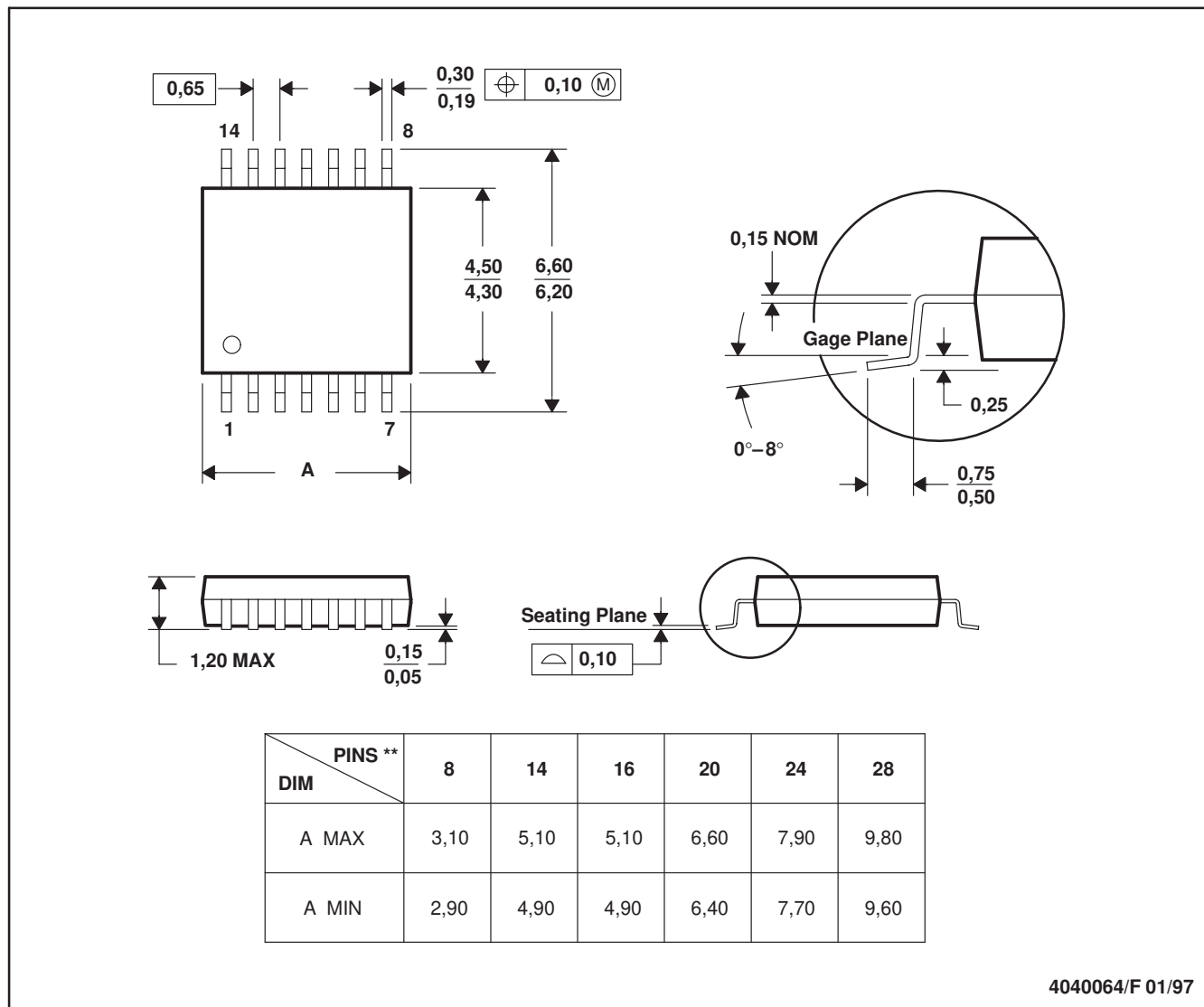
\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLC7528CDWR | SOIC         | DW              | 20   | 2000 | 346.0       | 346.0      | 41.0        |
| TLC7528CPWR | TSSOP        | PW              | 20   | 2000 | 346.0       | 346.0      | 33.0        |
| TLC7528EDWR | SOIC         | DW              | 20   | 2000 | 346.0       | 346.0      | 41.0        |
| TLC7528IDWR | SOIC         | DW              | 20   | 2000 | 346.0       | 346.0      | 41.0        |
| TLC7528IPWR | TSSOP        | PW              | 20   | 2000 | 346.0       | 346.0      | 33.0        |

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



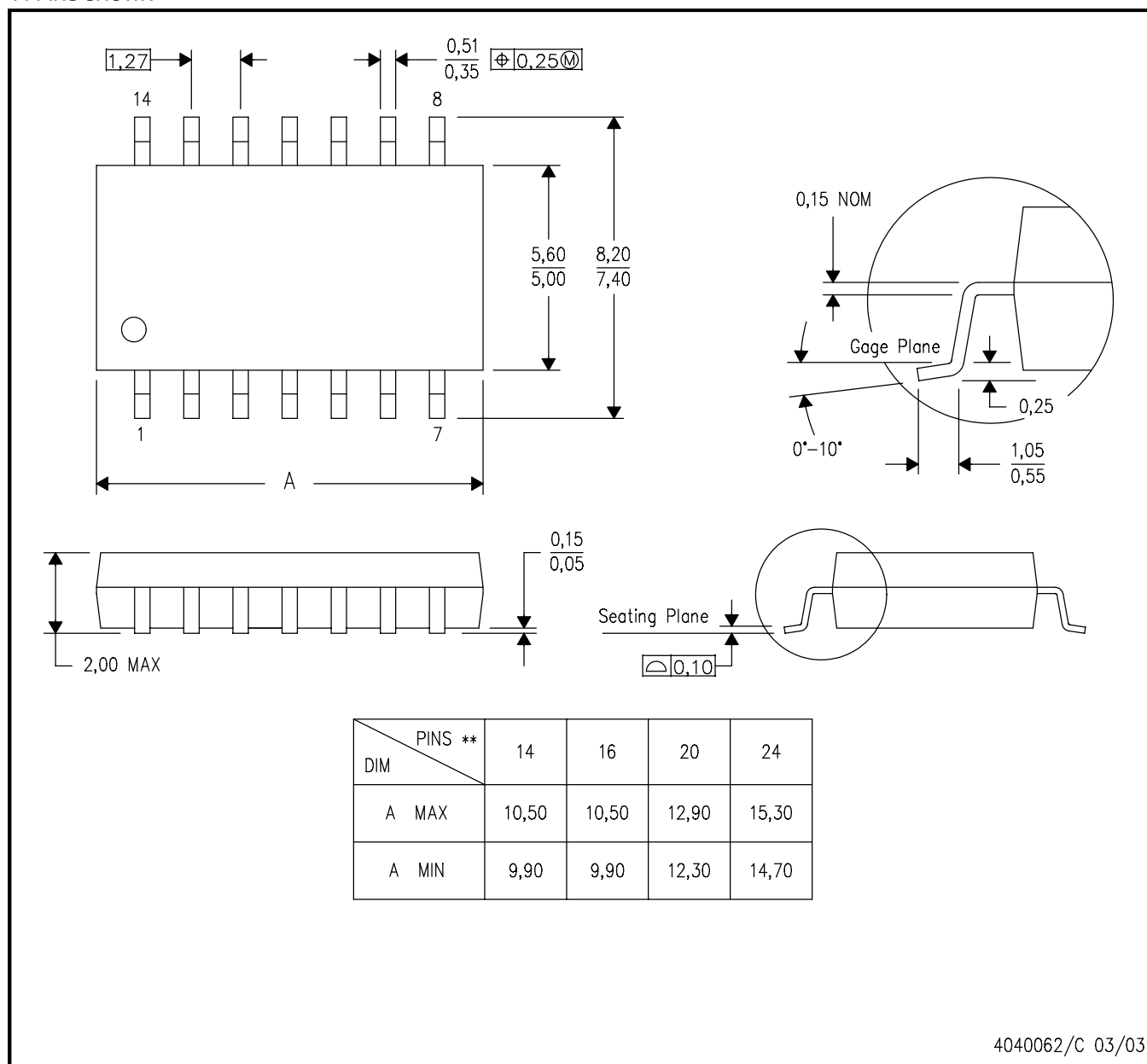
- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

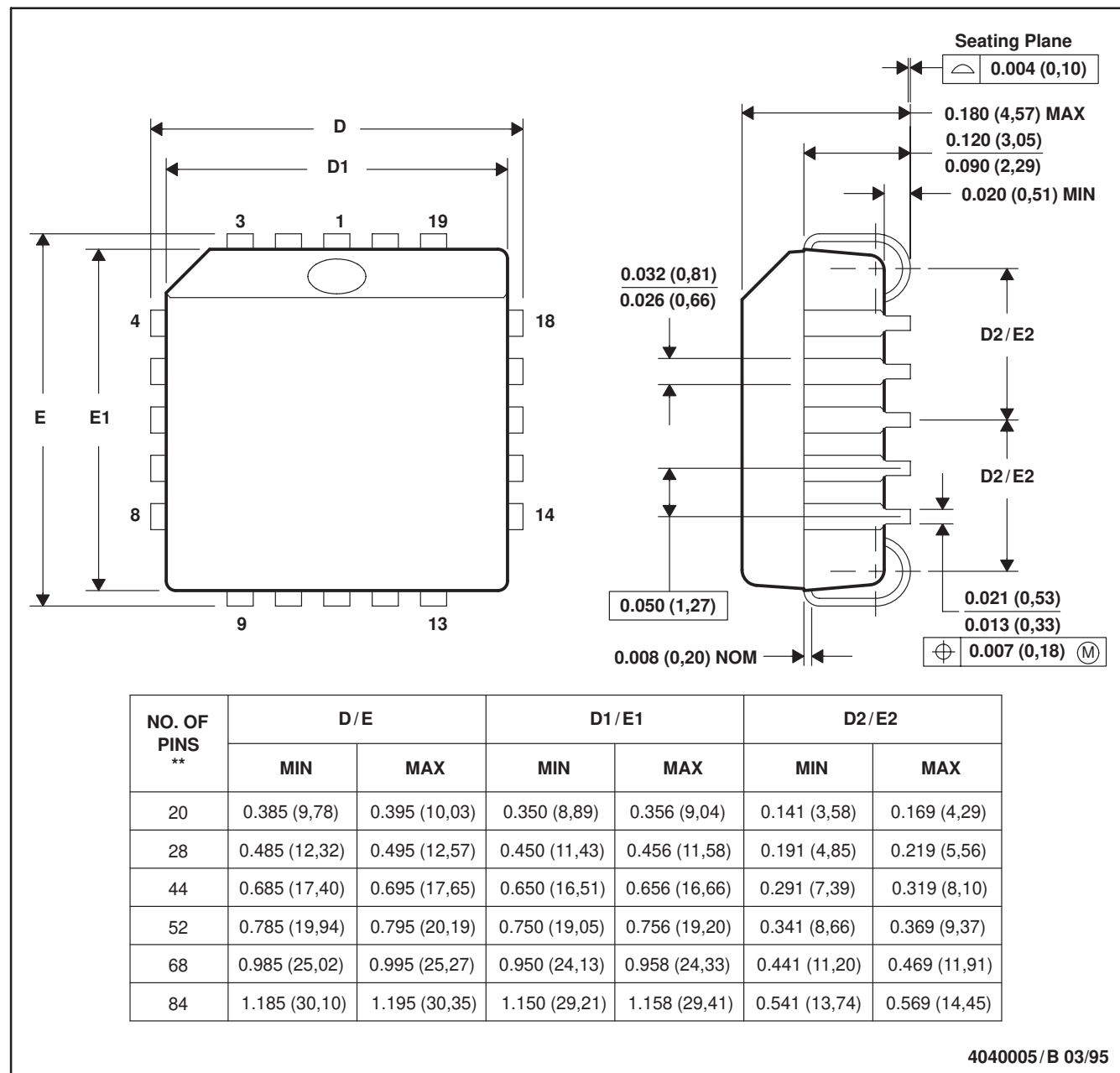


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

FN (S-PQCC-J\*\*)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN

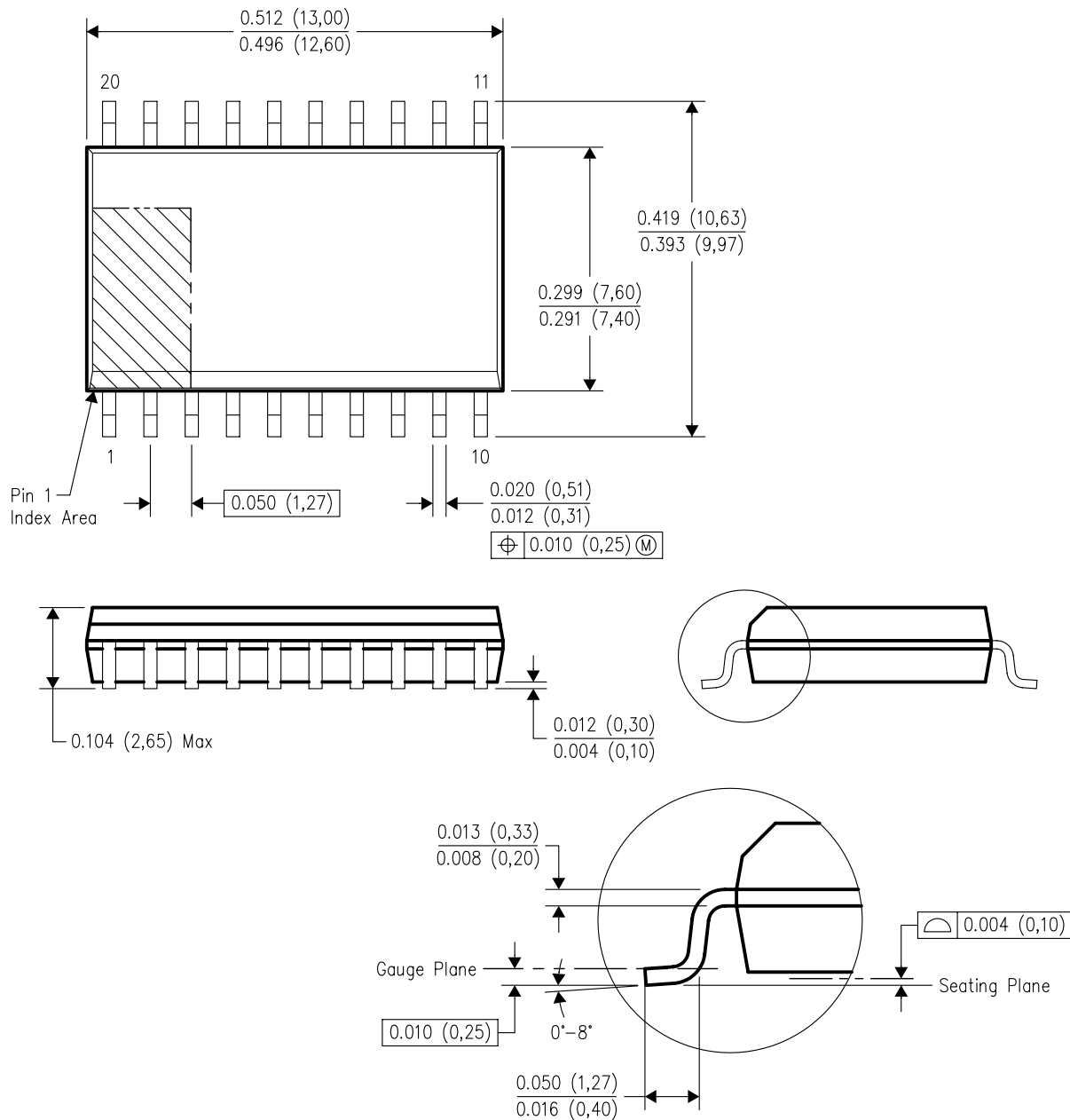


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-018



## DW (R-PDSO-G20)

## PLASTIC SMALL-OUTLINE PACKAGE



4040000-4/F 06/2004

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AC.

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| Interface                   | <a href="http://interface.ti.com">interface.ti.com</a>             |
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| Medical            | <a href="http://www.ti.com/medical">www.ti.com/medical</a>               |
| Military           | <a href="http://www.ti.com/military">www.ti.com/military</a>             |
| Optical Networking | <a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a> |
| Security           | <a href="http://www.ti.com/security">www.ti.com/security</a>             |
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