HEF4585B

4-bit magnitude comparator

Rev. 6 — 21 November 2011 Product data sheet

1. General description

The HEF4585B is a 4-bit magnitude comparator that compares two 4-bit words, A and B, and determines whether A is greater than B, A is equal to B, or A is less than B. Each word has four parallel inputs (A0 to A3 and B0 to B3) with A3 and B3 being the most significant inputs. Three outputs are provided: A greater than B (QA>B), A less than B (QA<B) and A equal to B (QA=B). Three expander inputs (IA>B, IA<B, and IA=B) allow cascading of the devices, to compare 8, 12, 16, ..., bits without external gates.

To operate a single device or a device in the least significant position in a cascaded chain, the expander inputs are connected as follows: IA=B = IA>B = HIGH and IA<B = LOW. All other cascaded devices have IA=B and IA<B connected to QA=B and QA<B respectively of the previous (less significant) device in the chain, while input IA>B is connected to a HIGH (see Figure 6). Operation is not restricted to pure binary code; the devices will work with any monotonic code. Table 3 describes the operation of the device under all possible logic conditions.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from −40 °C to +85 °C
- Complies with JEDEC standard JESD 13-B

3. Ordering information

Table 1. Ordering information

All types operate from −40 °C to +85 °C

Type number	Package		
	Name	Description	Version
HEF4585BP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
HEF4585BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

4. Functional diagram

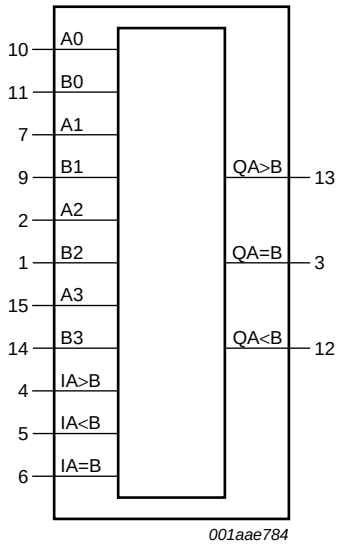


Fig 1. Functional diagram

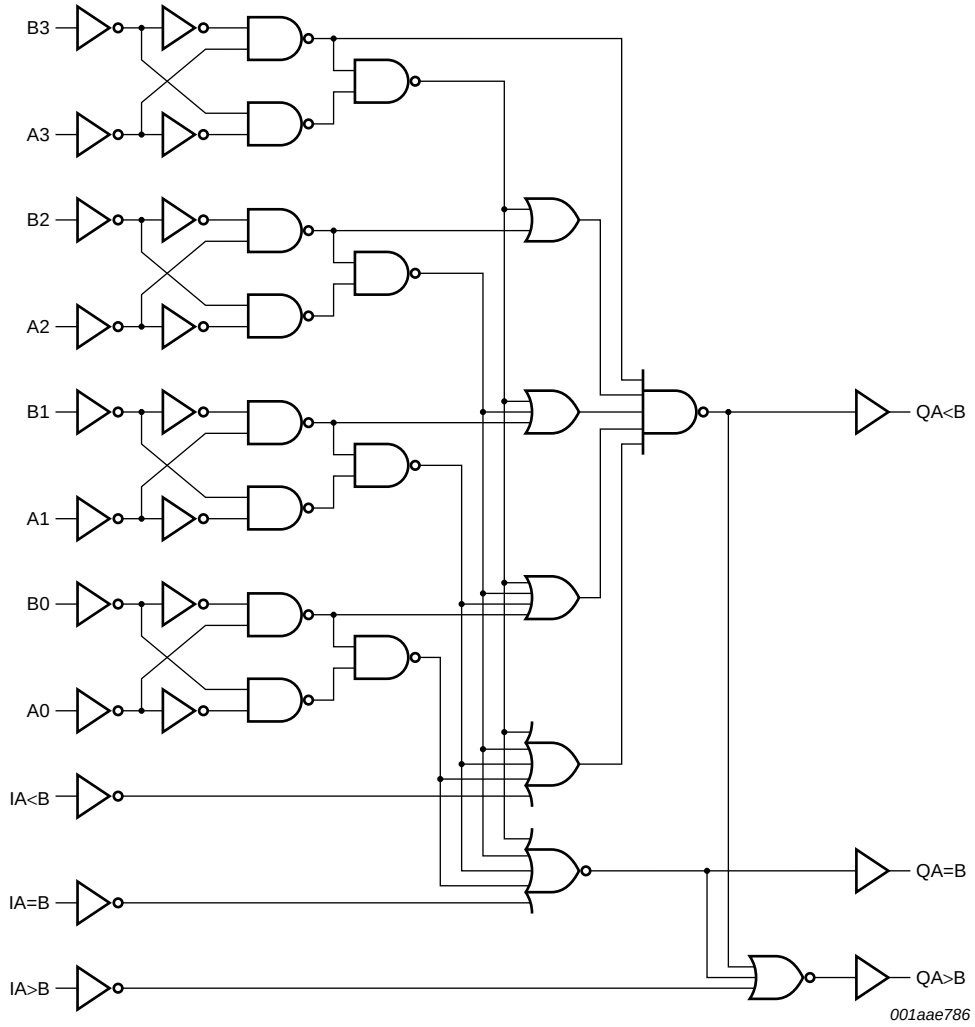


Fig 2. Logic diagram

5. Pinning information

5.1 Pinning

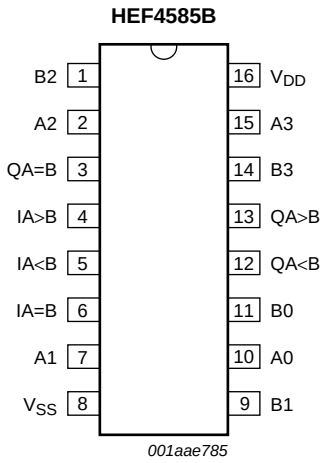


Fig 3. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
A[0:3]	10, 7, 2, 15	word A parallel input
B[0:3]	11, 9, 1, 14	word B parallel input
IA>B	4	expander input
IA=B	6	expander input
IA<B	5	expander input
QA>B	13	A greater than B output
QA=B	3	A equal to B output
QA<B	12	A less than B output
V_{DD}	16	supply voltage
V_{SS}	8	ground supply voltage

6. Functional description

Table 3. Function selection [1]

Comparing inputs				Cascading inputs			Outputs		
A3, B3	**A2, B2**	**A1, B1**	**A0, B0**	**IA>B**	**IA<B**	**IA=B**	**QA>B**	**QA<B**	**QA=B**
A3 > B3	X	X	X	H	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	H	X	X	H	L	L
	A2 < B2	X	X	X	X	X	L	H	L
	A2 = B2	A1 > B1	X	H	X	X	H	L	L
		A1 < B1	X	X	X	X	L	H	L
		A1 = B1	A0 > B0	H	X	X	H	L	L
			A0 < B0	X	X	X	L	H	L
			A0 = B0	X	L	H	L	L	H
				H	L	L	H	L	L
				X	H	L	L	H	L
				[2]					
				X	H	H	L	H	H
				L	L	L	L	L	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

[2] The first 11 lines describe the normal operation under all conditions that will occur in a single device or in a serial expansion scheme. The last 2 lines describe the operation under abnormal conditions on the cascading inputs. These conditions occur when the parallel expansion technique is used.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+18	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V		-	±10	mA
V_I	input voltage			–0.5	$V_{DD} + 0.5$	V
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{DD} + 0.5$ V		-	±10	mA
$I_{I/O}$	input/output current			-	±10	mA
T_{stg}	storage temperature			–65	+150	°C
T_{amb}	ambient temperature			–40	+85	°C
P_{tot}	total power dissipation	DIP16 package	[1]	-	750	mW
		SO16 package	[2]	-	500	mW
P	power dissipation	per output		-	100	mW

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	−40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{DD} = 5 V	-	-	3.75	μs/V
		V_{DD} = 10 V	-	-	0.5	μs/V
		V_{DD} = 15 V	-	-	0.08	μs/V

9. Static characteristics

Table 6. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = −40 °C		T_{amb} = 25 °C		T_{amb} = 85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\|I_O\|$ < 1 μA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$\|I_O\|$ < 1 μA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$\|I_O\|$ < 1 μA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$\|I_O\|$ < 1 μA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	V_O = 2.5 V	5 V	-	−1.7	-	−1.4	-	−1.1	mA
		V_O = 4.6 V	5 V	-	−0.52	-	−0.44	-	−0.36	mA
		V_O = 9.5 V	10 V	-	−1.3	-	−1.1	-	−0.9	mA
		V_O = 13.5 V	15 V	-	−3.6	-	−3.0	-	−2.4	mA
I_{OL}	LOW-level output current	V_O = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V_O = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V_O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I_I	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	μA
I_{DD}	supply current	I_O = 0 A	5 V	-	20	-	20	-	150	μA
			10 V	-	40	-	40	-	300	μA
			15 V	-	80	-	80	-	600	μA
C_I	input capacitance		-	-	-	-	7.5	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

V_{SS} = 0 V; T_{amb} = 25 °C; for test circuit see Figure 5 unless otherwise specified.

Symbol	Parameter	Conditions[1][2]	V_{DD}	Extrapolation formula[3]	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	An, Bn to Qn; see Figure 4	5 V	133 ns + (0.55 ns/pF)C_L	-	160	320	ns
			10 V	54 ns + (0.23 ns/pF)C_L	-	65	130	ns
			15 V	37 ns + (0.16 ns/pF)C_L	-	45	90	ns
		In to Qn; see Figure 4	5 V	83 ns + (0.55 ns/pF)C_L	-	110	220	ns
			10 V	34 ns + (0.23 ns/pF)C_L	-	45	90	ns
			15 V	22 ns + (0.16 ns/pF)C_L	-	30	60	ns
t_{PLH}	LOW to HIGH propagation delay	An, Bn to Qn; see Figure 4	5 V	123 ns + (0.55 ns/pF)C_L	-	150	300	ns
			10 V	49 ns + (0.23 ns/pF)C_L	-	60	120	ns
			15 V	37 ns + (0.16 ns/pF)C_L	-	45	90	ns
		In to Qn; see Figure 4	5 V	93 ns + (0.55 ns/pF)C_L	-	120	240	ns
			10 V	39 ns + (0.23 ns/pF)C_L	-	50	100	ns
			15 V	27 ns + (0.16 ns/pF)C_L	-	35	70	ns
t_t	transition time	see Figure 4	5 V	10 ns + (1.00 ns/pF)C_L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C_L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C_L	-	20	40	ns

[1] Qn is QA>B, QA<B or QA=B

[2] In is IA>B, IA<B or IA=B

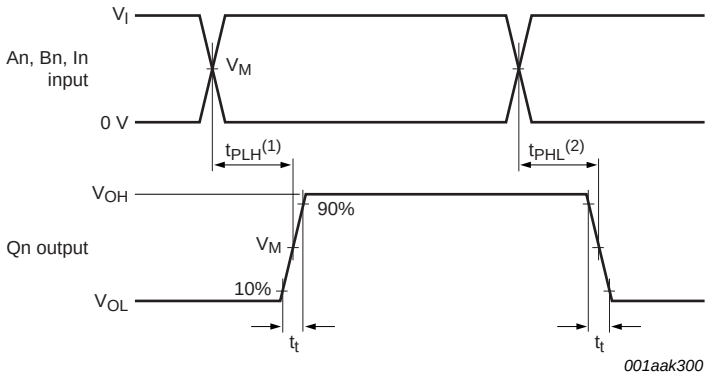
[3] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

Table 8. Dynamic power dissipation P_D

P_D can be calculated from the formulas shown. V_{SS} = 0 V; C_L = 50 pF; $t_r = t_f \leq 20$ ns; T_{amb} = 25 °C.

Symbol	Parameter	V_{DD}	Typical formula for P_D (µW)	where:
P_D	dynamic power dissipation	5 V	$P_D = 1250 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz,
		10 V	$P_D = 5500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_o = output frequency in MHz,
		15 V	$P_D = 15000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	C_L = output load capacitance in pF,
				V_{DD} = supply voltage in V,
				$\Sigma(f_o \times C_L)$ = sum of the outputs.

11. Waveforms

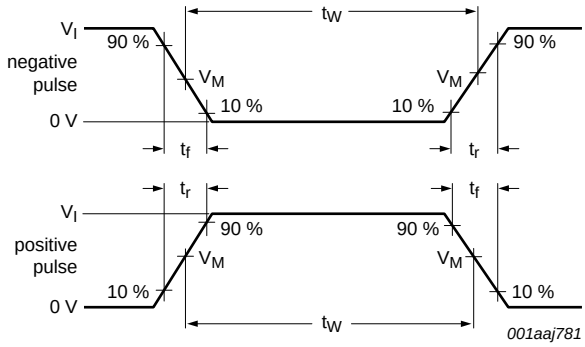


Measurement points shown in Table 9

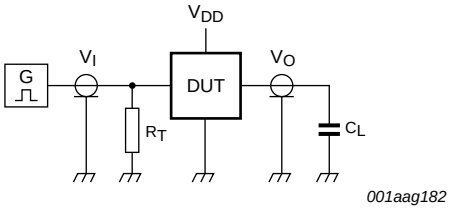
(1) Qn (QA>B, QA<B and QA=B) LOW to HIGH (t_{PLH}) transitions triggered by An, Bn or IA<B, IA>B and IA=B as shown by Table 3.

(2) Qn (QA>B, QA<B and QA=B) HIGH to LOW (t_{PHL}) transitions triggered by An, Bn or IA<B, IA>B and IA=B as shown by Table 3.

Fig 4. Waveforms showing switching times



a. Input waveforms



b. Test circuit

Test data is given in Table 9.

Definitions for test circuit:

DUT = Device Under Test

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig 5. Test circuit for measuring switching times

Table 9. Measurement points and test data

Supply voltage	Input			Load
	V_I	V_M	t_r, t_f	C_L
5 V to 15 V	V_{DD}	$0.5V_I$	≤ 20 ns	50 pF

12. Application information

Some examples of applications for the HEF4585B are:

- Process controllers
- Servo-motor control

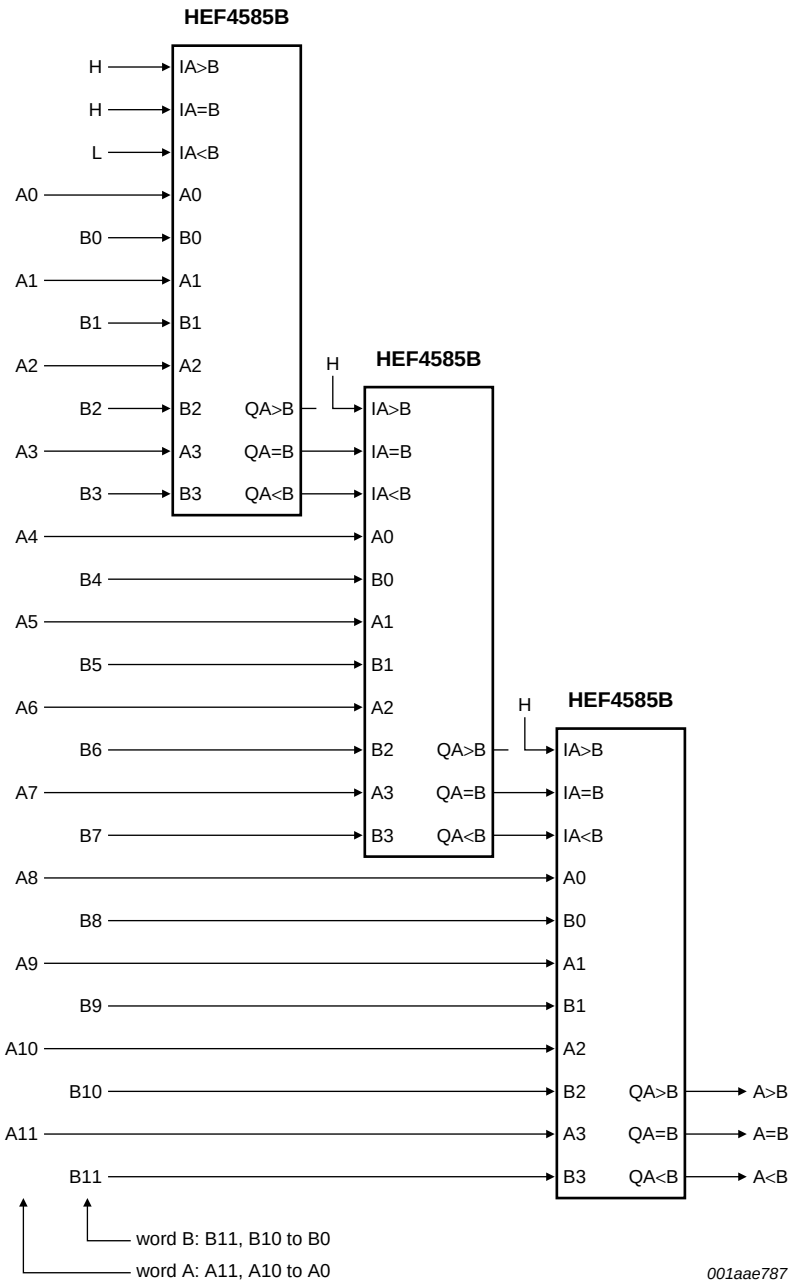
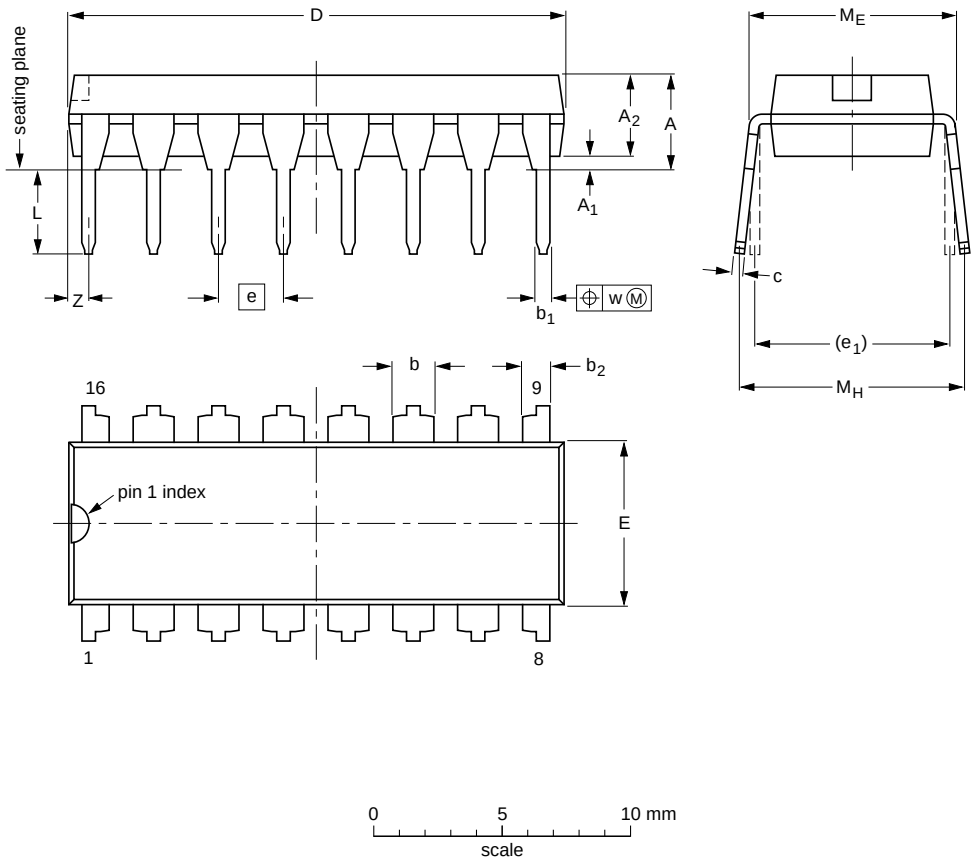


Fig 6. Example of cascading comparators

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

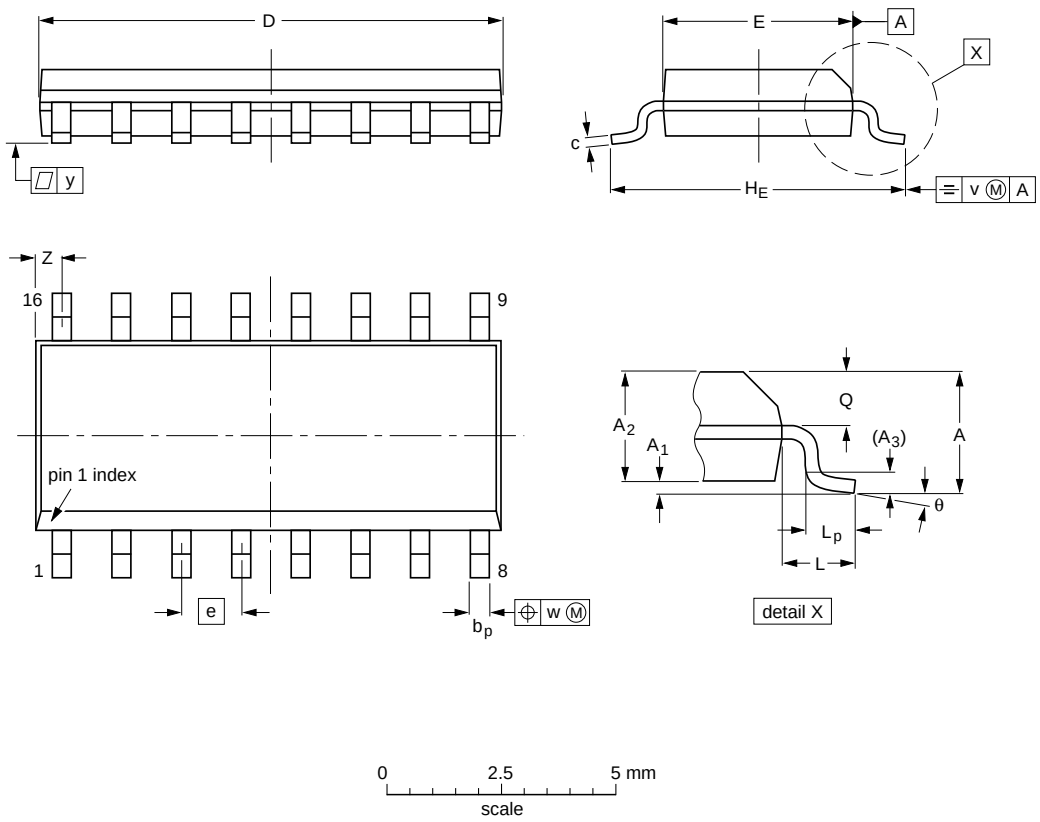
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 7. Package outline 38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

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OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 8. Package outline 109-1 (SO16)

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4585B v.6	20111121	Product data sheet	-	HEF4585B v.5
Modifications:	• Section Applications removed • Table 6: I_{OH} minimum values changed to maximum			
HEF4585B v.5	20091222	Product data sheet	-	HEF4585B v.4
HEF4585B v.4	20090810	Product data sheet	-	HEF4585B_CNV v.3
HEF4585B_CNV v.3	19950101	Product specification	-	HEF4585B_CNV v.2
HEF4585B_CNV v.2	19950101	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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17. Contents

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