EQCO30R5.D: for 3G/HD/SD-SDI Video Cable Equalizer

1.1 Introduction

The EQCO30R5 is a video equalizer for 3G/HD/SD-SDI video with speeds up to 2.97 Gbps. It is designed to be a direct replacement for competing video equalizers. In addition to the downlink functionality from camera to frame grabber, it further allows to transmit from this chip a 5 Mbps uplink signal from frame-grabber to a camera. Further, power can be provided over the same cable using the same chip and a few external components. The device also operates with 8B/10B coded signals up to 3.125 Gbps

1.2 Applications

This solution is useful and economical for many markets and applications, including the following:

- High Definition, high frame rate Pro-video HD/SDI frame store
- Surveillance, industrial/inspection, medical video inputs
- HDcctv applications

1.3 Features

- Long cable reach (Belden1694A):
  - 140m @ 2.97 Gbps
  - 200m @ 1.485
  - 450m @ 270 Mbps
- Compatible with all SMPTE 3G-SDI data-rates
  - SMPTE 259M – SDI - 143 to 360 Mbps
  - SMPTE 344M – 540 Mbps
  - SMPTE292M - HD-SDI – 1.485 Gbps
  - SMPTE372M – dual link HD-SDI – 2.97 Gbps
  - SMPTE424M– dual speed HD-SDI - 2.97 Gbps
- Pin compatible to Gennum and National Semiconductor parts
- Also operates with 8B/10B coding
- Single 3.3 V supply.
- Low Power 220 mW @ 3.3 V (80 mW with 1.2V supply)
- Better robustness due to transmit amplitude independent operation
- -40˚C to + 85˚C temperature range
- 16-pin, 0.65 mm pin pitch, 4 mm QFN package
- Pb-free and RoHS compliant

The EQCO30R5 video equalizer can be used in combination with the EQCO30T5 cable driver. This device also has the capability to receive the uplink signal whilst other key parameters remain complying to the SMPTE specifications. Ask EqcoLogic for the EQCO30T5 datasheet.

1.4 Typical Performance

Table 1 gives an overview of typical performance at room temperature for the video equalizer without using the uplink and without providing power over the same coax. When also providing power or using the uplink communication to the camera, a small length penalty may arise (in cable length, typically 10%) due to added parasitics and noise. The uplink operates to at least 400m at the 5 Mbps bit rate.

Belden

			Broadcast	RG59		
	Name	Belden 7731A	Belden 1694A	Belden 1505A	Belden 1505F	Belden 1855A
	Type	Long distance	Industry standard	Compromis Coax	Flexible	Thinnest cable
Diameter	(mm)	10.3	6.99	5.94	6.15	4.03
270Mbps	(m)	718	469	384	302	270
1.485Gbps	(m)	332	223	187	136	132
2.97Gbps	(m)	219	149	128	89	91

Gepco

			Broadcast	RG59		
	Name	Gepco VHD1100	Gepco VSD2001	Gepco VPM2000	Gepco VHD2000M	Gepco VHM203
	Type	Long distance	Industry standard	Compromis Coax	Flexible	Thinnest cable
Diameter	(mm)	10.3	6.91	6.15	6.15	4.16
270Mbps	(m)	772	502	387	305	273
1.485Gbps	(m)	372	241	187	138	133
2.97Gbps	(m)	252	163	128	91	92

Canare

			Broadcast	RG59		
	Name	Canare L-7CFB	Canare L-5CFB	Canare L-4CFB	Canare L-3CFB	Canare L-2.5CFB
	Type	Long distance	Industry standard	Compromis Coax	Flexible	Thinnest cable
Diameter	(mm)	10.3	6.99	5.94	6.15	4.03
270Mbps	(m)	615	434	344	287	223
1.485Gbps	(m)	281	201	161	135	109
2.97Gbps	(m)	182	132	107	90	73
			Broadcast	RG59		

Table 1: Typical equalization performance

2 Functional Description

2.1 Overview

The EQCO30R5 is a multi-rate adaptive cable equalizer, designed to restore signals received over coaxial cable. The EQCO30R5 chip is optimized for SMPTE HD/SDI signals but works equally well with 8B/10B coded signals. The device operates from a single 3.3V power supply. A sister device operates from a single 1.2V power supply which reduces power consumption at the cost of voltage compatibility with competitive parts. For more information on the 1.2V part please contact EqcoLogic.

The EQCO30T5 is a cable driver that matches to the EQCO30R5 since it can receive the uplink signal. Implementing the uplink requires very few additional components on both sides of the link and complies with the SMPTE specifications. The EQCO30T5 datasheet is available separately from EqcoLogic.

Figure 1 shows a typical communication link using the EQCO30T5 and EQCO30R5 chips:

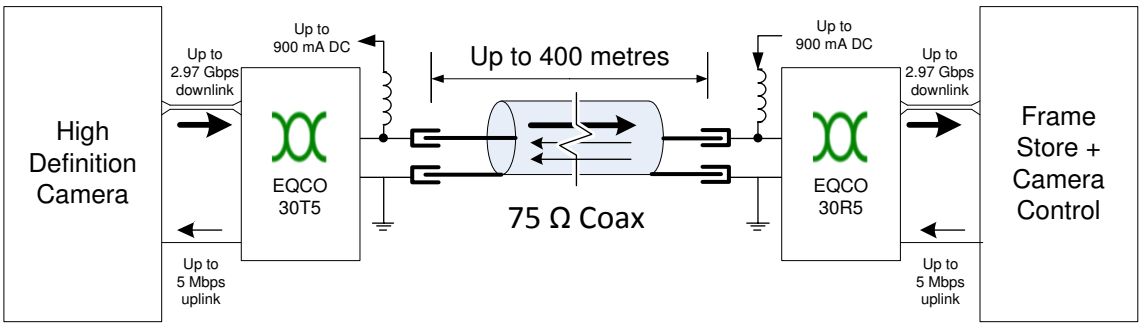

Figure 1: Typical EQCO30R5 set-up

The EQCO30R5 has a DC restore circuit to recover SMPTE pathological patterns in the data stream. The EQCO30R5 has a variable gain to compensate for low frequency attenuation through the coax and variations in transmit amplitude.

Figure 2 shows a block diagram of the EQCO30R5 showing electrical connections:

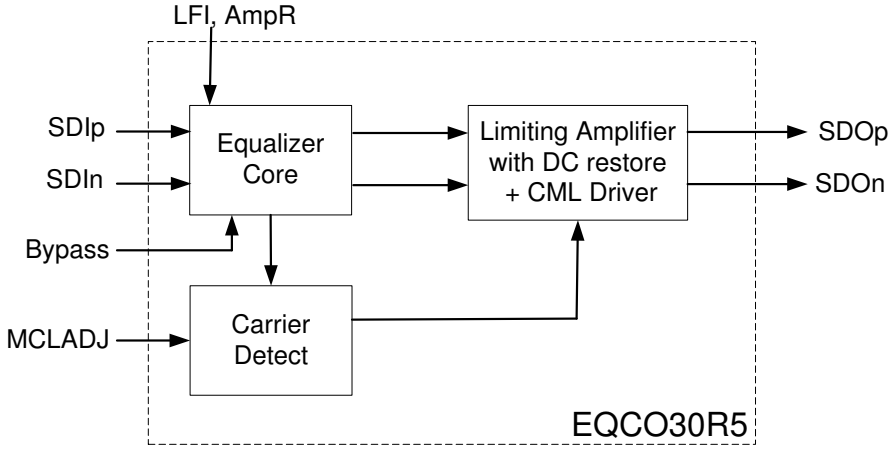

Figure 2: EQCO30R5 block diagram showing electrical connections

2.2 Package and Pinout

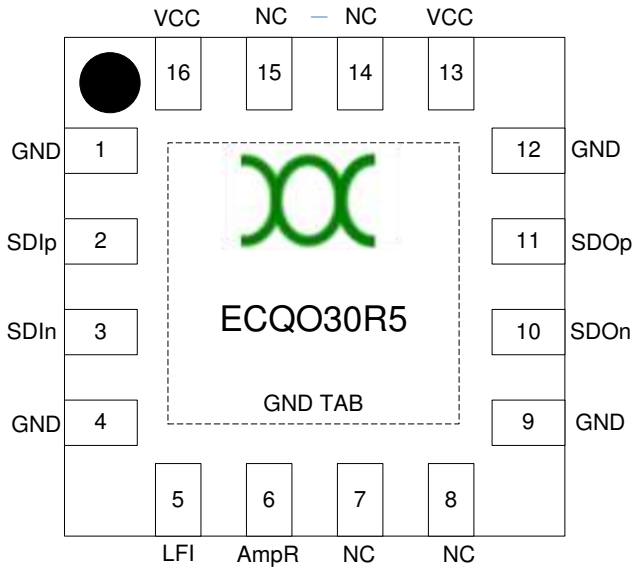

Figure 3: EQCO30R5.D Pin Layout (viewed from top)

2.3 Pin Descriptions

Pin Number	Pin Name	Signal Type	Description
(TAB)	GND	Power	Use as single point Ground
13,16	VCC	Power	+3.3 V of power supply
1,4,9,12	GND	Power	connect to ground of power supply
2,3	SDIp,SDIn	CML Input	Serial Input Positive/Negative Differential serial input, connect SDIn to ground reference via termination network. External 75 Ω termination is required
11, 10	SDOp/ SDOn	CML Output	Serial Output Positive/Negative -Differential serial output. Output has a swing of 2x370 mV and has 50 Ω on-chip termination resistors to internal Vdd (1.2 V).
5	LFI	input	Uplink signal (LOW=0V, HIGH=1.2V). When driving from 3.3V, an external series resistance is required of 6.2 kΩ)
6	AmpR	input	Connect to ground with 1 kΩ resistor, defining the uplink amplitude to 150 mV.
7	NC	input	Do not connect, used for internal testing
8	NC	input	Do not connect, used for internal testing
14	NC	input	Do not connect, used for internal testing
15	NC	input	Do not connect, used for internal testing

Table 2: EQCO30R5 Device Pin List

2.3.1 SDIp/SDIn

SDIp/SDIn together form a differential input pair. It is the differential voltage between these pins that the EQCO30R5 analyses and adaptively equalizes for signal level and frequency response. The equalizer automatically detects and adapts to signals with different edge rates, different attenuation levels and different cable characteristics. Both SDIp and SDIn inputs need to be terminated by an external 75 Ω resistor to GND.

2.3.2 SDOp/SDOn

SDOp/SDOn together form a differential CML pair outputting the reconstructed far end transmit signal. SDOp/SDOn are terminated on chip with 2x50 Ω resistors to 1.2V. These outputs are should be AC coupled to the deserializer (unless a 800mV-1V common mode voltage is acceptable). For SMPTE signals, it is best to use 4.7 μF AC-coupling capacitors.

2.3.3 LFI

The uplink input signal that will be transmitted on the SDIp/SDIn pair. LFI must be a 0-1.2V signal. The pin has internally a resistor of 3.6 kΩ. When driving with 3.3V (2.5V) signal, a resistor of 6.2 kΩ (3.9 kΩ) should be placed in series, close to the equalizer chip. When not using uplink communications, leave this pin floating.

2.3.4 AmpR

Resistor to GND that sets the transmit amplitude of the uplink output driver. Typical value R_{amp} = 1 kΩ for 150 mV transmit amplitude. When not using uplink communications, leave floating.

2.1 Circuit Operation

2.1.1 Equalizer Core

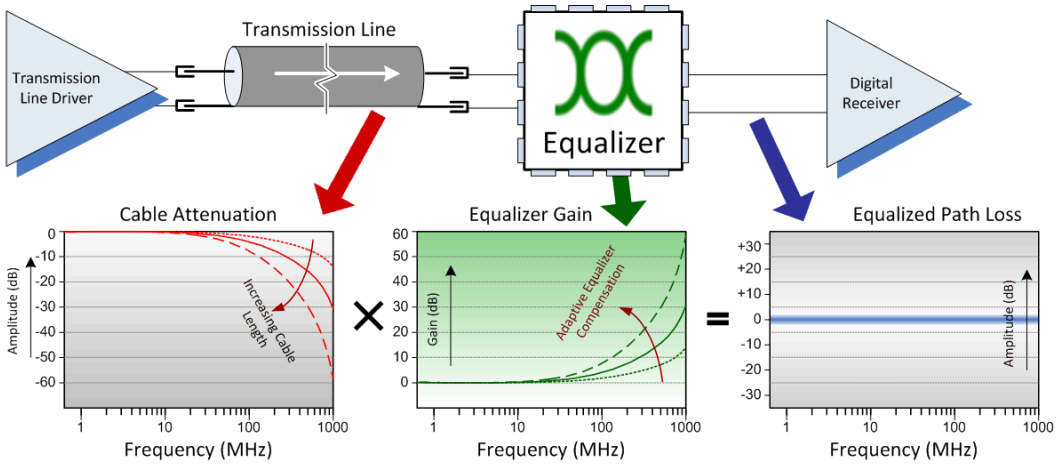

Figure 4: Principal of Equalizer Operation

The EQCO30R5 has an embedded equalizer [1] in the receive path with following characteristics:

- Auto-adaptive

  The equalizer controls a multiple pole analog filter which compensates for attenuation of the cable, as illustrated in Figure 4. The filter frequency response needed to restore the signal is automatically determined by the device using a time-continuous feedback loop that measures the frequency components in the signal. Upon the detection of a valid signal, the control loop converges within a few microseconds.

- Variable gain

  The EQCO30R5 equalizer has variable gain to compensate for low frequent attenuation through the coax and variations in transmit amplitude: this makes the equalizer performance more robust: A large margin for the transmit side amplitude variation is still present at the maximum lengths. Competing devices often only achieve maximum cable length when an exact 800mV is transmitted (and require room temperature, and exact 3.3 V power supply etc…).

- Variable Coax

  The equalizer also behaves in an excellent way receiving attenuated signals from types of cables other than Belden1694A.

- Multi-speed

  The EQCO30R5 works at data rates from 143 Mbps to 2.97 Gbps. With 8B/10B coding, the allowable bit rate is extended from 50 Mbps to 3.125 Gbps.

Example equalizer performance measurements can be found in Appendix 1.

2.1.2 Rx output driver

The output driver converts the output of the equalizer core to a CML-like signal and sends it onto a 100 Ω differential transmission line.

3 Electrical Specifications

3.1 Absolute Maximum Ratings

Stresses beyond those listed under this section may cause permanent damage to the device. These are stress ratings only and are not tested. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Conditions	Min	Typ	Max	Units
Storage Temperature		-65		+150	°C
Ambient Temperature	Power Applied	-55		+125	°C
Operating Temperature	Normal Operation (VCC=3.3 V±5%)	-40		+85	°C
Supply Voltage to Ground		-0.8		+3.6	V
DC Input Voltage		-0.8		+3.6	V
DC Voltage to Outputs		-0.8		+3.6	V
Current into Outputs	Outputs Low			90	mA
Electro Static Discharge (ESD) HBM	JEDEC EIA/JESD-A114A	>2.2			kV
Electro Static Discharge (ESD) contact	IEC 61000-4-2	>4			kV
Latch-Up Current		>100			mA(DC)

Table 3: Absolute Maximum Ratings

3.2 Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit
Power supply					
V_{CC}	Supply Voltage	3.15	3.3	3.45	V
I_s	Supply Current, both transmitting and receiving		55		mA
Operational bit rate					
BR_{smpte}	Bit rate using SMPTE data	0.143		3.0	Gbps
BR_{8B10B}	Bit rate using 8B/10B coded data	0.05		3.125	Gbps
SDIp connection to Coax					
Z_{coax}	Coax Cable Characteristic Impedance		75		Ω
R_{loss}	Coax Return Loss as seen on SDIp pin Frequency range = 1 MHz-1.5 GHz			-15	dB
R_{loss}	Coax Return Loss as seen on SDIp pin Frequency range = 1.5 GHz-3 GHz			-10	dB
ΔV_{TX}	Transmit Amplitude (at camera end into 75 Ω)	500	800	1200	mV
SDOp/SDOn Outputs (CML to 1.2V)					
ΔV_o	Output amplitude $V_{SDOp,n}$ (into 2 x 50 Ω)	2x300	2x 370	2x450	mV
V_{cmout}	Common-mode output voltage when AC coupled		0.83		V

Parameter	Description	Min	Typ	Max	Unit
R_{output}	Termination on SDOp/SDOn to VCC	-	50	-	Ω
t_{rise_o}	Rise /fall time 20% to 80% of $V_{SDOp,n}$	-	75	-	ps
Uplink parameters					
V_{LF}	Uplink transmit amplitude for Ramp = 1 kΩ, measured inside cable	110	150	190	mV
t_{rise_lf}	Rise /fall time 20% to 80% of LF output on SDIp with Ramp = 1 kΩ	30	40	55	ns
V_{ih}	LFI Input HIGH voltage	0.8	-	1.3	V
V_{il}	LFI Input LOW voltage	-0.5	-	0.4	V
R_{input}	Internal resistor to GND	-	3.6	-	kΩ

Table 4: Electrical Characteristics (Over the Operating VCC and -40 to 85 ^{o}C Range)

3.3 Jitter Numbers

Parameter	Conditions	Min	Typ	Max	Units
Jitter in equalizer output	2.97 Gbps Belden 1694A: 0-120m	-	-	0.25	UI
"	2.97 Gbps Belden 1694A: 120-140m	-	0.3*	-	UI
"	1.485 Gbps Belden 1694A: 0-160m	-	-	0.25	UI
"	1.485 Gbps Belden 1694A: 160-200m	-	0.3*	-	UI
"	270 Mbps Belden 1694A: 0-400m	-	-	0.2	UI
Additive jitter on LF output	8B/10B coded signal at 5 Mbps over full VCC and temperature range.	-	-	10	ns
DCD in LF output	8B/10B coded signal at 5 Mbps over full VCC and temperature range.	-	-	10	ns

Table 5: Jitter numbers (over operating VCC range at -40 to +85 ^{o}C, and full ΔV_{TX} range with pathological patterns)
(*=over operating VCC range @ 25 ^{o}C, and ΔV_{TX} +/- 10 %)

4 Package Drawing

A 16 pin Micro Lead frame Package (MLP) also known as Quad Flat No Lead (QFN) package is used. The package outline conforms to JEDEC MO-220.

Dimensions in Figure 5 and Figure 6 are in millimeters.

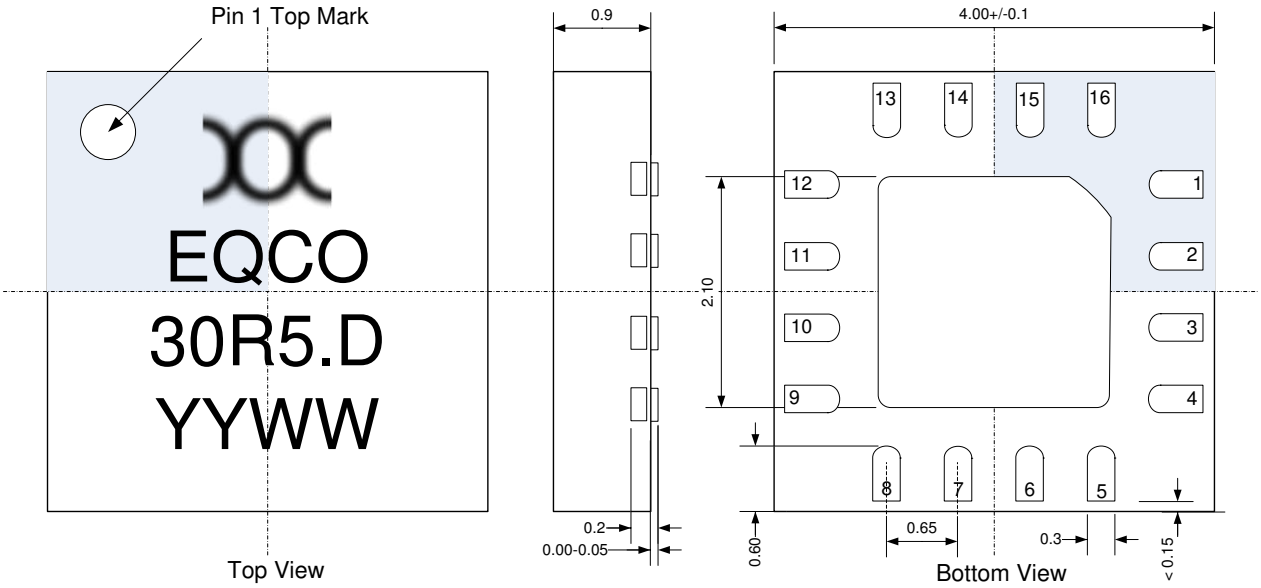

Figure 5: Package Drawing

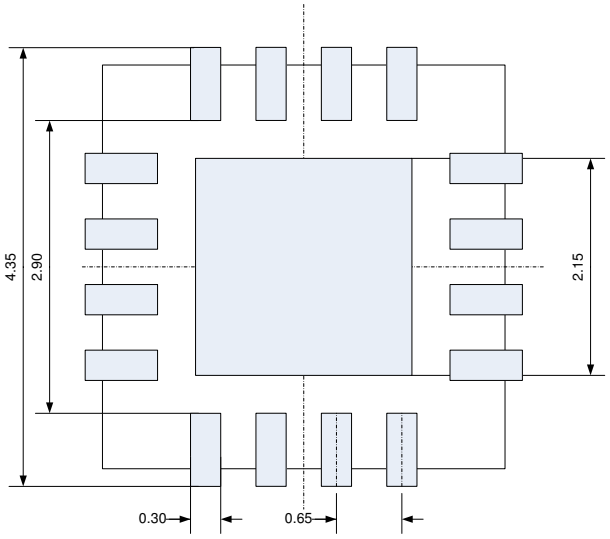

Figure 6: Recommended PCB Footprint

5 Application Information for SMPTE

5.1 Typical Application Circuit

Figure 7 illustrates a typical schematic implementation of the EQCO30R5 used as equalizer for SMPTE video signals:

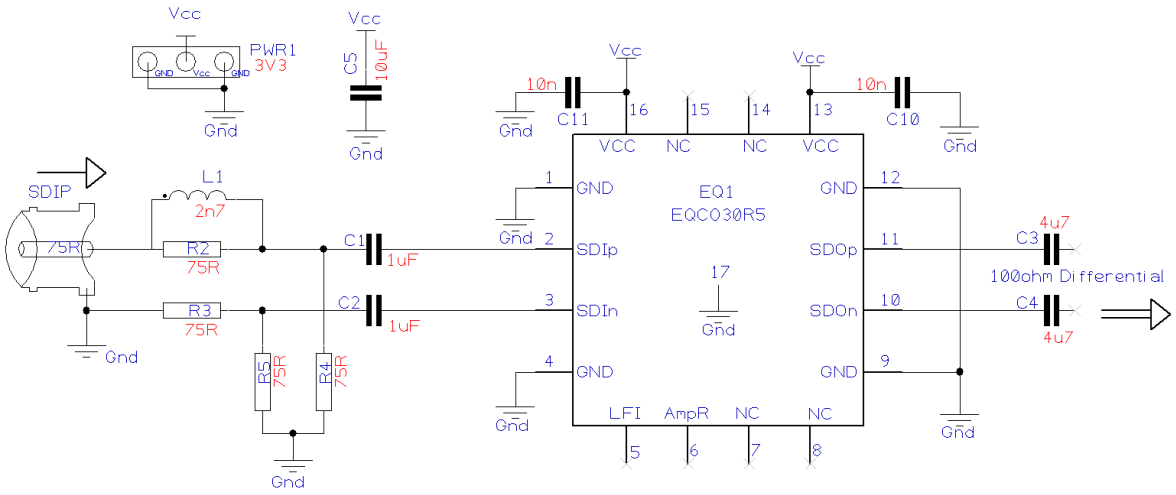

Figure 7: EQCO30R5 as video equalizer typical application circuit

5.1.1 Return loss network

For optimal return loss an external return loss network is needed. The value of R2 and R3 is 75Ω, the value of L1 is 2.7nH.

5.1.2 Guidelines for PCB layout

All components in the high speed signal path shall be 0402 size for minimal parasitic effects.

The transmission line between the BNC connector and the return loss network (R4, L1) shall be a 75Ω single ended transmission line. Component B is a 75Ω resistor, component L1 is a 2.7nH inductor. Component R6 is the 75Ω termination resistor to GND. Component E is the AC coupling capacitor connected to the input of the chip. 2 decoupling capacitors (C5) are placed between VCC and GND, close to the chip. The output of the chip is connected to the deserializer or FPGA with a 100Ω differential transmission line. To minimize unwanted parasitic effects a cutout of the ground and power plane is made underneath capacitors C6 and underneath the input pins of the EQCO30R5 chip.

Figure 8 shows a recommended layout for the EQCO30R5 implementation.

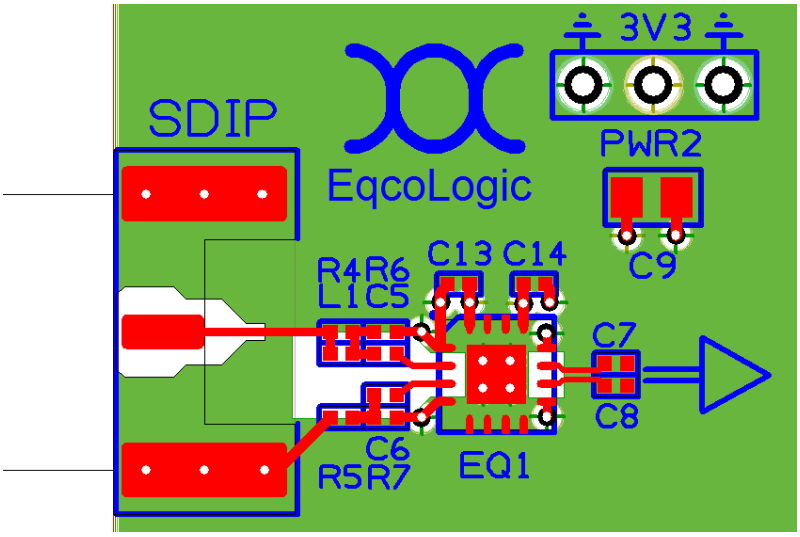

Figure 8: Recommended PCB layout for EQCO30R5

6 Application Information for bidirectional link

6.1 Typical Application Circuit

Figure 9 illustrates a typical schematic implementation [2] of the EQCO30R5 when used in a bidirectional link, including low speed uplink and power supply transmission over a single coax:

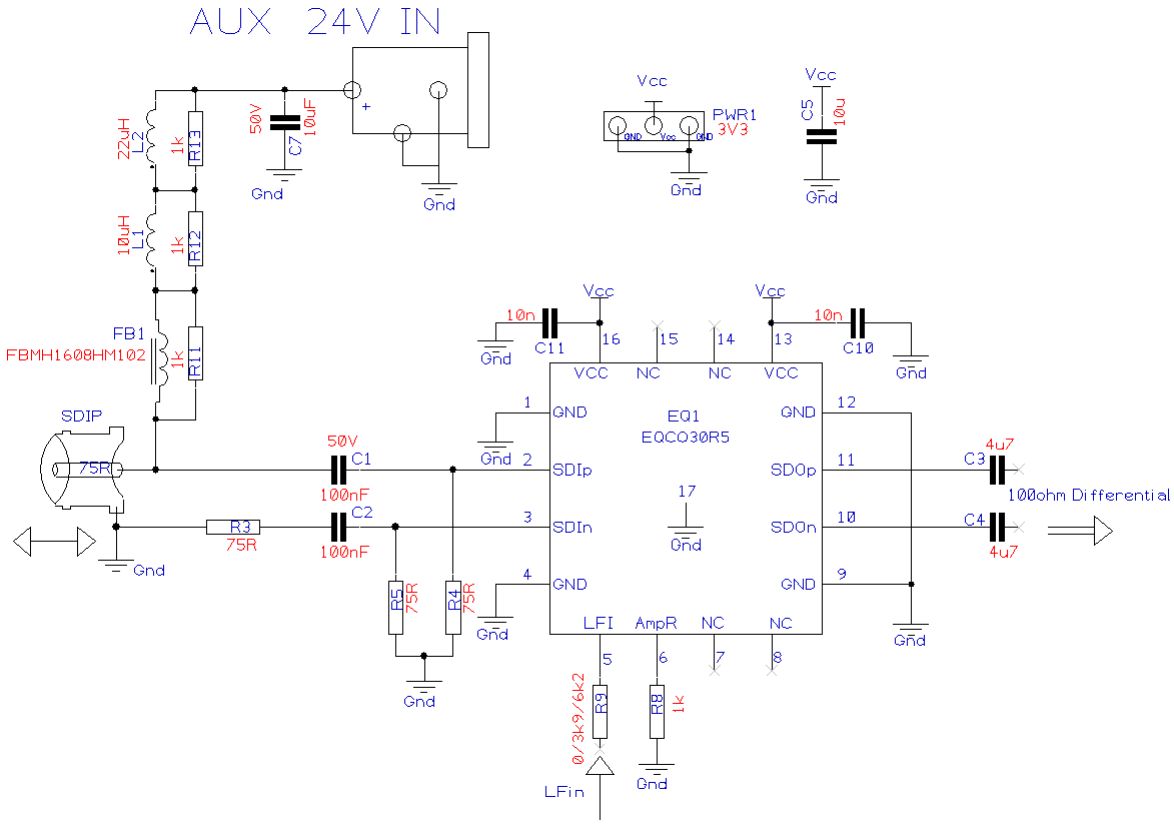

Figure 9: EQCO30R5 in bidirectional link (including power supply transmission)

6.1.1 Component recommendation

Ferrite Beads Fb1= FBMH1608HM102 from Taiyo Yuden

Inductor L1 = 1812PS_103 from Coilcraft

6.1.2 Bidirectional link in SMPTE applications

When using the bidirectional link with power supply transmission the components (FB1, L1 and L2) and layout around this components are very critical, changes in the design or components may result in decreased or performance.

6.1.3 PCB layout

All components in the high speed signal path shall be 0402 size for minimal parasitic effects.

Figure 10 shows a recommended layout for the EQCO30R5 with uplink and power over coax.

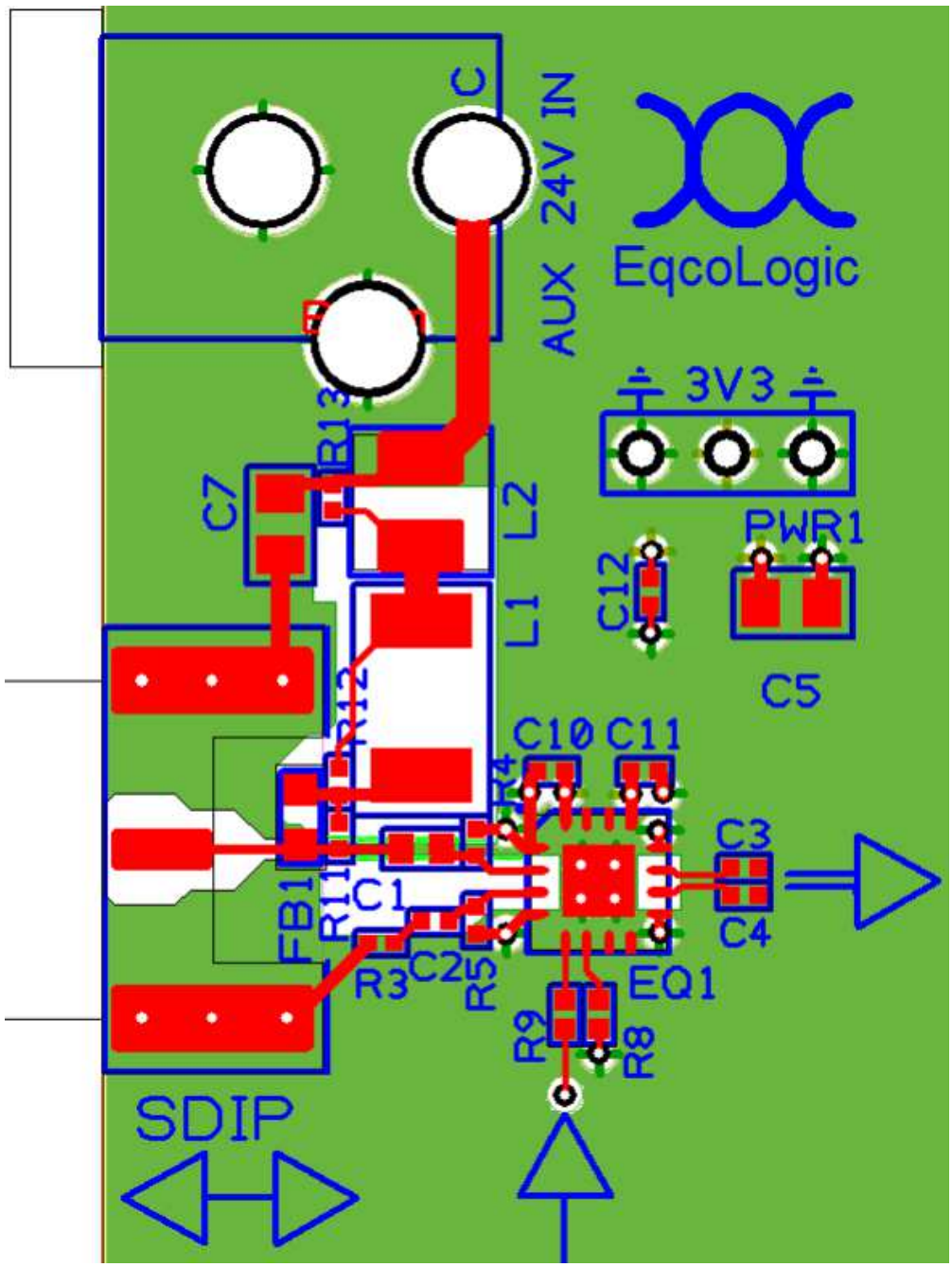

Figure 10: EQCO30R5 in bidirectional link PCB layout

7 Document Control

7.1 Version History

Version	Date	Author	Comments
1V0	27 Jan 2014	A.Peeters	Finalizing document
0v2	27 June 2013	A. Peeters	Revision
0v1	23 November 2011	B.Devuyst	New document

7.2 Document References

[1] Patents: US7894515B2 & EP2182688B1
[2] Patents pending: EP12174398.3, US20110103267A1, EP12153028.1, EP2648378A1 & US2013/301483A1

7.3 Disclaimer:

EQCOLOCIC MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Eqcologic reserves the right to make changes without further notice to the materials described herein. Eqcologic does not assume any liability arising out of the application or use of any product or circuit described herein. Eqcologic does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Eqcologic's product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Eqcologic against all charges.

EqcoLogic NV
c/o ETRO/VUB dept.
Pleinlaan 2
1050 Brussels

Phone: +32 2 629 1301
Email: techsupport@eqcologic.com
www: www.eqcologic.com

Appendix: Typical Equalizer Characteristics

All measurements at VCC = 3.3 V, Temp = +25 ºC, data pattern = prbs15 (including 20 µs of each polarity of pathological pattern), measured with Belden 1694A cable

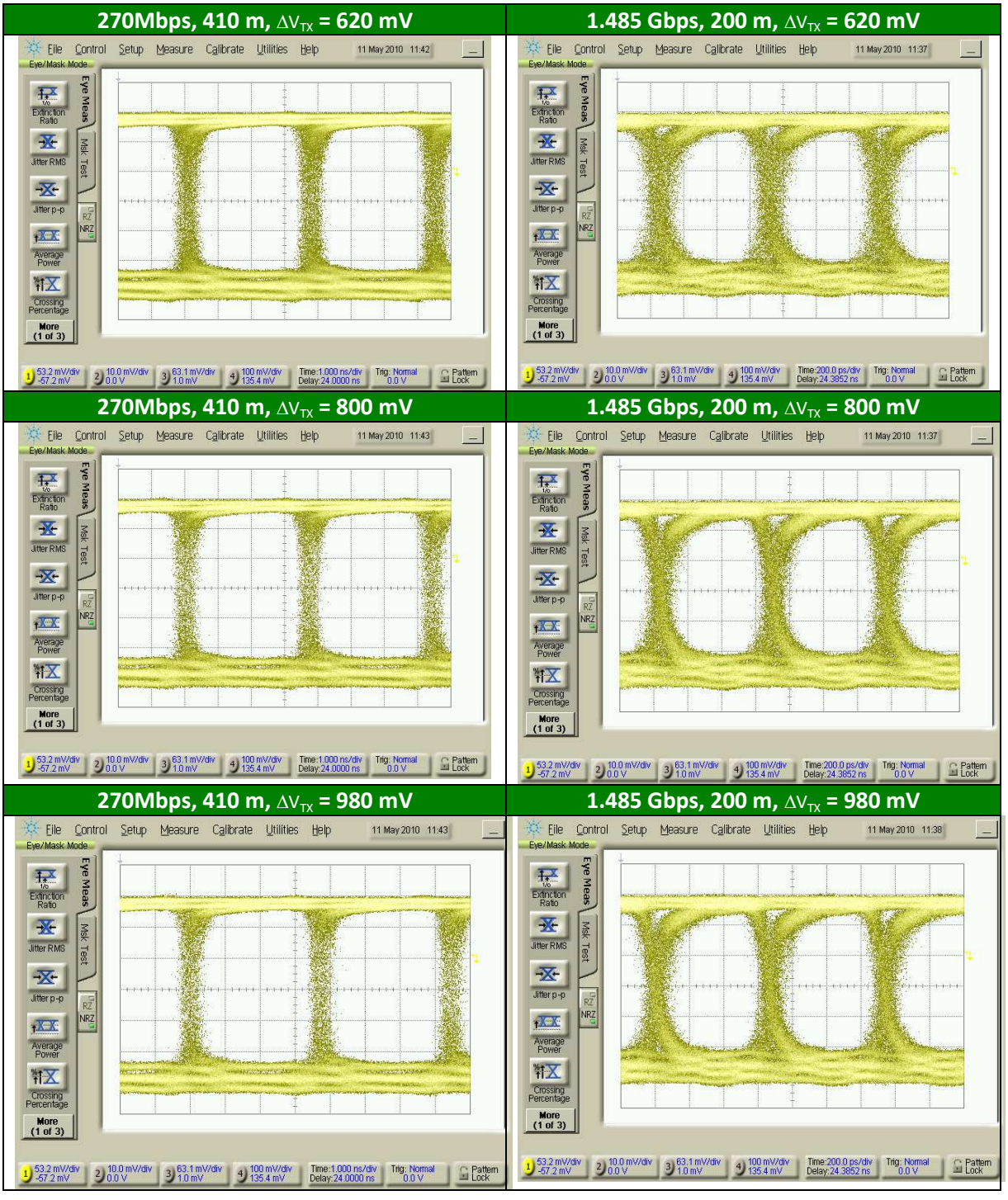

Figure 11: Typical equalizer performance at room temperature for different speeds.

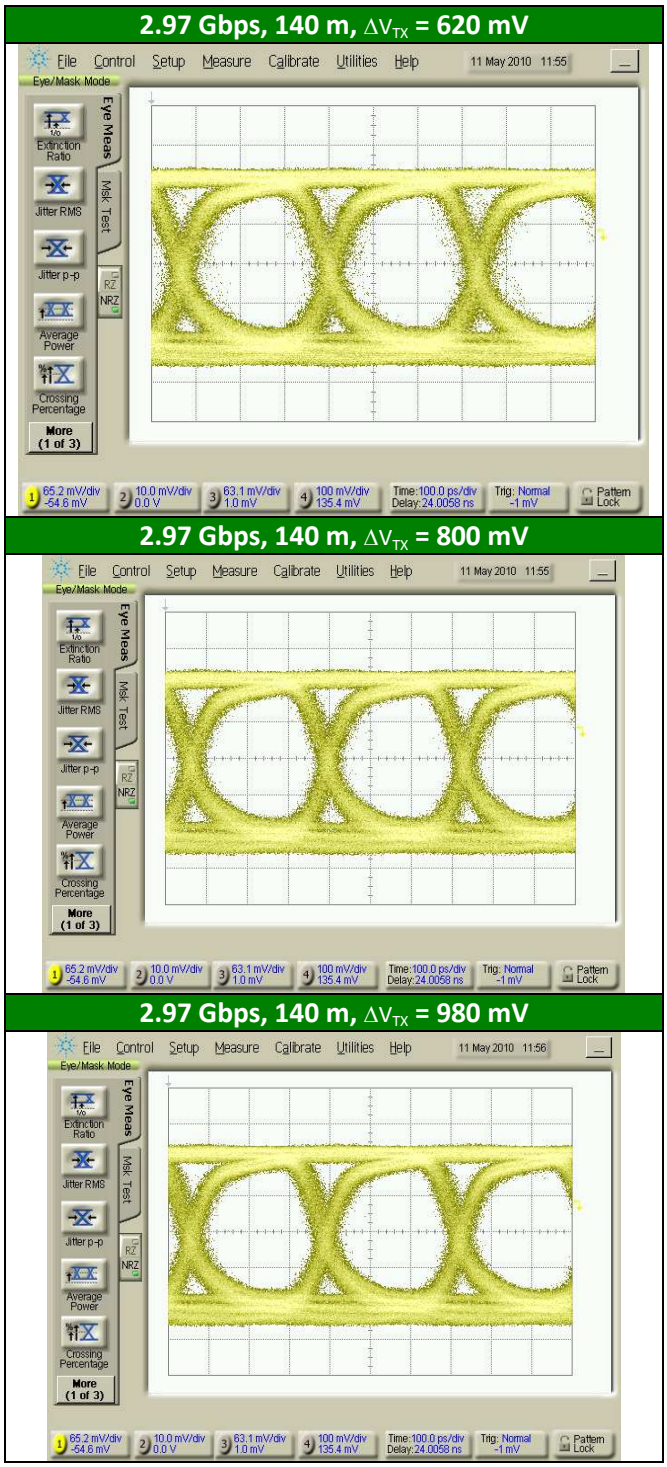

Figure 12: Typical equalizer performance at room temperature @ 2.97 Gbps.

