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Fairchild Semiconductor
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IEEE 1284 Interface Design Solutions

Applications note supporting the 74ACT1284, 74VHC161284 and 74LVX161284 devices

Introduction

The IEEE 1284 standard for high speed bi-directional peripheral data interface allows for significantly higher (2MB/sec) data throughput than previously possible. Fairchild Semiconductor offers several devices designed to support PC and PC peripherals that implement the IEEE 1284 protocol. This applications note discusses the IEEE 1284 standard, Fairchild's IEEE 1284 transceivers, and some application examples.

An Advanced Standard Built on a Legacy Interface

The IEEE 1284-1994 standard, "IEEE Standard Signaling Method for a Bidirectional Parallel Peripheral Interface for Personal Computers", describes the electrical criteria for implementing high-speed, bidirectional data transfers using standard parallel port-based protocols. Until the inception of IEEE 1284, a standard for bidirectional interface transfers had been absent in the computer industry. Since 1981 the standard parallel port (SPP), also known as the Centronics port, for PCs and PC peripherals has used a variety of slow and cumbersome electrical and software configurations. Many SPP applications possess unique implementations that render them non-standard, incompatible solutions.

IEEE 1284 describes criteria for asynchronous, interlocked, bidirectional data transfers with compatibility to older SPP modal protocols. Designs that accommodate the IEEE 1284 protocol have the potential for substantial performance increases. The 1284 standard documents the requirements that are necessary to create a new and comprehensive generation of advanced peripheral devices. As 1284-compliant devices displace older, non-compliant designs, the antiquated, unidirectional method of transferring data between the personal computer and peripheral will disappear.

Interface Modes

Five signaling modes are described in the IEEE 1284 standard. Three of these -- compatibility, nibble, and byte -- are SPP-associated legacy modes. The compatibility mode is supported by 1284-compliant devices and is the basis for detection and selection of advanced modes. There are two advanced modes -- enhanced parallel port (EPP) and the extended capabilities port (ECP). The ECP and EPP modes were the primary impetus for development of the IEEE 1284-1994 standard.

The 1284-compliant interface provides:

- Bidirectional extension to the personal computer parallel port
- Backward compatibility with the older, standard parallel port (SPP)
- Negotiation to ECP and EPP modes using Compatibility mode
- Interpretation of signals based on the currently selected mode of operation
- Increased interface performance

The Advanced Bidirectional Modes

The first truly bidirectional mode, EPP, was co-developed by Xircom, Inc. and Zenith Data Systems. Intel Corporation later implemented EPP in its 386SL chipset. EPP was the first to turn the SPP, also known as the Centronics port, into a high-speed bidirectional interface. EPP initiates four types of transfer cycles: data read/write and address read/write. It also uses asymmetric (level 1), bidirectional signaling driven by a host state machine. The state machine releases the PC's processor from directing the interface negotiation and other signaling chores.

ECP, proposed by Hewlett-Packard and Microsoft, was initially defined as an advanced method for communicating with printer and scanner peripherals. Today, a broad variety of peripherals use the ECP protocol. Unlike the pre-existing SPP method of combining compatibility and byte modes to achieve bidirectionality, ECP provides symmetric (level 2) bidirectional signaling without the requirement of switching between two modes. Another advantage of ECP is single-byte, run-length encoding (RLE). When dealing with rasterized images, RLE allows compression of identical bytes for higher data throughput. ECP also uses FIFO (first-in/first-out) technology and the dynamic memory access (DMA) system to more efficiently manage data streams.

Significant increases in interface performance are achieved with ECP and EPP modes. Both modes use half-duplex data communication whereby information can be transmitted in either direction, one direction at a time. By using half-duplex communication, ECP and EPP data transfer speeds can reach 2MB/s on an ISA bus and 10MB/s on the PCI. This is many times faster than the typical 150KB/s data transfers that are possible on the SPP.

The ECP and EPP modes require a host hardware state machine that automatically generates the control strobes that are necessary for cyclic I/O data transfers. Although there are differences in how protocols are implemented, both modes use fully interlocked signaling for word-length transfers within a single I/O cycle.

In order to attain the greater bandwidths afforded by ECP and EPP, system designers must insure an interface that is properly designed. Design imperatives for a 1284-compliant interface include:

1. Preservation of signal fidelity
2. Ability to drive IEEE prescribed 10-meter cable lengths
3. Rejection or reduction of input noise phenomenon
4. Immunity to electrical overstress and ESD (electrostatic discharge)

IEEE 1284 Interface Transceivers

Fairchild Semiconductor's IEEE 1284 transceivers are designed to drive and receive 1284-compliant signals across the parallel port. Fairchild offers three 1284-compliant transceivers: 74ACT1284, 74VHC161284, and 74LVX161284. The VHC and *CROSSVOLT*™ LVX advanced transceivers incorporate additional features relative to the 74ACT1284. These features include design enhancements that make the VHC and LVX devices easier to use. For example, termination resistors that are integrated into the outputs eliminate the need for an external termination network. This reduces the board space requirement, and simplifies port design and printed circuit layout. Also, the 74LVX161284, operating at 3.3V, is the first low voltage 1284-compliant transceiver with over-voltage tolerance.

74ACT1284

Introduced in 1994, the FACT™ 74ACT1284 was the first 1284-compliant, stand-alone transceiver. It is the predecessor to the VHC and LVX enhanced devices. Limited bit-breadth necessitates the use of up to three 74ACT1284 transceivers for full implementation of an IEEE 1284 port. Although still widely used, the 74ACT1284 lacks the number of signal paths necessary for a single-chip solution. Additionally, the 74ACT1284 does not incorporate integrated termination resistors. For applications that do not require the bit-breadth found on the VHC and LVX devices, the 74ACT1284 may be an ideal solution.

74ACT1284 Features:

- Level 1 and 2 signaling support
- 5V +/- 10% V_{CC} operation
- 14 mA B Port cable-side sink/source capability
- Guaranteed 350mV minimum hysteresis
- B Port outputs assume high impedance state during power-down
- TTL-compatible inputs
- FACT low CMOS power consumption
- SOIC and SSOP packaging

74VHC161284

The 74VHC161284 provides 8 bidirectional and 11 unidirectional paths. Hence, it is a single-chip solution for implementing a 1284-compliant port design. The VHC transceiver operates at 5 Volt nominal levels. Outputs on the cable-side can be configured for either open-drain NMOS or high-drive CMOS on the B Port. There are pull-up and series termination resistors at the outputs on the cable-side of the VHC transceiver. These resistors have a guaranteed range for termination of the interface cable medium.

74VHC161284 Features:

- Replaces up to three 74ACT1284 devices
- Level 1 and 2 signaling support
- On-board IEEE 1284 cable termination resistors
- B and Y output resistance optimized for driving IEEE 1284 prescribed cable
- B and Y outputs assume high impedance mode during power down
- 5V +/- 10% V_{CC} operation
- 14mA B Port cable-side sink/source capability
- Guaranteed 800mV hysteresis on control inputs
- I/Os on cable-side have integrated pull-up resistors
- Flow-through packaging pin configuration
- Single-chip solution

74LVX161284

The *CROSSVOLT* LVX161284 is a low voltage (3.3V +/- 10% V_{CC}) IEEE 1284 transceiver with TTL-input thresholds. Like the 74VHC161284, this device contains 8 bidirectional data buffers and 11 control and status buffers for accommodation of all prescribed IEEE 1284 signals. Package pin configurations are optimized for flow-through data from the peripheral (A-side) to the host PC (B-side). IEEE 1284-specified pull-up and series termination resistors are included on the device at the outputs on the cable-side B Port. These terminators are optimized for driving an IEEE 1284 cable. Outputs on the cable-side B Port can be configured to either an open-drain NMOS or high-drive CMOS format.

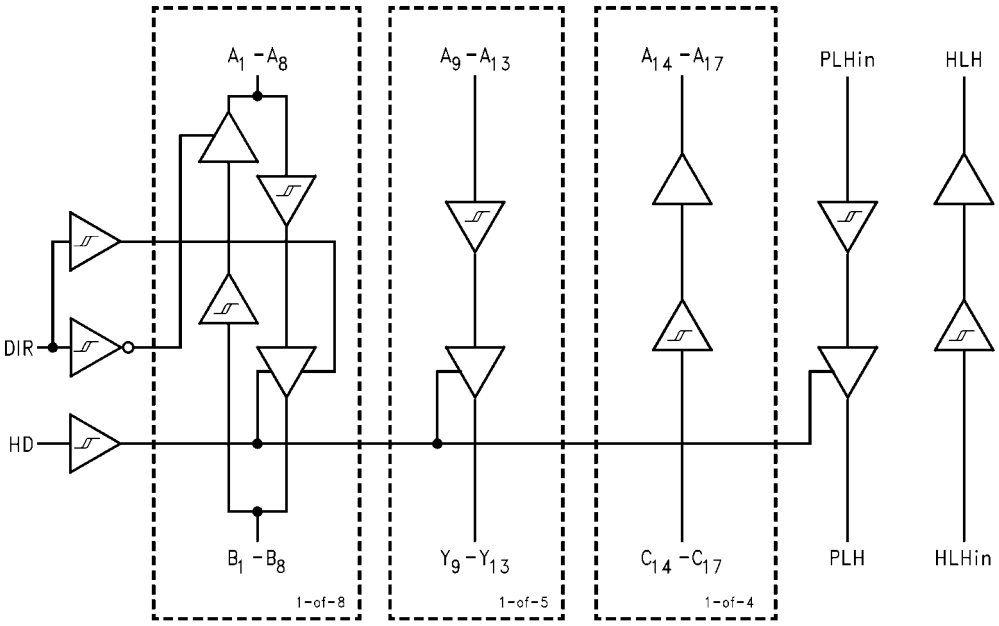
The cable-side B Port can be connected to a separate power supply via pull-ups. This allows outputs to be driven by a higher supply voltage compared to the A Port. In addition, all inputs (except HLH) and outputs on the cable-side B Port contain internal pull-up resistors connected to the V_{CC_cable} for proper termination and open drain mode. Outputs on the peripheral-side A Port are standard low voltage CMOS and are designed to interface with 3.3V logic. The cable-side B Port has over-voltage protection to allow outputs to interface with signals that are up to 5.5V with respect to ground.

A higher speed version is also available, the LVX161284A. The "A" version of the LVX transceiver is identical to the non-A product except for the elimination of the output edge rate control circuitry. Without output slew rate control, faster propagation delays are guaranteed. The LVX161284A is offered for high-end applications that do not need to be fully IEEE 1284-compliant.

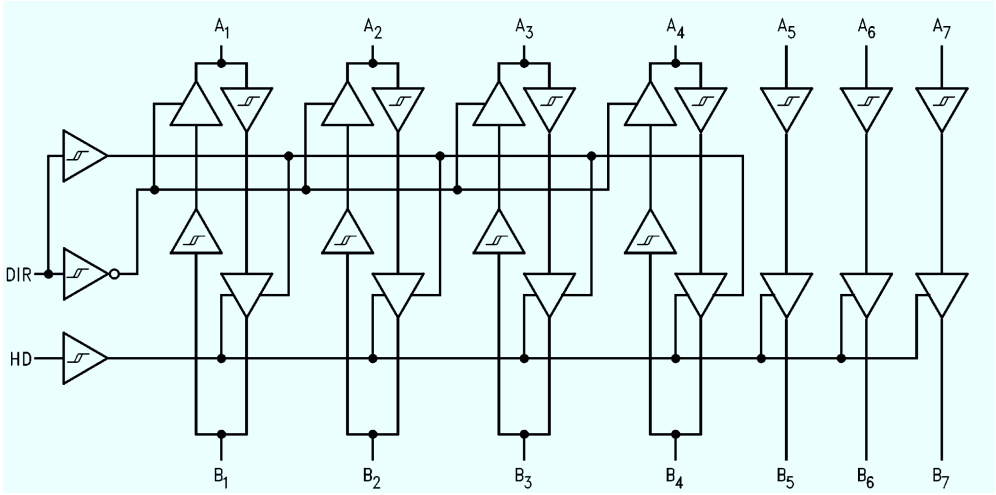
74LVX161284 Features:

- Level 1 and 2 signaling support
- 3.3V +/- 10% V_{CC} operation
- Translation capability allows the cable-side to interface with 5V signals
- Guaranteed 800mV minimum hysteresis on control inputs
- B and Y output resistance optimized to drive IEEE 1284 prescribed cable
- B and Y outputs in high impedance mode during power down
- 14mA B Port source/sink capability
- I/Os on cable-side B Port have integrated pull-up resistors
- Flow-through pin configuration
- Single-chip solution

IEEE 1284 Interface Transceivers (Continued)



74LVX/VHC161284



74ACT1284

FIGURE 1. Logic Diagrams for 74LVX/VHC161284 and 74ACT1284

Application of 1284 Transceivers

The application examples outlined below show interconnection of the 74VHC161284 and 74LVX161284 enhanced 1284 transceiver devices with various connectors. These examples reveal differences between the connection and signal naming conventions for the ECP and EPP advanced bidirectional modes.

Peripheral ECP Application

Figure 2 shows the peripheral signal (A Port) connections for the 1284-B connector. Device selection is dependent on whether the design is 5V (VHC) or 3.3V (*CROSSVOLT* LVX). VHC and LVX devices are essentially the same from a features and pinout standpoint.

Most PC chassis use the 1284-A connector; however, the 1284-A does not accommodate all signals. The PLH (Peripheral Logic High) and HLH (Host Logic High) signals are usually eliminated in the cable due to the low pin-count of the 1284-A connector (see Figure 5). PLH and HLH signals are used during the initialization phase to indicate a power-on condition at the host and peripheral. Although not recommended, many designs tie the PLH and HLH signal lines to a logic HIGH as a work-around solution. This problem can be eliminated in 1284-compliant designs by fitting the IEEE recommended 1284-C connectors at both the host and peripheral ports.

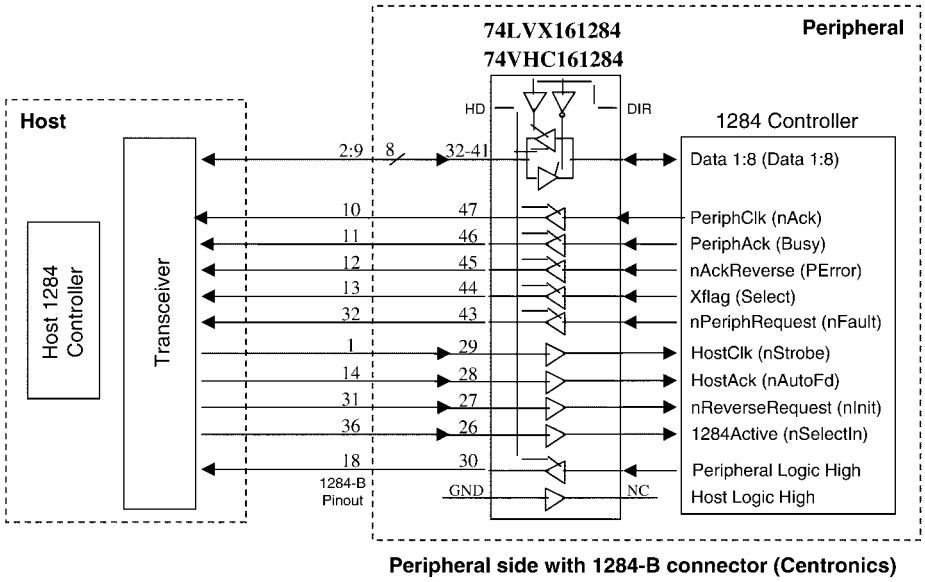


FIGURE 2. Peripheral Side Application — Extended Capabilities Port Signals

Application of 1284 Transceivers (Continued)

Peripheral EPP Application

The EPP advanced mode connection scheme and signals are shown in Figure 3. The recommended 1284-C connector is shown at the peripheral in this application. Figure 6 depicts the connection diagram for this application and indicates the commonly used 1284-A connector at the host PC. See Figure 7 for viewing connections for the IEEE recommended 1284-C connector. This is a connection diagram for both the host and peripheral sides.

It should be noted that there is no IEEE 1284 signal designated for driving the direction pin on 1284-compliant transceivers. The direction signal for bidirectional data flow control is generally programmed and driven from a circuit block referred to as the controller. The peripheral controller function is customarily implemented through use of a microprocessor or an ASIC (application specific integrated circuit) on the peripheral. On the host-side, the controller is usually a single chip multi-functional device that may incorporate UARTs, disk and keyboard, and 1284 interface controller functions. One such device is National Semiconductor's Super I/O Sidewinder PC87323VF.

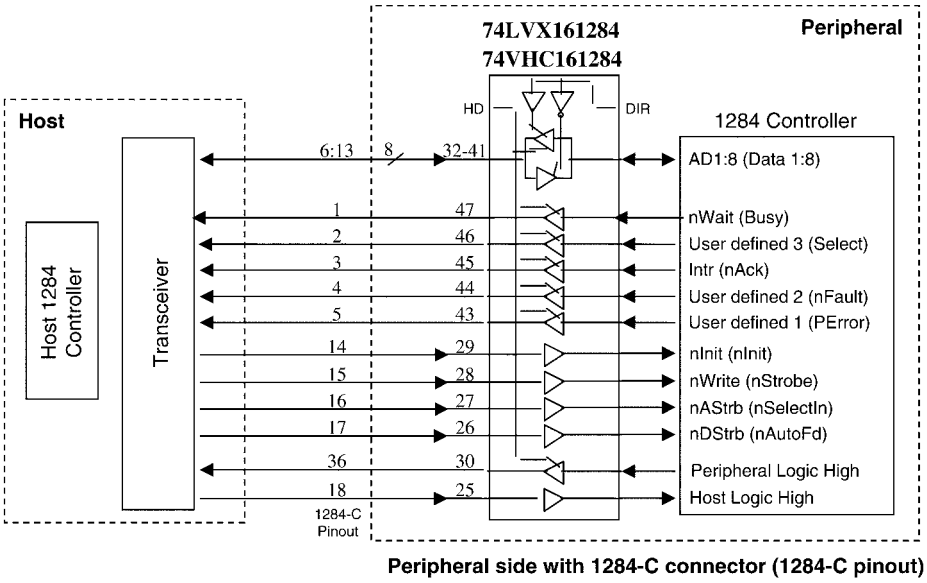
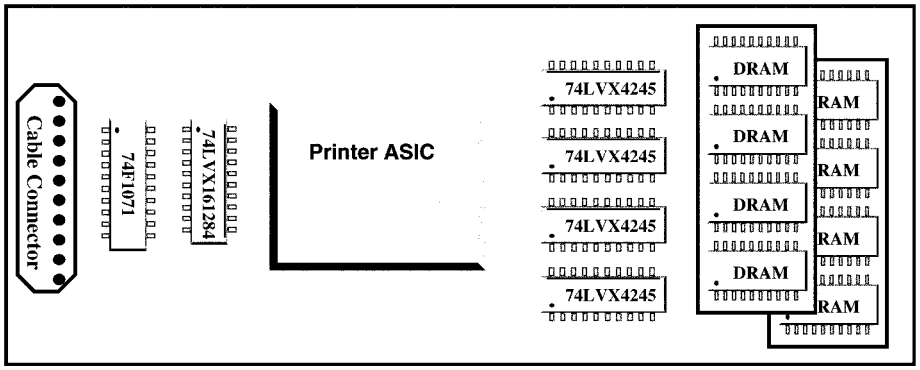


FIGURE 3. Peripheral Side Application — Extended Parallel Port Signals

Application of 1284 Transceivers (Continued)

Peripheral Board Layout

Figure 4 depicts a typical printer peripheral printed circuit board layout design. This board achieves IEEE 1284 drive and receive requirements by using Fairchild's 74VHC161284 transceiver. The 74F1071 device shown in the circuit is a bus protection diode array. Bus protection diode arrays increase the reliability of the port circuitry by suppressing over-voltage transient events.



Available Printer Support Products
•74ACT1284 (7 bits), 74LVX161284 (17 bits), and 74VHC161284 (17 bits) IEEE 1284 Transceivers
•74F1071 18-bit Undershoot/Overshoot Clamp and ESD Protection Device

FIGURE 4. Typical Laser Printer Board

Connection Diagrams

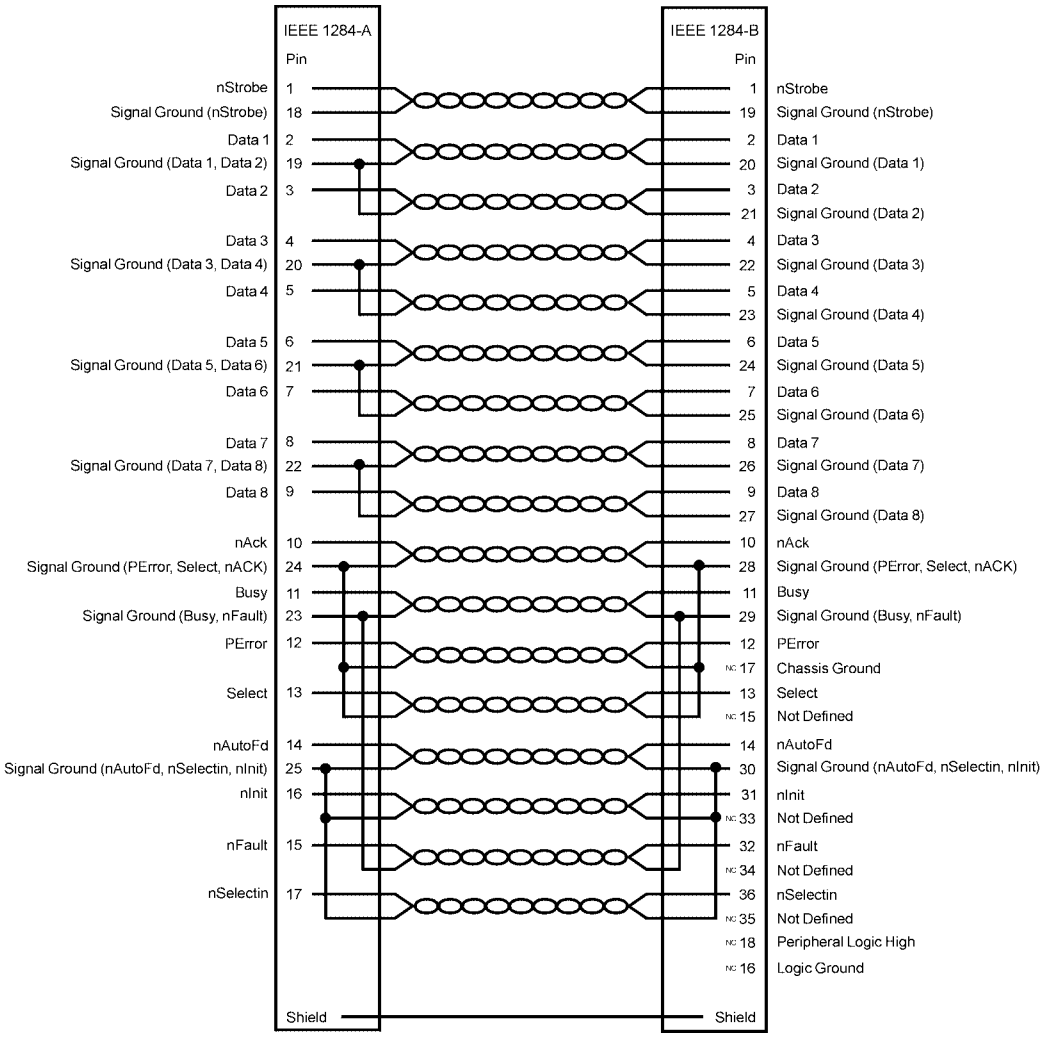


FIGURE 5. IEEE 1284-A (host) to IEEE 1284-B (peripheral) wiring diagram

Connection Diagrams (Continued)

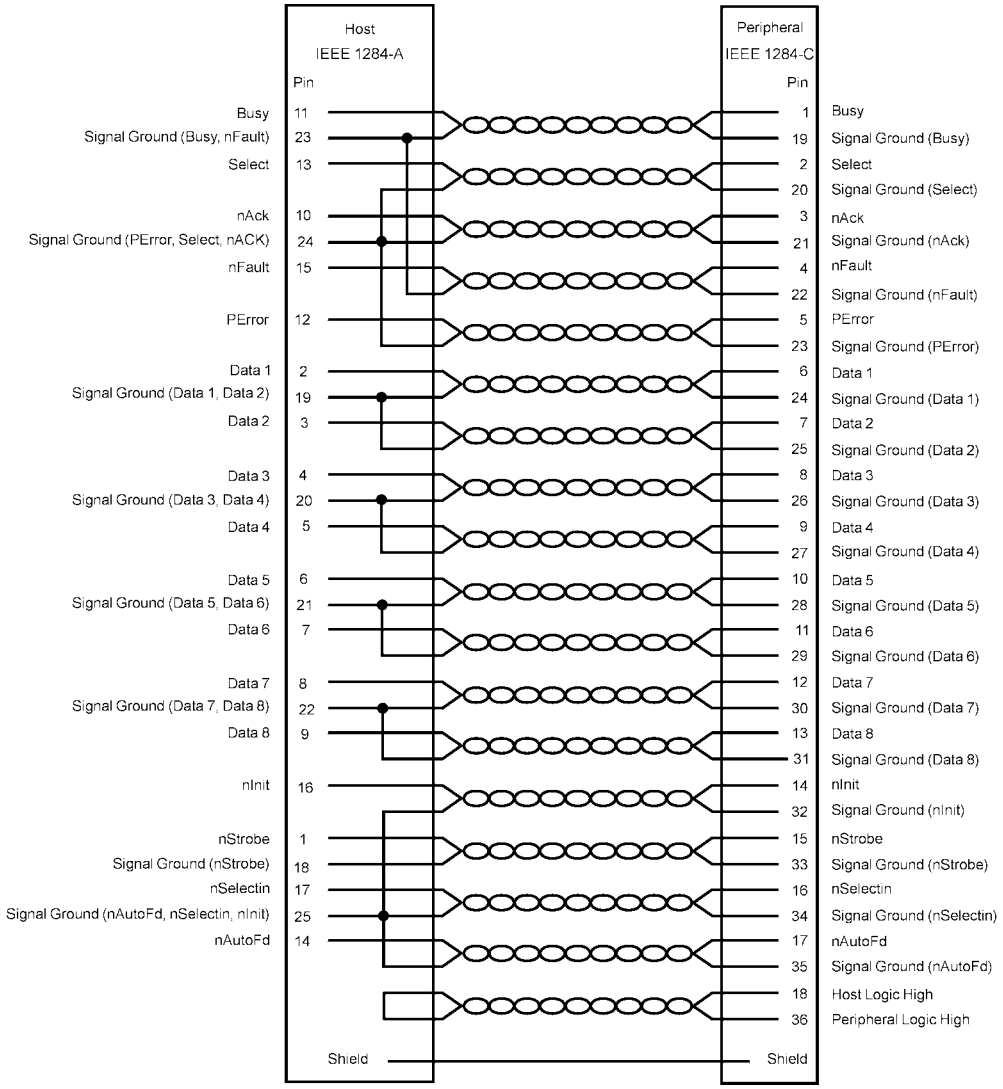


FIGURE 6. IEEE 1284-A (host) to IEEE 1284-C (peripheral) wiring diagram

Connection Diagrams (Continued)

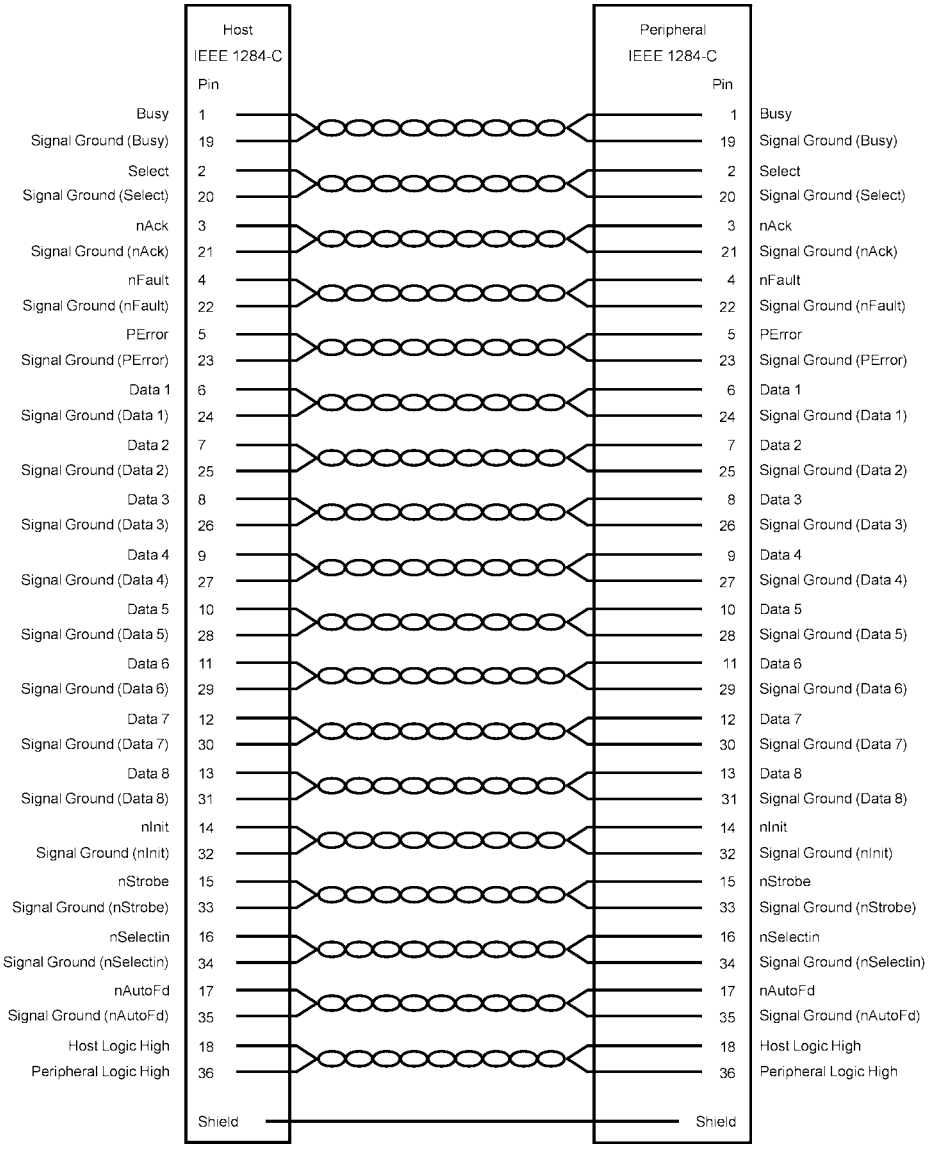


FIGURE 7. IEEE 1284-C (host) to IEEE 1284-C (peripheral) wiring diagram

Interface Notes:

1. IEEE 1284 specifies distinct signal names for each of the five signaling modes. One purpose for this applications note is to help define signal connections as they apply to the IEEE 1284 interface. The variation in signal naming is often confusing to those designing 1284 peripheral devices. Since all 1284-compliant designs must be capable of negotiating to an advanced mode, simple adherence to an advanced mode connection scheme can serve to eliminate this confusion.
2. Upon power-up, assertion of the Host Logic High (HLH) and Peripheral Logic High (PLH) signals indicate that the interface is ready to communicate. All other interface signals should be valid 500ms after these signals exceed 3.0 volts. If these signals are not present, a time-out or an interface 'hang' can occur. This is an issue because the majority of PC manufacturers do not use the IEEE-recommended 1284-C connector at the parallel port. Since devices with IEEE 1284-A connectors do not support the HLH and PLH signals, there is no reliable way to initiate a transfer. The IEEE 1284-C, a 36-pin connector, accommodates the HLH and PLH signals. The IEEE 1284-C is recommended for all host and peripheral interface designs.
3. The designer should be aware of a difference between vendor-specified output LOW voltage (V_{OL}) and the IEEE requirement for this parameter. The difference applies to the advanced transceivers, 74VHC161284 and 74LVX161284, and is due to the inclusion of series termination resistors. These terminator resistors cause the vendor's datasheet output LOW voltage specification to be higher than what the IEEE 1284 standard specifies. These integrated resistors, referred to as "Rs" in the standard, have an associated voltage drop that increases the maximum LOW level voltage present at the output. The output series resistors increase the transceiver's output impedance to a range between 35 and 55 Ω from the nominal 6 to 24 Ω. These resistors adhere to the IEEE 1284 termination scheme and are included on-chip to simplify 1284 designs.
4. In addition, pull-up termination resistors are integrated into the 74VHC161284 and 74LVX161284 advanced IEEE 1284 transceivers. These pull-up resistors terminate the cable with a deliberate high-impedance mismatch in order to produce a reflection that essentially doubles the voltage appearing at the receiver. These pull-up terminations are part of the required termination network detailed in the IEEE 1284 standard for level 2 signaling.
5. It is important to note that provision of the direction (DIR) pin signal is typically supplied by the interface controller device as this signal is not innate to the 1284 interface. This is the signal that facilitates bidirectional capability on 1284-compliant transceivers.

Summary

IEEE 1284-1994 documents the requirements for a high-speed, bidirectional communication interface. The standard changes the PC peripheral design prerogative by setting precedence for a communication standard between the host PC and peripheral. This applications note describes the parallel port and its relation to the advanced IEEE 1284 modes, ECP and EPP. Application examples depict Fairchild's advanced 1284 transceivers to emphasize the advantages of the 1284-compliant interface peripheral. Several of the most common connection schemes and associated connectors are included for reference.