Features

- High Performance, Low Power AVR® 8-Bit Microcontroller
- Advanced RISC Architecture
  - 120 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
- Non-volatile Program and Data Memories
  - 2/4/8K Byte of In-System Programmable Program Memory Flash (ATtiny25/45/85)
    - Endurance: 10,000 Write/Erase Cycles
  - 128/256/512 Bytes In-System Programmable EEPROM (ATtiny25/45/85)
    - Endurance: 100,000 Write/Erase Cycles
  - 128/256/512 Bytes Internal SRAM (ATtiny25/45/85)
  - Programming Lock for Self-Programming Flash Program and EEPROM Data Security
- Peripheral Features
  - 8-bit Timer/Counter with Prescaler and Two PWM Channels
  - 8-bit High Speed Timer/Counter with Separate Prescaler
    - 2 High Frequency PWM Outputs with Separate Output Compare Registers
    - Programmable Dead Time Generator
  - USI – Universal Serial Interface with Start Condition Detector
  - 10-bit ADC
    - 4 Single Ended Channels
    - 2 Differential ADC Channel Pairs with Programmable Gain (1x, 20x)
    - Temperature Measurement
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
- Special Microcontroller Features
  - debugWIRE On-chip Debug System
  - In-System Programmable via SPI Port
  - External and Internal Interrupt Sources
  - Low Power Idle, ADC Noise Reduction, and Power-down Modes
  - Enhanced Power-on Reset Circuit
  - Programmable Brown-out Detection Circuit
  - Internal Calibrated Oscillator
- I/O and Packages
  - Six Programmable I/O Lines
  - 8-pin PDIP, 8-pin SOIC and 20-pad QFN/MLF
- Operating Voltage
  - 1.8 - 5.5V for ATtiny25/45/85V
  - 2.7 - 5.5V for ATtiny25/45/85
- Speed Grade
  - ATtiny25/45/85V: 0 - 4 MHz @ 1.8 - 5.5V, 0 - 10 MHz @ 2.7 - 5.5V
  - ATtiny25/45/85: 0 - 10 MHz @ 2.7 - 5.5V, 0 - 20 MHz @ 4.5 - 5.5V
- Industrial Temperature Range
- Low Power Consumption
  - Active Mode:
    - 1 MHz, 1.8V: 300 µA
  - Power-down Mode:
    - 0.1µA at 1.8V

8-bit AVR® Microcontroller with 2/4/8K Bytes In-System Programmable Flash

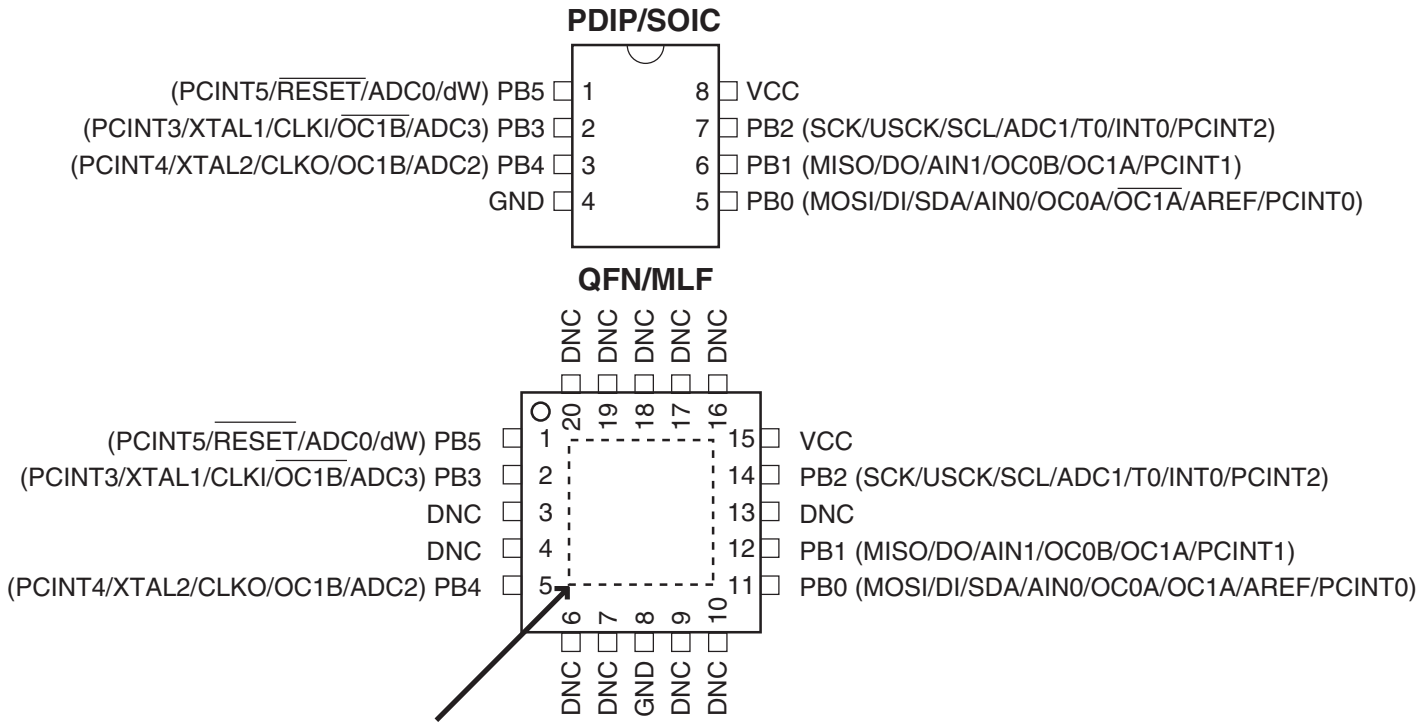
ATtiny25/V *
ATtiny45/V
ATtiny85/V *

* Preliminary Summary

2586KS–AVR–01/08

1. Pin Configurations

Figure 1-1. Pinout ATtiny25/45/85



NOTE: Bottom pad should be soldered to ground.
DNC: Do Not Connect

1.1 Pin Descriptions

1.1.1 VCC

Supply voltage.

1.1.2 GND

Ground.

1.1.3 Port B (PB5..PB0)

Port B is a 6-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATtiny25/45/85 as listed in “Alternate Functions of Port B” on page 61.

On ATtiny25, the programmable I/O ports PB3 and PB4 (pins 2 and 3) are exchanged in ATtiny15 Compatibility Mode for supporting the backward compatibility with ATtiny15.

1.1.4 $\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running and provided the reset pin has not been disabled. The minimum pulse length is given in Table 21-4 on page 170. Shorter pulses are not guaranteed to generate a reset.

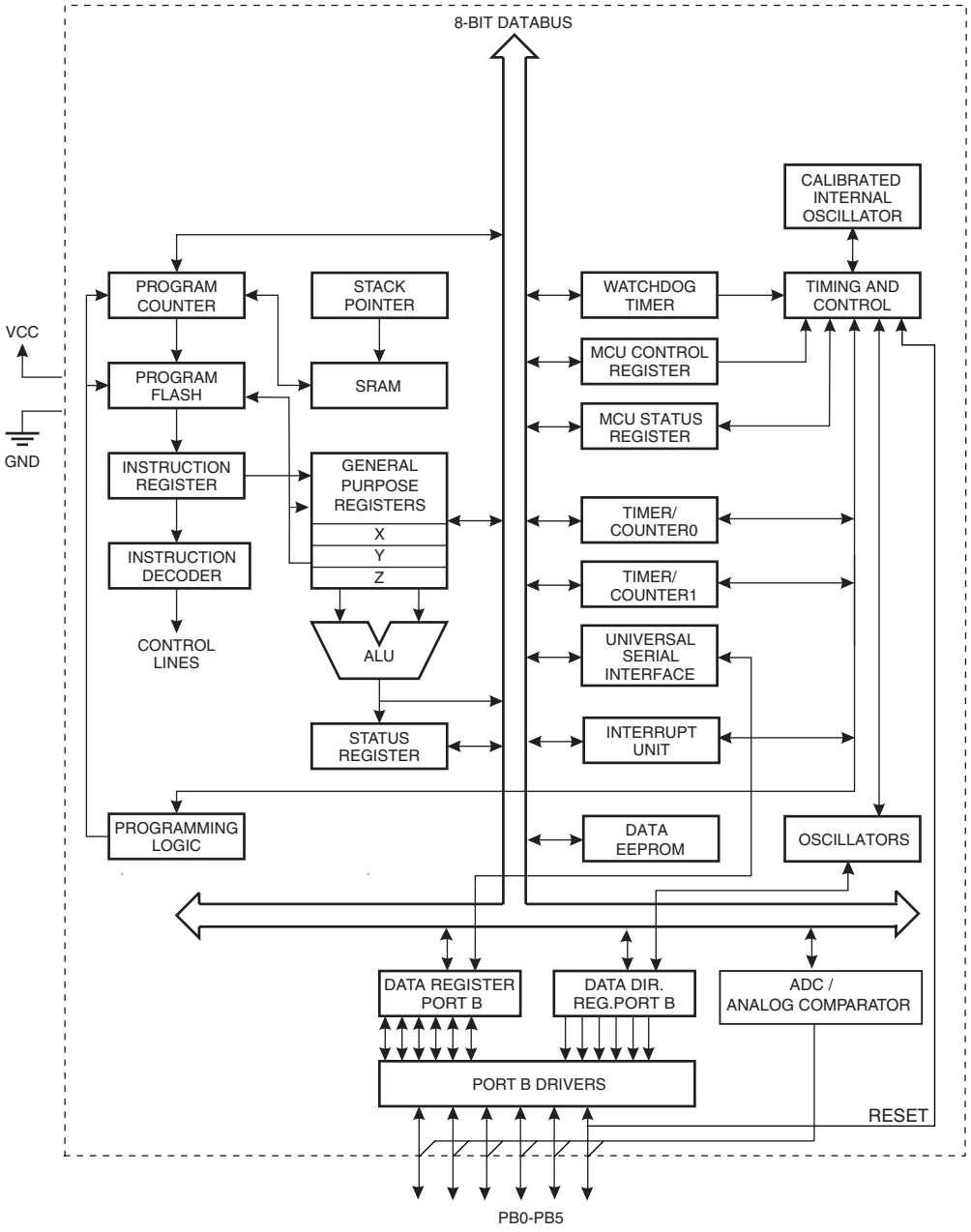
The reset pin can also be used as a (weak) I/O pin.

2. Overview

The ATtiny25/45/85 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny25/45/85 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

2.1 Block Diagram

Figure 2-1. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent

registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATtiny25/45/85 provides the following features: 2/4/8K byte of In-System Programmable Flash, 128/256/512 bytes EEPROM, 128/256/256 bytes SRAM, 6 general purpose I/O lines, 32 general purpose working registers, one 8-bit Timer/Counter with compare modes, one 8-bit high speed Timer/Counter, Universal Serial Interface, Internal and External Interrupts, a 4-channel, 10-bit ADC, a programmable Watchdog Timer with internal Oscillator, and three software selectable power saving modes. Idle mode stops the CPU while allowing the SRAM, Timer/Counter, ADC, Analog Comparator, and Interrupt system to continue functioning. Power-down mode saves the register contents, disabling all chip functions until the next Interrupt or Hardware Reset. ADC Noise Reduction mode stops the CPU and all I/O modules except ADC, to minimize switching noise during ADC conversions.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the Program memory to be re-programmed In-System through an SPI serial interface, by a conventional non-volatile memory programmer or by an On-chip boot code running on the AVR core.

The ATtiny25/45/85 AVR is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators and Evaluation kits.

3. About

3.1 Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

3.2 Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

For I/O Registers located in the extended I/O map, “IN”, “OUT”, “SBIS”, “SBIC”, “CBI”, and “SBI” instructions must be replaced with instructions that allow access to extended I/O. Typically, this means “LDS” and “STS” combined with “SBRS”, “SBRC”, “SBR”, and “CBR”. Note that not all AVR devices include an extended I/O map.

3.3 Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

4. Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x3F	SREG	I	T	H	S	V	N	Z	C	page 8
0x3E	SPH	–	–	–	–	–	–	SP9	SP8	page 11
0x3D	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	page 11
0x3C	Reserved	–								
0x3B	GIMSK	–	INT0	PCIE	–	–	–	–	–	page 53
0x3A	GIFR	–	INTF0	PCIF	–	–	–	–	–	page 53
0x39	TIMSK	–	OCIE1A	OCIE1B	OCIE0A	OCIE0B	TOIE1	TOIE0	–	page 84/page 106
0x38	TIFR	–	OCF1A	OCF1B	OCF0A	OCF0B	TOV1	TOV0	–	page 84
0x37	SPMCSR	–	–	RSIG	CTPB	RFLB	PGWRT	PGERS	SPMEN	page 149
0x36	Reserved	–								
0x35	MCUCR	BODS	PUD	SE	SM1	SM0	BODSE	ISC01	ISC00	page 38,page 52, page 66,
0x34	MCUSR	–	–	–	–	WDRF	BORF	EXTRF	PORF	page 47,
0x33	TCCR0B	FOC0A	FOC0B	–	–	WGM02	CS02	CS01	CS00	page 82
0x32	TCNT0	Timer/Counter0								page 83
0x31	OSCCAL	Oscillator Calibration Register								page 32
0x30	TCCR1	CTC1	PWM1A	COM1A1	COM1A0	CS13	CS12	CS11	CS10	page 92, page 103
0x2F	TCNT1	Timer/Counter1								page 94, page 105
0x2E	OCR1A	Timer/Counter1 Output Compare Register A								page 94, page 105
0x2D	OCR1C	Timer/Counter1 Output Compare Register C								page 95, page 106
0x2C	GTCCR	TSM	PWM1B	COM1B1	COM1B0	FOC1B	FOC1A	PSR1	PSR0	page 80, page 93, page
0x2B	OCR1B	Timer/Counter1 Output Compare Register B								page 95
0x2A	TCCR0A	COM0A1	COM0A0	COM0B1	COM0B0	–		WGM01	WGM00	page 80
0x29	OCR0A	Timer/Counter0 – Output Compare Register A								page 83
0x28	OCR0B	Timer/Counter0 – Output Compare Register B								page 84
0x27	PLLCSR	LSM	–	–	–	–	PCKE	PLLE	PLOCK	page 97, page 107
0x26	CLKPR	CLKPCE	–	–	–	CLKPS3	CLKPS2	CLKPS1	CLKPS0	page 33
0x25	DT1A	DT1AH3	DT1AH2	DT1AH1	DT1AH0	DT1AL3	DT1AL2	DT1AL1	DT1AL0	page 110
0x24	DT1B	DT1BH3	DT1BH2	DT1BH1	DT1BH0	DT1BL3	DT1BL2	DT1BL1	DT1BL0	page 110
0x23	DTPS1	-	-	-	-	-	-	DTPS11	DTPS10	page 109
0x22	DWDR	DWDR[7:0]								page 144
0x21	WDTCR	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0	page 47
0x20	PRR	–				PRTIM1	PRTIM0	PRUSI	PRADC	page 37
0x1F	EEARH								EEAR8	page 20
0x1E	EEARL	EEAR7	EEAR6	EEAR5	EEAR4	EEAR3	EEAR2	EEAR1	EEAR0	page 20
0x1D	EEDR	EEPROM Data Register								page 20
0x1C	EECR	–	–	EEPM1	EEPM0	EERIE	EEMPE	EEPE	EERE	page 21
0x1B	Reserved	–								
0x1A	Reserved	–								
0x19	Reserved	–								
0x18	PORTB	–	–	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	page 66
0x17	DDRB	–	–	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	page 66
0x16	PINB	–	–	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	page 66
0x15	PCMSK	–	–	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	page 54
0x14	DIDR0	–	–	ADC0D	ADC2D	ADC3D	ADC1D	AIN1D	AIN0D	page 125, page 142
0x13	GPIOR2	General Purpose I/O Register 2								page 10
0x12	GPIOR1	General Purpose I/O Register 1								page 10
0x11	GPIOR0	General Purpose I/O Register 0								page 10
0x10	USIBR	USI Buffer Register								page 118
0x0F	USIDR	USI Data Register								page 118
0x0E	USISR	USISIF	USIOIF	USIPF	USIDC	USICNT3	USICNT2	USICNT1	USICNT0	page 119
0x0D	USICR	USISIE	USIOIE	USIWM1	USIWM0	USICS1	USICS0	USICLK	USITC	page 120
0x0C	Reserved	–								
0x0B	Reserved	–								
0x0A	Reserved	–								
0x09	Reserved	–								
0x08	ACSR	ACD	ACBG	ACO	ACI	ACIE	–	ACIS1	ACIS0	page 124
0x07	ADMUX	REFS1	REFS0	ADLAR	REFS2	MUX3	MUX2	MUX1	MUX0	page 138
0x06	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	page 140
0x05	ADCH	ADC Data Register High Byte								page 141
0x04	ADCL	ADC Data Register Low Byte								page 141
0x03	ADCSRB	BIN	ACME	IPR	–	–	ADTS2	ADTS1	ADTS0	page 124, page 141
0x02	Reserved	–								
0x01	Reserved	–								
0x00	Reserved	–								

Note: 1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

2. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.

3. Some of the Status Flags are cleared by writing a logical one to them. Note that, unlike most other AVRs, the CBI and SBI instructions will only operation the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.

5. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add two Registers	Rd ← Rd + Rr	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	Rd ← Rd + Rr + C	Z,C,N,V,H	1
ADIW	Rdl,K	Add Immediate to Word	Rdh:Rdl ← Rdh:Rdl + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	Rd ← Rd - Rr	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	Rd ← Rd - K	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	Rd ← Rd - Rr - C	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	Rd ← Rd - K - C	Z,C,N,V,H	1
SBIW	Rdl,K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	Rd ← Rd • Rr	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	Rd ← Rd • K	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	Rd ← Rd v Rr	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	Rd ← Rd v K	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	Rd ← Rd ⊕ Rr	Z,N,V	1
COM	Rd	One's Complement	Rd ← 0xFF – Rd	Z,C,N,V	1
NEG	Rd	Two's Complement	Rd ← 0x00 – Rd	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	Rd ← Rd • (0xFF - K)	Z,N,V	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V	1
DEC	Rd	Decrement	Rd ← Rd – 1	Z,N,V	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V	1
CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V	1
SER	Rd	Set Register	Rd ← 0xFF	None	1
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC ← Z	None	2
RCALL	k	Relative Subroutine Call	PC ← PC + k + 1	None	3
ICALL		Indirect Call to (Z)	PC ← Z	None	3
RET		Subroutine Return	PC ← STACK	None	4
RETI		Interrupt Return	PC ← STACK	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1/2/3
CP	Rd,Rr	Compare	Rd – Rr	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	Rd – Rr – C	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	Rd – K	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) PC ← PC + 2 or 3	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) PC ← PC + 2 or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC←PC+k + 1	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC←PC+k + 1	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1/2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1/2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1/2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1/2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1/2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1/2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1/2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1/2
BIT AND BIT-TEST INSTRUCTIONS					
SBI	P,b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
CBI	P,b	Clear Bit in I/O Register	I/O(P,b) ← 0	None	2
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0	Z,C,N,V	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	Rd(0)←C,Rd(n+1)← Rd(n),C←Rd(7)	Z,C,N,V	1

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ROR	Rd	Rotate Right Through Carry	Rd(7)←C,Rd(n)← Rd(n+1),C←Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0)←Rd(7..4),Rd(7..4)←Rd(3..0)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Twos Complement Overflow.	V ← 1	V	1
CLV		Clear Twos Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
DATA TRANSFER INSTRUCTIONS					
MOV	Rd, Rr	Move Between Registers	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Word	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LD	Rd, X	Load Indirect	Rd ← (X)	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	Rd ← (X), X ← X + 1	None	2
LD	Rd, - X	Load Indirect and Pre-Dec.	X ← X - 1, Rd ← (X)	None	2
LD	Rd, Y	Load Indirect	Rd ← (Y)	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	Rd ← (Y), Y ← Y + 1	None	2
LD	Rd, - Y	Load Indirect and Pre-Dec.	Y ← Y - 1, Rd ← (Y)	None	2
LDD	Rd,Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	Rd ← (Z), Z ← Z+1	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	Z ← Z - 1, Rd ← (Z)	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2
LDS	Rd, k	Load Direct from SRAM	Rd ← (k)	None	2
ST	X, Rr	Store Indirect	(X) ← Rr	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	(X) ← Rr, X ← X + 1	None	2
ST	- X, Rr	Store Indirect and Pre-Dec.	X ← X - 1, (X) ← Rr	None	2
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	(Y) ← Rr, Y ← Y + 1	None	2
ST	- Y, Rr	Store Indirect and Pre-Dec.	Y ← Y - 1, (Y) ← Rr	None	2
STD	Y+q,Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	(Z) ← Rr, Z ← Z + 1	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	Z ← Z - 1, (Z) ← Rr	None	2
STD	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2
STS	k, Rr	Store Direct to SRAM	(k) ← Rr	None	2
LPM		Load Program Memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd ← (Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Inc	Rd ← (Z), Z ← Z+1	None	3
SPM		Store Program Memory	(z) ← R1:R0	None	
IN	Rd, P	In Port	Rd ← P	None	1
OUT	P, Rr	Out Port	P ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2
MCU CONTROL INSTRUCTIONS					
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/Timer)	None	1
BREAK		Break	For On-chip Debug Only	None	N/A

6. Ordering Information

6.1 ATtiny25

Speed (MHz)[3]	Power Supply	Ordering Code[2]	Package[1]	Operational Range
10	1.8 - 5.5V	ATtiny25V-10PU ATtiny25V-10SU ATtiny25V-10SSU ATtiny25V-10MU	8P3 8S2 S8S1 20M1	Industrial (-40°C to 85°C)
20	2.7 - 5.5V	ATtiny25-20PU ATtiny25-20SU ATtiny25-20SSU ATtiny25-20MU	8P3 8S2 S8S1 20M1	Industrial (-40°C to 85°C)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC},see Figure 21.3 on page 168

Package Type	
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S2	8-lead, 0.200" Wide, Plastic Gull-Wing Small Outline (EIAJ SOIC)
S8S1	8-lead, 0.150" Wide, Plastic Gull-Wing Small Outline (JEDEC SOIC)
20M1	20-pad, 4 x 4 x 0.8 mm Body, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

6.2 ATtiny45

Speed (MHz)[3]	Power Supply	Ordering Code[2]	Package[1]	Operational Range
10	1.8 - 5.5V	ATtiny45V-10PU ATtiny45V-10SU ATtiny45V-10MU	8P3 8S2 20M1	Industrial (-40°C to 85°C)
20	2.7 - 5.5V	ATtiny45-20PU ATtiny45-20SU ATtiny45-20MU	8P3 8S2 20M1	Industrial (-40°C to 85°C)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC},see Figure 21.3 on page 168

Package Type	
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S2	8-lead, 0.200" Wide, Plastic Gull-Wing Small Outline (EIAJ SOIC)
20M1	20-pad, 4 x 4 x 0.8 mm Body, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

6.3 ATtiny85

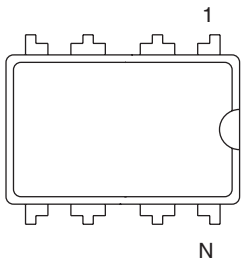
Speed (MHz)[3]	Power Supply	Ordering Code[2]	Package[1]	Operational Range
10	1.8 - 5.5V	ATtiny85V-10PU ATtiny85V-10SU ATtiny85V-10MU	8P3 8S2 20M1	Industrial (-40°C to 85°C)
20	2.7 - 5.5V	ATtiny85-20PU ATtiny85-20SU ATtiny85-20MU	8P3 8S2 20M1	Industrial (-40°C to 85°C)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC},see Figure 21.3 on page 168

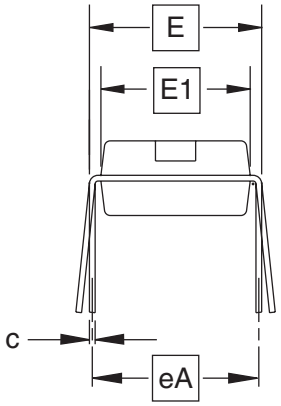
Package Type	
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S2	8-lead, 0.200" Wide, Plastic Gull-Wing Small Outline (EIAJ SOIC)
20M1	20-pad, 4 x 4 x 0.8 mm Body, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

7. Packaging Information

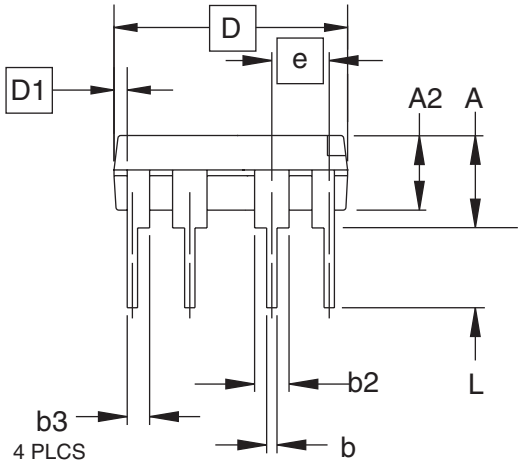
7.1 8P3



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = inches)

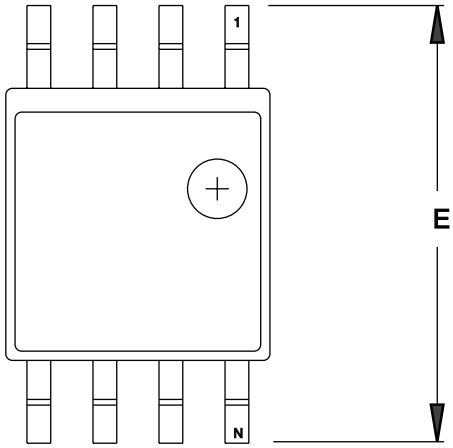
SYMBOL	MIN	NOM	MAX	NOTE
A			0.210	2
A2	0.115	0.130	0.195	
b	0.014	0.018	0.022	5
b2	0.045	0.060	0.070	6
b3	0.030	0.039	0.045	6
c	0.008	0.010	0.014	
D	0.355	0.365	0.400	3
D1	0.005			3
E	0.300	0.310	0.325	4
E1	0.240	0.250	0.280	3
e	0.100 BSC			
eA	0.300 BSC			4
L	0.115	0.130	0.150	2

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

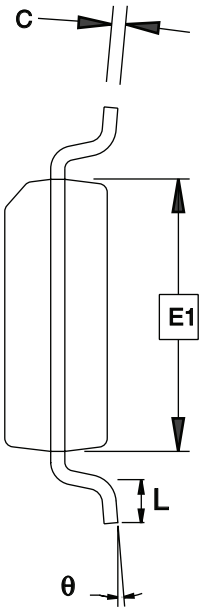
01/09/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8P3**, 8-lead, 0.300" Wide Body, Plastic Dual In-line Package (PDIP)	8P3	B

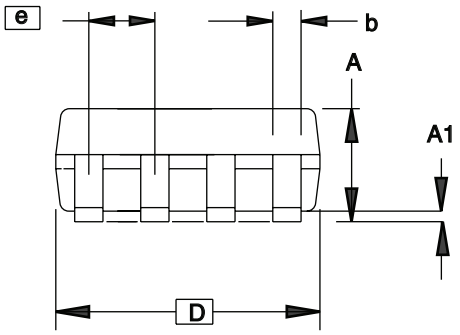
7.2 8S2



TOP VIEW



END VIEW



SIDE VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

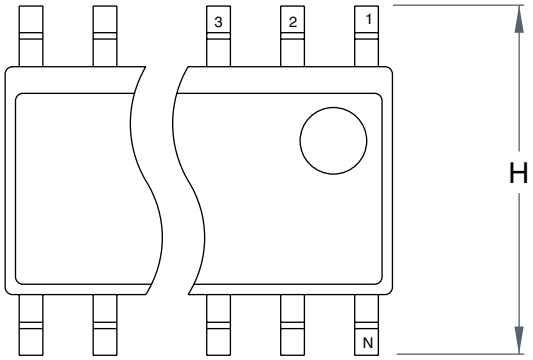
SYMBOL	MIN	NOM	MAX	NOTE
A	1.70		2.16	
A1	0.05		0.25	
b	0.35		0.48	5
C	0.15		0.35	5
D	5.13		5.35	
E1	5.18		5.40	2, 3
E	7.70		8.26	
L	0.51		0.85	
θ	0°		8°	
e	1.27 BSC			4

Notes:
1. This drawing is for general information only; refer to EIAJ Drawing EDR-7320 for additional information.
2. Mismatch of the upper and lower dies and resin burrs are not included.
3. It is recommended that upper and lower cavities be equal. If they are different, the larger dimension shall be regarded.
4. Determines the true geometric position.
5. Values b,C apply to plated terminal. The standard thickness of the plating layer shall measure between 0.007 to .021 mm.

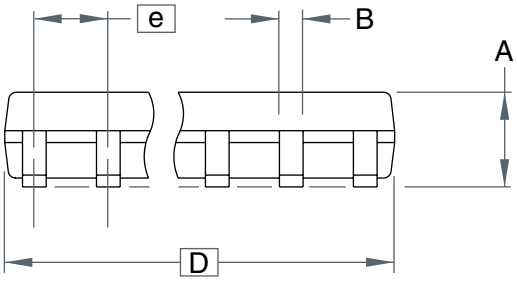
4/7/06

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8S2**, 8-lead, 0.209" Body, Plastic Small Outline Package (EIAJ)	8S2	D

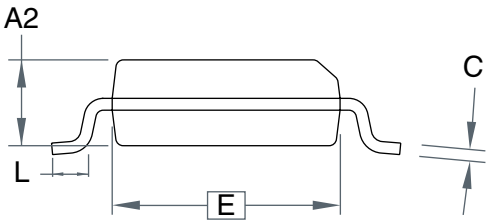
7.3 S8S1



Top View



Side View



End View

COMMON DIMENSIONS
(Unit of Measure = mm)

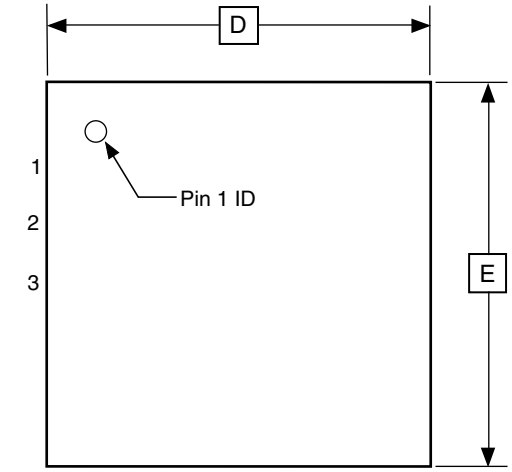
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.75	
B	–	–	0.51	
C	–	–	0.25	
D	–	–	5.00	
E	–	–	4.00	
e		1.27 BSC		
H	–	–	6.20	
L	–	–	1.27	

Note: This drawing is for general information only. Refer to JEDEC Drawing MS-012 for proper dimensions, tolerances, datums, etc.

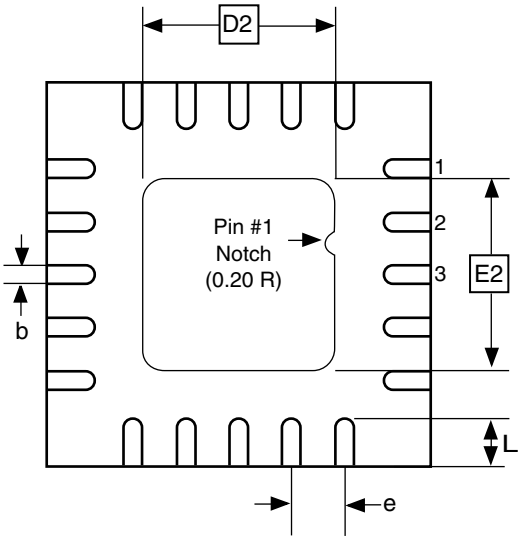
10/10/01

2325 Orchard Parkway San Jose, CA 95131	**TITLE** **8S1**, 8-lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**DRAWING NO.** 8S1	**REV.** A

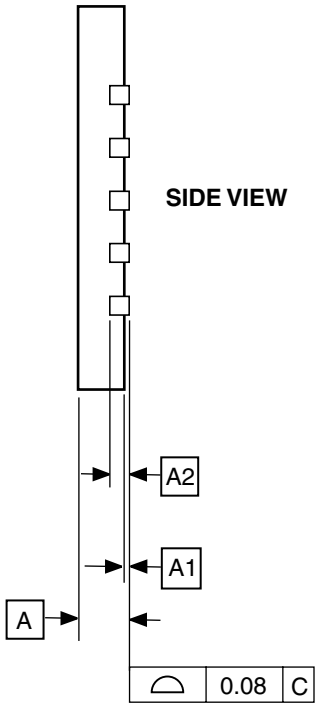
7.4 20M1



TOP VIEW



BOTTOM VIEW



Note: Reference JEDEC Standard MO-220, Fig. 1 (SAW Singulation) WGGD-5.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.70	0.75	0.80	
A1	–	0.01	0.05	
A2		0.20 REF		
b	0.18	0.23	0.30	
D		4.00 BSC		
D2	2.45	2.60	2.75	
E		4.00 BSC		
E2	2.45	2.60	2.75	
e		0.50 BSC		
L	0.35	0.40	0.55	

10/27/04

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20M1**, 20-pad, 4 x 4 x 0.8 mm Body, Lead Pitch 0.50 mm, 2.6 mm Exposed Pad, Micro Lead Frame Package (MLF)	20M1	A

8. Errata

8.1 Errata ATtiny25

The revision letter in this section refers to the revision of the ATtiny25 device.

8.1.1 Rev D and E

No known errata.

8.1.2 Rev B and C

- **EEPROM read may fail at low supply voltage / low clock frequency**

1. **EEPROM read may fail at low supply voltage / low clock frequency**
   Trying to read EEPROM at low clock frequencies and/or low supply voltage may result in invalid data.

   Problem Fix/Workaround
   Do not use the EEPROM when clock frequency is below 1 MHz and supply voltage is below 2V. If operating frequency can not be raised above 1 MHz then supply voltage should be more than 3V. Similarly, if supply voltage can not be raised above 2V then operating frequency should be more than 2 MHz.

   This feature is known to be temperature dependent but it has not been characterised. Guidelines are given for room temperature, only.

8.1.3 Rev A

Not sampled.

8.2 Errata ATtiny45

The revision letter in this section refers to the revision of the ATtiny45 device.

8.2.1 Rev F and G

No known errata

8.2.2 Rev D and E

- **EEPROM read may fail at low supply voltage / low clock frequency**

1. **EEPROM read may fail at low supply voltage / low clock frequency**
   Trying to read EEPROM at low clock frequencies and/or low supply voltage may result in invalid data.

   Problem Fix/Workaround
   Do not use the EEPROM when clock frequency is below 1 MHz and supply voltage is below 2V. If operating frequency can not be raised above 1 MHz then supply voltage should be more than 3V. Similarly, if supply voltage can not be raised above 2V then operating frequency should be more than 2 MHz.

   This feature is known to be temperature dependent but it has not been characterised. Guidelines are given for room temperature, only.

8.2.3 Rev B and C

- **PLL not locking**
- **EEPROM read from application code does not work in Lock Bit Mode 3**
- **EEPROM read may fail at low supply voltage / low clock frequency**
- **Timer Counter 1 PWM output generation on OC1B- XOC1B does not work correctly**

1. **PLL not locking**
   When at frequencies below 6.0 MHz, the PLL will not lock

   Problem fix / Workaround
   When using the PLL, run at 6.0 MHz or higher.

2. **EEPROM read from application code does not work in Lock Bit Mode 3**
   When the Memory Lock Bits LB2 and LB1 are programmed to mode 3, EEPROM read does not work from the application code.

   Problem Fix/Work around
   Do not set Lock Bit Protection Mode 3 when the application code needs to read from EEPROM.

3. **EEPROM read may fail at low supply voltage / low clock frequency**
   Trying to read EEPROM at low clock frequencies and/or low supply voltage may result in invalid data.

   Problem Fix/Workaround
   Do not use the EEPROM when clock frequency is below 1 MHz and supply voltage is below 2V. If operating frequency can not be raised above 1 MHz then supply voltage should be

more than 3V. Similarly, if supply voltage can not be raised above 2V then operating frequency should be more than 2 MHz.

This feature is known to be temperature dependent but it has not been characterised. Guidelines are given for room temperature, only.

4. **Timer Counter 1 PWM output generation on OC1B – XOC1B does not work correctly**
   Timer Counter1 PWM output OC1B-XOC1B does not work correctly. Only in the case when the control bits, COM1B1 and COM1B0 are in the same mode as COM1A1 and COM1A0, respectively, the OC1B-XOC1B output works correctly.

   Problem Fix/Work around
   The only workaround is to use same control setting on COM1A(1:0) and COM1B(1:0) control bits, see table 14-4 in the data sheet. The problem has been fixed for Tiny45 rev D.

8.2.4 Rev A

- **Too high power down power consumption**
- **DebugWIRE looses communication when single stepping into interrupts**
- **PLL not locking**
- **EEPROM read from application code does not work in Lock Bit Mode 3**
- **EEPROM read may fail at low supply voltage / low clock frequency**

1. **Too high power down power consumption**
   Three situations will lead to a too high power down power consumption. These are:
   – An external clock is selected by fuses, but the I/O PORT is still enabled as an output.
   – The EEPROM is read before entering power down.
   – VCC is 4.5 volts or higher.

   Problem fix / Workaround
   – When using external clock, avoid setting the clock pin as Output.
   – Do not read the EEPROM if power down power consumption is important.
   – Use VCC lower than 4.5 Volts.

2. **DebugWIRE looses communication when single stepping into interrupts**
   When receiving an interrupt during single stepping, debugwire will loose

   communication.

   Problem fix / Workaround
   – When singlestepping, disable interrupts.
   – When debugging interrupts, use breakpoints within the interrupt routine, and run into the interrupt.

3. **PLL not locking**
   When at frequencies below 6.0 MHz, the PLL will not lock

   Problem fix / Workaround
   When using the PLL, run at 6.0 MHz or higher.

4. **EEPROM read from application code does not work in Lock Bit Mode 3**

When the Memory Lock Bits LB2 and LB1 are programmed to mode 3, EEPROM read does not work from the application code.

Problem Fix/Work around

Do not set Lock Bit Protection Mode 3 when the application code needs to read from EEPROM.

5. **EEPROM read may fail at low supply voltage / low clock frequency**

Trying to read EEPROM at low clock frequencies and/or low supply voltage may result in invalid data.

Problem Fix/Workaround

Do not use the EEPROM when clock frequency is below 1 MHz and supply voltage is below 2V. If operating frequency can not be raised above 1 MHz then supply voltage should be more than 3V. Similarly, if supply voltage can not be raised above 2V then operating frequency should be more than 2 MHz.

This feature is known to be temperature dependent but it has not been characterised. Guidelines are given for room temperature, only.

8.3 Errata ATtiny85

The revision letter in this section refers to the revision of the ATtiny85 device.

8.3.1 Rev B and C

No known errata.

8.3.2 Rev A

- **EEPROM read may fail at low supply voltage / low clock frequency**

1. **EEPROM read may fail at low supply voltage / low clock frequency**
   Trying to read EEPROM at low clock frequencies and/or low supply voltage may result in invalid data.

   Problem Fix/Workaround
   Do not use the EEPROM when clock frequency is below 1 MHz and supply voltage is below 2V. If operating frequency can not be raised above 1 MHz then supply voltage should be more than 3V. Similarly, if supply voltage can not be raised above 2V then operating frequency should be more than 2 MHz.

   This feature is known to be temperature dependent but it has not been characterised. Guidelines are given for room temperature, only.

9. Datasheet Revision History

9.1 Rev. 2586K-01/08

1. Updated Document Template.
2. Added Sections:
   - “Data Retention” on page 6
   - “Low Level Interrupt” on page 51
   - “Device Signature Imprint Table” on page 153
3. Updated Sections:
   - “Internal PLL for Fast Peripheral Clock Generation - clkPCK” on page 24
   - “System Clock and Clock Options” on page 23
   - “Internal PLL in ATtiny15 Compatibility Mode” on page 24
   - “Sleep Modes” on page 35
   - “Software BOD Disable” on page 36
   - “External Interrupts” on page 51
   - “Timer/Counter1 in PWM Mode” on page 101
   - “USI – Universal Serial Interface” on page 111
   - “Temperature Measurement” on page 137
   - “Reading Lock, Fuse and Signature Data from Software” on page 147
   - “Program And Data Memory Lock Bits” on page 151
   - “Fuse Bytes” on page 152
   - “Signature Bytes” on page 154
   - “Calibration Bytes” on page 154
   - “System and Reset Characteristics” on page 170
4. Added Figures:
   - “Reset Pin Output Voltage vs. Sink Current (V_{CC} = 3V)” on page 188
   - “Reset Pin Output Voltage vs. Sink Current (V_{CC} = 5V)” on page 189
   - “Reset Pin Output Voltage vs. Source Current (V_{CC} = 3V)” on page 189
   - “Reset Pin Output Voltage vs. Source Current (V_{CC} = 5V)” on page 190
5. Updated Figure:
   - “Reset Logic” on page 41
6. Updated Tables:
   - “Start-up Times for Internal Calibrated RC Oscillator Clock” on page 28
   - “Start-up Times for Internal Calibrated RC Oscillator Clock (in ATtiny15 Mode)” on page 28
   - “Start-up Times for the 128 kHz Internal Oscillator” on page 29
   - “Compare Mode Select in PWM Mode” on page 89
   - “Compare Mode Select in PWM Mode” on page 101
   - “DC Characteristics. T_A = -40°C to 85°C (1)” on page 166
   - “Calibration Accuracy of Internal RC Oscillator” on page 169
   - “ADC Characteristics – Preliminary” on page 172

7. Updated Code Example in Section:
   – “Write” on page 17
8. Updated Bit Descriptions in:
   – “MCUCR – MCU Control Register” on page 38
   – “Bits 7:6 – COM0A1:0: Compare Match Output A Mode” on page 80
   – “Bits 5:4 – COM0B1:0: Compare Match Output B Mode” on page 80
   – “Bits 2:0 – ADTS2:0: ADC Auto Trigger Source” on page 142
   – “SPMCSR – Store Program Memory Control and Status Register” on page 149.
9. Updated description of feature “EEPROM read may fail at low supply voltage / low clock frequency” in Sections:
   – “Errata ATtiny25” on page 18
   – “Errata ATtiny45” on page 19
   – “Errata ATtiny85” on page 22
10. Updated Package Description in Sections:
   – “ATtiny25” on page 11
   – “ATtiny45” on page 12
   – “ATtiny85” on page 13
11. Updated Package Drawing:
   – “S8S1” on page 16
12. Updated Order Codes for:
   – “ATtiny25” on page 11

9.2 Rev. 2586J-12/06

1. Updated “Low Power Consumption” on page 1.
2. Updated description of instruction length in “Architectural Overview” , starting on page 7.
3. Updated Flash size in “In-System Re-programmable Flash Program Memory” on page 15.
4. Updated cross-references in sections “Atomic Byte Programming” , “Erase” and “Write” , starting on page 17.
5. Updated “Atomic Byte Programming” on page 17.
6. Updated “Internal PLL for Fast Peripheral Clock Generation - clkPCK” on page 24.
7. Replaced single clocking system figure with two: Figure 6-2 and Figure 6-3 on page 24.
8. Updated Table 6-1 on page 25, Table 6-12 on page 30 and Table 6-6 on page 28.
9. Updated “Calibrated Internal Oscillator” on page 27.
10. Updated Table 6-5 on page 27.
11. Updated “OSCCAL – Oscillator Calibration Register” on page 32.
12. Updated “CLKPR – Clock Prescale Register” on page 33.
13. Updated “Power-down Mode” on page 36.
14. Updated “Bit 0” in “PRR – Power Reduction Register” on page 39.
15. Added footnote to Table 8-3 on page 49.
16. Updated Table 10-5 on page 65.
17. Deleted “Bits 7, 2” in “MCUCR – MCU Control Register” on page 66.

18. Updated and moved section “Timer/Counter0 Prescaler and Clock Sources”, now located on page 68.
19. Updated “Timer/Counter1 Initialization for Asynchronous Mode” on page 89.
20. Updated bit description in “PLLCSR – PLL Control and Status Register” on page 97 and “PLLCSR – PLL Control and Status Register” on page 107.
21. Added recommended maximum frequency in“Prescaling and Conversion Timing” on page 129.
22. Updated Figure 17-8 on page 133 .
23. Updated “Temperature Measurement” on page 137.
24. Updated Table 17-3 on page 138.
25. Updated bit R/W descriptions in:
“TIMSK – Timer/Counter Interrupt Mask Register” on page 84,
“TIFR – Timer/Counter Interrupt Flag Register” on page 84,
“TIMSK – Timer/Counter Interrupt Mask Register” on page 95,
“TIFR – Timer/Counter Interrupt Flag Register” on page 96,
“PLLCSR – PLL Control and Status Register” on page 97,
“TIMSK – Timer/Counter Interrupt Mask Register” on page 106,
“TIFR – Timer/Counter Interrupt Flag Register” on page 106,
“PLLCSR – PLL Control and Status Register” on page 107 and
“DIDR0 – Digital Input Disable Register 0” on page 142.
26. Added limitation to “Limitations of debugWIRE” on page 144.
27. Updated “DC Characteristics” on page 166.
28. Updated Table 21-7 on page 171.
29. Updated Figure 21-6 on page 175.
30. Updated Table 21-11 on page 175.
31. Updated Table 22-1 on page 181.
32. Updated Table 22-2 on page 181.
33. Updated Table 22-30, Table 22-31 and Table 22-32, starting on page 192.
34. Updated Table 22-33, Table 22-34 and Table 22-35, starting on page 193.
35. Updated Table 22-37 on page 195.
36. Updated Table 22-44, Table 22-45, Table 22-46 and Table 22-47, starting on page 199.

9.3 Rev. 2586I-09/06

1. All Characterization data moved to “Electrical Characteristics” on page 166.
2. All Register Descriptions are gathered up in seperate sections in the end of each chapter.
3. Updated Table 11-3 on page 81, Table 11-5 on page 82, Table 11-6 on page 83 and Table 20-4 on page 152.
4. Updated “Calibrated Internal Oscillator” on page 27.
5. Updated Note in Table 7-1 on page 35.
6. Updated “System Control and Reset” on page 41.
7. Updated Register Description in “I/O Ports” on page 55.
8. Updated Features in “USI – Universal Serial Interface” on page 111.
9. Updated Code Example in “SPI Master Operation Example” on page 113 and “SPI Slave Operation Example” on page 114.
10. Updated “Analog Comparator Multiplexed Input” on page 123.

11. Updated Figure 17-1 on page 127.
12. Updated “Signature Bytes” on page 154.
13. Updated “Electrical Characteristics” on page 166.

9.4 Rev. 2586H-06/06

1. Updated “Calibrated Internal Oscillator” on page 27.
2. Updated Table 6.5.1 on page 32.
3. Added Table 21-2 on page 169.

9.5 Rev. 2586G-05/06

1. Updated “Internal PLL for Fast Peripheral Clock Generation - clkPCK” on page 24.
2. Updated “Default Clock Source” on page 31.
3. Updated “Low-Frequency Crystal Oscillator” on page 29.
4. Updated “Calibrated Internal Oscillator” on page 27.
5. Updated “Clock Output Buffer” on page 32.
6. Updated “Power Management and Sleep Modes” on page 35.
7. Added “Software BOD Disable” on page 36.
8. Updated Figure 16-1 on page 123.
9. Updated “Bit 6 – ACBG: Analog Comparator Bandgap Select” on page 124.
10. Added note for Table 17-2 on page 129.
11. Updated “Register Summary” on page 7.

9.6 Rev. 2586F-04/06

1. Updated “Digital Input Enable and Sleep Modes” on page 59.
2. Updated Table 20-16 on page 163.
3. Updated “Ordering Information” on page 11.

9.7 Rev. 2586E-03/06

1. Updated Features in “Analog to Digital Converter” on page 126.
2. Updated Operation in “Analog to Digital Converter” on page 126.
3. Updated Table 17-2 on page 138.
4. Updated Table 17-3 on page 138.
5. Updated “Errata” on page 18.

9.8 Rev. 2586D-02/06

1. Updated Table 6-12 on page 30, Table 6-10 on page 29, Table 6-3 on page 26, Table 6-9 on page 29, Table 6-5 on page 27, Table 9-1 on page 50,Table 17-4 on page 139, Table 20-16 on page 163, Table 21-8 on page 172.
2. Updated “Timer/Counter1 in PWM Mode” on page 89.
3. Updated text “Bit 2 - TOV1: Timer/Counter1 Overflow Flag” on page 96.
4. Updated values in “DC Characteristics” on page 166.
5. Updated “Register Summary” on page 7.
6. Updated “Ordering Information” on page 11.

7. Updated Rev B and C in "Errata ATtiny45" on page 19.
8. All references to power-save mode are removed.
9. Updated Register Adresses.

9.9 Rev. 2586C-06/05

1. Updated "Features" on page 1.
2. Updated Figure 1-1 on page 2.
3. Updated Code Examples on page 18 and page 19.
4. Moved "Temperature Measurement" to Section 17.12 page 137.
5. Updated "Register Summary" on page 7.
6. Updated "Ordering Information" on page 11.

9.10 Rev. 2586B-05/05

1. CLKI added, instances of EEMWE/EEWE renamed EEMPE/EEPE, removed some TBD.
   Removed "Preliminary Description" from "Temperature Measurement" on page 137.
2. Updated "Features" on page 1.
3. Updated Figure 1-1 on page 2 and Figure 8-1 on page 41.
4. Updated Table 7-2 on page 39, Table 10-4 on page 65, Table 10-5 on page 65
5. Updated "Serial Programming Instruction set" on page 157.
6. Updated SPH register in "Instruction Set Summary" on page 9.
7. Updated "DC Characteristics" on page 166.
8. Updated "Ordering Information" on page 11.
9. Updated "Errata" on page 18.

9.11 Rev. 2586A-02/05

Initial revision.

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